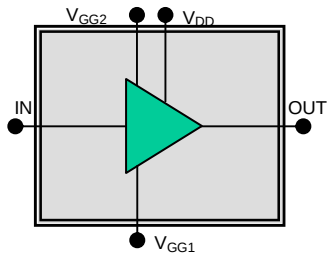
iT2007
10 MHz – 22 GHz High-Power Amplifier

Description

The iT2007 is a broadband GaAs MMIC traveling wave amplifier designed for high output power applications where low frequency extension capabilities are also required. The iT2007 provides saturated output power of 1 W up to 7 GHz and greater than 29 dBm up to 15 GHz. Average gain is 7 dB with flatness of +/-1dB up to 22 GHz. DC power consumption as low as 2.7 W is obtained by biasing for best output power and good linear performance. Input and output ports DC coupled.

Features

- Frequency range: 1 GHz – 22 GHz with low-frequency extension capability down to 10 MHz
- Psat (1 GHz – 7 GHz): 30 dBm
- Psat (7 GHz – 15 GHz): 29 dBm
- Psat (15 GHz – 20 GHz): >27 dBm
- Average gain with +/-1dB flatness: 7 dB
- DC power consumption: 2.7 W
- DC bias conditions: 9 V at 300 mA
- Full chip passivation for high reliability



Absolute Maximum Ratings

Symbol	Parameters/conditions	Min.	Max.	Units
V_{DD}	Positive supply voltage		11	V
V_{GG2}	Positive supply voltage	-3	5	V
V_{DD} - V_{GG2}	Gate to drain voltage		12	V
V_{GG1}	Negative supply voltage	-2	0	V
I_{DQ}	DC positive supply current		800	mA
I_{GG1}	Negative supply current		1.6	mA
Pin	RF input power		27	dBm
Pdiss_DC	DC power dissipation (no RF)		5	W
Tch	Operating channel temperature		150	℃
Tm	Mounting temperature (30 s)		320	℃
Tst	Storage temperature	-65	150	℃

Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
Tb	Operating temperature range (back side)	-40		85	^{0}C
V_{DD}	Positive bias supply			9	V
V_{GG2}	Positive bias supply		4		V
V_{GG1}	Negative bias supply	-0.4	-0.6	-0.9	V
I_{DQ}	DC supply drain current		300	400	mA

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Electrical Characteristics

(at 25 ℃)
50 ohm system
V_{DD} = +9
Quiescent current (I_{DQ} = 300 mA

1. Measured at 10 dB output back-off with respect to P_{1dB} single carrier. Δf = 10 MHz

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
BW	Frequency range	1		22	GHz
S21	Small signal gain	5	7		dB
	Gain flatness			+/-1	dB
S11	Input return loss	15	20		dB
S22	Output return loss	9	12		dB
S12	Isolation	30			dB
Psat	Saturated output power (3-dB gain comp.)				
	1 - 10 GHz	27.5	29.5		dBm
	1 - 18 GHz	27	28		dBm
	1 - 20 GHz	25.5	27.5		dBm
P_{1dB}	Output power at 1-dB gain compression				
	1 - 10 GHz	27	29		dBm
	1 - 18 GHz	25.5	27.5		dBm
	1 - 20 GHz	25	27		dBm
OIP3 (1)	Output third-order intercept point				
	7 GHz	41	43		dBm
	15 GHz	36	38		dBm
	20 GHz	34	36		dBm

Thermal Characteristics

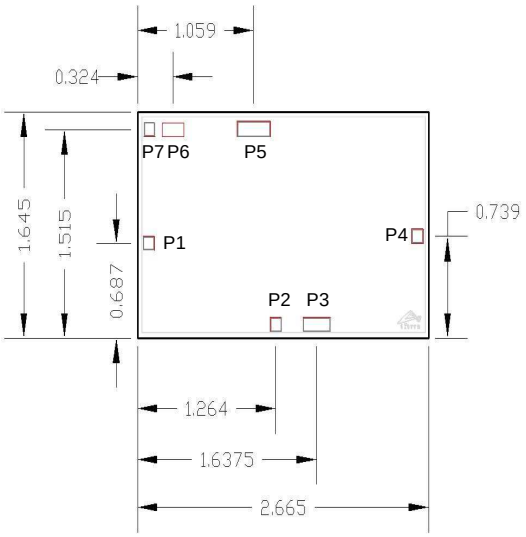
Symbol	Parameters/conditions	Rth_jb (°C/W)	Tch (°C)	MTFF (h)
Rth_jb	Thermal resistance junction-back side of die No RF: DC bias V_{DD} = 9 V, I_{DQ} = 300 mA , P_{DC} = 2.7 W Tbase = 70 C	11	99.7	>> +1E7
Rth_jb	Thermal resistance junction-back side of die RF applied: Saturated power 1 W, V_{DD} = 9 V, Pdiss = 3.8 W Tbase = 70 C	11	111.8	>> +1E7

Chip Layout and Bond Pad Locations

Back of chip
Is RF and DC ground

Pinouts and Pad Dimensions:

P1: RF input (100 x 100 µm)
P2: VGG1, Negative voltage (100 x 100 µm)
P3: Gate low frequency extension (250 x 100 µm)
P4: RF output and Vdd bias (option 2) by means of bias-tee (100 x 100 µm)
P5: Drain low frequency extension (300 x 100 µm)
P6: VDD Positive voltage (option 1) by means of choke (200 x 100 µm)
P7: VGG2 (100 x 100 µm)



All dimensions are in millimeters

Chip size tolerance: ± 20 µm
Chip thickness: 4 mil with a tolerance of ± 0.4 mil

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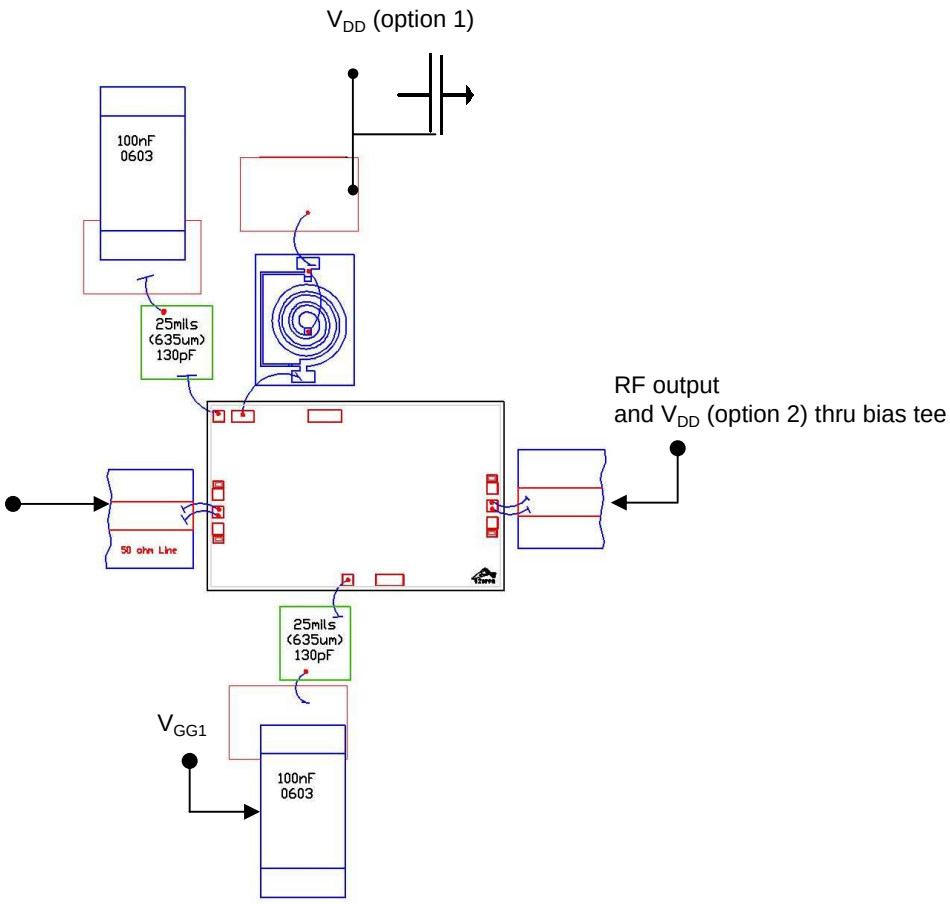
Recommended Assembly Diagram for 1 to 22 GHz Applications



1. For applications from 2 GHz and above, only an inductor (long bond wire) Lc> = 2 nH is necessary to provide drain bias.
2. The bypass capacitor must have a value high enough to isolate the bias supply (= >10 µF)

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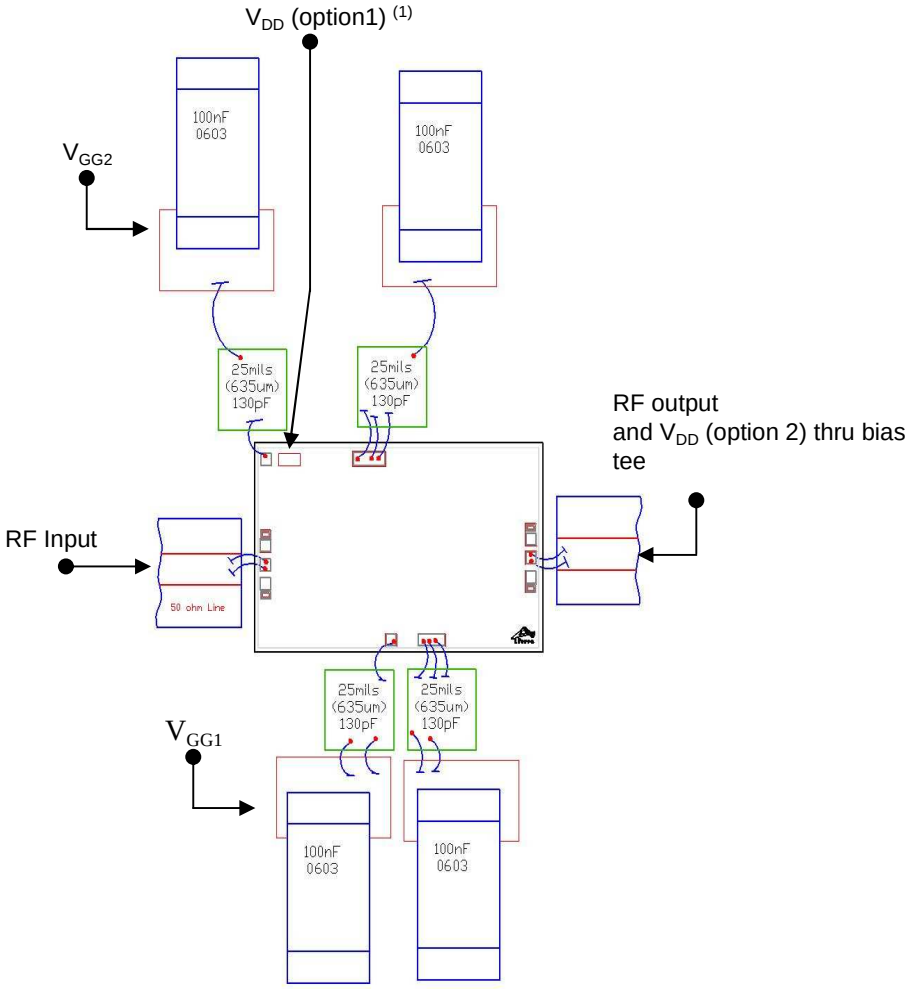
Recommended Assembly Diagram for 10 MHz to 22 GHz Applications



Appropriate low-frequency choke must be applied for 10 MHz applications

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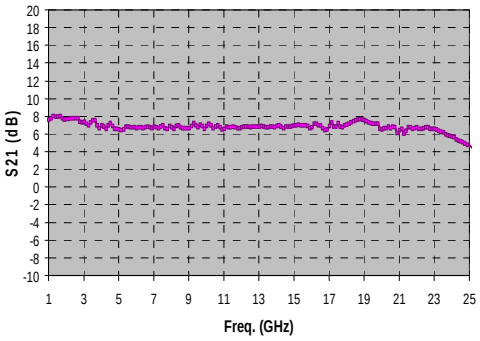
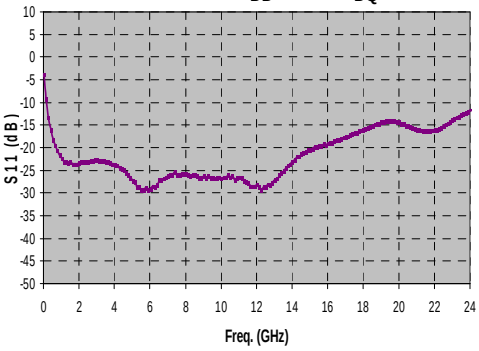
Performance Data, T = 25 ℃

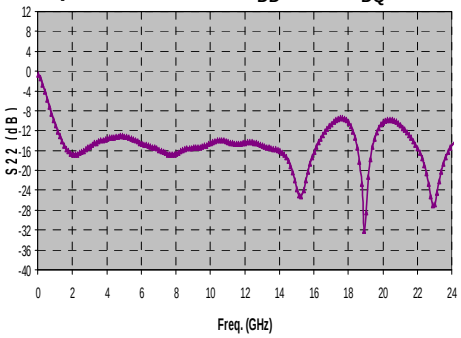
Small signal gain, V_{DD} = 9 V, I_{DQ}= 300 mA



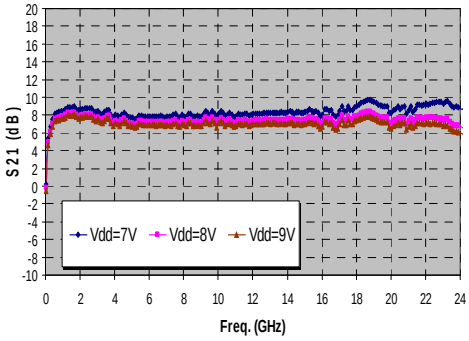
Input return loss, V_{DD} = 9 V, I_{DQ} = 300 mA



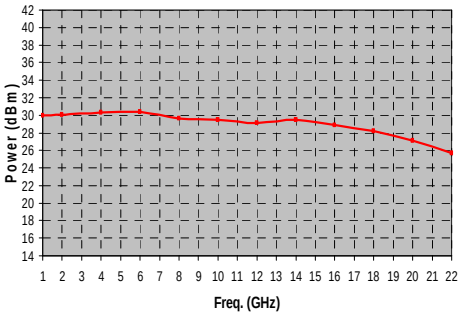
Output return loss, V_{DD} = 9 V, I_{DQ}=300 mA



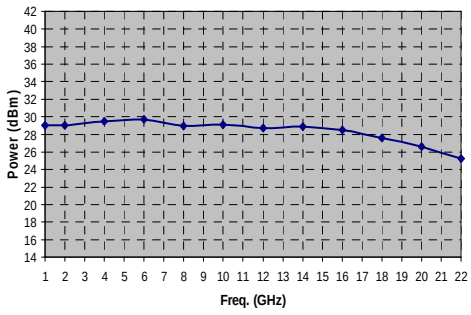
Gain vs. drain bias V_{DD}



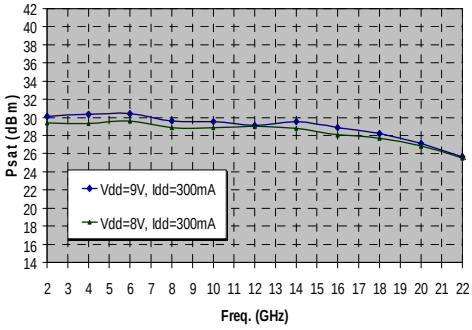
Saturated power, V_{DD} = 9 V, I_{DQ} = 300 mA



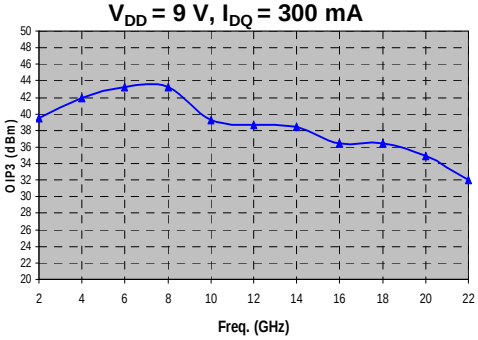
P_{1dB}, V_{DD} = 9 V, I_{DQ}=300 mA



Saturated power vs. drain bias V_{DD}



Output third order intercept point, V_{DD} = 9 V, I_{DQ} = 300 mA



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Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (V_{GG1}) WHILE CORRESPONDING DRAIN VOLTAGE (Vdd) IS PRESENT CAN DAMAGE THE AMPLIFIER.

The following procedure must be considered to properly test the amplifier.

The iT2007 amplifier is biased with a positive drain supply (V_{DD}) and one negative gate supply (V_{GG1}). The recommended bias conditions for the iT2007 is V_{DD}= 9.0 V, I_{DQ} = 300 mA. To achieve this drain current level, V_{G1} is typically biased between –0.7 V and –0.9 V. The gate voltage (V_{GG1}) MUST be applied prior to the drain voltage (V_{DD}) during power up and removed after the drain voltage is removed during the power down. Drain bias V_{DD} can be applied to the drain pad (7). Alternatively, the positive power supply can be applied through an external bias tee to the RF output pad.

For the second gate V_{GG2}, 3.8 V is required approximately (V_{DD}=9 V, V_{GG1}=-0.7 V). In general, $V_{GG2}=V_{DD}/2 - |V_{G1}|$. For example, when V_{DD} =9 V and V_{G1}=-0.7 V, the recommended voltage operation is: V_{GG1} =(9 V/2)-0.7 V=3.8 V.

It is recommended that bias V_{GG2} be applied before or at the same time as V_{DD}.

Low-Frequency Operation

External coupling capacitors are needed at the RF_IN (P1) and RF_OUT (P4) ports. The auxiliary gate pad (P3) and drain pad (P5) are provided to extend performance below 1 GHz. Connect these pads via large external capacitors to ground to maintain input and output VSWR at low frequencies. Do not apply bias to these pads.

Two options are allowed in order to provide the positive drain voltage V_{DD}. **Option 1** uses an on-chip pad (P6) where an appropriate value of inductance (choke) has to be used to maintain good matching over bandwidth, as reported in the assembly diagram. **Option 2** uses an external bias-tee directly from the pad at the RF output. For application as low as 10 MHz a large value of inductance must be used in parallel with appropriate resistors in order to optimize gain flatness.

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment for power devices should utilize gold/tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mil wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 12 mil long corresponding to a typical 2 mil gap between the chip and the substrate material.

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