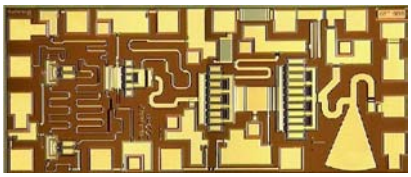
iTR20420
20-42 GHz General Purpose MMIC Amplifier

Description

The iTR20420 is a broadband general purpose driver amplifier designed for use in point to point radio, point to multi-point communications, LMDS, SatCom and other millimeter wave applications. The iTR20420 is a fully matched GaAs MMIC utilizing an advanced 0.15μm gate length PHEMT process.

Features

- Wideband 20 - 42 GHz operation
- 22 dB small signal gain (typ.)
- 23 dBm saturated power output (typ.)
- RF input/output internally matched to 50 Ohms
- Optional bonding configuration for multiplier applications
- Chip Size 1.720 mm x 0.760 mm x 50 μm



Absolute Ratings

Parameter	Symbol	Value	Unit
Positive DC Voltage (+3.5 V Typical)	V_D	+ 5	Volts
Negative DC Voltage	V_G	- 2	Volts
Simultaneous (V_D - V_G)	V_{DG}	+ 7	Volts
Positive DC Current	I_D	600	mA
RF Input Power (from 50 Ω source)	Pin	15	dBm
Operating Base Plate Temperature	Tc	-30 to +85	°C
Storage Temperature Range	Tstg	-55 to +125	°C
Thermal Resistance (Channel to Backside)	Rjc	57	°C/W

Electrical Characteristics[1]

Parameter	Min	Typ	Max	Unit
Frequency Range	20		42	GHz
Drain Supply Voltage (V_D)	2	3.5	5	V
Gate Supply Voltage (V_G)[2]	-2	-0.6	-0.15	V
Small Signal Gain[3]				
(f=20-22 GHz)	18	20		dB
(f=22-42 GHz)	20	22		dB
Gain Variation vs. Frequency		+/-2.5		dB
Power Output at 1 dB Compression		21		dBm

Parameter	Min	Typ	Max	Unit
Power Output Saturated[4]	22	23		dBm
Drain Current at P1dB Compression		355		mA
Drain Current at Psat		362		mA
Input Return Loss (Pin=-20 dBm)		12		dB
Output Return Loss (Pin=-20 dBm)		10		dB

Notes:
1. Operated at 25 °C, 50 Ohm system, V_D=+3.5 V, quiescent current (I_{DQ})=350 mA.
2. Typical range of the negative gate voltage is -0.9 to –0.15 V to set typical I_{DQ} of 350 mA.
3. Production measurements for small signal gain are made over a frequency range of 20 to 40 GHz.
4. Saturated power measurements are not 100% tested, but guaranteed by design.

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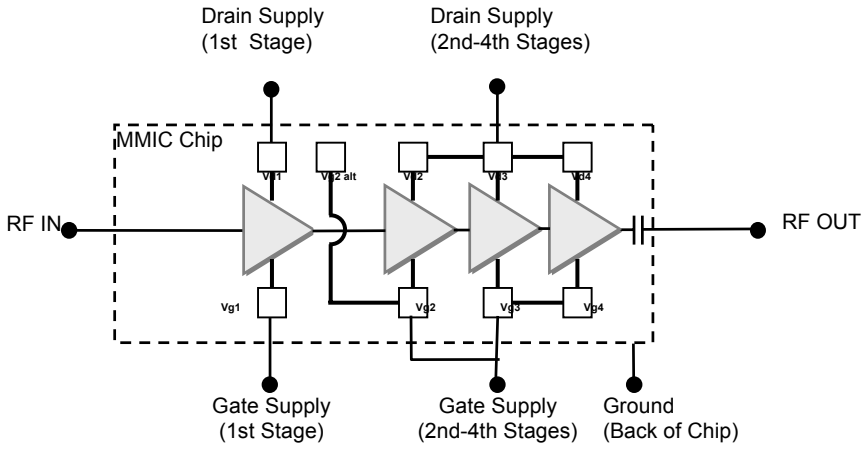
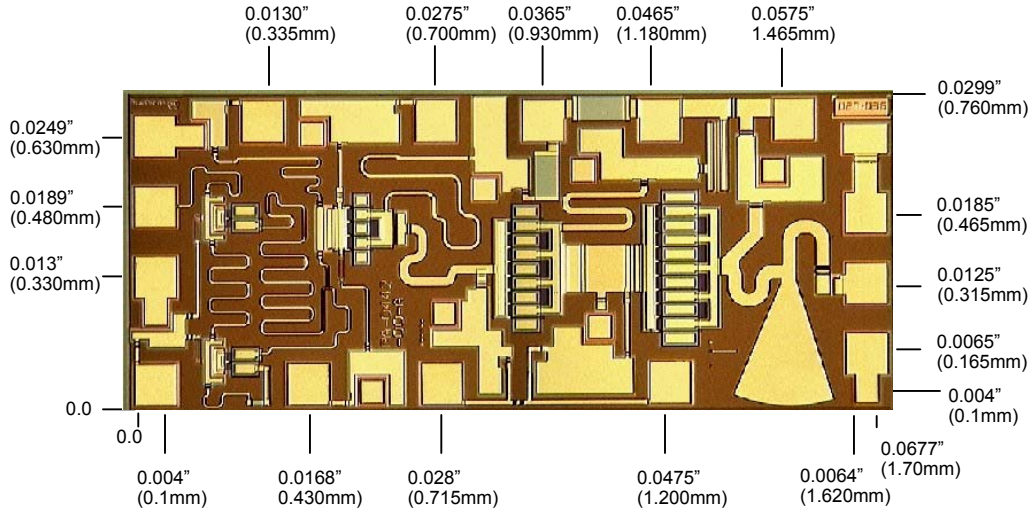
Functional Block Diagram



Chip Layout and Bond Pad Locations

Chip Size=0.0677” x 0.30” x 0.002” (1720 µm x 760 µm x 50 µm)



Back of Chip is RF and DC Ground

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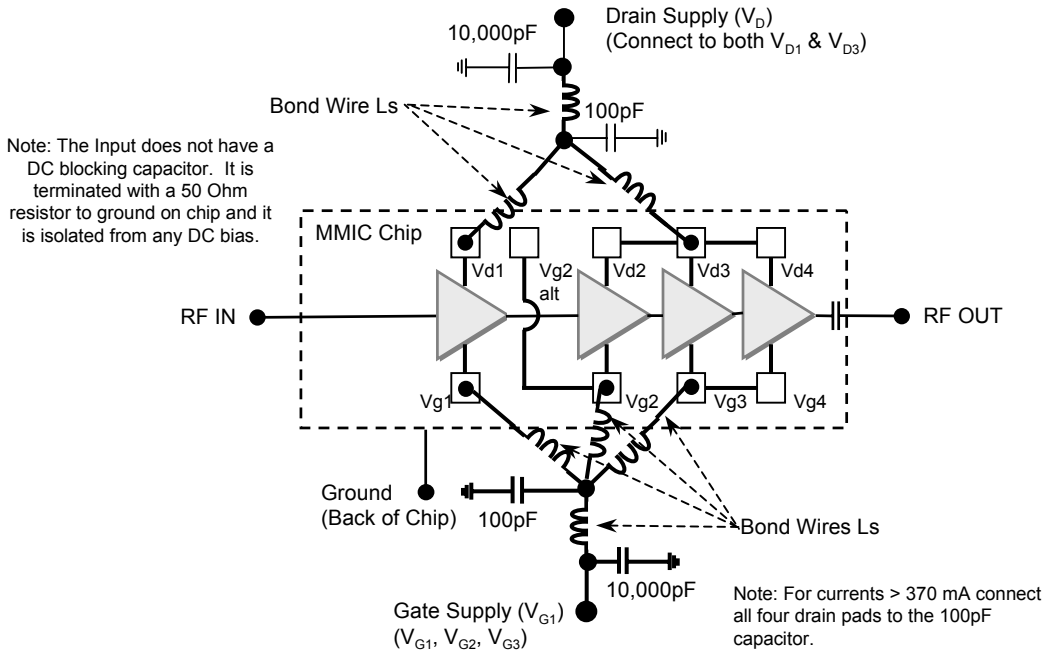
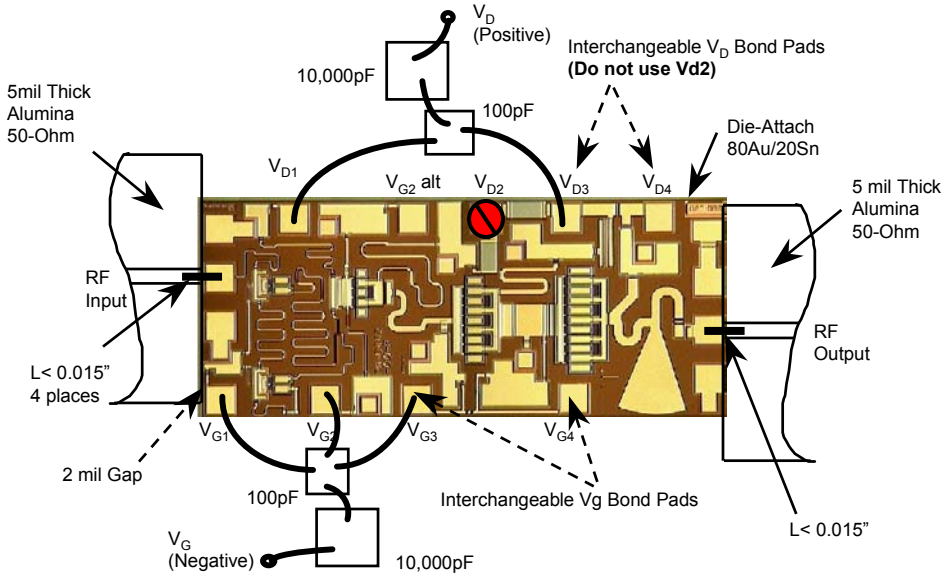
Schematic of Application Circuit



Recommended Assembly and Bonding Diagram



Notes:

1. Die-attach with 80Au/20Sn
2. Use 0.003" x 0.0005" gold ribbon for bonding.
3. RF input and output bonds should be less than 0.015" long with stress relief.
4. For currents > 370 mA connect all drain pads (Vd1, Vd3, & Vd4) to the 100 pF capacitor.
5. Back of chip is DC and RF ground.
6. Do not use Vd2 pad for drain bias connection

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Recommended Procedure
(for biasing and operation)

CAUTION: LOSS OF GATE VOLTAGE (V_G) WHILE DRAIN VOLTAGE (V_D) IS PRESENT CAN DAMAGE THE AMPLIFIER.

The following sequence must be followed to properly test the amplifier:

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the ground of the chip carrier.
Slowly apply negative gate bias supply voltage of -1.5 V to V_G.

Step 3: Slowly apply positive drain bias supply voltage of +3.5 V to V_D.

Step 4: Adjust gate bias voltage to set the quiescent current of I_{DQ}=350 mA.

Step 5: After the bias condition is established, the RF input signal may now be applied at the appropriate frequency band.

Step 6: Follow turn-off sequence of:

(i) Turn off RF input power,
(ii) Turn down and off drain voltage (V_D),
(iii) Turn down and off gate bias voltage (V_G).

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment for power devices should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC Ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012” long corresponding to a typical 2 mil gap between the chip and the substrate material.

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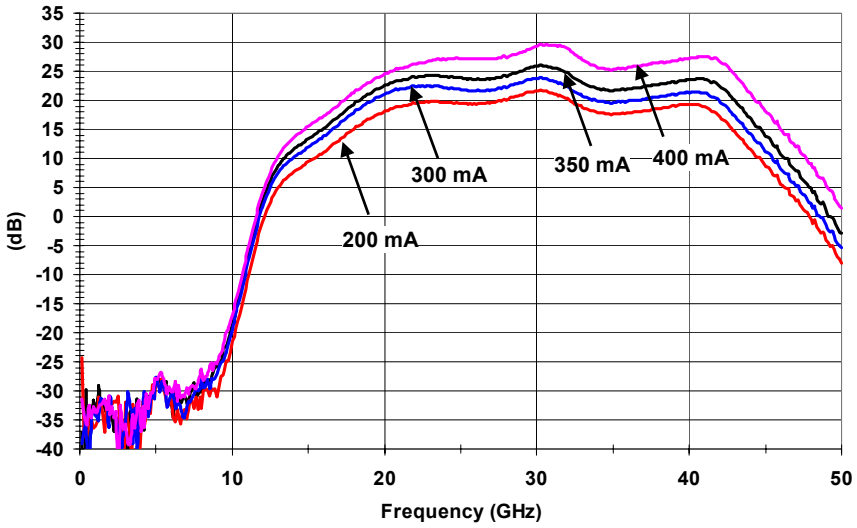
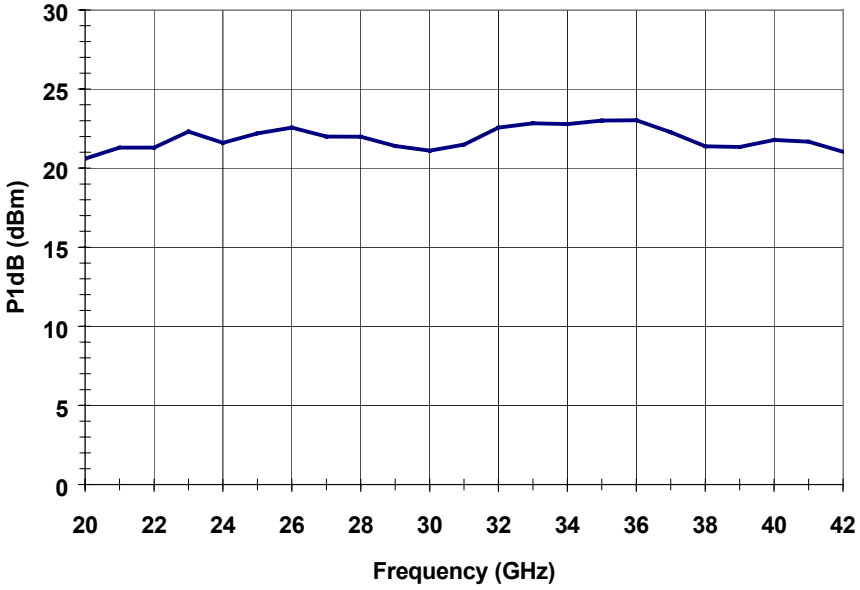
Performance Data

normal amplifier configuration

Typical SS Gain Vs. Frequency Vs. Supply Current
Bias V_D=3.5



Typical Output Power @ 1dB Compression
Bias V_D=3.5 V, I_{DQ}=350 mA



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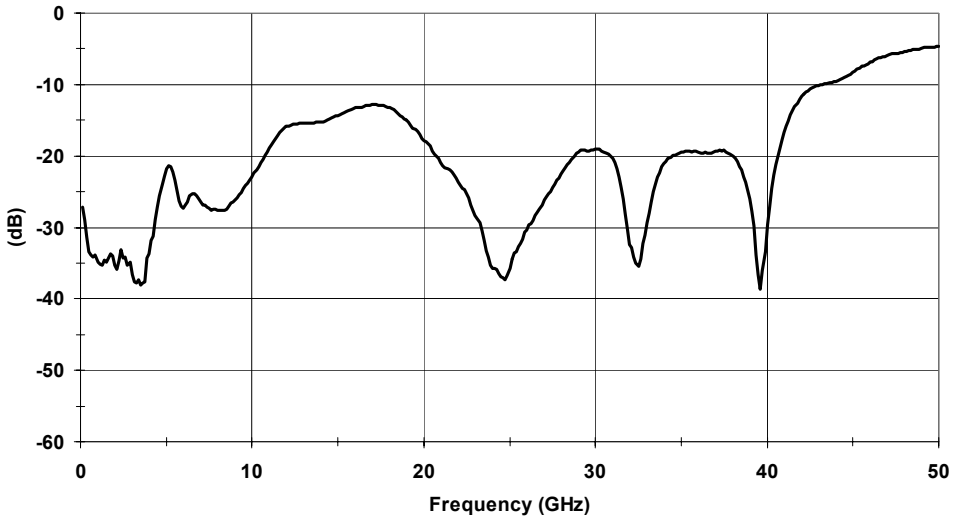
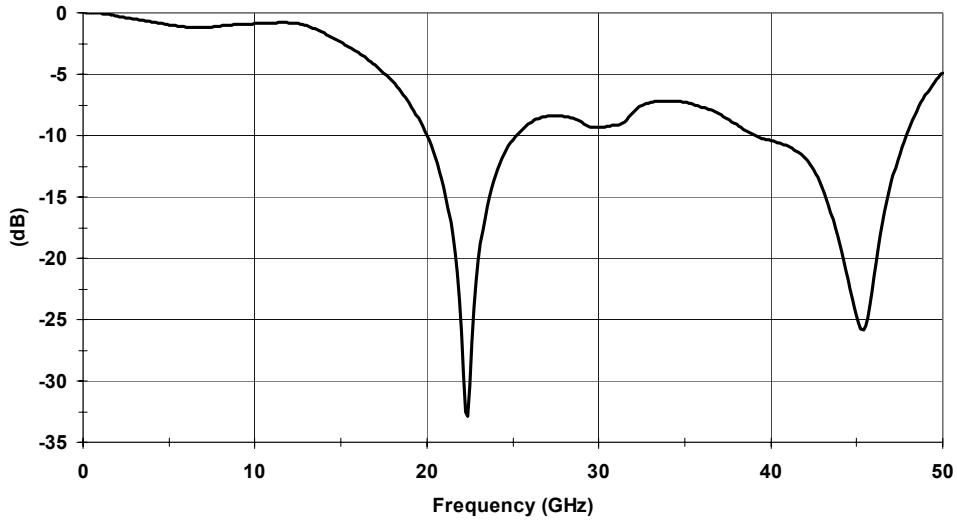
Performance Data

Typical Input Return Loss Vs. Frequency
Bias V_D=3.5 V, I_{DQ}=350 mA



Typical Output Return Loss Vs. Frequency
Bias V_D=3.5 V, I_{DQ}=350 mA



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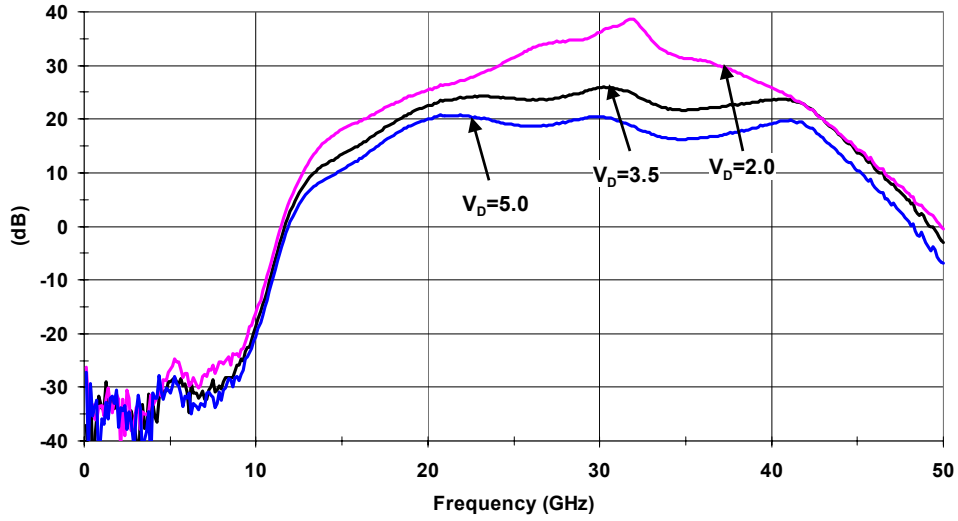
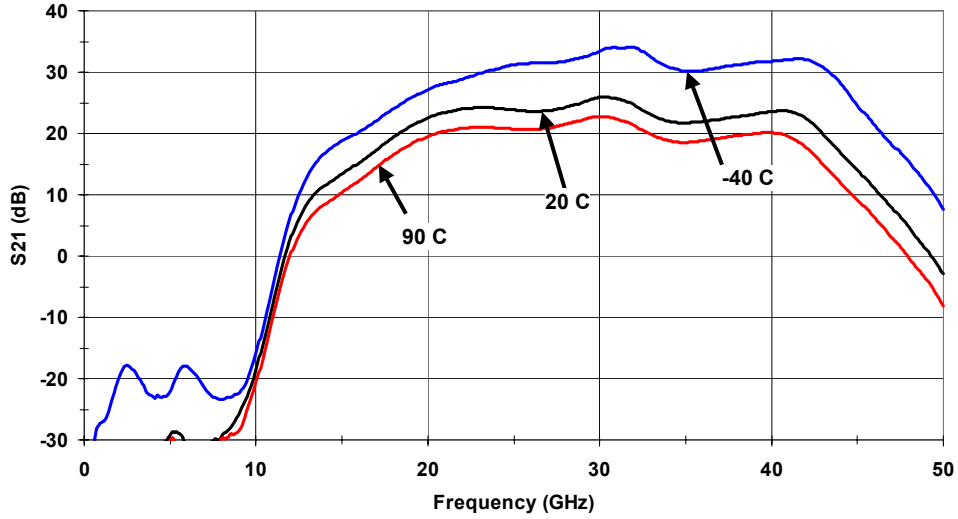
Performance Data

Typical SS Gain Vs. Frequency Vs. Supply Voltage
Supply Current=350 mA



Typical SS Gain Vs. Frequency Vs. Base Plate Temperature
Bias V_D=3.5 V, I_{DQ}=350 mA



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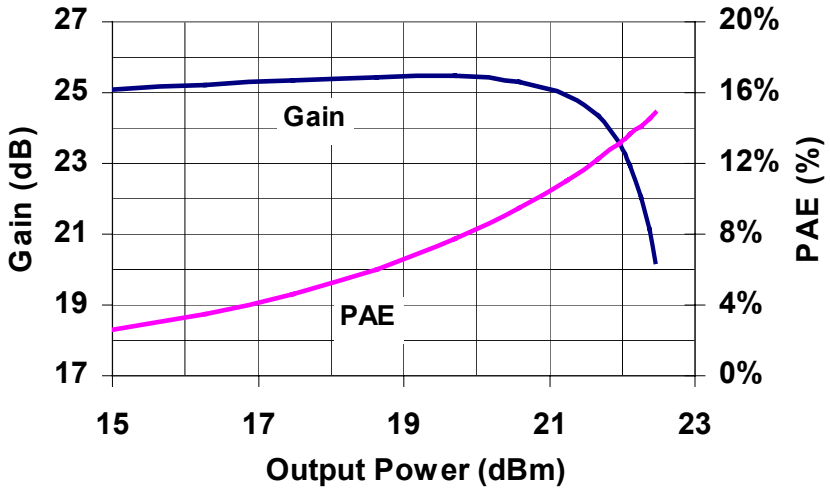
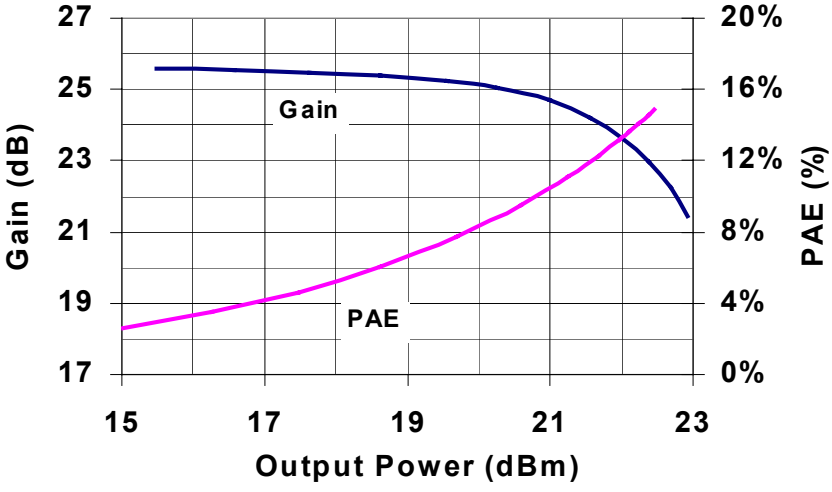
Performance Data

Gain Compression and PAE Vs. Output Power
Frequency=40 GHz, Bias Vd=3.5 V, Id=350 mA



Gain Compression and PAE Vs. Output Power
Frequency=30 GHz, Bias V_D=3.5 V, I_{DQ}=350 mA



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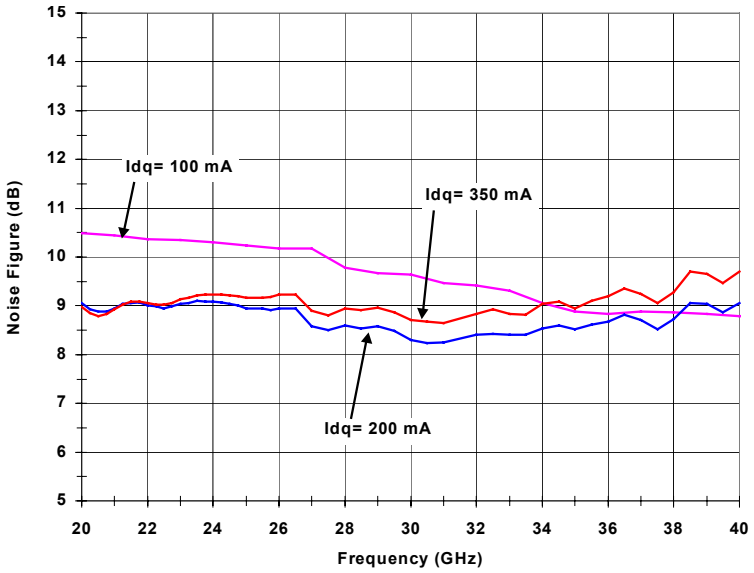
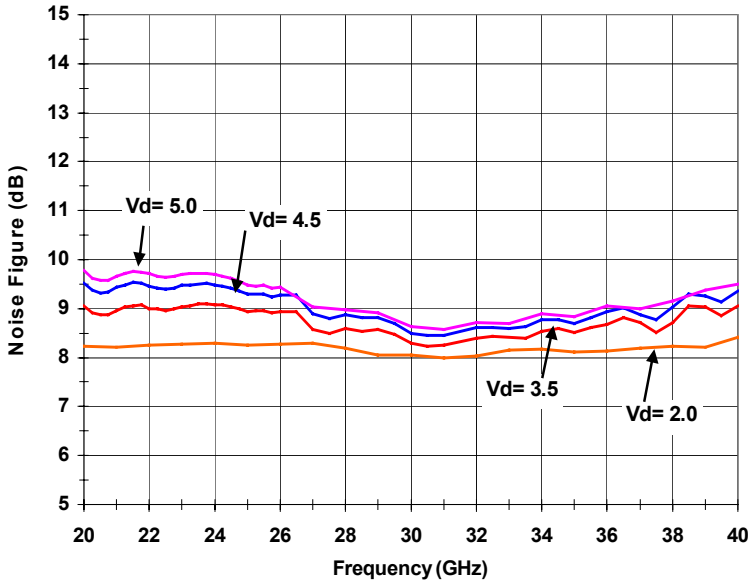
Performance Data

Noise Figure Vs. Frequency Vs. Supply Current
Bias V_D=3.5 Volts



Noise Figure Vs. Frequency Vs. Supply Voltage
Supply Current=200mA



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Application Information
multiplier operation

The iTR20420 can be used as an even harmonic multiplier or as an odd harmonic multiplier depending on the type of DC biasing arrangement being used. Optimum DC bias is applied to peak the desired harmonic which falls into the 20 to 42 GHz passband. The following application information will detail the configuration and procedure for using the iTR20420 as an even harmonic multiplier and as an odd harmonic multiplier. Typical measured data is provided at selected frequencies within the passband with the iTR20420 configured as a doubler and as a tripler.

Multiplier Operation

The iTerra iTR20420 is a four stage general purpose MMIC amplifier covering the 20-42 GHz passband. The amplifier has a steep gain roll off at the band edges and the input return loss of the amplifier is better than 10 dB from 42 GHz down to DC. Any multiplier harmonics, which fall in the passband, will get amplified and any harmonics that fall below the passband will get suppressed.

A deliberate design feature that makes the iTR20420 an effective multiplier is the ability to independently bias the first stage. This feature allows freedom to determine the optimum DC bias condition required to peak the desired harmonic and suppressing the unwanted harmonics. Optimum DC bias conditions depend largely on factors such as fundamental frequency, desired harmonic frequency, input power level, output power level and suppression requirements.

Test Set Up

The basic test set uses a source to provide the input signal at the desired frequency and power level. The DUT was biased either as an even harmonic or odd harmonic operation and the output was observed on a spectrum analyzer. The power of the harmonics was measured using the spectrum analyzer with all the cable losses accounted. Figure 1 shows the basic test set used.

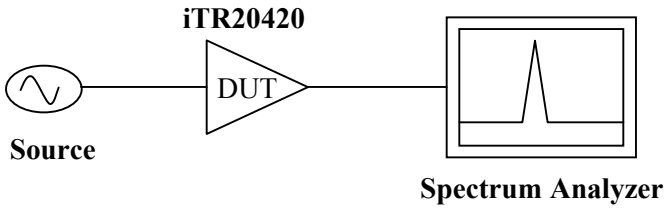

Figure 1. Basic test set up.

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Application Information

multiplier operation

Even Harmonic Operation

Even harmonics are generated whenever the symmetry of the input signal waveform is distorted. This is accomplished by biasing the first stage operating point in a region of the I-V curve where the device is near pinch-off. In this condition, the first stage becomes a half wave rectifier where conduction only occurs on positive half cycles of the input waveform. Thus, presenting an asymmetrical waveform consisting mainly of positive half cycles which is rich in even harmonics to the remaining stages of the amplifier.

For most even harmonic multiplier operations, the first stage is usually pinched off and the remaining stages are biased as a linear amplifier. As an example, the iTR20420 was evaluated as a doubler.

In the doubler operation, two drain voltages of +3.5V were used: One for first stage (V_{D1}) and the other (V_{D2}) for the remaining 3 stages tied together as shown in Figure 2. Independent biasing of the first stage was achieved by using two separate gate voltages. V_{G1} was used for stage one and set to V_{G1}=-1.0V (near pinch-off). V_{G2} was used for the remaining three stages. VG2 was adjusted until $_{IDQ}$=330mA.

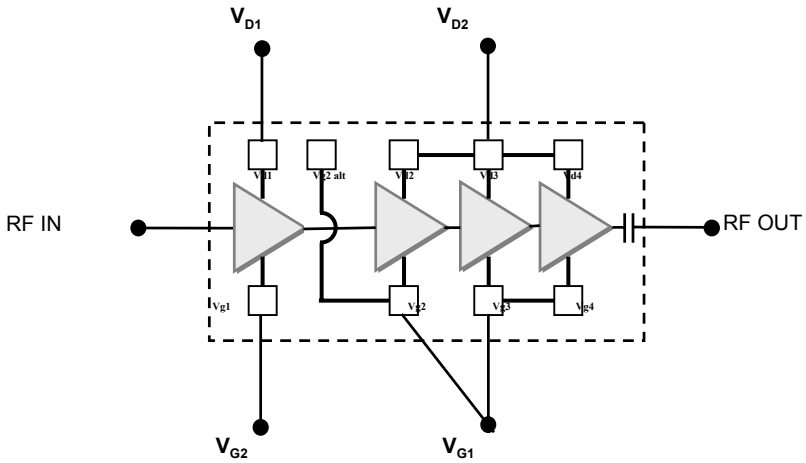

Figure 2. iTR20420 configured as doubler.

For each input frequency and input power level, V_{G1} was adjusted to peak the second harmonic. Small changes in V_{G2} and V_{D2} at this point help in suppressing odd harmonics. Figure 3 shows the doubler performance over the 20 to 42 GHz band for a fixed input power level of +12 dBm. The graph shows doubled frequencies with output power levels greater than +16dBm over the 20-42 GHz band. The graph also shows the increasing power level of the fundamental at the higher end of the band since the fundamental frequency approaches the lower band edge of the amplifier passband. Based on these measurements the iTR20420 can be used a doubler to give desired frequencies anywhere in the 20-42 GHz band with a conversion gain up to 8 dB and second harmonic power levels up to 20 dBm.

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Application Information

multiplier operation

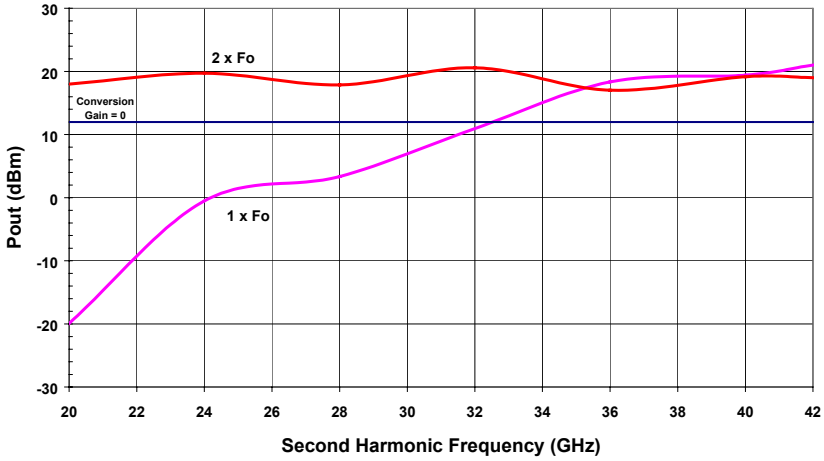

Figure 3. Measured Doubler Performance.

Odd Harmonic Operation

Odd harmonics are generally associated with a square wave. The iTR20420 is biased in such a way that causes the clipping of the input sine wave to closely approximate a square wave provided a high input drive level is maintained. If biased in a manner, which causes the input waveform to be clipped equally in the positive and negative cycles, then a symmetrical square wave will be approximated which contains odd harmonics.

As an example, the iTR20420 was biased as a tripler over the 20-40GHz band at selected frequencies. In this mode of operation all the drains voltages (V_{D1} and V_{D2}) were tied together and all the gate voltages were tied together as shown in Figure 4.

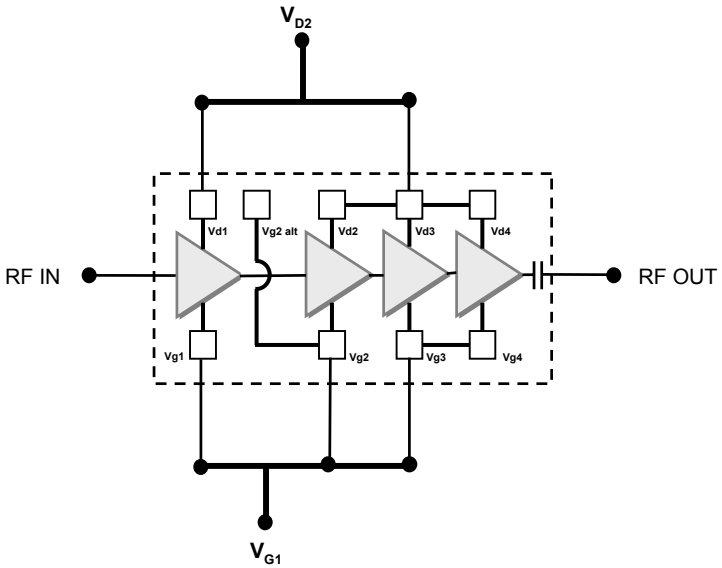

Figure 4. iTR20420 configured as tripler.

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Application Information

multiplier operation

The test set up for this mode of operation is as shown in Figure 1.The biasing procedure requires the gate voltage V_{G1} to be initially set to –1.0V. Next the drain voltage V_{D1} was set to +2.0V. The input frequency was selected to give the desired tripled output and the input drive level was set to +14dBm. The output of the iTR20420 was observed and the harmonics of the input frequency were visible on the spectrum analyzer display. The gate voltage V_{G1} was adjusted gradually to peak the third harmonic. Lowering V_{G1} resulted in peaking the third harmonic. Then the drain voltage V_{D1} was adjusted to tweak the power level of the third harmonic. Tweaking V_{G1} and V_{D1} at this point resulted in further optimization of the desired harmonic or suppression of the unwanted harmonic as required. The range for V_{G1} was between –0.1 to –0.6V and the range for V_{D1} was between +1.1 to +1.8V. The above procedure was repeated for each input frequency tested.

Figure 5 shows the tripled output for the iTR20420 biased as described above. Input frequencies were selected to give tripled frequencies falling in the 21 to 39 GHz band. The graph shows tripled output powers greater than +10dBm up to 39 GHz. The power levels of the first and second harmonics were also plotted to show the level of suppression of the unwanted harmonics. The graph shows for a tripled frequency of 30 GHz the output power was +14 dBm, the fundamental (10GHz) power level was –17 dBm and the second harmonic (20 GHz) power level was +3 dBm. The conversion gain for the tripled output at 30GHz was 0dB. For tripled frequencies between 21 to 39GHz, the conversion gain was better than –4 dB.

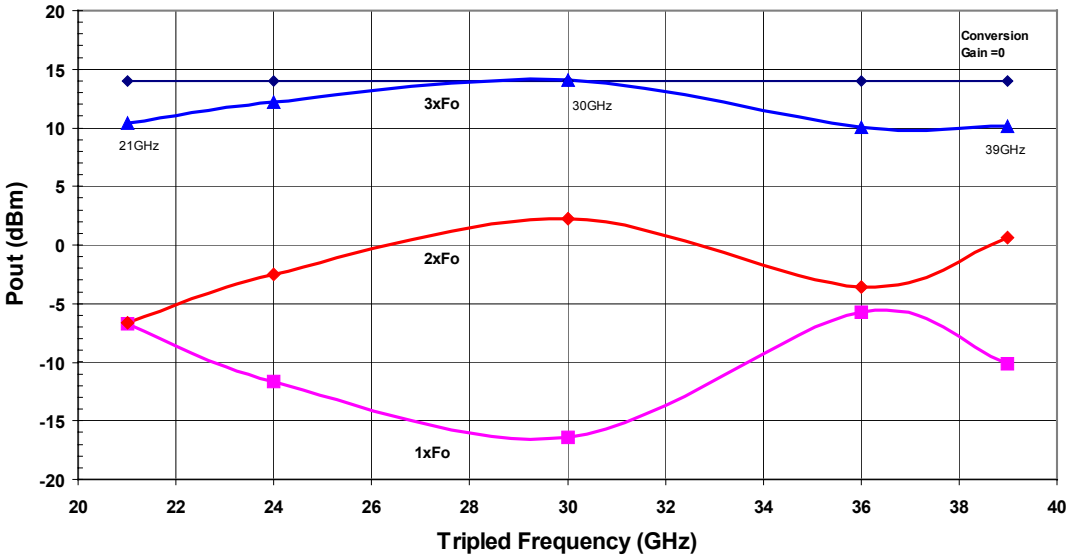

Figure 5. Measured Tripler Performance.

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