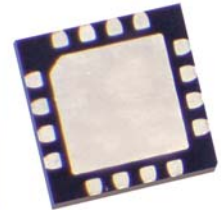


## Description

The iT3012 is a packaged differential-to-single-ended amplifier designed for use as an optical modulator predriver with limiting functionality in 10.7 Gb/s and 12.5 Gb/s (OC-192) optical transmitters and receivers. It allows single-ended input signals of 350 mVpp to 900 mVpp or differential signals of 250 mVpp to 1800 mVpp to be limited at a constant single-ended output voltage of 1.9 Vpp. It provides output voltage control and allows external offset correction. iT3012 also provides excellent linear performance when operating at lower output voltages. Both AC and DC input coupling are allowed. DC-coupled SCFL differential input (input "high" voltage = 0 V, input "low" voltage = -900 mV) is allowed.

## Features

- ❖ Limiting function with 1.9 Vpp single-ended output
- ❖ 3 dB bandwidth: 8 GHz
- ❖ Single-ended Gain: 17.5 dB
- ❖ Standard bias supply levels: -5 V or -5.2 V, +5 V
- ❖ Power consumption: 665 mW
- ❖ Low group delay and jitter
- ❖ Output voltage control
- ❖ AC and DC input coupling (SCFL compatible)
- ❖ AC and DC output coupling
- ❖ Low-cost JEDEC QFP-N (MO-220) package



## Absolute Maximum Ratings

Symbol	Parameters/conditions	Min.	Max.	Units
V <sub>ee</sub>	Power supply voltage	-8	0	V
V <sub>cc</sub>	Power supply voltage	0	8	V
V <sub>d</sub>	Applied voltage at data input (differential)		3	V
V <sub>m</sub>	Applied voltage at data input (single ended)		1.5	V
I <sub>DC IN (+),(-)</sub>	Offset control current		5	mA
T <sub>ch</sub>	Maximum channel temperature		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

## Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
T <sub>c</sub>	Operating temperature range (T <sub>case</sub> )	0		85	°C
V <sub>ee</sub>	Negative power supply voltage	-5.45	-5	-4.75	V
V <sub>cc</sub>	Positive power supply voltage	4.75	5	5.25	V
V <sub>cb2</sub>	First internal bias control voltage		0		V
I <sub>ee</sub>	Negative supply current	86	101	116	mA
I <sub>cc</sub>	Positive supply current	30	35	40	mA
V <sub>DC IN</sub>	Offset control voltage	-5		5	V
V <sub>ctrl</sub>	Voltage control pin	-2.7		0	V
V <sub>m</sub>	Applied peak-peak voltage at data input (single ended)	350		900	mV
V <sub>d</sub>	Applied peak-peak voltage at data input (differential)	250		1800	mV
V <sub>indc</sub>	DC input voltage (with DC-coupled input)	-0.5		0	V
R	Data bit rate			12.5	Gb/s



# iT3012 8 GHz, Differential-to-Single-Ended Amplifier

## Electrical Characteristics

At ambient temperature  
V<sub>ee</sub>=-5 V, V<sub>cc</sub>=+5 V

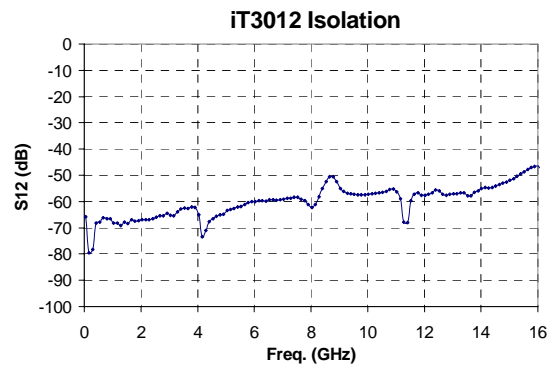
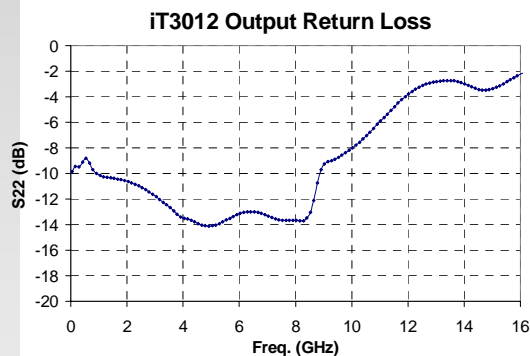
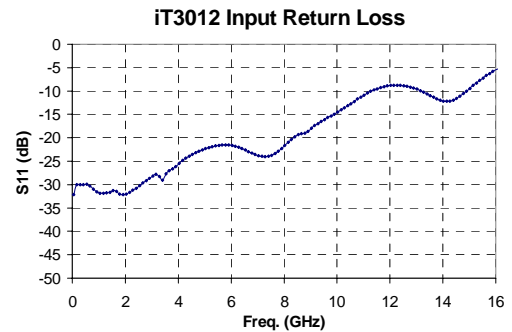
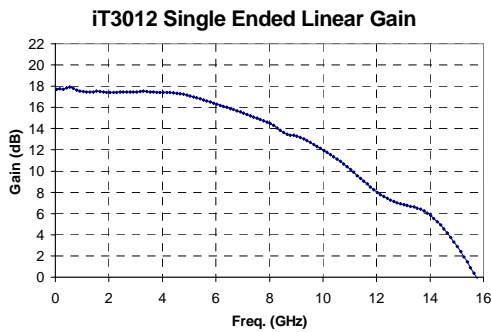
Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
P	Power consumption	565	665	765	mW
Z <sub>DCin</sub>	Input impedance at DCin, /DCin	900	1000	1100	Ohm
G	Single ended small signal gain	16.5	17.5		dB
B <sub>3dB</sub>	3 dB bandwidth	7	8		GHz
RL <sub>in</sub>	Input return loss (up to 10 GHz)	15	20		dB
RL <sub>out</sub>	Output return loss (up to 10 GHz)	8	10		dB
V <sub>out</sub>	Output peak-peak voltage (single ended) (V <sub>ctrl</sub> = -2.7V for max. output voltage)	1.75	1.9		V
ΔV <sub>out</sub>	V <sub>out</sub> sensitivity vs bias (V <sub>ee</sub> =-5 V +/-5%, V <sub>cc</sub> =5 V +/-5%)			+/-11	%
V <sub>outdc</sub>	DC output voltage (DC coupled to 50 ohm load)	200	300	400	mV
Tr <sub>se</sub>	Output rise time (single ended)		28	32	psec
Tf <sub>se</sub>	Output fall time (single ended)		20	28	psec
J <sub>RMS</sub>	RMS jitter degradation (*)		1	1.5	psec

$$(*) J_{RMS} = \sqrt{(J_{RMS\_dut})^2 - (J_{MRS\_thru})^2}$$

## S-Parameter Data

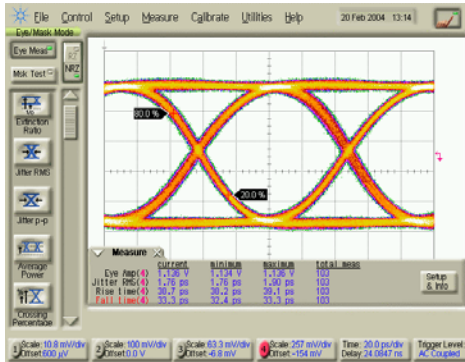
Measured on connectorized evaluation board

V<sub>ee</sub>=-5 V, V<sub>cc</sub>=+5 V

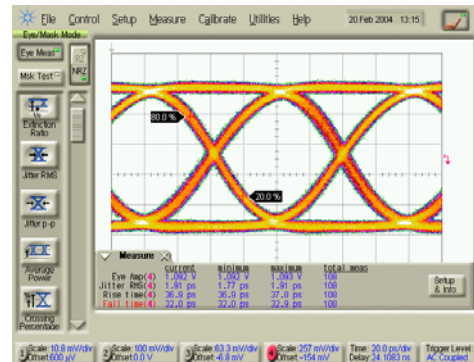


### Eye Diagram Performance

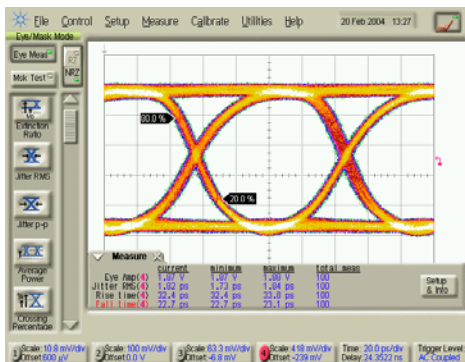
Vee=-5 V, Vcc=+5 V



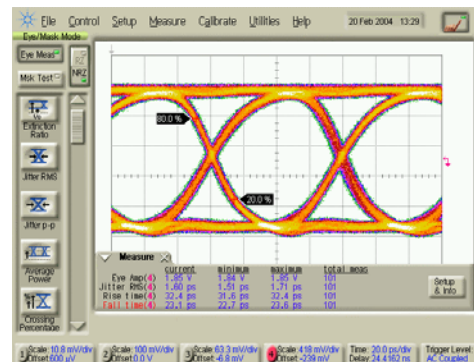
Linear performance  
Bit rate: 10.7 Gb/s  
Vin=±75 mVpp, Vout=±1.1 Vpp



Linear performance  
Bit Rate: 12.5 Gb/s  
Vin=±75 mVpp, Vout=±1.1 Vpp

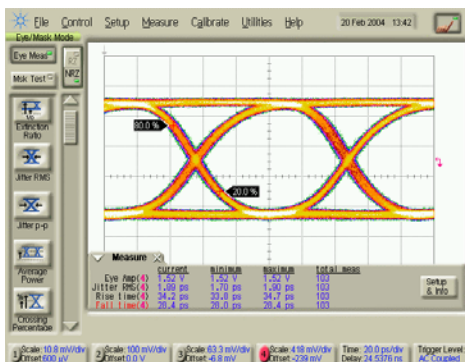


Saturated performance  
Bit Rate: 10.7 Gb/s  
Vin=±400 mVpp, Vout=±1.9 Vpp

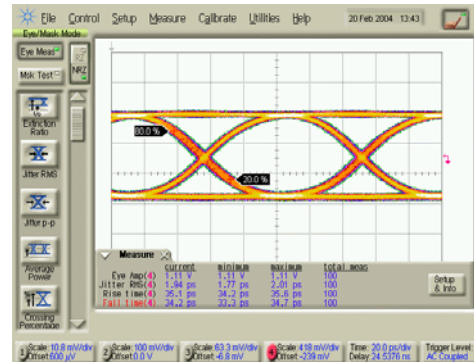


Saturated performance  
Bit Rate: 12.5 Gb/s  
Vin=±400 mVpp, Vout=±1.9 Vpp

### Voltage Control

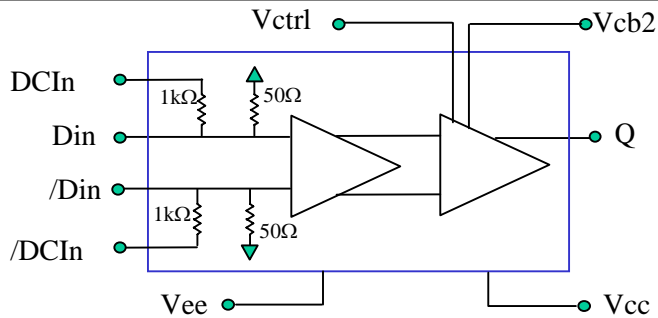


Bit rate: 10.7 Gb/s  
Vtrl=-1.5 V, Vout=1.7 Vpp



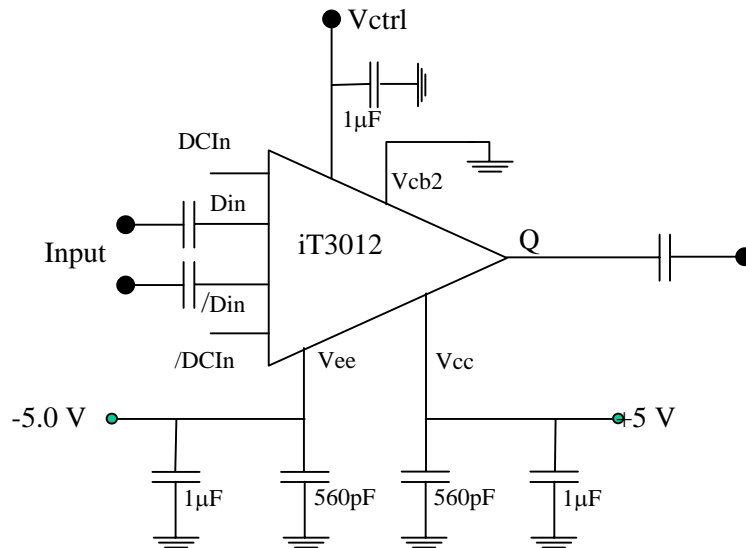
Bit rate: 10.7 Gb/s  
Vtrl=-1.1 V, Vout=1.0 Vpp

## System Diagram



## Recommended Operational Setup

DC blocking capacitors optional



### Bias Conditions

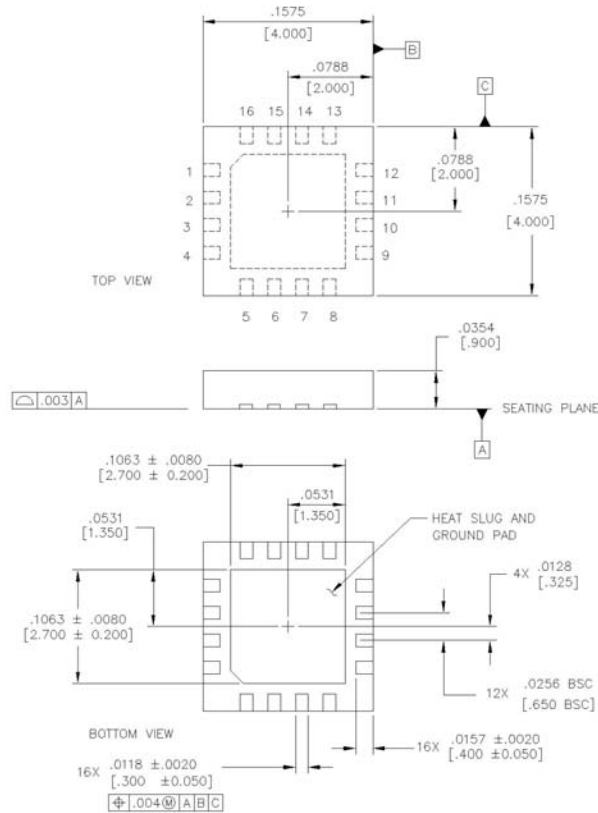
#### For Vee = -5 V Bias Condition

- Apply +5.0 V at Vcc
- Apply -5 V at Vee
- Vcb2 = 0 V
- Vctrl = -2.7 V or open for maximum output voltage
- Vctrl from -2.7 V to -1 V for output voltage control

#### For Vee = -5.2 V Bias Conditions

- Apply +5 V at Vcc
- Apply -5.2 V at Vee
- Vcb2 = 0V
- Vctrl = -1.8V for maximum output voltage
- Vctrl from -1.8 V to -1 V for output voltage control

### Package Drawing, Pinouts



#### Pin Outs:

P1: GND	P9: GND
P2: Din (RF input)	P10: N/C
P3: /Din (/RF input)	P11: Q (RF out)
P4: GND	P12: GND
P5: /DCin	P13: Vcb2
P6: Vee	P14: Vctrl (voltage control)
P7: N/C	P15: Vcc
P8: N/C	P16: DCin

- NOTES: (UNLESS OTHERWISE SPECIFIED)
1. DIMENSIONS: INCHES [mm]
  2. EXCEPT WHERE NOTED, TOLERANCE ON DIMENSIONS ARE:  $\pm \frac{.0039}{[0.100]}$