iT3022D
10 GHz, 6 dB-Gain Differential Buffer

Description

The iT3022D is a differential buffer amplifier designed for use in applications up to 10 GHz. It supports fully differential operation as well as single-ended-to-differential and single-ended-to-single-ended operation. The iT3022D is ideal for any RF application in which a highly-linear, low-gain differential buffer is required, such as microwave communications, test equipment, digital receiver systems, front ends for digital sampling oscilloscopes, and single-ended differential transformers. The amplifier provides excellent linear performance. AC and DC input coupling are accommodated as well as DC-coupled SCFL differential inputs.

Features

- Buffer function
- 3-dB bandwidth: 10 GHz
- Single-ended gain: 6 dB
- Standard bias supply: -5 V, +5 V
- Power consumption: 1.35 W
- 1% total harmonic distortion at Pout: 0 dBm
- Low group delay
- Low jitter
- CMRR: >20 dB at 10 GHz
- AC and DC input coupling (SCFL compatible)
- AC and DC output coupling

Absolute Maximum Ratings

Symbol	Parameters/conditions	Min.	Max.	Units
Vee	Power supply voltage	-8	0	V
Vcc	Power supply voltage	0	8	V
Vd	Applied voltage at data input (differential)		3	V
Vm	Applied voltage at data input (single ended)		1.5	V
Ioffset (+),(-)	Offset control current		5	mA
Tch	Maximum channel temperature		150	℃
Tstg	Storage temperature	-65	150	℃

Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
Tc	Operating temperature range (Tcase)	0		85	°C
BR	Bit error rate			12.5	GHz
Vee	Negative power supply voltage	-5.25	-5	-4.75	V
Vcc	Positive power supply voltage	4.75	5	5.25	V
Iee	Negative supply current	115	135	155	mA
Icc	Positive supply current	115	135	155	mA
V_{offset} (+)/(-)	Offset control voltage	-5		5	V
Vm	Applied peak-peak voltage at data input (single ended)		300	500	mVpp
Vd	(differential)		300	500	mVpp
HL s.e.	High Level (single-ended input)	0	150	250	mV
HL diff.	High Level (differential input)	-500	150	150	mV
	Input/output interface	AC and DC coupled			

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Electrical Characteristics

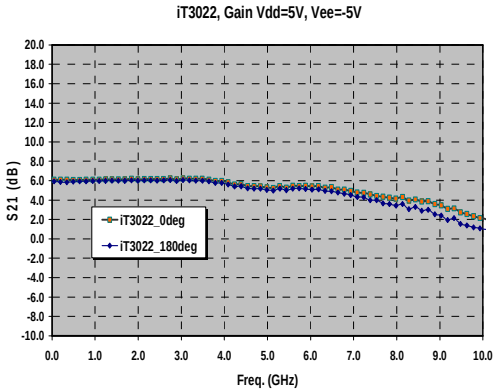
At ambient temperature Vee =-5 V, Vcc = +5 V (Measured on connectorized evaluation board)

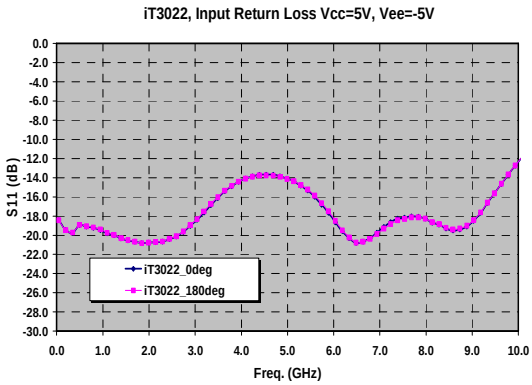
Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
P	Power consumption	1150	1350	1550	mW
Zin offset	Input impedance at offset pins	1350	1500	1650	Ohm
G	Small signal gain	5	6		dB
ΔG	Gain flatness (DC to 1 GHz)			0.4	dBpp
B3dB	3 dB bandwidth	9	10		GHz
RLin	Input return loss (up to 10 GHz)	13	15		dB
RLout	Output return loss (up to 10 GHz)	13	15		dB
ΔVout	Vout sensitiviy vs bias (Vee = -5 V +/-5%, Vcc = 5 V +/-5%)			+/-11	%
Voutdc	DC output voltage (DC coupled to 50 ohm load)	10	70	180	mV
Trse	Output rise time (single-ended)		40	45	ps
Tfse	Output fall time (single-ended)		45	50	ps
NF	Noise figure		7.5	8	dB
CMRR	Common mode rejection ratio	20			dB

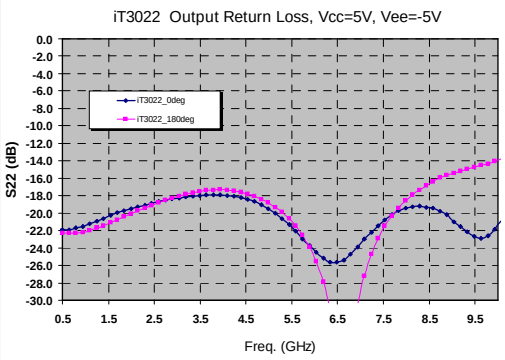
S-Parameter Data

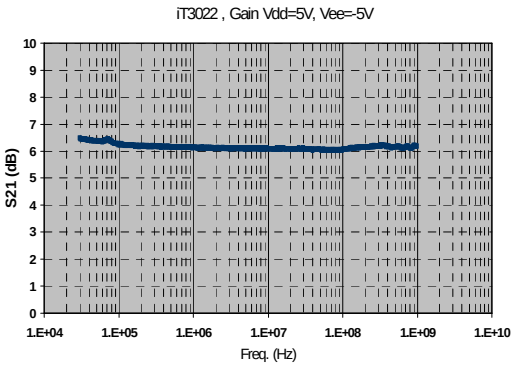
At ambient temperature Vee = -5 V, Vcc = +5 V

Measured on connectorized evaluation board. Single-ended input, inverting (/Q), and non-inverting (Q) outputs are shown in the same plot.









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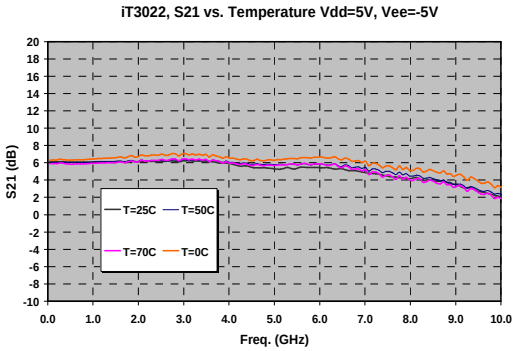
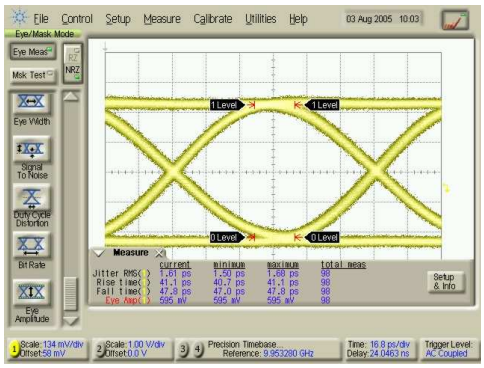
S21 vs. Temperature

Vee = -5 V, Vcc = +5 V

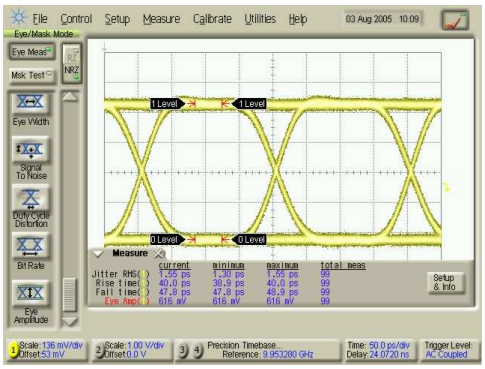


Eye Diagram Performance

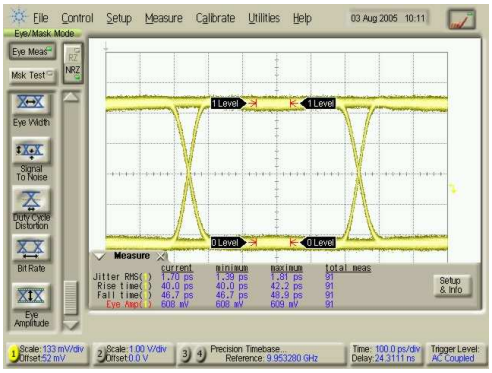
Vee = -5 V, Vcc = +5 V



Linear performance
Bit rate: 10 Gb/s
Vin = 300 mVpp, Vout = 600 mVpp



Linear performance
Bit rate: 5 Gb/s
Vin = 300 mVpp, Vout = 600 mVpp



Linear performance
Bit rate: 2 Gb/s
Vin = 300 mVpp, Vout = 600 mVpp

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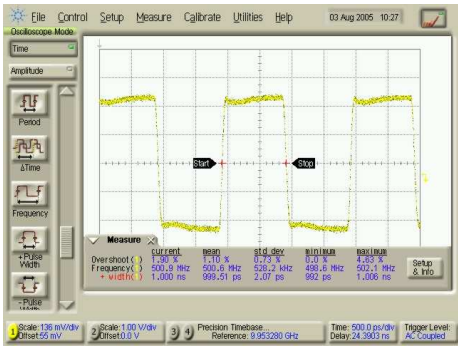
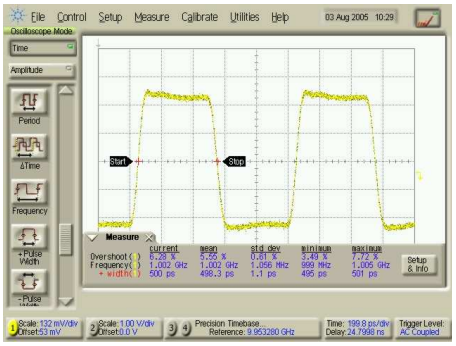
Time Domain Performance

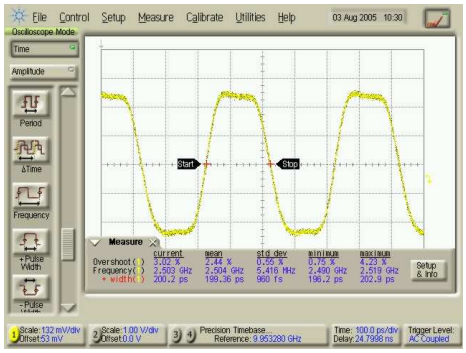
Vee = -5 V
Vcc = +5 V



Bit rate: 1 Gb/s
Vin = 300 mVpp, Vout = 600 mVpp



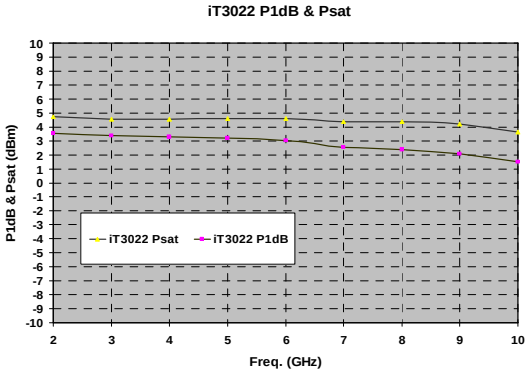
Bit rate: 2 Gb/s
Vin = 300 mVpp, Vout = 600 mVpp



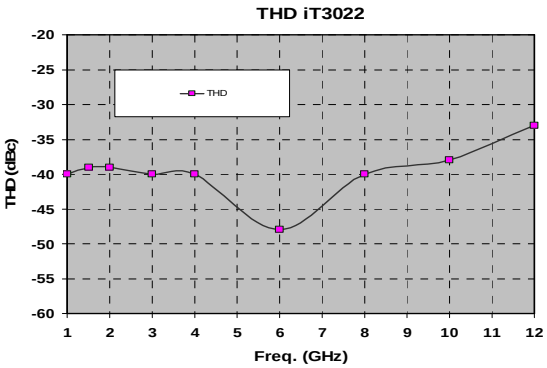
Bit rate: 5 Gb/s
Vin = 300 mVpp, Vout = 600 mVpp

Power Performance and Total Harmonic Distortion

At ambient temperature
Single-ended input
Vee = -5 V
Vcc = +5 V



P1dB and Psat vs. frequency



Total harmonic distortion
Single-ended Pout = 0dBm

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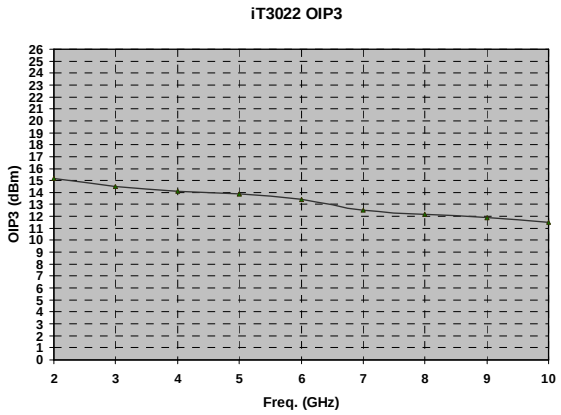
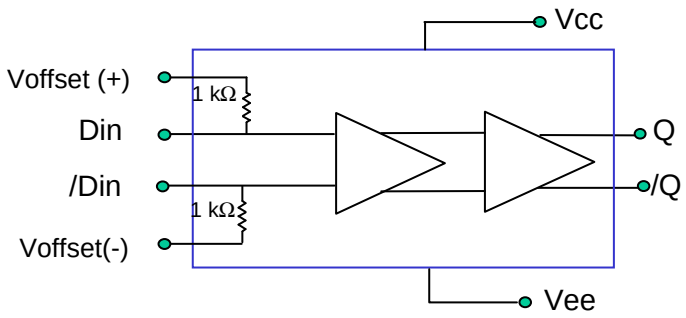
OIP3 Data

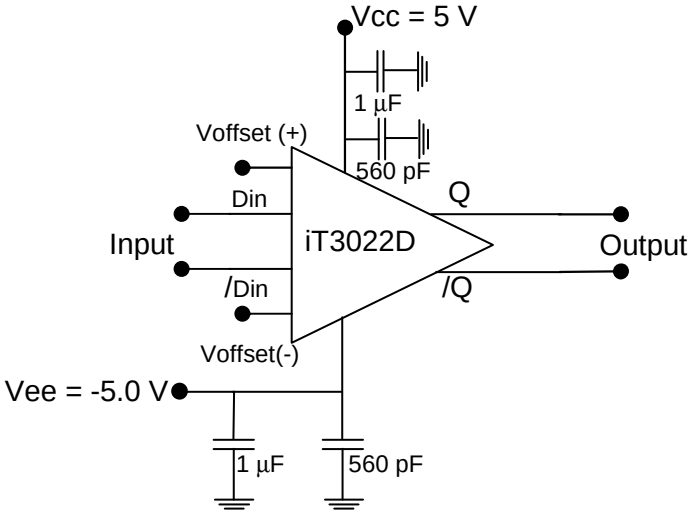
Ambient temperature
Single-ended input
Vee = -5 V, Vcc = +5 V



Device Diagram



Recommended Operational Setup



Bias sequence

- Apply +5.0 V at Vcc
- Apply -5 V at Vee

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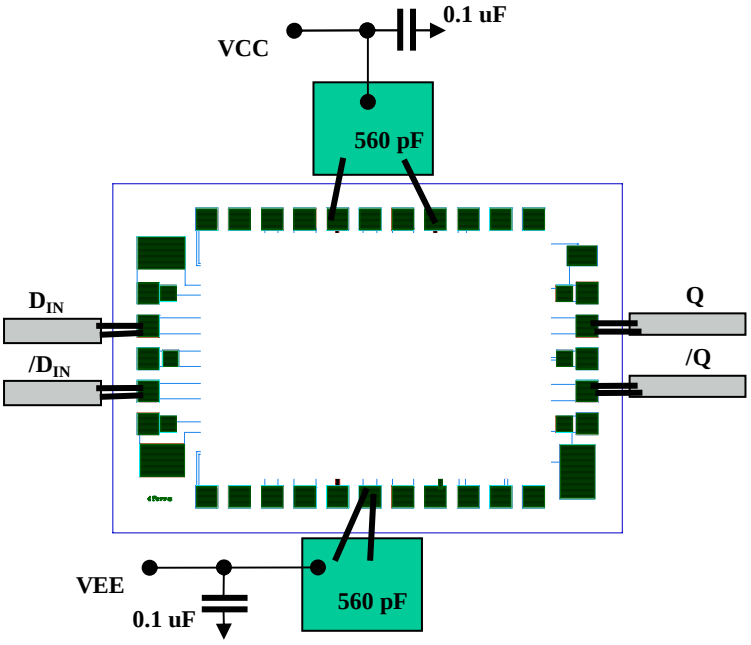
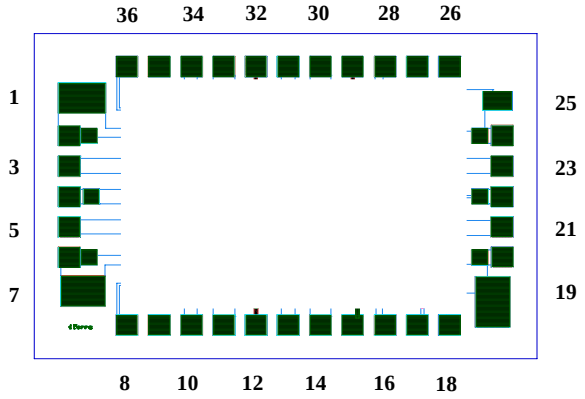
Assembly Diagram





Pin	Designation	Description	Pin	Designation	Description
P1	GND	Ground	P19	GND	Ground
P2	GND	Ground	P20	GND	Ground
P3	Vinp	Data Input +	P21	Voutn	Data Output -
P4	GND	Ground	P22	GND	Ground
P5	Vinn	Data Input -	P23	Voutp	Data Output +
P6	GND	Ground	P24	GND	Ground
P7	GND	Ground	P25	GND	Ground
P8	Vimn-	Input DC Offset Control -	P26	Not used	
P9	Not used		P27	Not used	
P10	GND	Ground	P28	GND	Ground
P11	GND	Ground	P29	GND	Ground
P12	Vcc1	Positive Supply (+5V)	P30	Vcc3	Positive Supply (+5V)
P13	Vee1	Negative Supply (-5 V)	P31	Vee1	Negative Supply (-5 V)
P14	GND	Ground	P32	GND	Ground
P15	Vcc2	Positive Supply (+5V)	P33	Vcc4	Positive Supply (+5V)
P16	GND	Ground	P34	GND	Ground
P17	Ref. Res	50ohm resistor	P35	Not used	
P18	Not used		P36	Vimn+	Input DC Offset Control +

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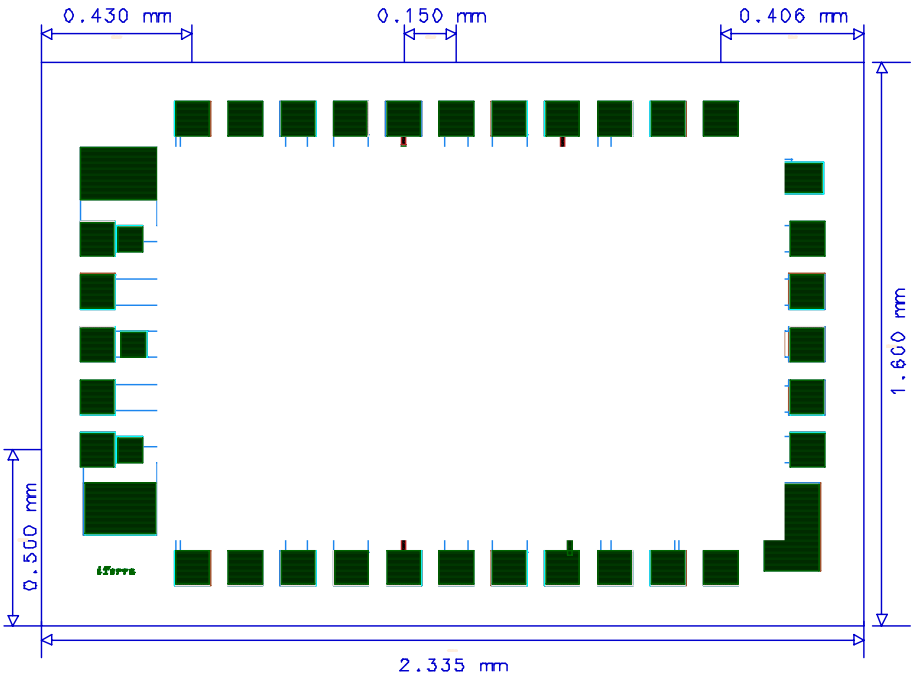
Chip Layout and Bond Pad Locations

(Back of chip is RF and DC ground)



Chip size tolerance: ± 20 µm
Chip thickness: 4 mil with a tolerance of ± 0.4 mil

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