iT4005D
12.5 Gb/s GaAs MMIC D Flip-Flop
(Advanced Information)

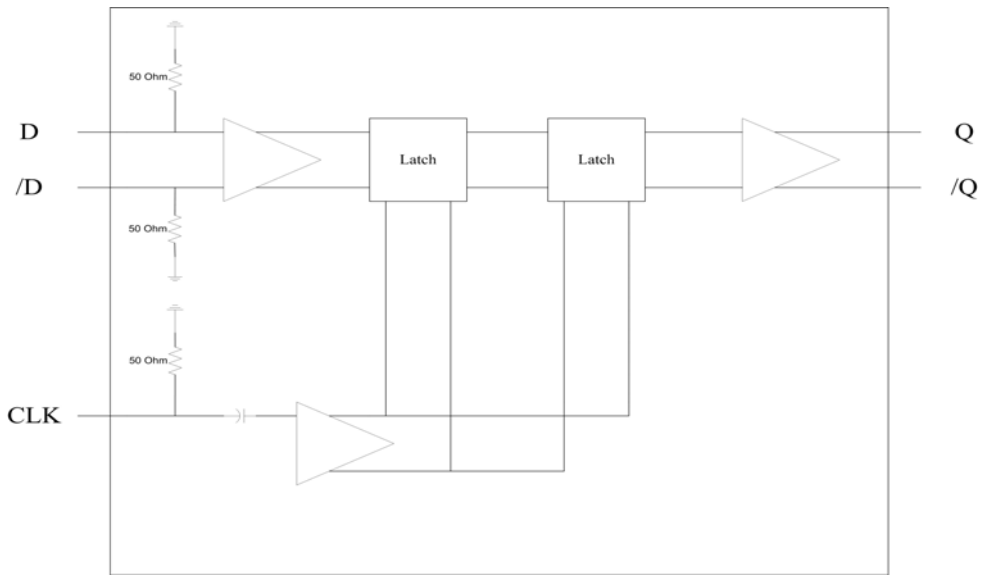
Description

The iT4005D is a high-speed D-type flip flop fabricated using 1-µm HBT GaAs technology. Its high output voltage, excellent rise and fall time and the high eye diagram quality at all clock frequencies makes the iT4005D suitable for very high speed and complex digital applications such as decision circuits, waveform shaping, register implementation, and timing adjustment. The device consists of a master-slave latch designed using an ECL topology guarantee high-speed operation. The data and clock inputs and data outputs are DC coupled. At the data input port, the iT4005D tolerates a wide range of operating conditions, and the internal 50-ohm resistors avoid the need for external terminations for impedance matching. The iT4005D uses SCFL I/O levels and allows either single-ended or differential data input and output. For the clock, a single-ended, DC-coupled input with an internal 50-ohm resistor followed by a DC block is provided. An amplitude of 700 mV peak-to-peak for the clock is recommended, although depending on the operating frequency, a lower amplitude may be usable. An on-chip output buffer provides an excellent eye diagram at a 12.5 GHz clock frequency.

Features

- 2-13 GHz clock frequency range
- 900 mVpp single ended output dynamic
- Output rise time (20%-80%): 25 ps
- Output fall time (20%-80%): 24 ps
- DC coupled clock input
- DC coupled data input
- 50 ohm matched DC-coupled data output
- Differential or single-ended inputs
- Low power consumption:
  1 W at -5.2 V (VQH = 0.0 V, VQL = -0.9 V)
  0.7 W at -4.5 V (VQH = 0.0 V, VQL = -0.6 V)
  0.5 W at -4.0 V (VQH = 0.0 V, VQL = -0.4 V)

Device Diagram



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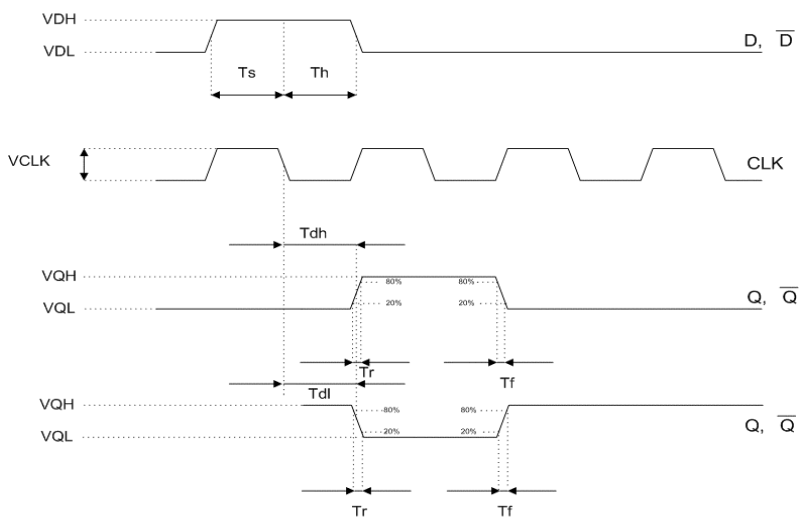
Timing Diagram



Absolute Maximum Ratings

Stresses in excess of those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational section of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters/conditions	Min.	Max.	Units
Vee	Power supply voltage	-5.5	0	V
VDH	Data/clock input voltage level, high level	-1.2	1.2	V
VDL	Data/clock input voltage level, low level	-1.2	1.2	V
Ta	Operating temperature range – die	-15	125	°C
Tstg	Storage temperature	-65	150	°C

Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
Ta	Operating temperature range – die	0		85	°C
Vee	Power supply voltage		-5.0		V
Vindc	Data DC input voltage common mode	-0.4	0	0.1	V
Vinpp	Data input voltage level (single-ended, peak-to-peak)		0.5		V
VCLKdc	Clock input voltage common mode		0		V
VCLK	Clock input voltage (single-ended, peak-to-peak)		0.7		V

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Electrical Characteristics

Symbol	Parameters	Min	Typ	Max	Units
Vee	Power supply voltage	-5.45	-5.0	-4.00	V
VCLK	Input clock voltage amplitude	0.5	0.7	1.0	V
VCLKdc	Input clock voltage common mode	-0.2	0	0.2	V
VDH	Data input voltage level, high level (single ended) (2)	-0.6	0.25	0.6	V
VDL	Data input voltage level, low level (single ended) (2)	-1	-0.25	0.6	V
Vinppd	Data/clock input voltage level differential peak to peak	0.50	1.0	2.0	
Vindc	DC input voltage (with DC-coupled input) (3)	-0.75	0	0.25	V
VQH	Data output voltage amplidude high	-0.05	0	0	V
VQL	Data output voltage amplidude low	-1.1	-0.85	-0.4	V
Tr	Output rise time (20% - 80%)		25		ps
Tf	Output fall time (20% - 80%)		24		ps
Tdl	Output fall delay (CLK vs. Q,Qb) (4)		33		ps
Tdh	Output rise delay (CLK vs. Q,Qb) (4)		35		ps
Ts	Minimum setup time		12		ps
Th	Minimum hold time		12		ps
PM1	Phase margin at 12.5 Gb/s NRZ input (5)		224		deg
PM2	Phase margin at 10.7 Gb/s NRZ input (5)		290		deg
FMAx	Clock frequency (6)	2	12.5	13	GHz
RMAx	Input data rate (6)	2	12.5	13	Gb/s
RLin	Minimum input return loss (up to 13 GHz)		10		dB
RLout	Minimum output return loss (up to 13 GHz)		10		dB
Jpp	Peak to peak jitter		5		ps
Jrms	RMS jitter		0.9		ps
Ic	Power supply current		185		mA
Pd	Power dissipation		0.925		W

1. Electrical characteristics at ambient temperature.

2. Minimum and maximum values for VDH and VDL have to be set in order to satisfy the following rule: 0.2 V <(VDH - VDL) <1 V

3. In case of single-ended input, the unused one must be tied to Vindc which must be nominally set to the applied input mean value.

4. Output change state on input rising edge.

5. Calculated as follows in the following equation:

$$\frac{\text{PM[deg]} = \text{PM(measured) [ps]}}{\text{BitDuration [ps]* 360 [ps]}}$$

where:

$$\text{BitDuration[ps]} = \frac{1}{\text{BitRate[Gb/s]}}$$

6. Duty cycle 50%. Asymmetrical duty cycle may reduce maximum frequency.

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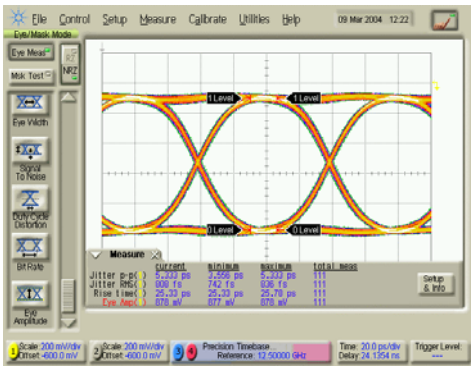
Eye Diagram Performance



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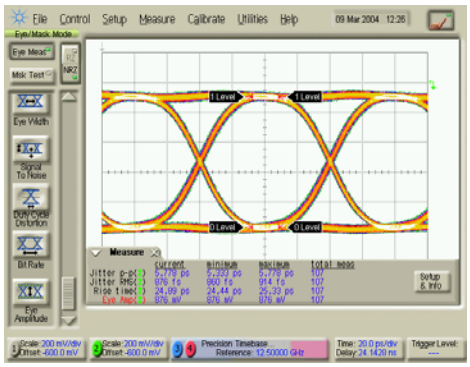
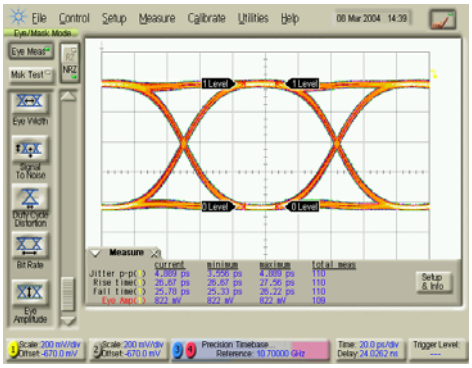


Q\

Output at 12.5 Gb/s. Power supply = -5.2 V



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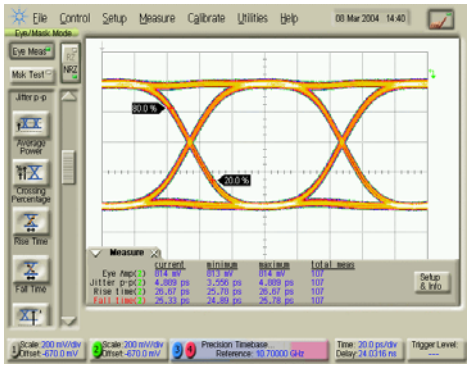

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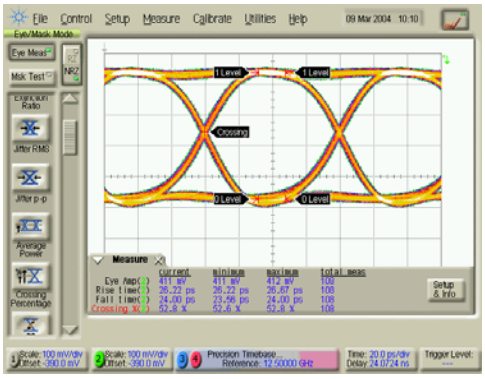
Output at 10.7 Gb/s. Power supply = -5.2 V



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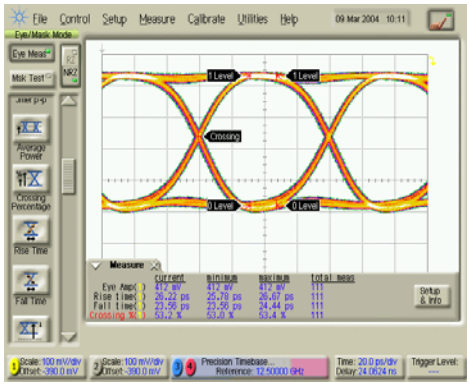

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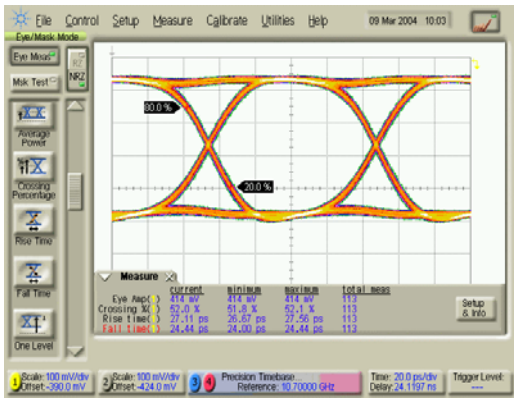
Output at 12.5 Gb/s. Power supply = -4 V

Eye Diagram Performance (cont.)



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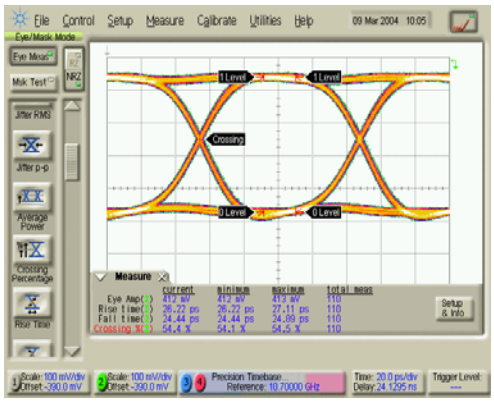

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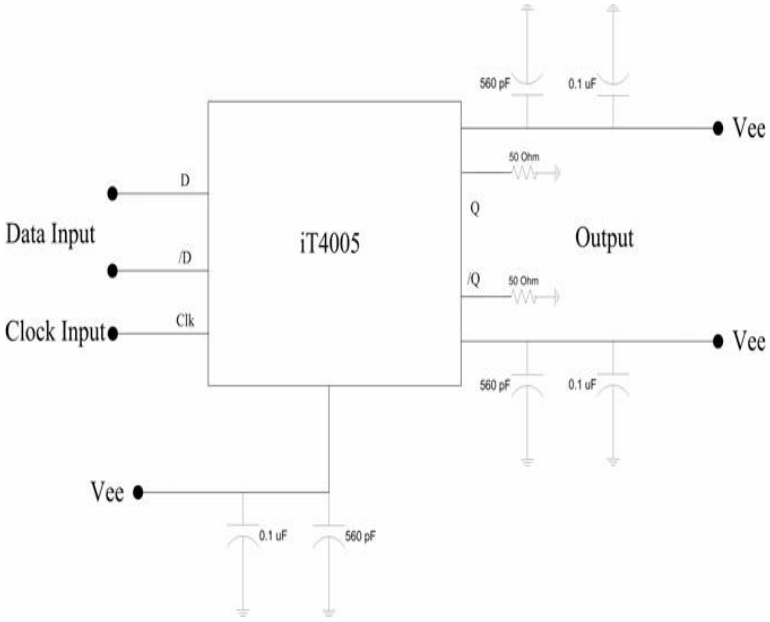
Output at 12.5 Gb/s. Power supply = -4 V

Recommended Operational Setup

Bias Conditions

Connect inputs
Apply -5.0 V at Vee
Apply RF signals to the inputs
Tune Vindc for optimal eye diagram in case of single-ended input.



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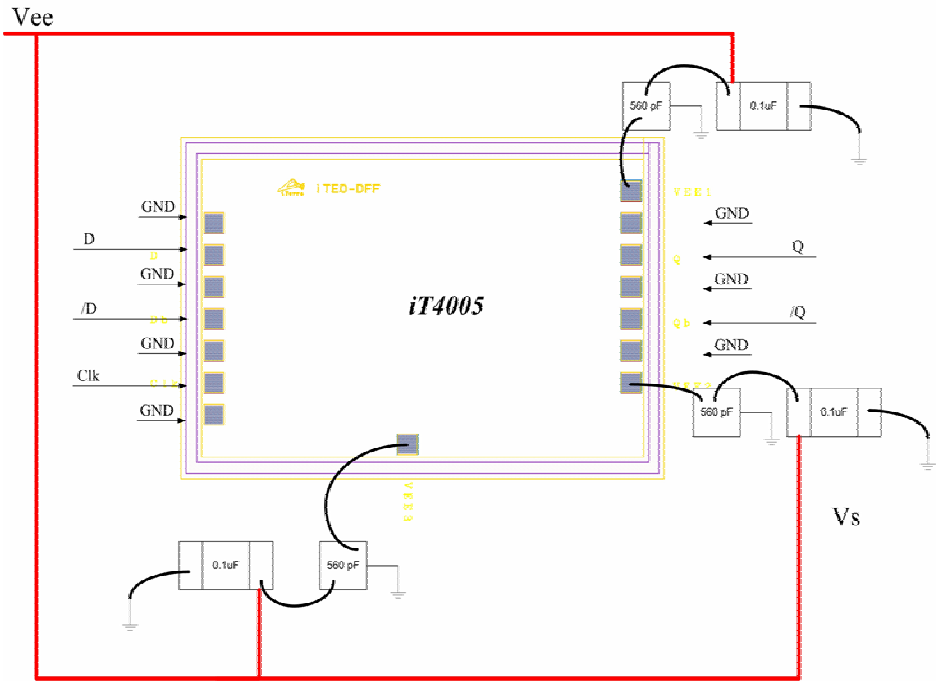
Recommended Chip Mounting



Pad Positions And Chip Dimensions

Chip size:
1600 µm ±10 µm x 2335 µm
±10 µm edge to edge

Chip thickness:
104 µm ±3 µm

Pad size:
100 µ m x 100 µm

RF pad pitch:
150 µm

Unlabeled pads are ground and may be left floating