iT4050D
Dual LVDS-to-SCFL Level Translator

Description

The iT4050D is a wideband LVDS-to-SCFL level translator fabricated using 0.1μm HBT GaAs technology. It is based on ECL topology to guarantee high-speed operation. The two translators are fully independent, allowing power consumption to be optimized according to the application. The device can translate NRZ streams with data rate up to 3.125 Gb/s or clock signals with a frequency up to 3.125 GHz. The inputs and outputs of the iT4050D are DC coupled. At the input side, internal 100-ohm resistors between the two differential lines avoid the need for external impedance matching terminations. The input levels are fully compliant with LVDS specifications. The iT4050D uses SCFL output levels and allows either single ended or differential data output. The excellent rise and fall time and the good quality of the eye diagram at all data rates up to 3.125 Gb/s makes the iT4050D suitable for interfacing a generic LVDS output buffer with all iTerra SCFL parts.

Features

- Wideband signal handling: Up to 3.125 Gb/s NRZ
- Input sensitivity: 350 mV differential
- 450 mV pp typical single-ended output
- Jitter RMS: <2 ps
- Output rise time (20% – 80 %): <55 ps
- Output fall time (20% – 80 %): <55 ps
- 100-ohm (differential) matched DC-coupled inputs
- 50-ohm matched DC-coupled outputs
- Differential or single-ended output
- Power consumption: 140 mW per translator

Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters/conditions	Min.	Max.	Units
V_{DD}	Power supply voltage	0	2.75	V
V_{EE}	Power supply voltage	-3.63	0	V
V_{IH}	Input voltage level, high level	0	2.4	V
V_{IL}	Input voltage level, low level	0	2.4	V
T_A	Operating temperature range - die	-15	125	ºC
T_{STG}	Storage temperature	-65	150	ºC

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Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
T_A	Operating temperature range – die	0		85	ºC
V_{DD}	Positive power supply voltage		2.5		V
V_{EE}	Negative power supply voltage		-3.3		V
V_{IH}	Input voltage level, high level (single ended)		1.4		V
V_{IL}	Input voltage level, low level (single ended)		1.05		V
V_{INDC}	DC input voltage (with DC-coupled input)		1.22		V

Electrical Characteristics

1. Electrical characteristics at ambient temperature.

2. In case of single-ended input the unused pin has to be tied to VINDC.

3. In case of single-ended output, the unused pad must be terminated with 50 ohms to ground.

4. On a 3-Gb/s PRBS pattern, DC coupled output.

5. Current and power dissipation are per converter.

Symbol	Parameters/conditions	Typ.	Units
V_{DD}	Positive power supply voltage	2.5	V
V_{EE}	Negative power supply voltage	-3.3	V
V_{IH}	Input voltage level, high level (single ended)	1.4	V
V_{IL}	Input voltage level, low level (single ended)	1.05	V
V_{INDC}	DC input voltage (with DC-coupled input) (2)	1.22	V
V_{OUT}	Data output voltage amplitude (3)	450	mV
V_{OH}	Output voltage level, high level (Single ended)	0	V
V_{OL}	Output voltage level, low level (single ended)	-450	mV
T_R	Output rise time (20%-80%)	55	ps
T_F	Output fall time (20%-80%)	55	ps
S_{22}	Output return loss (up to 7 GHz)	15	dB
J_{p-p}	Peak-to-peak jitter (4)	12	ps
J_{rms}	RMS jitter (4)	2	ps
I_{DD}	Positive power supply current (5)	8	mA
I_{EE}	Negative power supply current (5)	36	mA
P_D	Power dissipation (5)	140	mW

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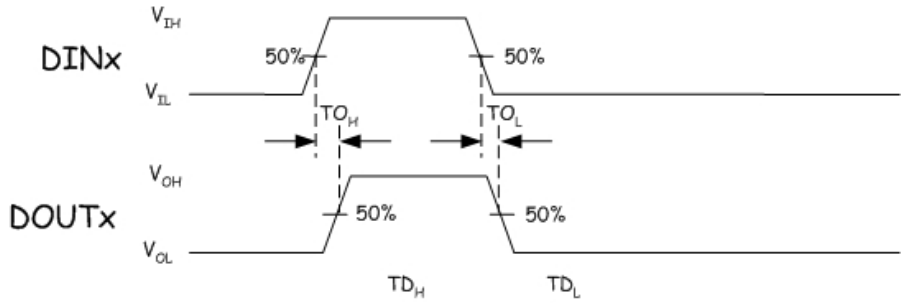
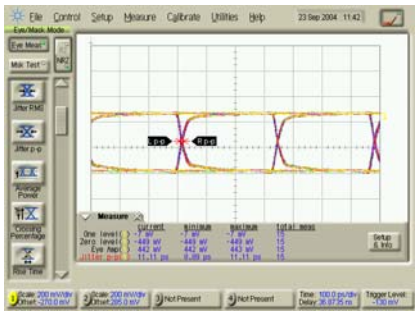
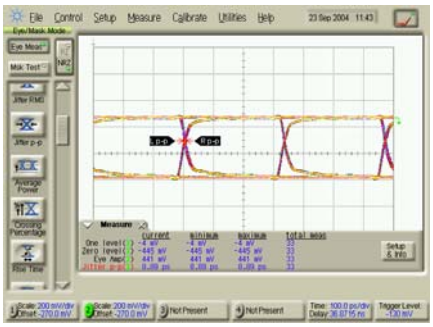
Timing Diagram



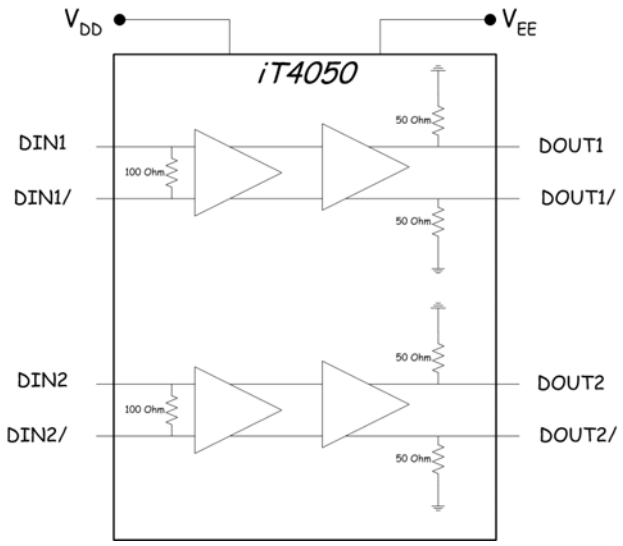
Eye Diagram Performance





Die measurements (OUT and OUT/)
VDD: +2.5 V, Vee: -3.3 V
Input data rate: 3 Gb/s
Differential data input (1.1 V/0.6 V)
With two separated 50-ohms to ground termination, DC-coupled output

Device Diagram



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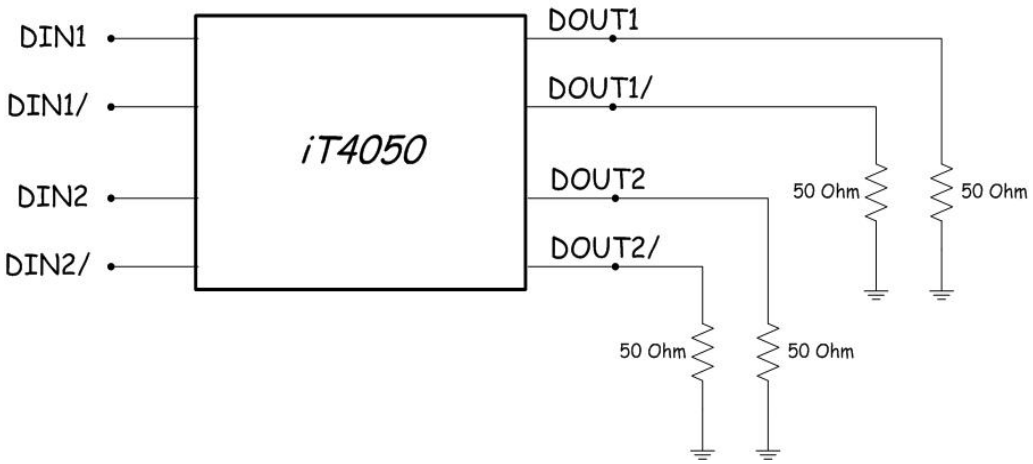
Recommended Operational Setup



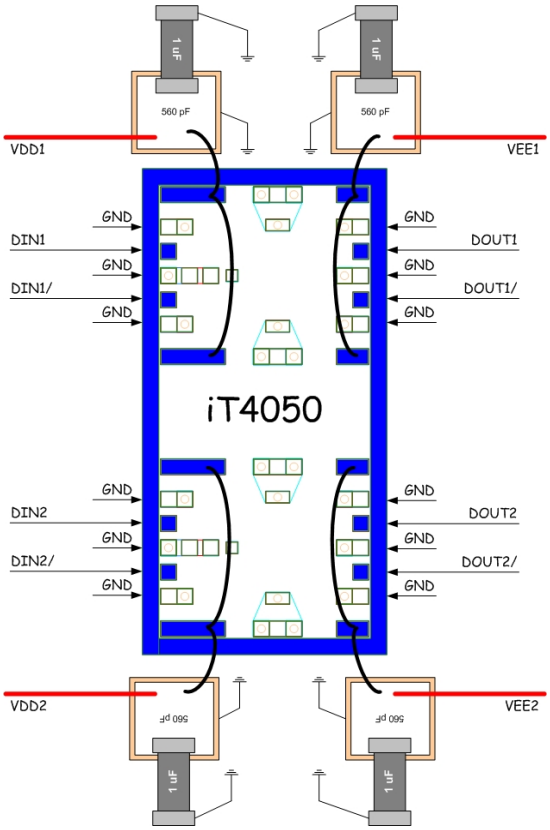
Recommended Chip Mounting

Chip size:
1400 µm ±10 µm
x 2900 µm ±10 µm

Chip thickness:
104 µm ±3 µm

Pad size:
100 µm x 100 µm

RF pad pitch:
150 µm



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Pad Positions and Chip Dimensions

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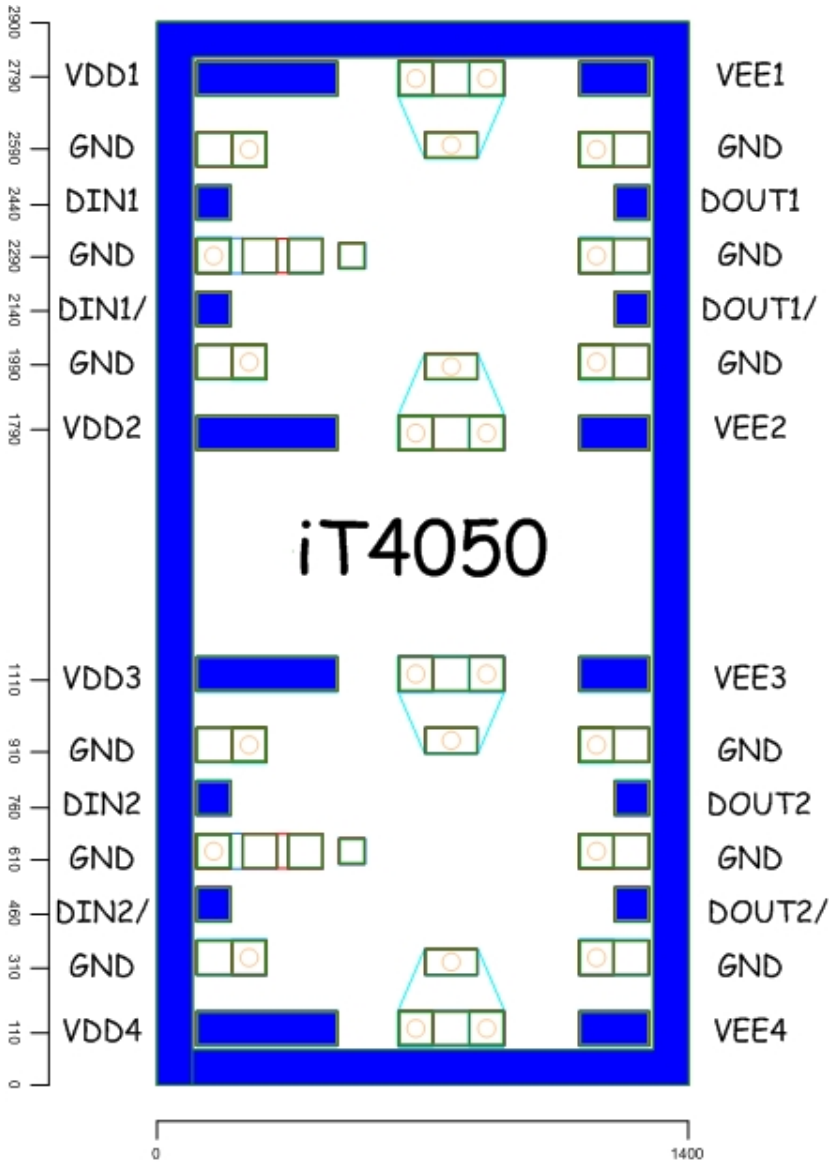

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