iT4051D
DUAL RocketIO to SCFL Level Translator
(Advanced Information)

Description

The iT4051D is a wideband RocketIO-to-SCFL level translator fabricated using 0.1 μm HBT GaAs technology. It is based on ECL topology guarantee high-speed operation. The two translators are fully independent each other allowing reduced power consumption according to the application. The device can translate NRZ streams with data rates up to 3.125 Gb/s or clock signals with a frequency up to 3.125 GHz. The iT4051D inputs and outputs are DC coupled. At the input side, internal 50-ohm resistors eliminate the need for external impedance matching terminations. The input levels are fully compliant with the Xilinx RocketIO specifications. The iT4051D uses SCFL output levels and allows either single-ended or differential data output. The excellent rise and fall time and the good quality of the eye diagram at all data rates up to 3.125 Gb/s makes the iT4051D suitable for interfacing the RocketIO output buffers with all iTerra SCFL parts.

Features

- Wideband signal handling: Up to 3.125 Gb/s NRZ
- Input sensitivity: 500 mV single ended
- 450 mV p-p typical single-ended output
- Jitter RMS: <2ps
- Output rise time (20% – 80 %): < 33 ps
- Output fall time (20% – 80 %): < 33 ps
- 50-ohm matched DC-coupled inputs and outputs
- Differential or single-ended I/O
- Power consumption: 175 mW per translator

Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters/conditions	Min.	Max.	Units
V_{DD}	Power supply voltage	0	2.75	V
V_{EE}	Power supply voltage	-3.63	0	V
V_{IH}	Input voltage level, high level	1.5	3.5	V
V_{IL}	Input voltage level, low level	1.5	3.5	V
T_A	Operating temperature range - die	-15	125	ºC
T_{STG}	Storage temperature	-65	150	ºC

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Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
T_A	Operating temperature range – die	0		85	ºC
V_{DD}	Positive power supply voltage		2.5		V
V_{EE}	Negative power supply voltage		-3.3		V
V_{IH}	Input voltage level, high level (single ended)		2.4		V
V_{IL}	Input voltage level, low level (single ended)		1.6		V
V_{INDC}	DC input voltage (with DC-coupled input)		2.0		V

Electrical Characteristics

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive power supply voltage		2.5		V
V_{EE}	Negative power supply voltage		-3.3		V
V_{IH}	Input voltage level, high level (single ended)		2.4		V
V_{IL}	Input voltage level, low level (single ended)		1.6		V
V_{INDC}	DC input voltage (with DC-coupled input) (2)		2.0		V
V_{OUT}	Data output voltage amplitude (3)		450		mV
V_{OH}	Output voltage level, high level (single ended)		0		V
V_{OL}	Output voltage level, low level (single ended)		-450		mV
T_R	Output rise time (20%-80%)		33		ps
T_F	Output fall time (20%-80%)		33		ps
S_{11}	Input return loss (up to 10 GHz)		15		dB
S_{22}	Output return loss (up to 10GHz)		15		dB
J_{p-p}	Peak-to-peak jitter (4)		12		ps
J_{rms}	RMS jitter (4)		2		ps
I_{DD}	Positive power supply current (5)		20		mA
I_{EE}	Negative power supply current (5)		38		mA
P_D	Power dissipation (5)		175.4		mW

1. Electrical characteristics at ambient temperature.

2. In case of single ended input the unused pin must be tied to VINDC.

3. In case of single-ended output the unused pad must be terminated with 50 ohms to ground.

4. On a 3-Gb/s PRBS pattern, DC-coupled output.

5. Current and power dissipation are per converter.

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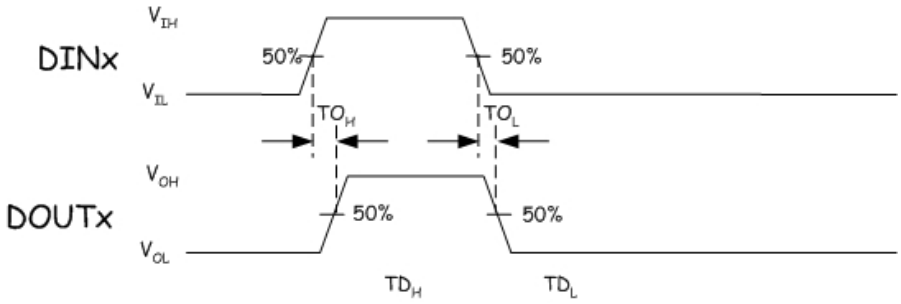
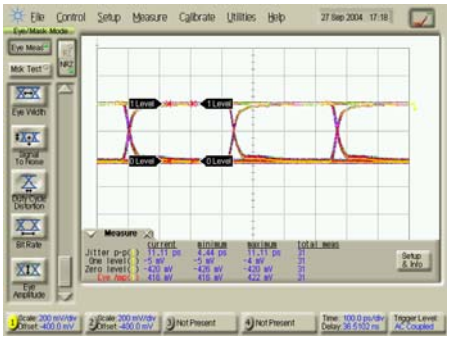
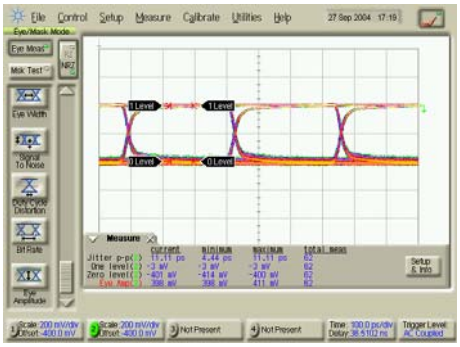
Timing Diagram

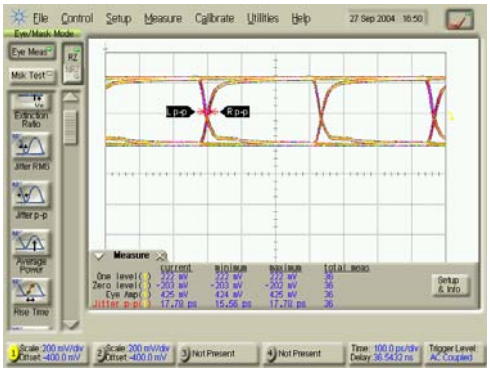


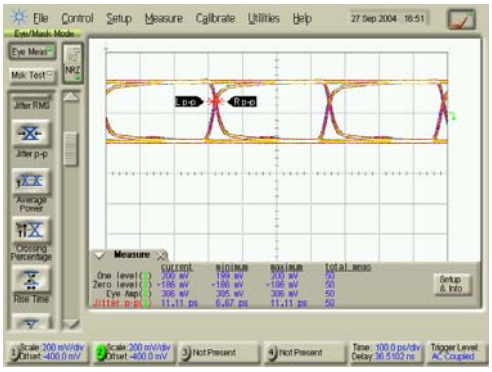
Eye Diagram Performance





Die measurements (OUT and OUT/)
VDD: +2.5 V, VEE: -3.3 V
Input data rate: 3 Gb/s
Single-ended data input (2.6 V/2.1V)
DC-coupled output





Die measurement (OUT and OUT/)
VDD: +2.5 V, Vee: -3.3 V Input data rate: 3 Gb/s
Input data rate: 3 Gb/s
Single-ended data input (2.6 V/2. V)
AC-coupled output

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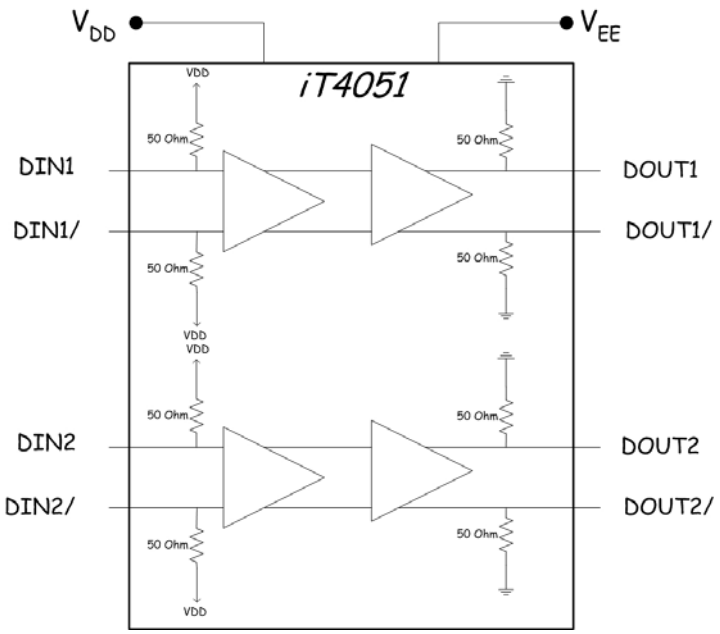
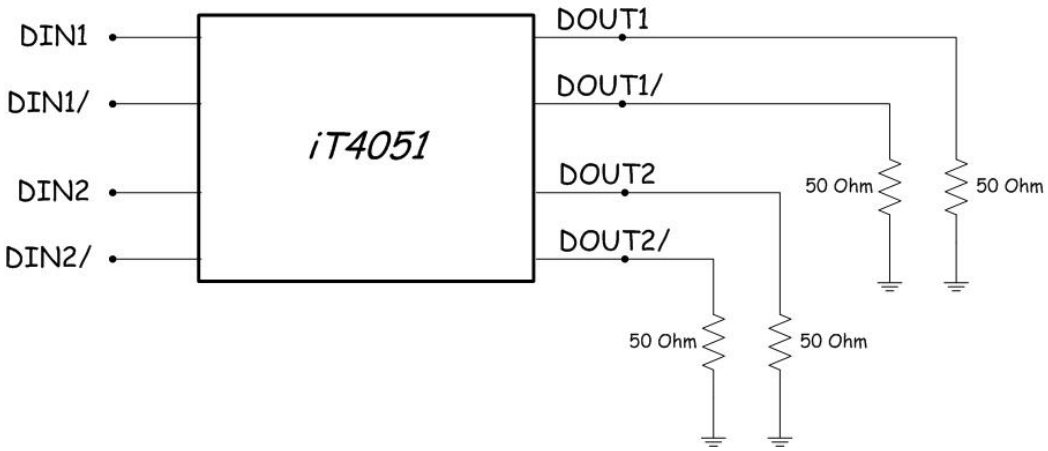
Device Diagram



Recommended Operational Setup



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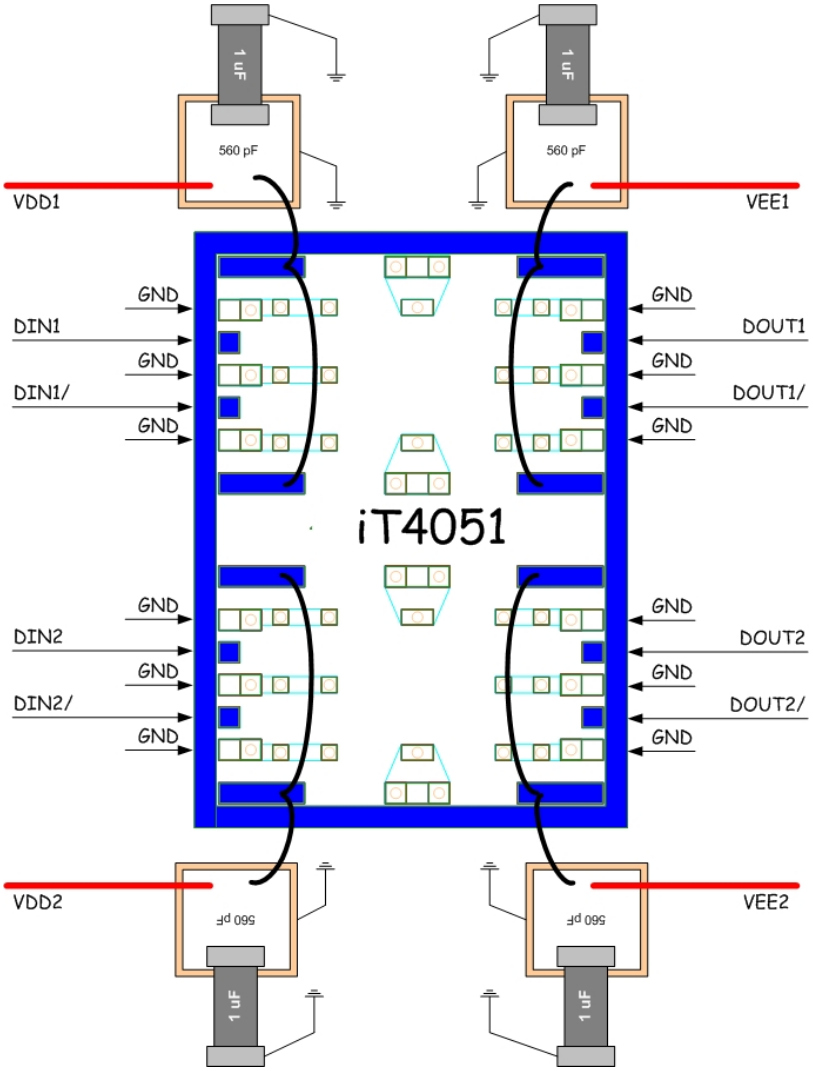
Recommended Chip Mounting

Chip size:
1900 µm ±10 µm
x 2650 µm ±10 µm

Chip thickness:
104 µm ±3 µm

Pad size:
100 µm x 100 µm

RF pad pitch:
150 µm



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Pad Positions and Chip Dimensions

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Chip thickness:
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Pad size:
100 µm x 100 µm

RF pad pitch:
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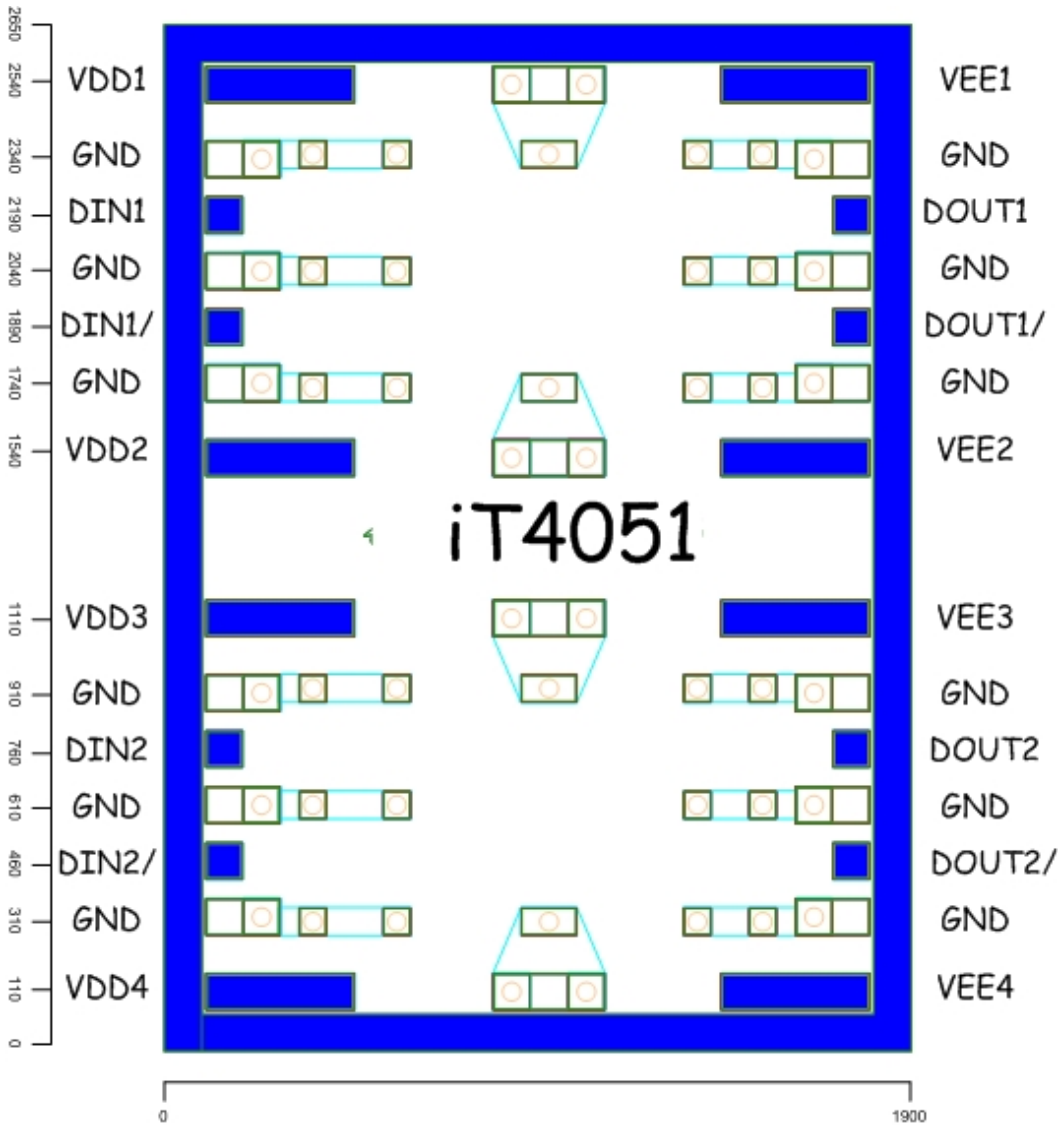

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