iT5025
40-Gb/s, 8-Vpp Optical Modulator Driver

Description

The iT5025 is a broadband GaAs MMIC traveling wave amplifier that delivers high output power and moderate gain from 30 kHz to 40 GHz. It is well suited for use as a general-purpose, extremely broadband driver in OC-768 40 Gb/s optical communication systems, as well as any broadband application requiring flat gain response and excellent port matches.

Seven P-HEMT cascode stages provide 8 Vpp output voltage to drive a $LiNbO_3$ external modulator. The iT5025 incorporates advanced MBE technology, Ti-Pt-Au gate metallization, silicon nitride passivation, and polyimide for scratch protection. Low-frequency extension capabilities are also provided.

Features

- Frequency range: 30 kHz to 40 GHz
- Gain: 10 dB
- Gain flatness: ±0.7 dB
- Output voltage: 8 Vpp
- P1dB at 20 GHz: +21 dBm
- Psat at 20 GHz: +23 dBm
- Return loss
  - Input: –12 dB
  - Output: –10 dB
- Low-frequency operation
- Available in die form

Absolute Maximum Ratings

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
Vdd	Positive drain voltage			9	V
Idd	Total drain current			500	mA
Vg1	First gate voltage			3	V
Vg2	Second gate voltage			8	V
P_{DC}	DC power dissipation			4	W
Pin	RF input power			25	dBm
Tch	Operating channel temperature			160	ºC
Tcase	Operating case temperature			-40 to +95	ºC
Tmax	Maximum assembly temperature			310	ºC

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Electrical Characteristics

1. Small signal data measured in wafer Form with T=25℃.

2. Performance may be extended to lower frequencies by means of off-chip circuitry.

Test conditions:
Vdd = 7 V,
Ids(RF) = 210 mA

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
BW	3 dB bandwidth	5		41	GHz
S_{21}	Small gain signal		10		dB
RL_{in}	Input return loss		-15		dB
RL_{out}	Output return loss		-12		dB
S_{12}	Isolation		-35		dB
GD	Group delay up to 40 GHz		±10		Ps
	Bit rate		43.5		Gb/s
Vout	Saturated output voltage		+8		Vpp
	Power detector output		0.37		V/Vpp
	Power detector output (RF off)		6.8		V
	Eye crossing control (by means of Vg)	30		70	%
	Voltage control (by means of Vd)	5		8	V

DC Specifications/ Physical Properties

1. Measured in wafer form with T_{chuck} = 25° C

Symbol	Parameters/conditions	Min.	Typ.	Max	Units
I_{DSS}	Saturated drain current (V_{dd}=6.0 V, V_{g1}=0.0 V, V_{g2} = open circuit)		420		mA
V_P	First gate pinch-off voltage (V_{dd} = 7.0 V, I_{dd} = 10 mA, V_{g2} = open circuit)		-1.8		V
V_{G2}	Second gate voltage self biased (V_{dd} = 7.0 V, V_{g1}= 0.0 V, I_{dd}= 10 mA)		NA		V
I_{dSOFF} (V_{G1})	First gate pinch-off current (V_{dd}=7.0 V, V_{g1}= -3.5 V, V_{g2} = open circuit)		55		mA
IdOFF (V_{G2})	Second gate pinch-off current (V_{dd} = 7.0 V, V_{g1} = 0.0 V, V_{g2}= -3.5 V)		NA		mA

Biasing and Operation

The iT5025 amplifier is biased with a single positive drain supply (VDD) and single negative gate supply (V_{g1}). The recommended bias conditions for the iT5025 are V_{dd}= 7.0 V, I_{dd} = 220 mA. To achieve this drain current level, V_{g1} is typically biased between –0.4 V and –0.5 V. V_{g2} must be set at approximately 3.5 V. The gate voltage (V_{g1}) MUST be applied prior to the drain voltage (V_{dd}) during power up and removed after the drain voltage is removed during power down. Drain bias V_{dd} can be applied through an external bias tee at the RF output pad. External coupling capacitors are needed on RFIN and RFOUT ports. The drain bias pad is connected to RFOUT.

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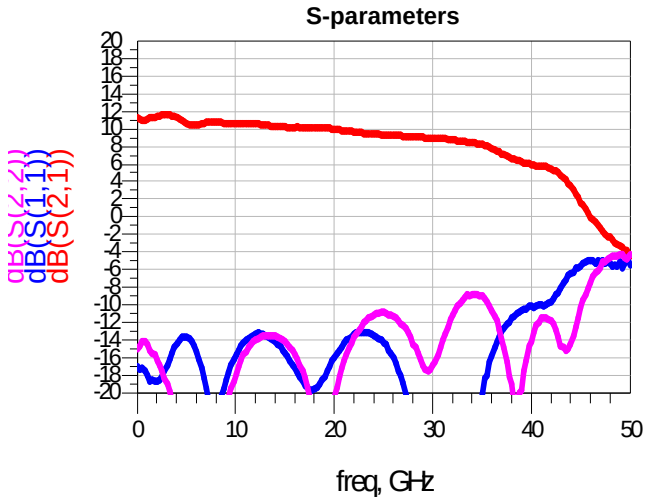
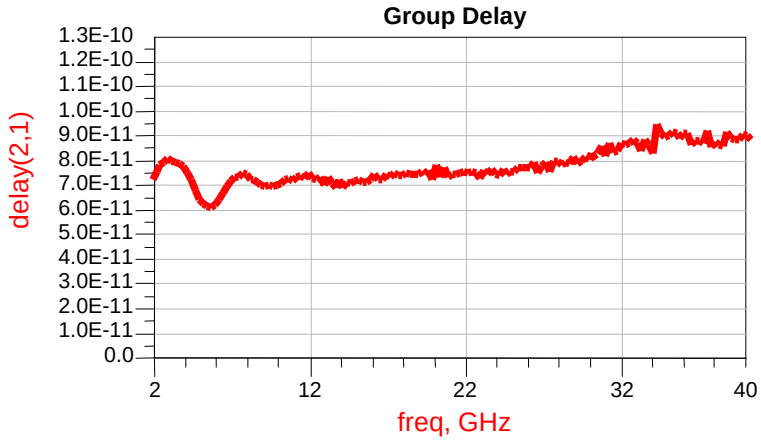
Biasing and Operation (cont.)

External RF choke inductance must be large enough to cover the lowest operating frequency. See the bonding diagram for recommended bonding connections. Off-chip resistor can help reduce the gain at frequency below 200 MHz in order to achieve good eye-diagram performance. The auxiliary gate (G2) and drain (D1) contact pads are used to extend performance below 2 GHz. Connect G1 and D1 through large external capacitors to ground to maintain input and output VSWR at low frequencies. Do not apply bias to these pads.

Small Signal Measured Performance





Bias: Vdd = 7.0 V, Vg1 = -0.5 V, Vg2 = 3.4 V, Idd = 210 mA

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Pad Positions And Dimensions

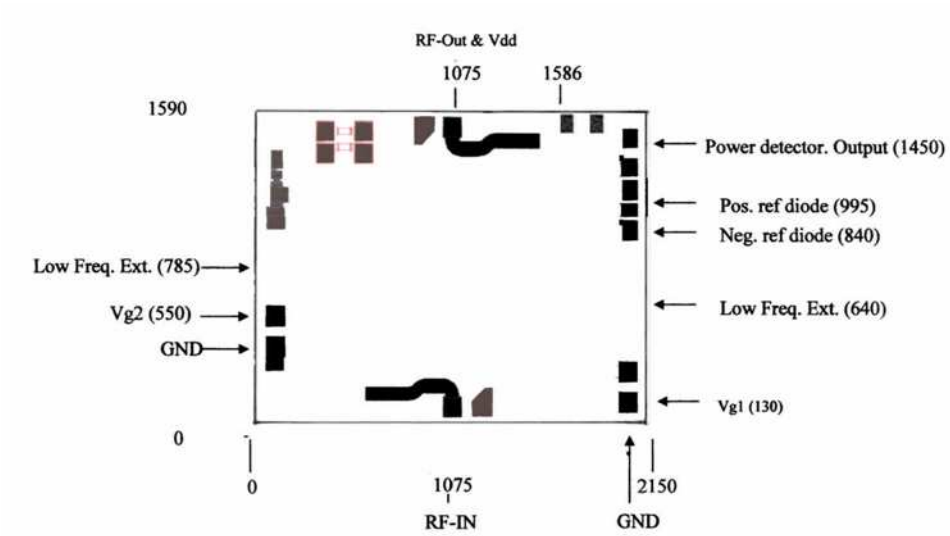
All dimensions in µm

Chip size:
2.150 µm ±10 µm x
1.520 µm ±10 µm

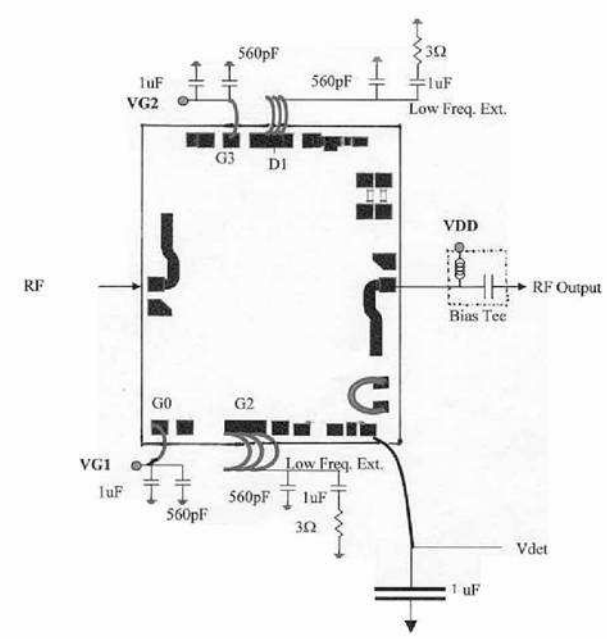
Chip thickness:
104 µm ± 3 µm

Typical bond pad size:
100 x 100 µm

Center-to-center pad spacing: 150 µm



Assembly Schematic



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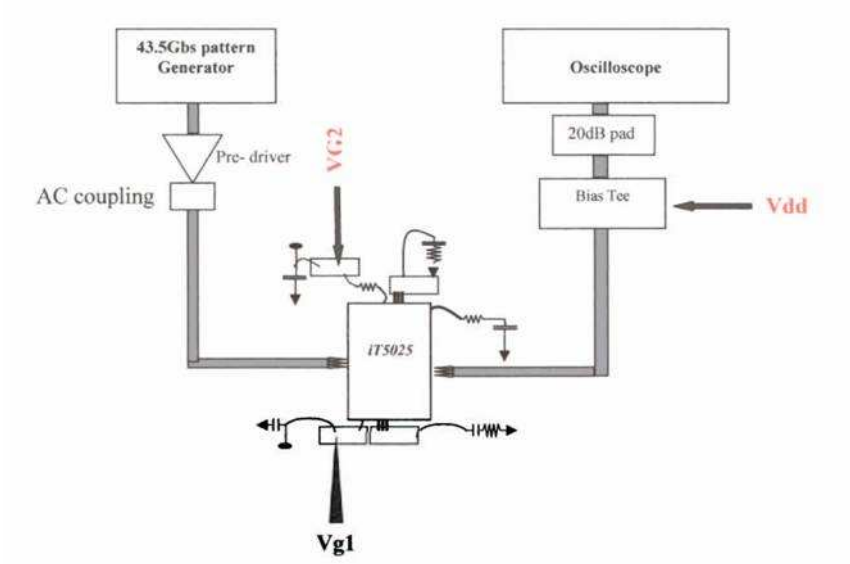
Optical Modulator Driver Application

The iT5025 amplifier has been designed to drive 40 Gb/s $LiNbO_3$ modulators, providing an output voltage of 8 Vpp. In order to achieve the best eye diagram performance, the assembly diagram reported in this data sheet must be considered and the following bias procedure is recommended:

1.Disable RF during the initial biasing
2.Set V_{g1} to –1 V
3.Set V_{g2} to 1 V
4. Set V_{dd} to 7 V
5. Set V_{g2} = 3.5 approximately
6. Increase Vg1 in order to bring current close to 200 to 220 mA (this should correspond to about V_{g1}= -0.4).
7.Apply RF signal at 2 Vpp, small decreasing of current can be observed.
8. Increase input signal to 3 to 3.5 Vpp with output voltage of 8 Vpp (current decrease of about 5%)
9. Adjust V_{g1} to center eye crossing.

Eye diagram test results reported in this data sheet are at a data rate of 43.5 Gb/s

43.5 Gb/s Eye Diagram Probe Test Set Up



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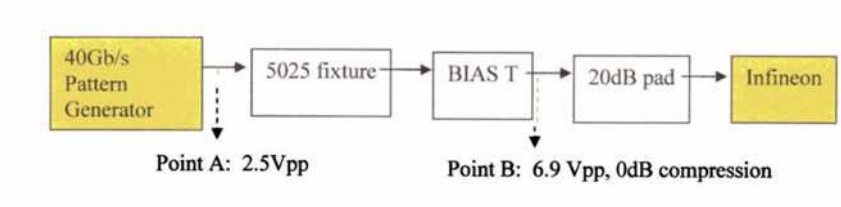
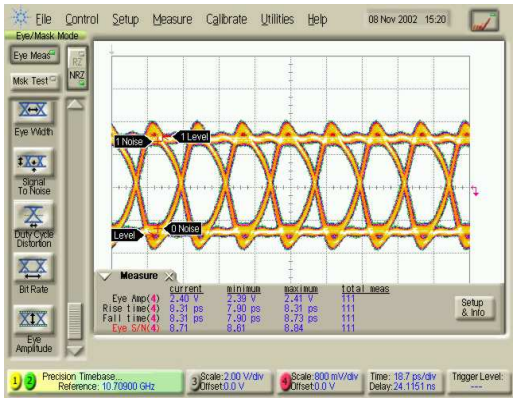
Eye Diagram Measured Performance

Test Set Up Block Diagram



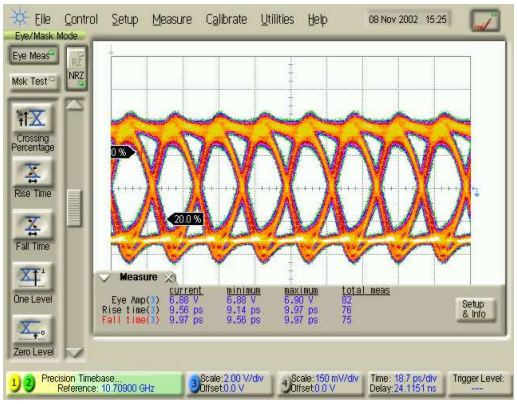
Bias conditions: Vg1 = -0.4 V, Vdd = 7 V, Vg2 = 3.4 V, Idd = 210 mA

Waveform at point A



Input signal 40 Gb/s pbrs 2^31
Vin = 2.5 Vpp
Rt/Ft = 8 ps, Jitter RMS = 0.51 ps,
Jitter pp = 4 ps

Waveform at point B



Output signal
Vout = 6.9 Vpp, 0 dB compression
Rt/Ft = 9.8 ps, Jitter RMS = 0.9 ps,
Jitter pp = 5.2 ps

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