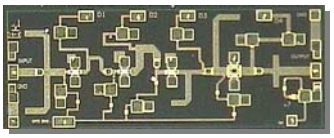
# iTR33001
# 33 GHz Buffer Amplifier MMIC

## Description

The iTR33001 is a 4-stage GaAs MMIC amplifier designed as a 33 GHz Buffer Amplifier for use in the LO chain of point to point radios, point to multi- point communications, LMDS, and other millimeter wave applications. In conjunction with other iTerra amplifiers, multipliers and mixers it forms part of a complete 38 GHz transmit/receive chipset. The iTR33001 utilizes iTerra's 0.25µm power PHEMT process and is sufficiently versatile to serve in a variety of medium power amplifier applications.

## Features

- 4 mil substrate
- Small-signal gain 24 dB (typ.)
- Saturated power out 19 dBm (typ.)
- Voltage detector included to monitor Pout
- Chip size 3.2 mm x 1.2 mm x 100 µm





## Absolute Ratings

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Positive DC voltage (+4 V Typical) | Vd | +6 | Volts |
| Negative DC voltage | Vg | -2 | Volts |
| Simultaneous (Vd - Vg) | Vdg | 8 | Volts |
| Positive DC Current | $I_D$ | 173 | mA |
| RF Input Power (from 50 Ω source) | $P_{IN}$ | +8 | dBm |
| Operating Baseplate Temperature | $T_C$ | -30 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | -55 to +125 | °C |
| Thermal Resistance (Channel to Backside) | $R_{jc}$ | 130 | °C/W |

## Electrical Characteristics

(At 25°C), 50 Ω system, Vd=+4 V, Quiescent Current Idq=112 mA

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Frequency Range | 32 | | 35 | GHz |
| Gate Supply Voltage (Vg)[1] | | -0.2 | | V |
| Gain Small Signal (Pin= -15 dBm) | 20 | 24 | | dB |
| Gain Variation vs. Frequency | | 2.0 | | dB |
| Power Output Saturated: (Pin=+1 dBm) | 17 | 19 | | dBm |
| Drain Current at Psat | | 120 | | mA |

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Power Added Efficiency (PAE): at Psat | | 15 | | % |
| Input Return Loss (Pin=-15 dBm) | | 12 | | dB |
| Output Return Loss (Pin=-15 dBm) | | 12 | | dB |
| DC Detector Voltage at Pout=18 dBm | | 1.0 | | V |

**Note:**
1. Typical range of gate voltage is -0.5 to 0V to set Idq of 112 mA.



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## Application Information

**CAUTION: THIS IS AN ESD SENSITIVE DEVICE.**

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

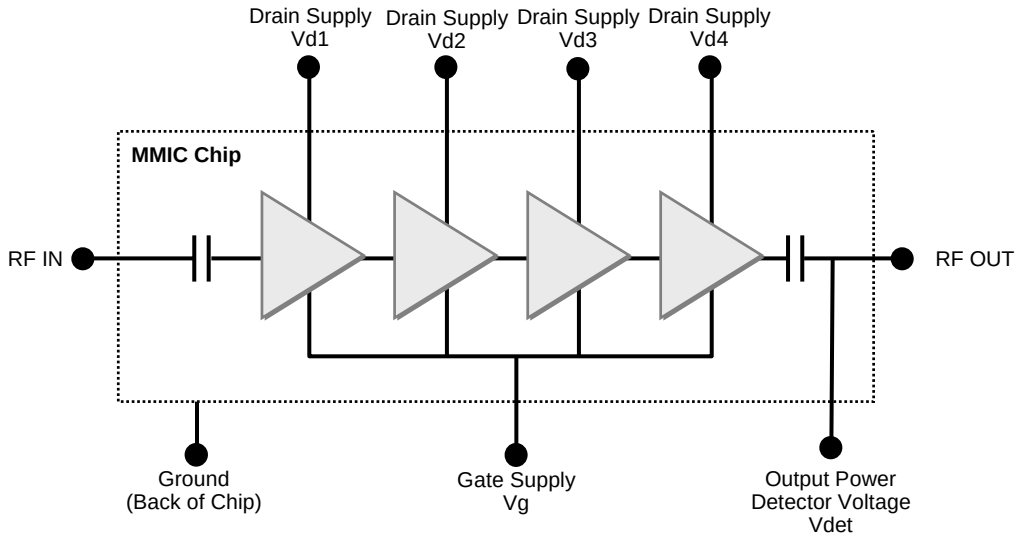
Die attachment should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC ground.



These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012" long corresponding to a typical 2 mil gap between the chip and the substrate material.

**Figure 1**
Functional Block Diagram




**Note:**
Detector delivers > 0.1 V DC into 3k Ω load resistor for >+18 dBm output power. If output power level detection is not desired, do not connect to detector bond pad.



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**Figure 2**
Schematic of Application Circuit

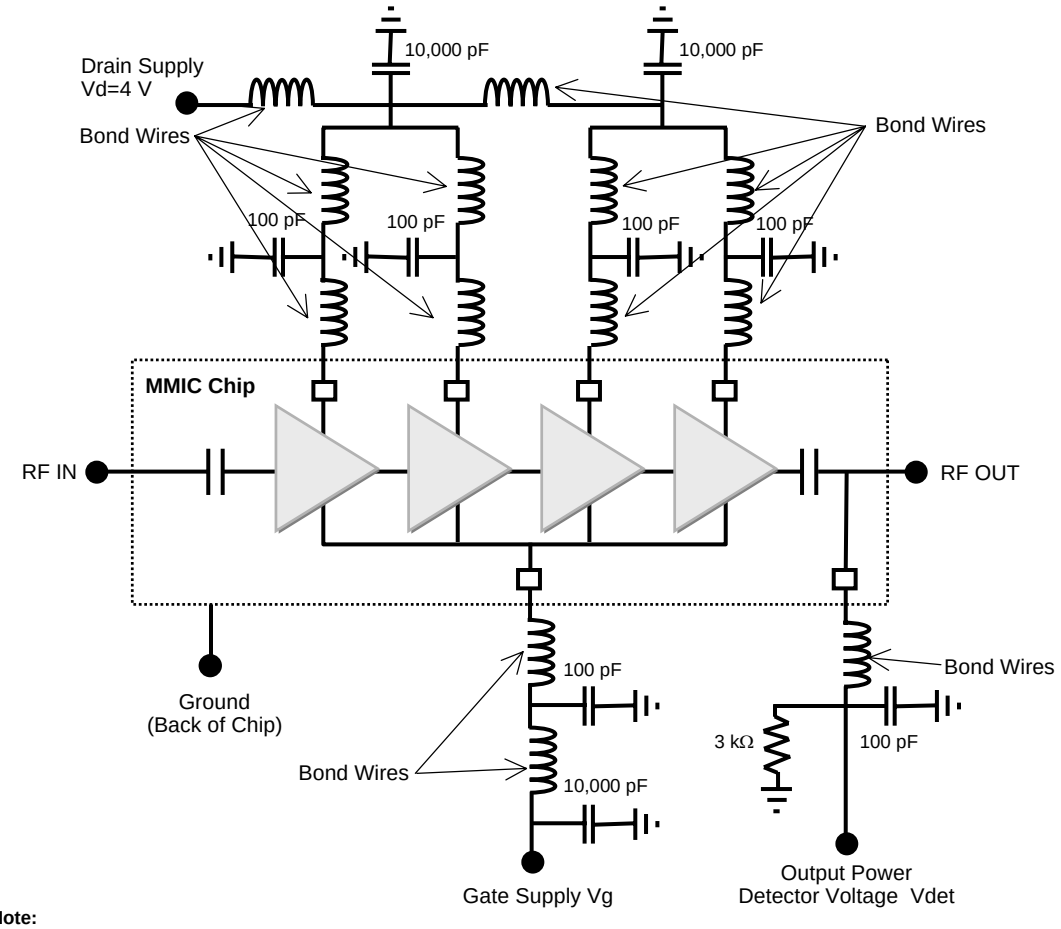


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**Figure 3**
Chip layout and Bond Pad Locations

Chip Size is 3.19 mm x 1.19 mm x 100 μm.
Back of chip is RF and DC ground

*Dimensions in mm*

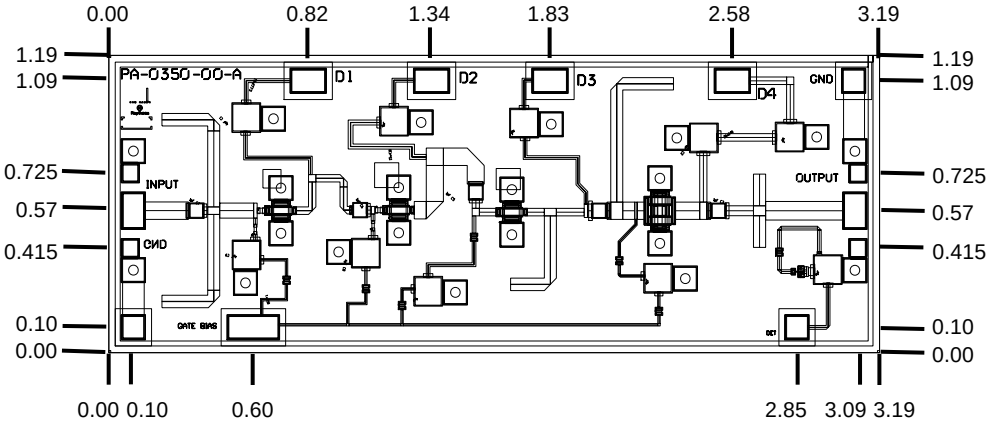



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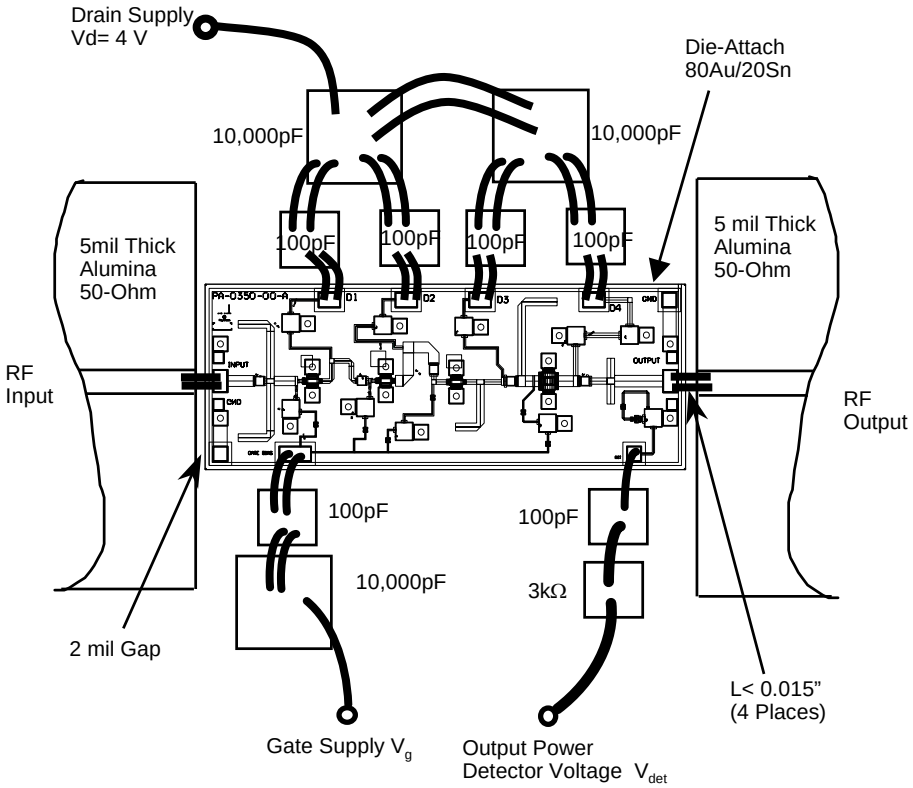
**Figure 4**
Recommended Assembly Diagram




**Note:**
Use 0.003" by 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief.

## Test Procedure
for biasing and operation

**CAUTION: LOSS OF GATE VOLTAGE (VG) WHILE DRAIN VOLTAGE (VD) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.**

The following sequence must be followed to properly test the amplifier.

**Step 1:** Turn off RF input power.

**Step 2:** Connect the DC supply grounds to the grounds of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5 V to Vg.

**Step 3:** Slowly apply positive drain bias supply voltage of +4 V to Vd.

**Step 4:** Adjust gate bias voltage to set the quiescent current of Idq=112 mA.

**Step 5:** After the bias condition is established, RF input signal may now be applied at the appropriate **frequency band.**

**Step 6:** Follow turn-off sequence of:

(i) Turn off RF input power,
(ii) Turn down and off drain voltage (Vd),
(iii) Turn down and off gate bias voltage (Vg).



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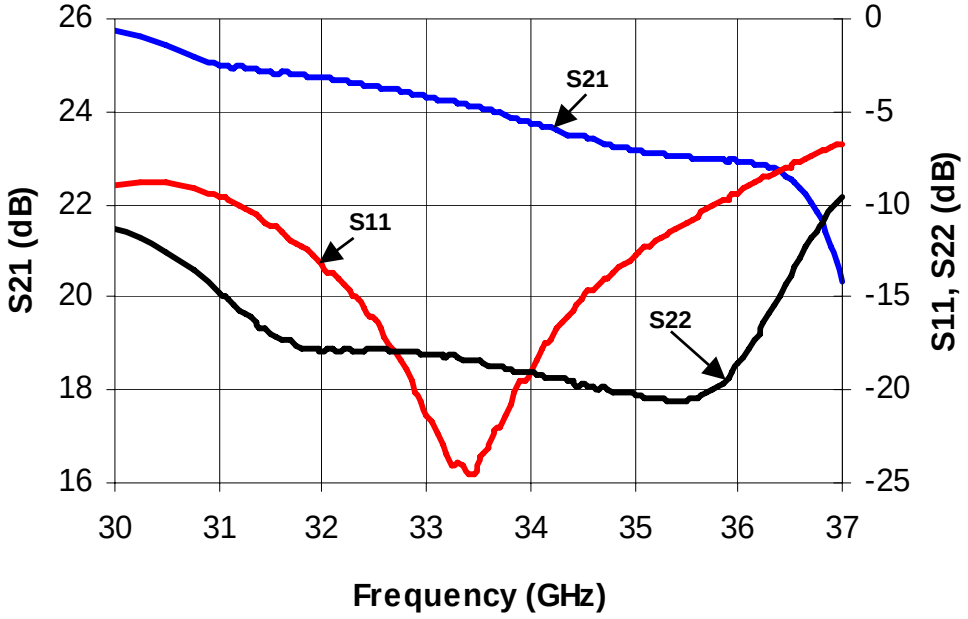
**Performance Data**



**iTR33001 33 GHz BA, Typical Small Signal Performance**
**50 Ω Fixture Measurements, Vd=4 V, Idq= 112 mA, T=25 °C**

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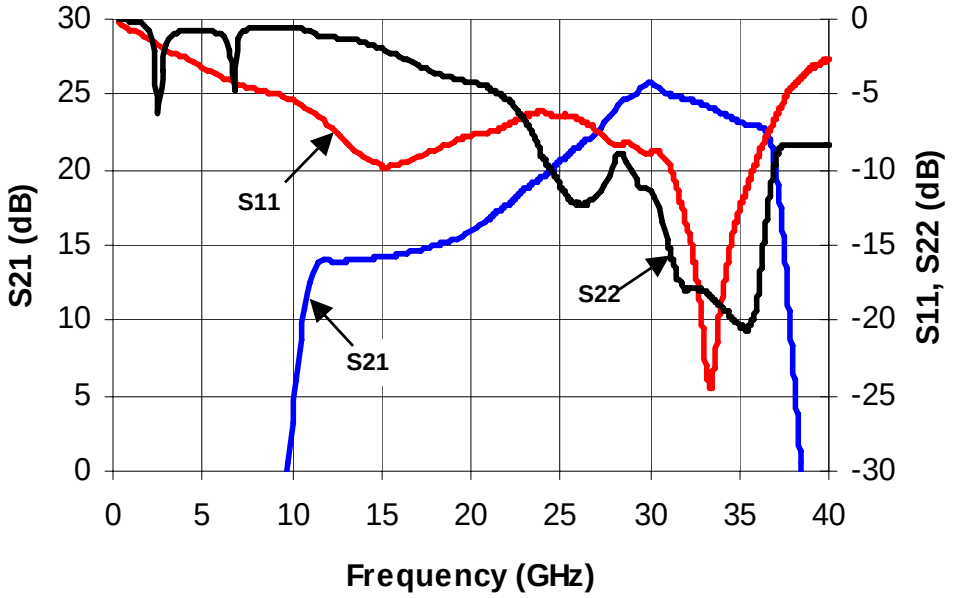








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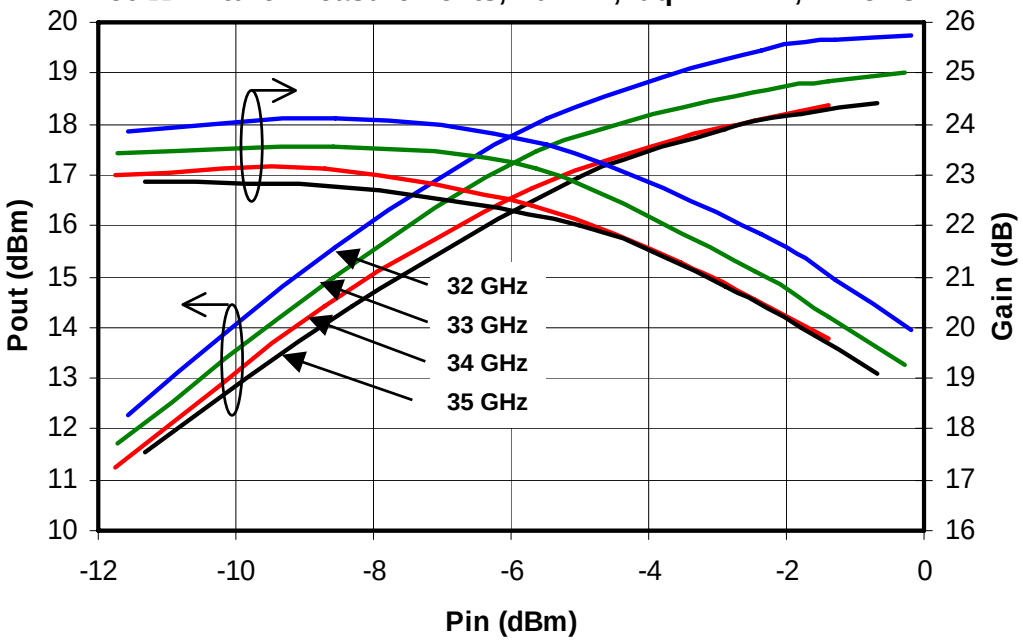
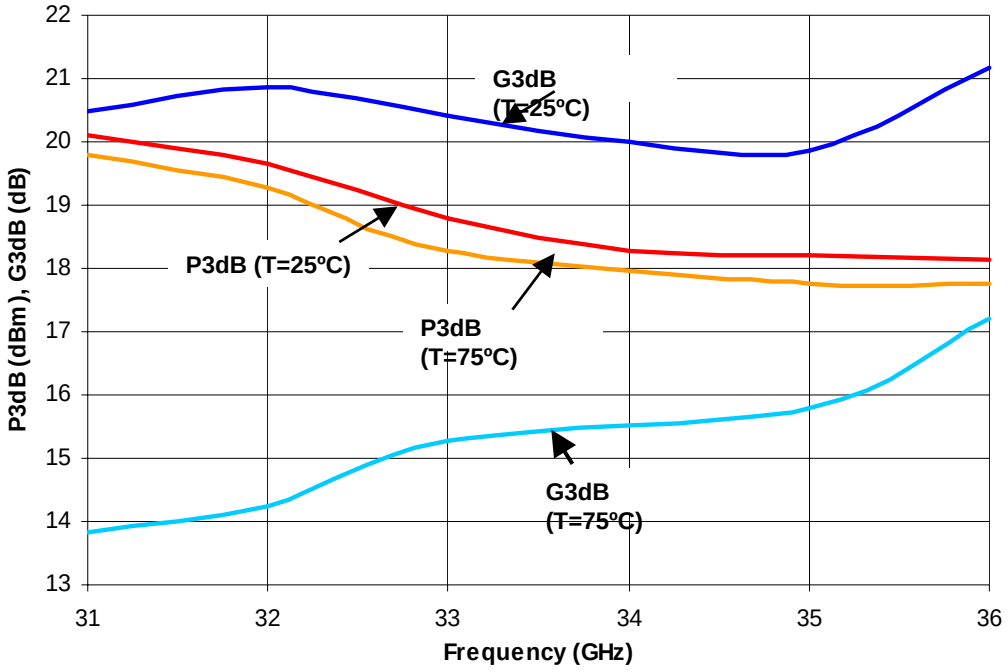
**Performance Data**

**iTR33001 33 GHz BA, Power Output and Gain Vs. Power In 50 Ω Fixture Measurements, Vd=4 V, Idq=112 mA, T=25 °C**




**iTR33001 33 GHz BA, Power Output and Gain at 3 dB Compression Vs. Frequency and Temperature, 50 Ω Fixture Measurements, Vd=4 V, Idq=112 mA**



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