AC/DC Primary-Side Rapid Charge™ PWM Controller with High Resolution Voltage/Current Control

1 Description

The iW1791 is a high performance AC/DC power supply controller for rapid charge applications that supports high resolution voltage/current control. It uses Dialog's ***PrimAccurate***™ technology to minimize external component count and simplify system design. The device operates in quasi-resonant mode to provide high efficiency and it also provides a number of key built-in protection features. The iW1791 can achieve tight multi-level constant voltage and multi-level constant current regulation without a traditional secondary feedback circuit. It also eliminates the need for loop compensation components while maintaining stability over all operating conditions.

The iW1791 is optimized to work with Dialog's secondary-side controllers that use the proprietary digital link (DLNK) technology. The iW1791 and DLNK-based secondary-side controller chipset together can implement various rapid charge protocols, such as USB Power Delivery (USB PD), Qualcomm® Quick Charge™ 2.0 and 3.0 (QC2.0 and QC3.0) technologies, etc. to achieve fast and smooth voltage transitions upon request by mobile devices (MD). The iW1791 and compatible secondary-side controller from Dialog use the DLNK communction protocol for output voltage requests, output current limits, output voltage undershoot and over voltage information from the secondary to the primary.

In addition, the iW1791 uses source charging technology to charge up V_{CC} before startup, which eliminates the external active start-up (ASU) circuit and still can achieve < 20mW no-load power consumption at typical 5V output setting.

Dialog's innovative proprietary technology ensures that power supplies designed with the iW1791 and Dialog's secondary-side controllers can provide output voltage configurations of 3V to 20V for USB PD, 5V/9V/12V for QC2.0 and 3.6V to 12V in 200mV increments for QC3.0 and other proprietary protocols.

2 Features

- Supports 10mV DLNK voltage step request required by USB PD programmable power supply (PPS) and other proprietary rapid charge protocols
- Source charging V_{CC} technology eliminates the active start-up (ASU) and maintain ultra-low no-load power consumption (< 20mW) at 230V_{AC} with typical 5V output setting
- High V_{CC} pin voltage rating eliminates external V_{CC} LDO
- Tight multi-level constant-voltage and multi-level constant-current regulation with primary-side feedback and control
- Proprietary optimized load adaptive maximum constant frequency PWM switching with quasi-resonant operation achieves best size, efficiency, and common mode noise
- Backward compatible with QC2.0/3.0 and other proprietary rapid charge protocols with secondary-side interface circuits
- Multi-mode PWM/PFM control improves efficiency at various load conditions
- No audible noise over entire operating range
- User-configurable 4-level cable drop compensation independent of output voltage
- Proprietary secondary-to-primary digital communication with single optocoupler for all the rapid charge information:
  - » Output voltage request
  - » Output current limit
  - » Output voltage undershoot detection for fast dynamic load response
  - » Over-voltage protection
- ***EZ-EMI***® design enhances manufacturability
- Built-in single-point fault protections against output short-circuit including soft short and half short, output over-voltage, and output over-current
- ***SmartDefender+***™ control technology addresses issues of soft shorts in cables and connectors by effectively reducing the average output power at fault conditions without latch

3 Applications

- Rapid-charging AC/DC adapters for smart phones, tablets and other portable devices.

Qualcomm® Quick Charge™ 2.0 and 3.0 are products of Qualcomm Technologies, Inc.

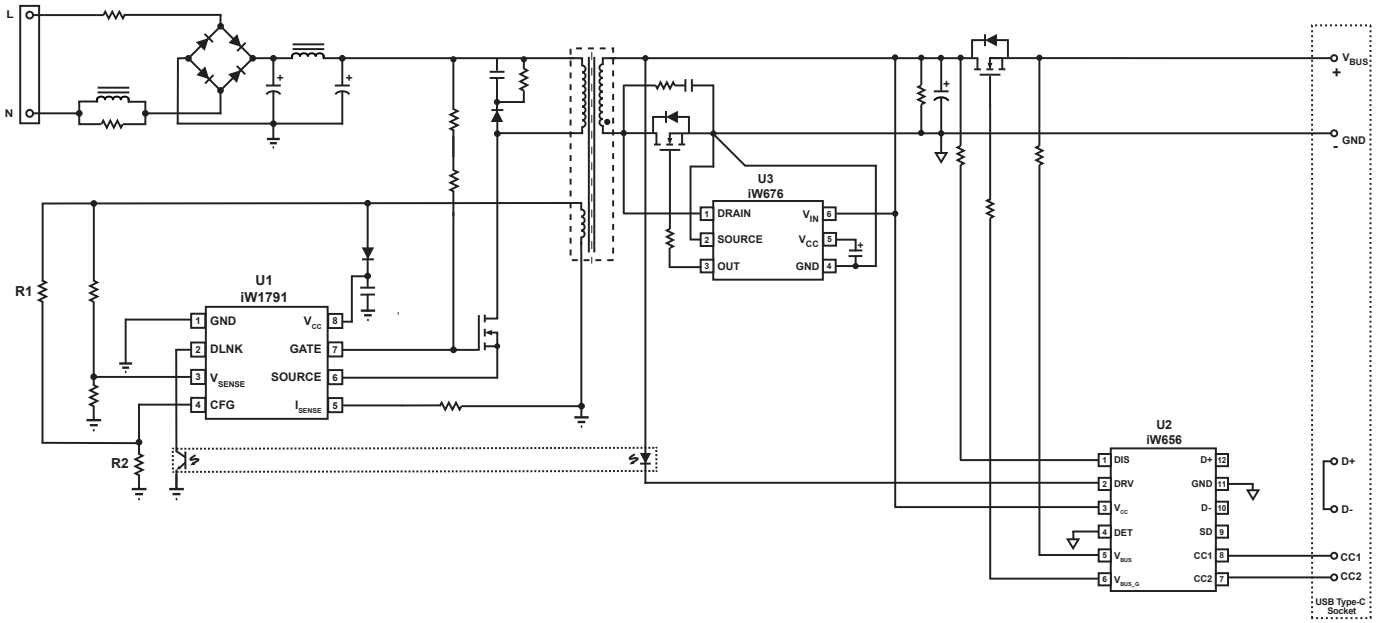


Figure 3.1 : iW1791 Typical Application Circuit for Standard USB PD with Optional QC2.0/QC3.0 Enabled (Using iW656 as Secondary-Side Controller for USB PD and iW676 as Synchronous Rectifier Controller.)

4 Pinout Description

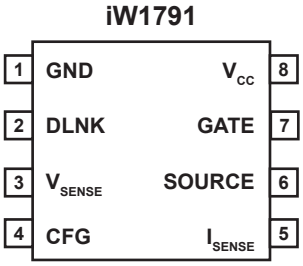


Figure 4.1 : 8-Lead SOIC-8 Package

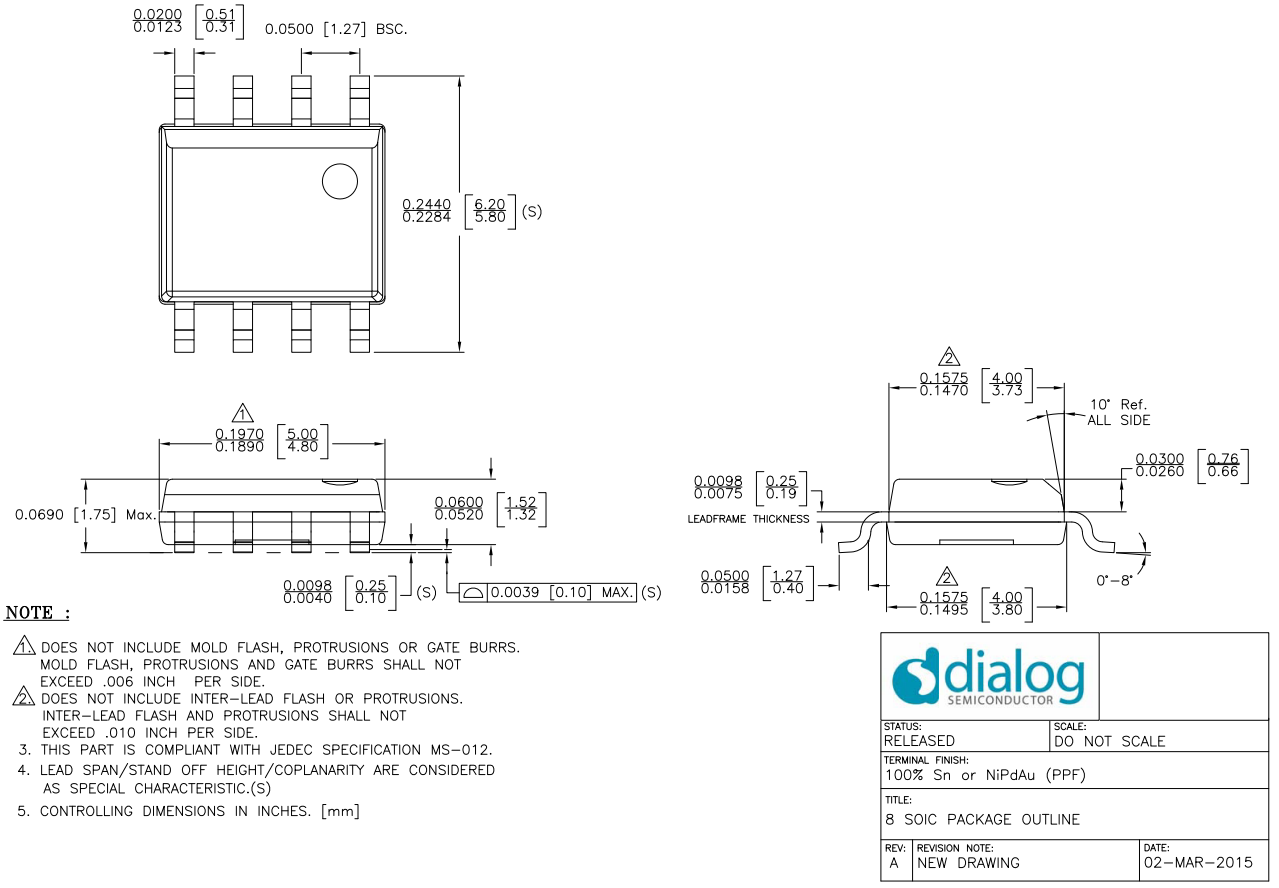
Pin Number	Pin Name	Type	Pin Description
1	GND	Ground	Ground.
2	DLNK	Analog Input	Digital communication link signal. Used for secondary-side to primary-side communication for all rapid change information, which includes output voltage requests, output current limits, output voltage undershoot, and over-voltage protection.
3	V_{SENSE}	Analog Input	Auxiliary voltage sense. Used for primary-side regulation and secondary-to-primary communication through main transformer.
4	CFG	Analog Input	Used for CDC configuration and auxiliary winding open protection.
5	I_{SENSE}	Analog Input	Primary-side current sense. Used for cycle-by-cycle peak-current control and limit in primary-side CV/CC regulation.
6	SOURCE	Power Input	Connect to the source of external power MOSFET. Inside the IC, it is connected to internal MOSFET and startup V_{CC} charge circuit.
7	GATE	Output	Gate drive for external MOSFET switch.
8	V_{CC}	Power Input	IC power supply.

5 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to the Electrical Characteristics section.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 1, I_{CC} = 20mA max)	V_{CC}	-0.3 to 45.0	V
Continuous DC supply current at V_{CC} pin (V_{CC} = 15V)	I_{CC}	20	mA
V_{SENSE} input (pin 3, I_{VSENSE} ≤ 10mA)		-0.7 to 10.0	V
CFG (pin 4)		-0.7 to 5.0	V
DLNK (pin 2)		-0.3 to 5.5	V
I_{SENSE} input (pin 5)		-0.7 to 5.0	V
SOURCE input (pin 6)		-0.7 to 25.0	V
GATE (pin 7)		-0.3 to 30	V
Maximum junction temperature	T_{JMAX}	150	°C
Operating junction temperature	T_{JOPT}	-40 to 150	°C
Storage temperature	T_{STG}	-65 to 150	°C
Thermal resistance junction-to-ambient	θ_{JA}	160	°C/W
ESD rating per JEDEC JESD22-A114		±2,000	V
Latch-up test per JESD78D		±100	mA

6 Physical Dimensions



NOTE :

1. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 INCH PER SIDE.
2. DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 INCH PER SIDE.
3. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MS–012.
4. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
5. CONTROLLING DIMENSIONS IN INCHES. [mm]

STATUS: RELEASED	SCALE: DO NOT SCALE
TERMINAL FINISH: 100% Sn or NiPdAu (PPF)	
TITLE: 8 SOIC PACKAGE OUTLINE	
REV: A / REVISION NOTE: NEW DRAWING	DATE: 02–MAR–2015

7 Ordering Information

Part Number	Options						Package	Description
	Protocol Supported	Default k_{CC} at Start-up	CC Shutdown Voltage	OVP/ OTP Latch	CC Shutdown Latch	Supported DLNK Voltage Information Resolution		
iW1791-00	USB PD/QC	0.422	66% for all V_{BUS} except 6.5V for V_{BUS} = 9V	No	No	25mV/Step	SOIC-8	Tape & Reel[1]
iW1791-01	USB PD/QC	0.422	2.9V for VBUS ≤ 12V 3.2V for VBUS > 12V	No	No	25mV/Step	SOIC-8	Tape & Reel[1]
iW1791-02	USB PD/QC	0.422	2.9V for VBUS ≤ 12V 3.2V for VBUS > 12V	No	No	10mV/Step	SOIC-8	Tape & Reel[1]
iW1791-05	Direct Charge	0.422	2.9V for VBUS ≤ 12V 3.2V for VBUS > 12V	No	No	10mV/Step	SOIC-8	Tape & Reel[1]
iW1791-22	USB PD/QC	0.422	2.9V for VBUS ≤ 12V 3.2V for VBUS > 12V	Yes	No	10mV/Step	SOIC-8	Tape & Reel[1]
iW1791-23	USB PD/QC	0.422	2.9V for V_{BUS} < 3.4V; 3.0V for 3.4V ≤ V_{BUS} < 9V; 6.5V for 9V ≤ V_{BUS} < 12V; 10V for V_{BUS} ≥ 12V	Yes	No	10mV/Step	SOIC-8	Tape & Reel[1]

Note 1: Tape & Reel packing quantity is 2,500/reel. Minimum packing quantity is 2,500.

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