Digital Green-Mode Synchronous Rectifier Controller

1.0 Features

- Digital adaptive turn-off control minimizes dead-time and eliminates the parallel Schottky diode
- Integrated pulse linear regulator (PLR) allows SR operation at low system output voltage down to 2V in typical 5V, 2.5A USB charger applications
- Wide input operating voltage up to 30V
- Optimized 5V MOSFET gate driver
- Intelligent low power management achieves ultra-low no-load operating current < 0.65mA
- Lossless MOSFET V_{DS} sensing for SR timing control
- 6-pin SOT23 package

2.0 Description

The iW673 is a high performance synchronous rectifier controller with an integrated MOSFET driver for flyback converters operating at discontinuous conduction mode. Combined with the MOSFET, the iW673 can emulate the diode rectifier at the secondary side of the flyback to reduce conduction loss. The iW673 determines the timing of the driver by sensing the voltage across the $R_{DS(ON)}$ to achieve lossless sensing. The iW673 uses proprietary digital adaptive turn-off control technology to minimize the turn-off deadtime of the synchronous rectifier so that the parallel Schottky diode required by conventional synchronous rectifiers can be eliminated. The integrated driver has strong driving capability for high efficiency. The operating power consumption of the controller excluding the driver is less than 4mW at no load to achieve the ultra-low no-load power consumption for 5V applications. The iW673 integrates a pulse linear regulator to maintain the operation of the synchronous rectifier at low system output voltage when the system is operating in constant current (CC) mode.

3.0 Applications

- Compact AC/DC adapters/chargers for media tablets and smart phones

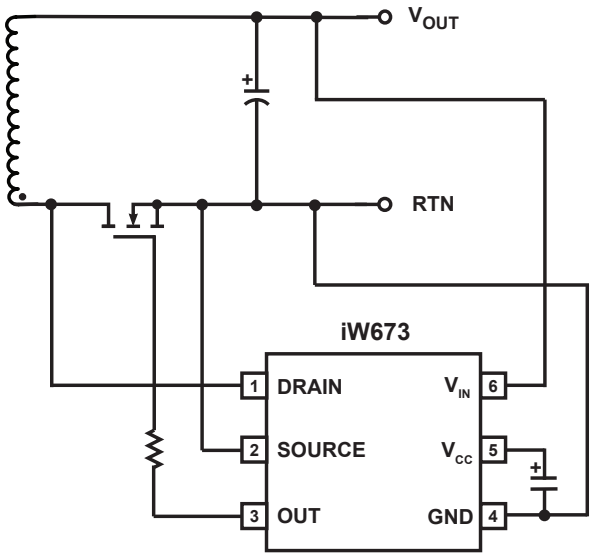


Figure 3.1: iW673 Typical Application Circuit

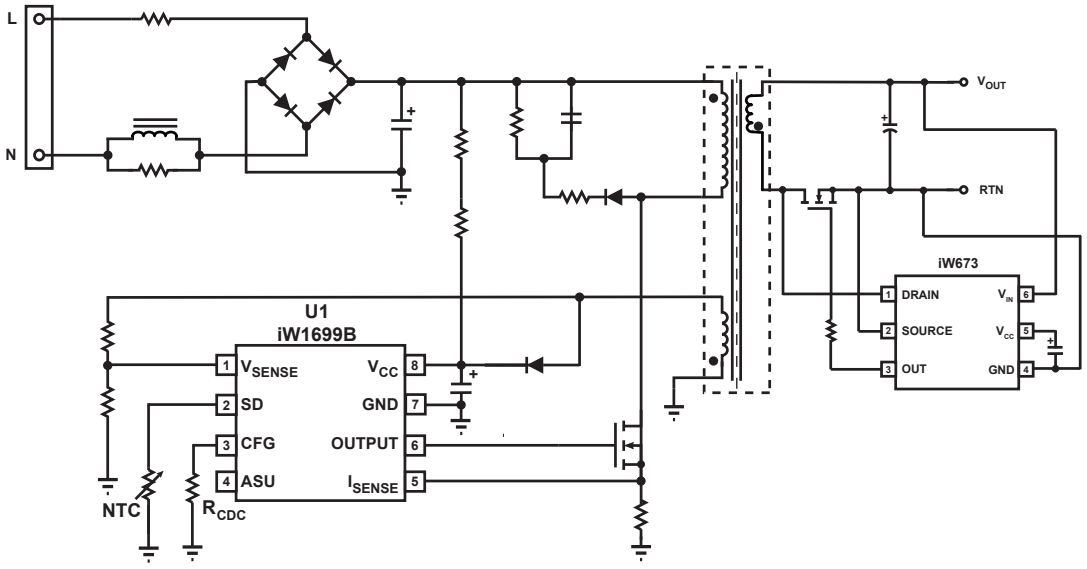


Figure 3.2: iW673 Typical Application Circuit (Using iW1699B as Primary-Side Controller)
(Achieving <40mW No-Load Power Consumption in 5V, 2.5A Adapter Designs with Fast Dynamic Load Response, and Supporting Constant Current Operation down to 2V System Output)

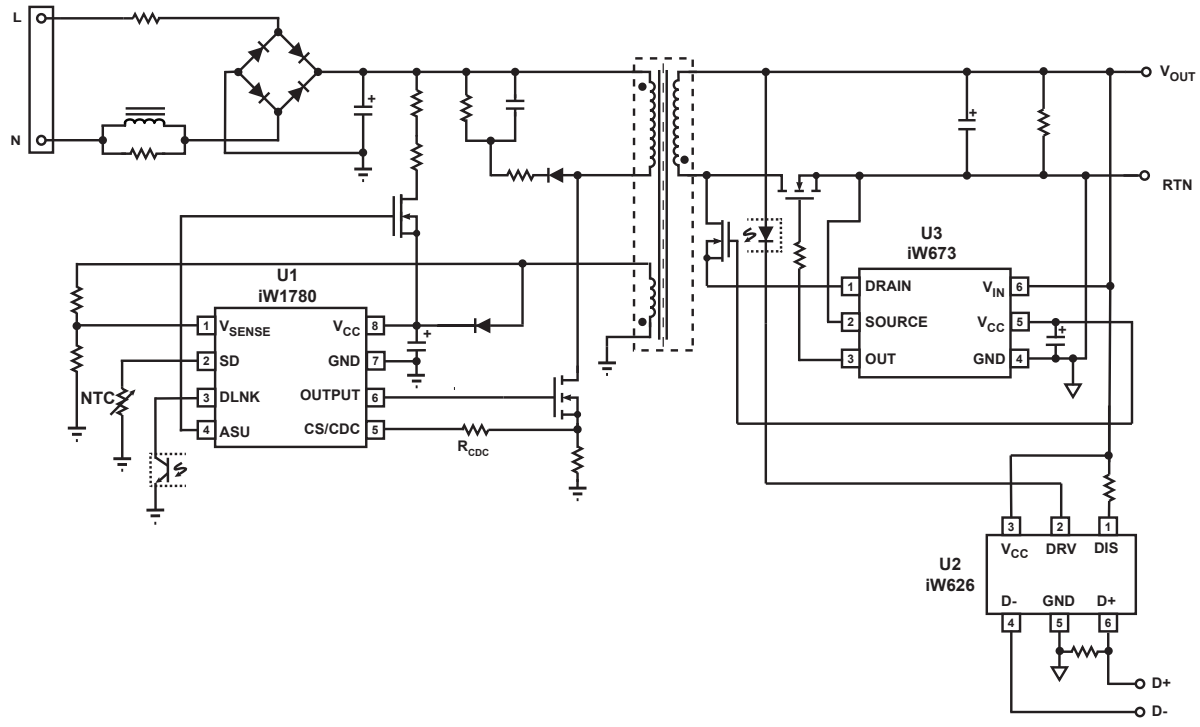


Figure 3.3: iW673 Typical Application Circuit for Multi-Level Output Voltage and Current
(Using iW1780 as Primary-Side Controller and iW626 as Secondary-Side Controller for QC2.0)
(Achieving <20mW No-Load Power Consumption)

Note: The DFET clamping circuit at the DRAIN pin of iW673 is not needed if the maximum voltage on the drain of the SR MOSFET is lower than 60V.

4.0 Pinout Description

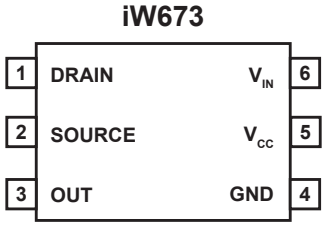


Figure 4.1: 6-Pin SOT23 Package

Pin #	Name	Type	Pin Description
1	DRAIN	Analog Input	Synchronous rectifier MOSFET drain voltage sensing and the Pulse Linear Regulator (PLR) input.
2	SOURCE	Analog input	Synchrnous rectifier MOSFET source voltage sensing input.
3	OUT	Output	Synchronous rectifier MOSFET driver.
4	GND	Ground	Ground.
5	V_{CC}	Power Input	LDO and PLR output. Connect this pin to a capacitor.
6	V_{IN}	Analog Input	Input of the internal LDO and output voltage sensing circuit. Connect to adapter/charger output for bias voltage. The internal LDO clamps the V_{CC} voltage at 5V when V_{IN} > 5V.

5.0 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges that can cause permanent damage if exceeded. For maximum safe operating conditions, refer to Electrical Characteristics in Section 6.0.

Parameter	Symbol	Value	Units
V_{IN} DC supply voltage range (pin 6, I_{CC} = 15mA max)	V_{IN}	-0.3 to 33	V
Continuous DC supply current at V_{IN} pin (V_{IN} = 30V)	I_{VO}	15	mA
Continuous DC supply current at V_{CC} pin (V_{CC} = 5.5V)	I_{VCC}	15	mA
Gate peak output current	I_G	±3	A
DRAIN pin voltage	V_D	-1.5 to 60	V
DRAIN peak input current	I_{DRAIN}	300	mA
V_{CC} pin voltage	V_{CC}	-0.6 to 6	V
Junction temperature	T_J	-40 to 150	°C
Storage temperature		–65 to 150	°C
ESD rating per JEDEC JESD22-A114		2,000	V

6.0 Electrical Characteristics

V_{CC} = 5V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low Dropout Regulator (LDO) and Pulse Linear Regulator (PLR) Blocks						
Switching between LDO and PLR						
PLR disable rising threshold at V_{IN} pin	$V_{LR\_DISABLE}$		4.65	4.8	4.9	V
PLR disable hysteresis at V_{IN} pin	V_{LR_HYS}		0.13	0.16	0.22	V
PLR enable falling threshold at V_{IN} pin	V_{LR_ENABLE}		4.45	4.65	4.75	V
LDO						
DC regulation voltage	V_{LDO}	V_{IN} = 6A, I_{LDO} = 5mA	4.75	5	5.25	V
Pulse Linear Regulator (PLR)						
Regulated output voltage at V_{CC}	V_{PLROUT}		4.2	5	TBD	V
Synchronous Rectifier Block						
Bias Voltage Supply						
DC supply operating voltage (Note 2)	V_{CC}				5.5	V
Bias current	I_{CC_BIAS}	OUT pin floating, 50kHz		640	1300	µA
Bias current, no load	I_{CC_NL}	OUT pin floating, 1kHz		430	650	µA
UVLO for SR Driver Block, at V_{CC} Pin						
V_{CC} POR threshold, SR	$V_{CC\_SR\_POR}$	Voltage applied on V_{CC} and V_{IN} floating	3.13	3.3	3.47	V
UVLO hysteresis, SR	$V_{CC\_\_SR\_HYS}$	Voltage applied on V_{CC} and V_{IN} floating	0.15	0.24	0.26	V
V_{CC} UVLO threshold, SR	$V_{CC\_\_SR\_UVLO}$	Voltage applied on V_{CC} and V_{IN} floating	2.9	3.1	3.22	V
Gate Driver						
Gate pull-up resistor	R_{UP}		2.5	4	6.5	Ω
Gate pull-down resistor	R_{DOWN}		1	2	4.1	Ω
Gate output high voltage (Note 1)	V_{G_H}		V_{CC}-0.3	V_{CC}-0.2	5.5	V
Gate output low voltage (Note 1)	V_{G_L}		0	0.15	0.25	V
Gate rising time (Note 1)	t_{G_RISE}	1V to 4V, 3.3nF		44		ns
Gate falling time (Note 1)	t_{G_FALL}	4V to 1V, 3.3nF		31		ns
SR function enable threshold, at V_{IN} pin	V_{SR_ENABLE}		1.1	1.3	1.5	V
SR function enable hysteresis, at V_{IN} pin	$V_{SR\_ENABLE\_HYS}$		0.09	0.12	0.15	V

Electrical Characteristics (continued)

V_{CC} = 5V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	
Turn-on threshold	V_{ON_TH}		-153	-120	-100	mV
Turn-off threshold, initial	$V_{OFF\_TH\_INIT}$			0		mV
Minimun off delay comparator threshold	$V_{MIN\_OFF\_TH}$		0.4	0.6	0.8	V
Minimum On/Off Time						
Minimum on time	t_{ON_MIN}		0.7	0.8	0.9	µs
Minimum off time (Note 3)	t_{OFF_MIN}		2.2	2.4	2.7	µs

Notes:

Note 1: These parameters are not 100% tested. They are guaranteed by design and/or characterization.

Note 2: The parameters are recommended maximum operation range of the pin.

Note 3: The minimum off time increases if the actual on time is the same as the minimum on time. See Section 9.3 for more information.

7.0 Typical Performance Characteristics

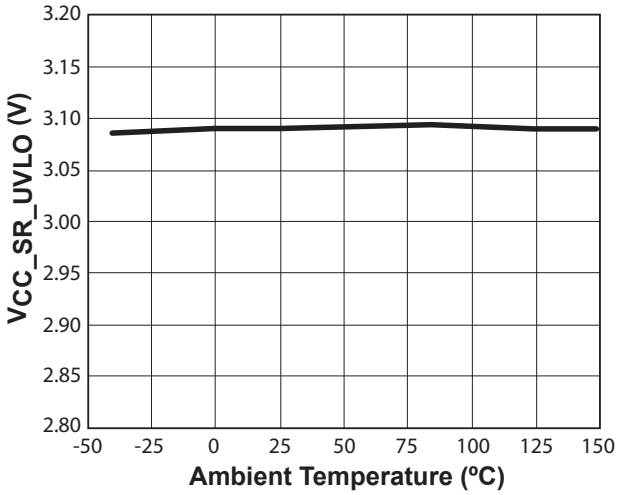


Figure 7.1 : V_{CC} UVLO Voltage vs.Temperature

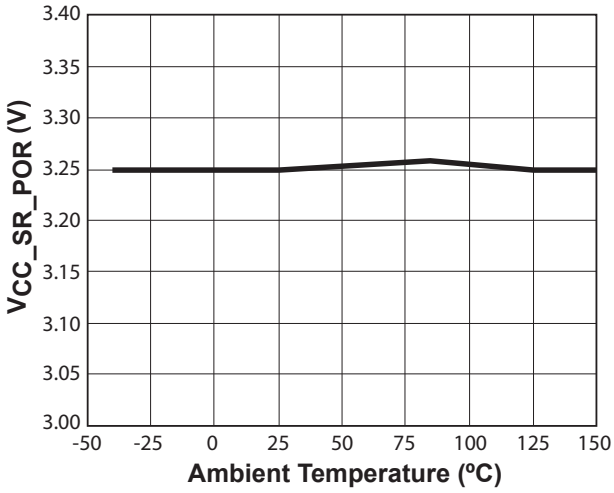


Figure 7.2 : V_{CC} POR Voltage vs.Temperature

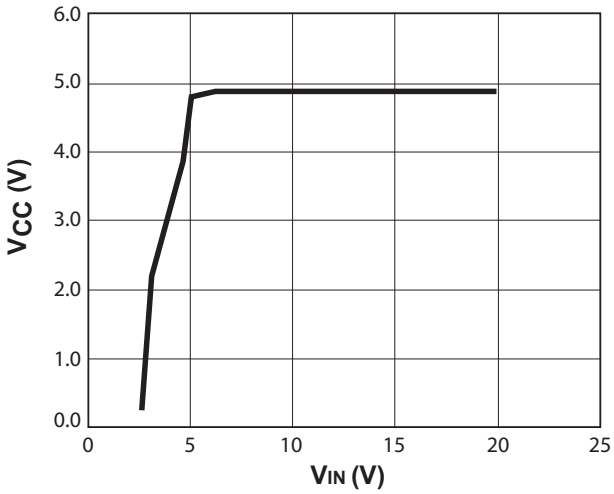


Figure 7.3 : LDO Regulation

8.0 Functional Block Diagram

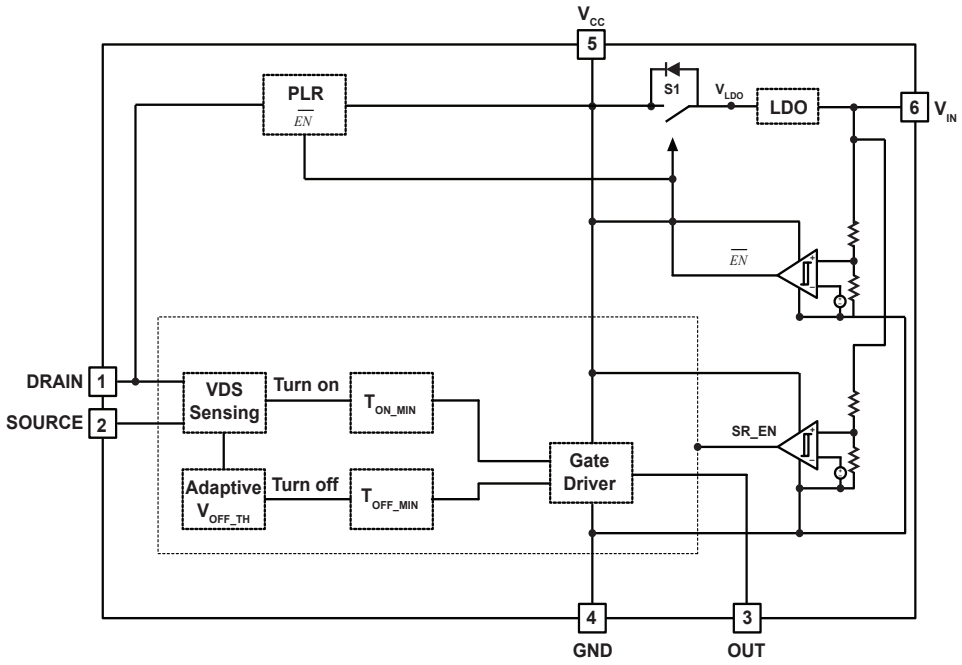


Figure 8.1: iW673 Functional Block Diagram

9.0 Theory of Operation

The iW673 is a synchronous rectifier controller that uses a new, proprietary digital adaptive turn-off control technology to minimize the turn-off deadtime. This results in a lower diode conduction loss at the deadtime so that no parallel Schottky diode is required. A Pulse Linear Regulator (PLR) is integrated into the controller to provide regulated voltage to the V_{CC} of the iW673, so that the controller can operate at constant current (CC) mode in which the system output voltage may drop to as low as 2V. This significantly reduces the conduction loss at CC mode and relieves the thermal stress at the secondary side. The PLR is disabled when system output voltage is higher than 4.8V, in which case the system output powers the iW673 through its internal LDO. The internal LDO supports up to 30V to cover a wide range of system outputs including 5V, 12V, and 20V.

Figure 8.1 shows the block diagram of iW673. It measures the voltage across the synchronous MOSFET to achieve lossless current sensing for the driver timing control. The digital SR logic control block generates the gate driver control signal based on the drain-to-source voltage of the synchronous MOSFET. The gate driver control signal is fed into the integrated MOSFET driver to drive the synchronous MOSFET.

The iW673 enters light load mode when the switching frequency of the flyback is low. The operating current is reduced to 650µA to reduce the light load and no load loss of the whole system.

9.1 Pin Detail

Pin 1 – DRAIN

Synchronous MOSFET drain voltage sensing and Pulse Linear Regulator (PLR) input. Connect this pin as close to the drain of the MOSFET as possible to avoid noise picked up from the traces.

The PLR is at the ON state when the V_{IN} pin (directly connected to flyback output) voltage is lower than 4.8V. The peak current to this pin at start-up can be as high as 300mA. The average current at normal operation is less than 10mA. Note that the voltage rating of the pin is 60V. In 12V or 20V system output applications, the synchronous MOSFET's drain voltage may be above the DRAIN pin's maximum voltage rating. In this case, DFET is needed to clamp the DRAIN pin voltage. Refer to Section 9.4 for details.

Pin 2 – Source

Synchronous MOSFET source voltage sensing. Connect this pin as close to the source of the MOSFET as possible to avoid noise picked up from the traces.

Pin 3 – OUT

Gate drive for the external synchronous MOSFET switch.

Pin 4 – GND

Ground.

Pin 5 – V_{CC}

Output of Pulse Linear Regulator and the internal linear regulator. It provides bias voltage for the controller. A capacitor (typical 4.7µF) must be connected between the V_{CC} pin and GND.

Pin 6 – V_{IN}

Internal linear regulator (LDO) input. Connect this pin to the flyback output. The internal linear regulator output is internally connected to V_{CC} through a MOSFET (S1 in Figure 8.1).

This pin is also the input of PLR-enable comparator. This comparator enables PLR when flyback output is lower than 4.8V. When PLR is at the ON state, the MOSFET S1 is at the OFF state to avoid reverse current from V_{CC} to V_{IN} pin. The body diode of the MOSFET S1 still allows positive current from the LDO to the V_{CC}. When flyback output is higher than 4.8V, the PLR is at the OFF state and the S1 is at the ON state.

This pin is also the input of synchronous rectification function comparator. The synchronous rectification function is disabled if the V_{IN} pin voltage is lower than 1.3V.

9.2 Powering the Controller

Internal circuits of the controller require bias voltage between 3V and 5.5V from the capacitor at the V_{CC} pin. Depending on the flyback output voltage level and the connection, the V_{CC} is powered by either the internal linear regulator or the internal pulse linear regulator.

For 5V application with constant current (CC) mode support, the V_{IN} pin must be connected to the flyback output and the PLRIN pin must be connected to the drain of the synchronous MOSFET through a diode. Ensure that the maximum voltage on the drain of the synchronous MOSFET does not exceed the voltage rating of the PLRIN pin.

When the flyback operates at constant current mode, the flyback output voltage may drop to as low as 2V. In order to provide sufficient bias voltage for the continuous operation of the synchronous rectifier controller at constant current mode, the pulse linear regulator provides bias current to the

controller from the drain on the synchronous MOSFET. The IC monitors the flyback output voltage at the V_{IN} pin. When flyback output voltage is lower than 4.8V, the PLR block is enabled. Pulse current from the drain of the synchronous MOSFET charges and maintains the V_{CC} voltage level at 5V. In order to prevent reverse current from V_{CC} to V_{IN} pin, the MOSFET S1 between the LDO output and the V_{CC} pin is at the OFF state when the PLR is at the ON state.

At normal operation when the flyback output is higher than 4.8V, the PLR is at the OFF state and the switch MOSFET S1 is at the ON state. The flyback output provides the operating current through the LDO into the V_{CC} pin. The LDO regulates the V_{CC} voltage at 5V. When the flyback output is close to 5V, the LDO cannot maintain V_{CC} regulation and it operates at pass through mode. In this mode the drop-out voltage from the V_{IN} pin to V_{CC} pin is smaller than 0.4V when the V_{IN} pin current is 5mA.

At startup, both PLR and the internal linear regulator are enabled. Although the switch S1 is turned off, the LDO is still able to charge the V_{CC} up through the body diode of S1. Since the PLR has stronger current capability and higher input voltage level, it may charge up the V_{CC} voltage higher than the flyback output voltage during the startup. Once the flyback output voltage reaches 4.8V, the PLR is at the OFF state. The switch S1 is at the ON state and the internal LDO provides the operating current to V_{CC}.

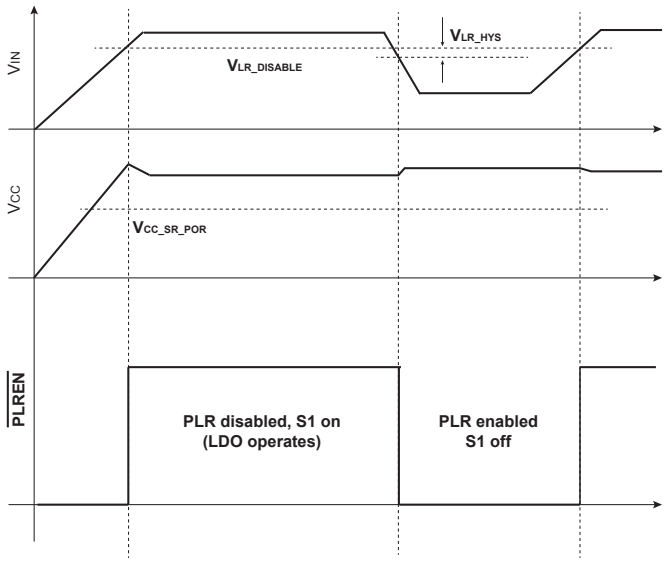


Figure 9.1: Start-up Sequencing Diagram

9.3 V_{DS} Sensing and Synchronous Rectifier Driving Scheme

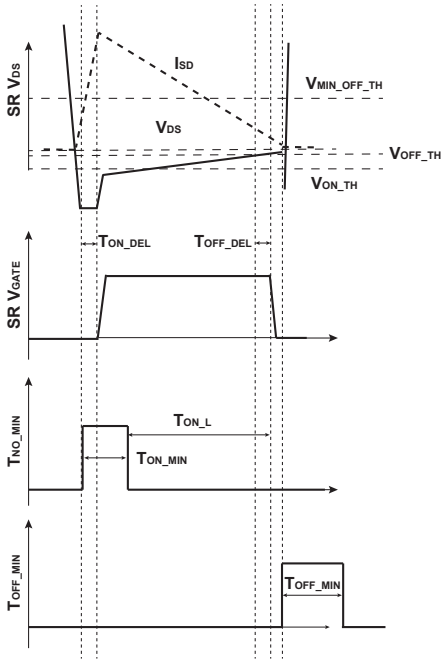


Figure 9.2: SR Control Block Sequencing Diagram

The synchronous rectifier (SR) control block monitors the synchronous MOSFET's drain voltage (V_{DS}) to determine the driver timing. When the V_{DS} is below the V_{ON_TH} (-120mV), control block turns on the synchronous MOSFET with its built-in driver. The driver has a minimum on time (T_{ON_MIN}, 0.8us) to avoid the noise from turning off the driver immediately.

As the current I_{SD} decreases, V_{DS} increases and gets close to 0 mV. The SR driver is turned off when the V_{DS} reaches V_{OFF_TH}. For iW673, Dialog's proprietary adaptive turn-off technology minimizes the turn-off deadtime.

After the SR driver turns off, the V_{DS} rises. When the V_{DS} reaches $V_{MIN\_OFF\_TH}$, the SR control block initiates a 2.5µs timer during which the SR remains off to avoid the ringing from turning on the synchronous MOSFET.

During the startup, the system output voltage may be too low to reset the transformer so that the system may operate at the Continuous Current Mode (CCM). To avoid the SR operation at CCM, a comparator at V_{IN} pin monitors the system output. When V_{IN} voltage is lower than 1.3V, the whole SR control block is disabled.

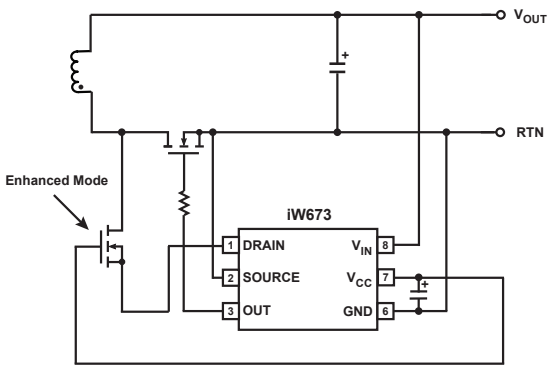
If the T_{ON_L} is smaller than 100ns, the following T_{OFF_MIN} is extended to 5µs.

9.4 High Voltage Support for DRAIN Pin

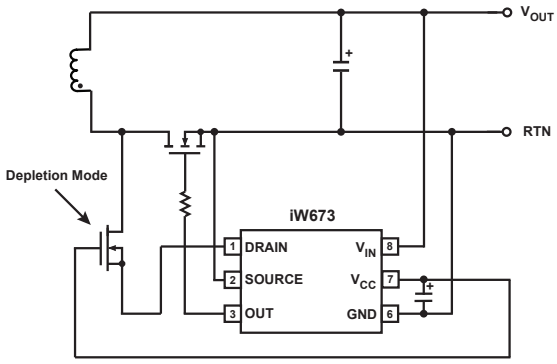
The maximum voltage rating of the V_{IN} pin is 30V. Therefore, the iW673 can support a wide range of system output voltages, such as 5V, 9V, 12V, 19V or above. However, the maximum voltage ratings of the DRAIN pin is limited to 60V, which provides enough margins for a typical 5V output design but may not be sufficient for higher output designs. During a system design stage, it is recommended to evaluate the voltage stress on the drain of the SR MOSFET. If the maximum drain-to-source voltage on the SR MOSFET is close to or higher than 60V, an external voltage clamping circuit is required to protect the DRAIN pin.

Figure 9.3 shows recommended voltage clamping circuits for different applications in which the voltage stress on the drain of the SR MOSFET exceeds 60V. If the PLRIN function is not used, the DRAIN pin can be protected with a NMOS, as shown in Figure 9.3(a). By connecting the gate of the NMOS to V_{CC} of iW673, the DRAIN pin voltage (connected to the source of the NMOS) is clamped below $V_{CC} – V_{TH}$, where the V_{TH} is the turn-on threshold of the NMOS. The V_{TH} of the NMOS is recommended to be smaller than 3V (maximum 2.5V preferred) to allow proper operation of the iW673.

If the PLRIN function is used, in order for the PLR circuit to operate properly, the maximum DRAIN voltage should be higher than the V_{CC} voltage. The enhanced mode NMOS cannot be used as the clamping circuit. Instead, a depletion NMOS is recommended as the clamping circuit for such applications, as shown in Figure 9.3(b). By connecting the gate of the depletion mode NMOS to V_{CC} of iW673, the DRAIN pin voltage (connected to the source of the depletion mode NMOS) is clamped below $V_{CC} – V_{TH}$, where the V_{TH} is the turn-on threshold of the depletion mode NMOS and has a negative value. The V_{TH} of the depletion mode NMOS is recommended to be lower than -5V to allow enough current driving capability of the pulse linear regulator.



(a) Voltage Clamping Circuit for DRAIN Only, PLRIN Not Used



(b) Voltage Clamping Circuit for Both DRAIN and PLRIN (Current at PLRIN Pin is also Clamped.)

Figure 9.3: Clamping Circuit for DRAIN Pin of the iW673

9.5 Layout Considerations

Layout of the system printed circuit board is very important for high performance of the controller IC in terms of accurate signal sensing and lower driving related loss.

The switching on and off of the active device in the switch mode power supply causes fast change of current and voltage in the circuit. Such fast current change induces voltage transient on the parasitic impedance of the power devices, interconnect or circuit traces. This voltage transient may be picked up by the signal sensing circuit of the controller and compromise its performance. Thus it is important to reduce this voltage transient by minimizing the parasitic impedance with proper layout. The critical components must be placed as close to each other as possible and be connected with wide and short traces.

Figure 9.4 shows the critical components and their connections on the secondary side of a flyback converter with synchronous rectifier. The synchronous MOSFET and the output capacitor must be close to each other. And the PCB trace between them must be wide and short. The GND pin of the iW673 must be connected to the source of the MOSFET with single point connection. If vias are used in the layout for the ground connection, it is recommended to use at least two vias in parallel to reduce their impedance.

To reduce the ringing at the turn-on and turn-off transient of the synchronous MOSFET, the gate driving current loop must be as small as possible.

The V_{CC} capacitor (C_{VCC}) must be as close to the IC as possible to minimize the loop.

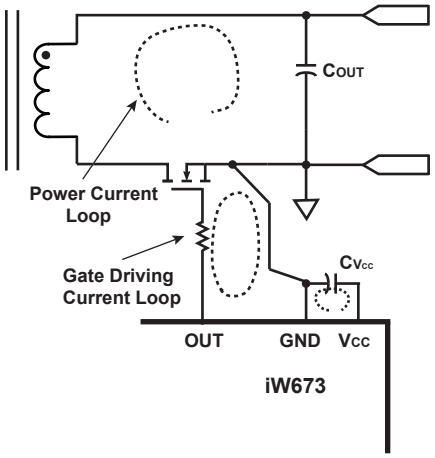


Figure 9.4: Power Loops at the Secondary Side of the Flyback

Figure 9.5 shows the connection for V_{DS} voltage sensing. It is very important that the source of synchronous MOSFET is directly connected to the SOURCE pin of the iW673. The DRAIN pin must be connected as close to the drain of synchronous MOSFET as possible. The voltage sensing loops must be minimized to reduce the coupling of noise.

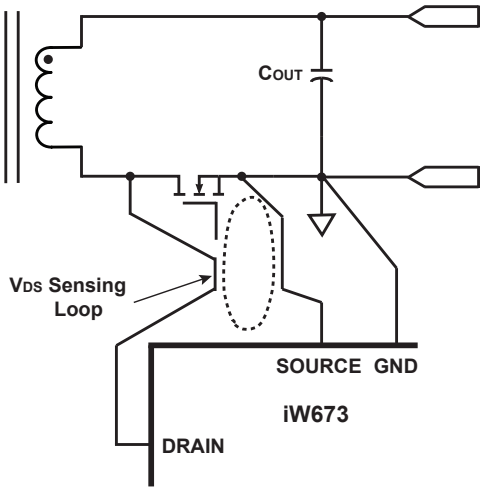


Figure 9.5: Voltage Sensing Loops at the Secondary Side of the Flyback

Figure 9.6 shows an example of an improper layout connection. In this layout the SOURCE of the iW673 is not connected to the source of the MOSFET. Instead, it is connected closer to the system output connector at point B. The trace between point A and B carries the output current. Such current causes voltage drop on the trace and introduces an offset on the V_{DS} sensing circuit. This offset changes with the load current and affects the turn-off timing of the iW673. To avoid this issue, the SOURCE of the iW673 must be connected directly to point A.

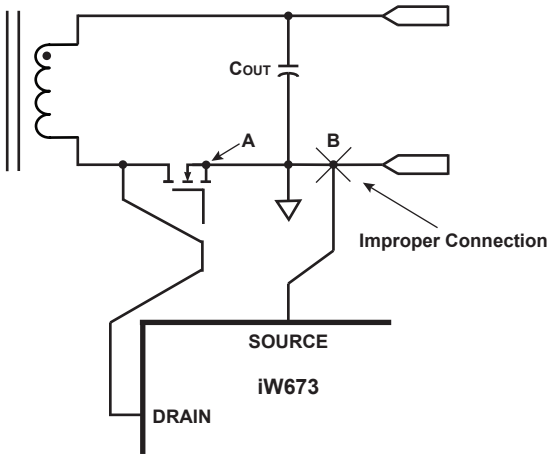
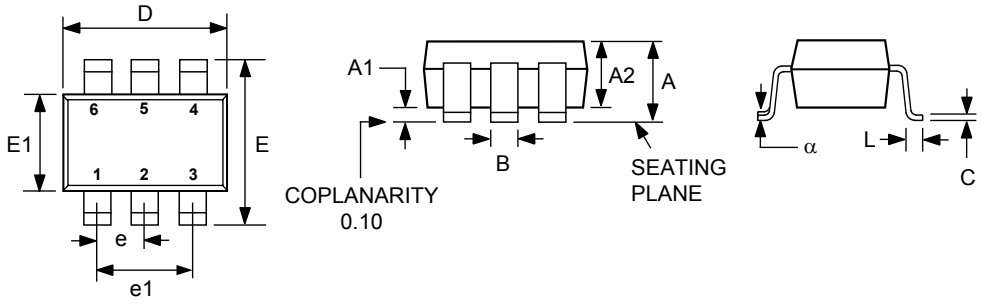


Figure 9.6: Example of Improper Ground Connection

10.0 Physical Dimensions

6-Lead SOT Package



Symbol	Millimeters	
	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.30	0.50
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.55
α	0°	8°

Compliant to JEDEC Standard MO-178AB

Controlling dimensions are in millimeters

This package is RoHS compliant and Halide free.

Soldering Temperature Resistance:

[a] Package is IPC/JEDEC Std 020D Moisture Sensitivity Level 1

[b] Package exceeds JEDEC Std No. 22-A111 for Solder Immersion Resistance; packages can withstand 10 s immersion < 260ºC

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.25 mm per side.

The package top may be smaller than the package bottom. Dimensions D and E1 are are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs and interlead flash, but including any mismatch between top and bottom of the plastic body.

11.0 Ordering Information

Part Number	Options	Package	Description
iW673-00	N/A	SOT23, 6 pin	Tape & Reel[1]

Note 1: Tape & Reel packing quantity is 2,500/reel. Minimum ordering quantity is 2,500.

Digital Green-Mode Synchronous Rectifier Controller

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United Kingdom
Dialog Semiconductor (UK) Ltd
Phone: +44 1793 757700

Germany
Dialog Semiconductor GmbH
Phone: +49 7021 805-0

The Netherlands
Dialog Semiconductor B.V.
Phone: +31 73 640 88 22

Email
info_pcbg@diasemi.com

North America
Dialog Semiconductor Inc.
Phone: +1 408 845 8500

Japan
Dialog Semiconductor K. K.
Phone: +81 3 5425 4567

Taiwan
Dialog Semiconductor Taiwan
Phone: +886 281 786 222

Web site:
www.dialog-semiconductor.com

Singapore
Dialog Semiconductor Singapore
Phone: +65 648 499 29

Hong Kong
Dialog Semiconductor Hong Kong
Phone: +852 2607 4271

Korea
Dialog Semiconductor Korea
Phone: +82 2 3469 8200

China
Dialog Semiconductor (Shenzhen)
Phone: +86 755 2981 3669

Dialog Semiconductor (Shanghai)
Phone: +86 21 5424 9058