mXT1664T3 2.0

maXTouch 1664-node Touchscreen Controller

maXTouch® Adaptive Sensing Touchscreen Technology

- Up to 32 X (transmit) lines and 52 Y (receive) lines for use by touchscreen.
- A maximum of 1664 nodes can be allocated to the touchscreen
- Touchscreen size of 15.6 inches (16:10 aspect ratio), assuming a sensor electrode pitch of 6.5 mm. Other sizes are possible with different electrode pitches and appropriate sensor material
- Multiple touch support with up to 16 concurrent touches tracked in real time
- Dual-boot OS support for Microsoft® Windows® and Android™

Touch Sensor Technology

- Discrete/out-cell support including glass and PET film-based sensors
- Support for standard (for example, Diamond) and proprietary sensor patterns (review of designs by Microchip or a Microchip-qualified touch sensor module partner is recommended)

Front Panel Material

- Works with PET or glass, including curved profiles (configuration and stack-up to be approved by Microchip or a Microchip-qualified touch sensor module partner)
- Glass 0.4 mm to 4.5 mm (dependent on screen size, touch size, configuration and stack-up)
- Plastic 0.2 mm to 2.2 mm (dependent on screen size, touch size, configuration and stack-up)

Touch Performance

- Moisture/Water Compensation
  - No false touch with condensation or water drop up to 22 mm diameter
  - One-finger tracking with condensation or water drop up to 22 mm diameter
- Glove Support
  - Multiple-finger glove touches up to 1.5 mm thickness (subject to stack-up design)
  - Single-finger glove touch up to 5 mm thickness (subject to stack-up design)
- Mutual capacitance and self capacitance measurements supported for robust touch detection

- Noise suppression technology to combat ambient, charger, and power-line noise
  - Up to 240 V_{PP} between 1 Hz and 1 kHz sinusoidal waveform
  - Up to 20 V_{PP} between 1 kHz and 1 MHz sinusoidal waveform
- Stylus Support
  - Supports passive stylus with 1.5 mm contact diameter, subject to configuration, stack-up, and sensor design
- Scan Speed
  - Up to 250 Hz reporting rate for one finger (subject to configuration)
  - Typical report rate for 16 touches ≥100 Hz (subject to configuration)
  - Initial touch latency <10 ms for first touch from idle (subject to configuration)
  - Configurable to allow for power and speed optimization

Enhanced Algorithms

- Lens bending algorithms to remove display noise
- Touch suppression algorithms to remove unintentional large touches, such as palm
- Palm Recovery Algorithm for quick restoration to normal state

Power Saving

- Programmable timeout for automatic transition from active to idle states
- Pipelined analog sensing detection and digital processing to optimize system power efficiency

Application Interfaces

- I^2C slave with support for Standard mode (up to 100 kHz), Fast mode (up to 400 kHz), Fast-mode Plus (up to 1 MHz), High Speed mode (up to 3.4 MHz)
- USB HID interface for Microsoft Windows 8.x and later versions
- HID-I^2C interface for Microsoft Windows 8.x and later versions
- Interrupt to indicate when a message is available
- SPI Debug Interface to read the raw data for tuning and debugging purposes

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Power Supply

- Digital (Vdd) 3.3 V nominal
- Digital I/O (VddIO) 3.3 V nominal
- Analog (AVdd) 3.3 V nominal
- High voltage external X line drive (XVdd) up to 10 V

Packages

- 136-ball UFBGA 7 × 7 × 0.6 mm, 0.5 mm pitch
- 162-ball UFBGA 10 × 5 × 0.6 mm, 0.5 mm pitch

Operating Temperature

- −40°C to +85°C

PIN CONFIGURATION

0.1 136-ball UFBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	X31	X30	X28	X25	X22	X19	XVDD	GND	X12	X9	X6	X3	X1
B	XVDD	X29	X27	X24	X21	X18	X16	X14	X11	X8	X5	X2	X0
C	GND	GND	X26	X23	X20	X17	X15	X13	X10	X7	X4	XVDD	VREGBOOST
D	AVDD	VDDCORE	GND								GND	GND	AVDD
E	Y27	Y26	AVDD								AVDD	Y0	Y1
F	Y30	Y29	Y28			GPIO0	GPIO4	GND			Y2	Y3	Y4
G	Y33	Y32	Y31			CHG		DBG_SS TEST			Y5	Y6	Y7
H	Y36	Y35	Y34			NOISE_IN	GPIO3	DBG_DATA XTAL_XOUT		DS0	Y8	Y9	Y10
J	Y39	Y38	Y37								Y11	Y12	Y13
K	Y42	Y41	Y40	VDDIO	USBDM	I2CMODE	GND	PTCXY0	PTCXY1	NC	Y14	Y15	Y16
L	Y45	Y44	Y43	GND	SDA	COMMSEL	GPIO2	DBG_CLK XTAL_XIN	PTCXY2	NC	Y17	Y18	Y19
M	Y48	Y47	Y46	GND	SCL	ADDSEL USBDP	GPIO1	GPIO5	PTCXY3	GND	Y20	Y21	Y22
N	Y51	Y50	Y49	AVDD	RESET	VDD	VDDCORE	VDDIO	PTCXY4	AVDD	Y23	Y24	Y25

Top View

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TABLE 1: PIN LISTING – 136-BALL UFBGA

Ball	Name	Type	Supply	Description	If Unused...
A1	X31	S	XVdd	X matrix drive line	Leave open
A2	X30	S	XVdd	X matrix drive line	Leave open
A3	X28	S	XVdd	X matrix drive line	Leave open
A4	X25	S	XVdd	X matrix drive line	Leave open
A5	X22	S	XVdd	X matrix drive line	Leave open
A6	X19	S	XVdd	X matrix drive line	Leave open
A7	XVDD	P	–	X line drive power	–
A8	GND	P	–	Ground	–
A9	X12	S	XVdd	X matrix drive line	Leave open
A10	X9	S	XVdd	X matrix drive line	Leave open
A11	X6	S	XVdd	X matrix drive line	Leave open
A12	X3	S	XVdd	X matrix drive line	Leave open
A13	X1	S	XVdd	X matrix drive line	Leave open
B1	XVDD	P	–	X line drive power	–
B2	X29	S	XVdd	X matrix drive line	Leave open
B3	X27	S	XVdd	X matrix drive line	Leave open
B4	X24	S	XVdd	X matrix drive line	Leave open
B5	X21	S	XVdd	X matrix drive line	Leave open
B6	X18	S	XVdd	X matrix drive line	Leave open
B7	X16	S	XVdd	X matrix drive line	Leave open
B8	X14	S	XVdd	X matrix drive line	Leave open
B9	X11	S	XVdd	X matrix drive line	Leave open
B10	X8	S	XVdd	X matrix drive line	Leave open
B11	X5	S	XVdd	X matrix drive line	Leave open
B12	X2	S	XVdd	X matrix drive line	Leave open
B13	X0	S	XVdd	X matrix drive line	Leave open
C1	GND	P	–	Ground	–
C2	GND	P	–	Ground	–
C3	X26	S	XVdd	X matrix drive line	Leave open
C4	X23	S	XVdd	X matrix drive line	Leave open
C5	X20	S	XVdd	X matrix drive line	Leave open
C6	X17	S	XVdd	X matrix drive line	Leave open
C7	X15	S	XVdd	X matrix drive line	Leave open
C8	X13	S	XVdd	X matrix drive line	Leave open
C9	X10	S	XVdd	X matrix drive line	Leave open
C10	X7	S	XVdd	X matrix drive line	Leave open
C11	X4	S	XVdd	X matrix drive line	Leave open
C12	XVDD	P	–	X line drive power	–
C13	VREGBOOST	O	AVdd	Voltage booster control	Leave open
D1	AVDD	P	–	Analog power	–
D2	VDDCORE	P	–	Digital power	–
D3	GND	P	–	Ground	–

TABLE 1:   PIN LISTING – 136-BALL UFBGA (CONTINUED)

Ball	Name	Type	Supply	Description	If Unused...
D11	GND	P	–	Ground	–
D12	GND	P	–	Ground	–
D13	AVDD	P	–	Analog power	–
E1	Y27	S	AVdd	Y line connection	Leave open
E2	Y26	S	AVdd	Y line connection	Leave open
E3	AVDD	P	–	Analog power	–
E11	AVDD	P	–	Analog power	–
E12	Y0	S	AVdd	Y line connection	Leave open
E13	Y1	S	AVdd	Y line connection	Leave open
F1	Y30	S	AVdd	Y line connection	Leave open
F2	Y29	S	AVdd	Y line connection	Leave open
F3	Y28	S	AVdd	Y line connection	Leave open
F6	GPIO0	I/O	VddIO	General purpose I/O; see Section 2.5.8 "GPIO Pins"	Connect to GND
F7	GPIO4	I/O	VddIO	General purpose I/O; see Section 2.5.8 "GPIO Pins"	Connect to GND
F8	GND	P	–	Ground	–
F11	Y2	S	AVdd	Y line connection	Leave open
F12	Y3	S	AVdd	Y line connection	Leave open
F13	Y4	S	AVdd	Y line connection	Leave open
G1	Y33	S	AVdd	Y line connection	Leave open
G2	Y32	S	AVdd	Y line connection	Leave open
G3	Y31	S	AVdd	Y line connection	Leave open
G6	$\overline{\text{CHG}}$	OD	VddIO	Change line interrupt. This line is briefly set (~100 ms) as an input after power-up or reset for diagnostic purposes	–
G8	$\overline{\text{DBG\_SS}}$	I/O	VddIO	Debug SS line; requires external pull-up to VddIO	Pull up to VddIO
	$\overline{\text{TEST}}$	–		Reserved for factory use	
G11	Y5	S	AVdd	Y line connection	Leave open
G12	Y6	S	AVdd	Y line connection	Leave open
G13	Y7	S	AVdd	Y line connection	Leave open
H1	Y36	S	AVdd	Y line connection	Leave open
H2	Y35	S	AVdd	Y line connection	Leave open
H3	Y34	S	AVdd	Y line connection	Leave open
H6	NOISE_IN	I	VddIO	Noise present input	Connect to GND
H7	GPIO3	I/O	VddIO	General purpose I/O; see Section 2.5.8 "GPIO Pins"	Connect to GND

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TABLE 1: PIN LISTING – 136-BALL UFBGA (CONTINUED)

Ball	Name	Type	Supply	Description	If Unused...
H8	DBG_DATA	O	VddIO	Debug data; see Section 2.5.9 "SPI Debug Interface"	I²C Mode: Connect to test point Connect to GND
	XTAL_XOUT	O		USB mode: External oscillator output; see Section 2.5.6 "XTAL_XOUT and XTAL_XIN"	
H10	DS0	S	AVdd	Driven Shield signal; used as guard track between X/Y signals and ground	Leave open
H11	Y8	S	AVdd	Y line connection	Leave open
H12	Y9	S	AVdd	Y line connection	Leave open
H13	Y10	S	AVdd	Y line connection	Leave open
J1	Y39	S	AVdd	Y line connection	Leave open
J2	Y38	S	AVdd	Y line connection	Leave open
J3	Y37	S	AVdd	Y line connection	Leave open
J11	Y11	S	AVdd	Y line connection	Leave open
J12	Y12	S	AVdd	Y line connection	Leave open
J13	Y13	S	AVdd	Y line connection	Leave open
K1	Y42	S	AVdd	Y line connection	Leave open
K2	Y41	S	AVdd	Y line connection	Leave open
K3	Y40	S	AVdd	Y line connection	Leave open
K4	VDDIO	P	–	Digital power	–
K5	USBDM	USB	VddIO	USB mode: Data Minus	Connect to GND
K6	I2CMODE	I	VddIO	I²C Mode: Selects I²C mode; see Section 7.2 "I²C Mode Selection – I2CMODE Pin"	–
K7	GND	P	–	Ground	–
K8	PTCXY0	I/O	AVdd	Reserved for future use	Leave open
K9	PTCXY1	I/O	AVdd	Reserved for future use	Leave open
K10	NC	–	–	No connection	–
K11	Y14	S	AVdd	Y line connection	Leave open
K12	Y15	S	AVdd	Y line connection	Leave open
K13	Y16	S	AVdd	Y line connection	Leave open
L1	Y45	S	AVdd	Y line connection	Leave open
L2	Y44	S	AVdd	Y line connection	Leave open
L3	Y43	S	AVdd	Y line connection	Leave open
L4	GND	P	–	Ground	–
L5	SDA	OD	VddIO	I²C Mode: Serial Data	–
L6	COMMSEL	I	VddIO	Communications Interface Selection; see Section 7.1 "Host Communication Mode Selection – COMMSEL Pin"	–
L7	GPIO2	I/O	VddIO	General purpose I/O; see Section 2.5.8 "GPIO Pins"	Connect to GND
L8	DBG_CLK	O	VddIO	Debug clock; see Section 2.5.9 "SPI Debug Interface"	I²C Mode: Connect to test point Connect to GND
	XTAL_XIN	I		USB mode: External oscillator input; see Section 2.5.6 "XTAL_XOUT and XTAL_XIN"	
L9	PTCXY2	I/O	AVdd	Reserved for future use	Leave open
L10	NC	–	–	No connection	–

TABLE 1:   PIN LISTING – 136-BALL UFBGA (CONTINUED)

Ball	Name	Type	Supply	Description	If Unused...
L11	Y17	S	AVdd	Y line connection	Leave open
L12	Y18	S	AVdd	Y line connection	Leave open
L13	Y19	S	AVdd	Y line connection	Leave open
M1	Y48	S	AVdd	Y line connection	Leave open
M2	Y47	S	AVdd	Y line connection	Leave open
M3	Y46	S	AVdd	Y line connection	Leave open
M4	GND	P	–	Ground	–
M5	SCL	OD	VddIO	I^{2}C Mode: Serial Clock input	–
M6	ADDSEL	I	VddIO	I^{2}C Mode: Address select; see Section 7.3 "I^{2}C Address Selection – ADDSEL Pin"	–
	USBDP	USB		USB mode: Data Plus	
M7	GPIO1	I/O	VddIO	General purpose I/O; see Section 2.5.8 "GPIO Pins"	Connect to GND
M8	GPIO5	I/O	VddIO	General purpose I/O; see Section 2.5.8 "GPIO Pins"	Connect to GND
M9	PTCXY3	I/O	AVdd	Reserved for future use	Leave open
M10	GND	P	–	Ground	–
M11	Y20	S	AVdd	Y line connection	Leave open
M12	Y21	S	AVdd	Y line connection	Leave open
M13	Y22	S	AVdd	Y line connection	Leave open
N1	Y51	S	AVdd	Y line connection	Leave open
N2	Y50	S	AVdd	Y line connection	Leave open
N3	Y49	S	AVdd	Y line connection	Leave open
N4	AVDD	P	–	Analog power	–
N5	$\overline{\text{RESET}}$	I	VddIO	Reset low. It is recommend that this line is connected to the host system.	Pull up to VddIO
N6	VDD	P	–	Digital power	–
N7	VDDCORE	P	–	Digital core power	–
N8	VDDIO	P	–	Digital power	–
N9	PTCXY4	I/O	AVdd	Reserved for future use	Leave open
N10	AVDD	P	–	Analog power	–
N11	Y23	S	AVdd	Y line connection	Leave open
N12	Y24	S	AVdd	Y line connection	Leave open
N13	Y25	S	AVdd	Y line connection	Leave open

Key:

I	Input only	O	Output only	I/O	Input or output
OD	Open drain output	P	Ground or power	S	Sense pin

0.2 162-ball UFBGA

Top View

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	NC	NC	NC	NC	NC	GND	AVDD	Y42	Y46	Y50	GND	AVDD	NC	NC	NC	DS0	VDDIO	$\overline{RESET}$	SCL
B	NC	NC	NC	NC	NC	VDDCORE	Y38	Y41	Y45	Y49	NC	NC	NC	NC	NC	NC	GND	USBDM	SDA
C	NC	X31	X30	X29	X28	GND	Y37	Y40	Y44	Y48	NC	NC	NC	NC	NC	NC	AVDD	COMMSEL	ADDSEL USBDP
D	X27	X26	X25	X24	X23	XVDD	Y36	Y39	Y43	Y47	Y51	NC	NC	NC	NC	GND	GND	NOISE_IN	I2CMODE
E	X22	X21	X20	X19	GND										GND	GND	AVDD	GPIO0	$\overline{CHG}$
F	X18	X17	X16	X15	X14	XVDD	Y0	Y3	Y7	Y11	Y15	Y18	Y21	Y25	Y29	GND	GND	GPIO2	GPIO1
G	X13	X12	X11	X10	X9	GND	Y1	Y4	Y8	Y12	Y16	Y19	Y22	Y26	Y30	Y33	VDDIO	GPIO4	GPIO3
H	X8	X7	X6	X5	X4	XVDD	Y2	Y5	Y9	Y13	Y17	Y20	Y23	Y27	Y31	Y34	VDD	DBG_CLK XTAL_XIN	GPIO5
J	X3	X2	X1	X0	VREGBOOST	GND	AVDD	Y6	Y10	Y14	GND	AVDD	Y24	Y28	Y32	Y35	VDDCORE	$\overline{DBG\_SS}$ $\overline{TEST}$	DBG_DATA XTAL_XOUT

TABLE 2:   PIN LISTING – 162-BALL UFBGA

Ball	Name	Type	Supply	Description	If Unused...
A1	SCL	OD	VddIO	I^{2}C Mode: Serial Clock input	–
A2	$\overline{\text{RESET}}$	I	VddIO	Reset low. It is recommend that this line is connected to the host system.	Pull up to VDDIO
A3	VDDIO	P	–	Digital power	–
A4	DS0	S	AVdd	Driven Shield signal; used as guard track between X/Y signals and ground	Leave open
A5	NC	–	–	No connection	–
A6	NC	–	–	No connection	–
A7	NC	–	–	No connection	–
A8	AVDD	P	–	Analog power	–
A9	GND	P	–	Ground	–
A10	Y50	S	AVdd	Y line connection	Leave open
A11	Y46	S	AVdd	Y line connection	Leave open
A12	Y42	S	AVdd	Y line connection	Leave open
A13	AVDD	P	–	Analog power	–
A14	GND	P	–	Ground	–
A15	NC	–	–	No connection	–
A16	NC	–	–	No connection	–
A17	NC	–	–	No connection	–
A18	NC	–	–	No connection	–
A19	NC	–	–	No connection	–
B1	SDA	OD	VddIO	I^{2}C Mode: Serial Data	–
B2	USBDM	USB	VddIO	USB mode: Data Minus	Connect to GND
B3	GND	P	–	Ground	–
B4	NC	–	–	No connection	–
B5	NC	–	–	No connection	–
B6	NC	–	–	No connection	–
B7	NC	–	–	No connection	–
B8	NC	–	–	No connection	–
B9	NC	–	–	No connection	–
B10	Y49	S	AVdd	Y line connection	Leave open
B11	Y45	S	AVdd	Y line connection	Leave open
B12	Y41	S	AVdd	Y line connection	Leave open
B13	Y38	S	AVdd	Y line connection	Leave open
B14	VDDCORE	P	–	Digital core power	–
B15	NC	–	–	No connection	–
B16	NC	–	–	No connection	–
B17	NC	–	–	No connection	–
B18	NC	–	–	No connection	–
B19	NC	–	–	No connection	–
C1	ADDSEL	I	VddIO	I^{2}C Mode: Address select; see Section 7.3 "I^{2}C Address Selection – ADDSEL Pin"	–
	USBDP	USB		USB mode: Data Plus	

TABLE 2:   PIN LISTING – 162-BALL UFBGA (CONTINUED)

Ball	Name	Type	Supply	Description	If Unused...
C2	COMMSEL	I	VddIO	Communications Interface Selection; see Section 7.1 "Host Communication Mode Selection – COMMSEL Pin"	–
C3	AVDD	P	–	Analog power	–
C4	NC	–	–	No connection	–
C5	NC	–	–	No connection	–
C6	NC	–	–	No connection	–
C7	NC	–	–	No connection	–
C8	NC	–	–	No connection	–
C9	NC	–	–	No connection	–
C10	Y48	S	AVdd	Y line connection	Leave open
C11	Y44	S	AVdd	Y line connection	Leave open
C12	Y40	S	AVdd	Y line connection	Leave open
C13	Y37	S	AVdd	Y line connection	Leave open
C14	GND	P	–	Ground	–
C15	X28	S	XVdd	X matrix drive line	Leave open
C16	X29	S	XVdd	X matrix drive line	Leave open
C17	X30	S	XVdd	X matrix drive line	Leave open
C18	X31	S	XVdd	X matrix drive line	Leave open
C19	NC	–	–	No connection	–
D1	I2CMODE	I	VddIO	I^{2}C Mode: Selects I^{2}C mode; see Section 7.2 "I^{2}C Mode Selection – I2CMODE Pin"	–
D2	NOISE_IN	I	VddIO	Noise present input	Connect to GND
D3	GND	P	–	Ground	–
D4	GND	P	–	Ground	–
D5	NC	–	–	No connection	–
D6	NC	–	–	No connection	–
D7	NC	–	–	No connection	–
D8	NC	–	–	No connection	–
D9	Y51	S	AVdd	Y line connection	Leave open
D10	Y47	S	AVdd	Y line connection	Leave open
D11	Y43	S	AVdd	Y line connection	Leave open
D12	Y39	S	AVdd	Y line connection	Leave open
D13	Y36	S	AVdd	Y line connection	Leave open
D14	XVDD	P	–	X line drive power	–
D15	X23	S	XVdd	X matrix drive line	Leave open
D16	X24	S	XVdd	X matrix drive line	Leave open
D17	X25	S	XVdd	X matrix drive line	Leave open
D18	X26	S	XVdd	X matrix drive line	Leave open
D19	X27	S	XVdd	X matrix drive line	Leave open
E1	$\overline{\text{CHG}}$	OD	VddIO	Change line interrupt. This line is briefly set (~100 ms) as an input after power-up or reset for diagnostic purposes	–

TABLE 2:   PIN LISTING – 162-BALL UFBGA (CONTINUED)

Ball	Name	Type	Supply	Description	If Unused...
E2	GPIO0	I/O	VddIO	General purpose I/O; see Section 2.5.8 "GPIO Pins"	Connect to GND
E3	AVDD	P	–	Analog power	–
E4	GND	P	–	Ground	–
E5	GND	P	–	Ground	–
E15	GND	P	–	Ground power	–
E16	X19	S	XVdd	X matrix drive line	Leave open
E17	X20	S	XVdd	X matrix drive line	Leave open
E18	X21	S	XVdd	X matrix drive line	Leave open
E19	X22	S	XVdd	X matrix drive line	Leave open
F1	GPIO1	I/O	VddIO	General purpose I/O; see Section 2.5.8 "GPIO Pins"	Connect to GND
F2	GPIO2	I/O	VddIO	General purpose I/O; see Section 2.5.8 "GPIO Pins"	Connect to GND
F3	GND	P	–	Ground	–
F4	GND	P	–	Ground	–
F5	Y29	S	AVdd	Y line connection	Leave open
F6	Y25	S	AVdd	Y line connection	Leave open
F7	Y21	S	AVdd	Y line connection	Leave open
F8	Y18	S	AVdd	Y line connection	Leave open
F9	Y15	S	AVdd	Y line connection	Leave open
F10	Y11	S	AVdd	Y line connection	Leave open
F11	Y7	S	AVdd	Y line connection	Leave open
F12	Y3	S	AVdd	Y line connection	Leave open
F13	Y0	S	AVdd	Y line connection	Leave open
F14	XVDD	P	–	X line drive power	–
F15	X14	S	XVdd	X matrix drive line	Leave open
F16	X15	S	XVdd	X matrix drive line	Leave open
F17	X16	S	XVdd	X matrix drive line	Leave open
F18	X17	S	XVdd	X matrix drive line	Leave open
F19	X18	S	XVdd	X matrix drive line	Leave open
G1	GPIO3	I/O	VddIO	General purpose I/O; see Section 2.5.8 "GPIO Pins"	Connect to GND
G2	GPIO4	I/O	VddIO	General purpose I/O; see Section 2.5.8 "GPIO Pins"	Connect to GND
G3	VDDIO	P	–	Host interface power	–
G4	Y33	S	AVdd	Y line connection	Leave open
G5	Y30	S	AVdd	Y line connection	Leave open
G6	Y26	S	AVdd	Y line connection	Leave open
G7	Y22	S	AVdd	Y line connection	Leave open
G8	Y19	S	AVdd	Y line connection	Leave open
G9	Y16	S	AVdd	Y line connection	Leave open
G10	Y12	S	AVdd	Y line connection	Leave open
G11	Y8	S	AVdd	Y line connection	Leave open
G12	Y4	S	AVdd	Y line connection	Leave open
G13	Y1	S	AVdd	Y line connection	Leave open

TABLE 2:   PIN LISTING – 162-BALL UFBGA (CONTINUED)

Ball	Name	Type	Supply	Description	If Unused...
G14	GND	P	–	Ground	–
G15	X9	S	XVdd	X matrix drive line	Leave open
G16	X10	S	XVdd	X matrix drive line	Leave open
G17	X11	S	XVdd	X matrix drive line	Leave open
G18	X12	S	XVdd	X matrix drive line	Leave open
G19	X13	S	XVdd	X matrix drive line	Leave open
H1	GPIO5	I/O	VddIO	General purpose I/O; see Section 2.5.8 "GPIO Pins"	Connect to GND
H2	DBG_CLK	O	VddIO	Debug clock; see Section 2.5.9 "SPI Debug Interface"	I²C Mode: Connect to test point Connect to GND
	XTAL_XIN	I		USB mode: External oscillator input; see Section 2.5.6 "XTAL_XOUT and XTAL_XIN"	
H3	VDD	P	–	Digital power	–
H4	Y34	S	AVdd	Y line connection	Leave open
H5	Y31	S	AVdd	Y line connection	Leave open
H6	Y27	S	AVdd	Y line connection	Leave open
H7	Y23	S	AVdd	Y line connection	Leave open
H8	Y20	S	AVdd	Y line connection	Leave open
H9	Y17	S	AVdd	Y line connection	Leave open
H10	Y13	S	AVdd	Y line connection	Leave open
H11	Y9	S	AVdd	Y line connection	Leave open
H12	Y5	S	AVdd	Y line connection	Leave open
H13	Y2	S	AVdd	Y line connection	Leave open
H14	XVDD	P	–	High voltage power	–
H15	X4	S	XVdd	X matrix drive line	Leave open
H16	X5	S	XVdd	X matrix drive line	Leave open
H17	X6	S	XVdd	X matrix drive line	Leave open
H18	X7	S	XVdd	X matrix drive line	Leave open
H19	X8	S	XVdd	X matrix drive line	Leave open
J1	DBG_DATA	O	VddIO	Debug data; see Section 2.5.9 "SPI Debug Interface"	I²C Mode: Connect to test point Connect to GND
	XTAL_XOUT	O		USB mode: External oscillator output; see Section 2.5.6 "XTAL_XOUT and XTAL_XIN"	
J2	$\overline{\text{DBG\_SS}}$	I/O	VddIO	Debug SS line; requires external pull-up to VddIO	Pull up to VddIO
	$\overline{\text{TEST}}$	–		Reserved for factory use	
J3	VDDCORE	P	–	Digital power	–
J4	Y35	S	AVdd	Y line connection	Leave open
J5	Y32	S	AVdd	Y line connection	Leave open
J6	Y28	S	AVdd	Y line connection	Leave open
J7	Y24	S	AVdd	Y line connection	Leave open
J8	AVDD	P	–	Analog power	–
J9	GND	P	–	Ground	–

TABLE 2: PIN LISTING – 162-BALL UFBGA (CONTINUED)

Ball	Name	Type	Supply	Description	If Unused...
J10	Y14	S	AVdd	Y line connection	Leave open
J11	Y10	S	AVdd	Y line connection	Leave open
J12	Y6	S	AVdd	Y line connection	Leave open
J13	AVDD	P	–	Analog power	–
J14	GND	P	–	Ground	–
J15	VREGBOOST	O	AVdd	Voltage booster control	Leave open
J16	X0	S	XVdd	X matrix drive line	Leave open
J17	X1	S	XVdd	X matrix drive line	Leave open
J18	X2	S	XVdd	X matrix drive line	Leave open
J19	X3	S	XVdd	X matrix drive line	Leave open

Key:

I	Input only	O	Output only	I/O	Input or output
OD	Open drain output	P	Ground or power	S	Sense pin

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1.0   OVERVIEW OF MXT1664T3

The Microchip maXTouch family of touch controllers brings industry-leading capacitive touch performance to customer applications. The mXT1664T3 features the latest generation of Microchip adaptive sensing technology that utilizes a hybrid mutual and self capacitive sensing system in order to deliver unparalleled touch features and a robust user experience.

- **Patented capacitive sensing method** – The mXT1664T3 uses a unique charge-transfer acquisition engine to implement Microchip's patented capacitive sensing method. Coupled with a state-of-the-art CPU, the entire touchscreen sensing solution can measure, classify and track a number of individual finger touches with a high degree of accuracy in the shortest response time.

- **Capacitive Touch Engine (CTE)** – The mXT1664T3 features an acquisition engine, which uses an optimal measurement approach to ensure almost complete immunity from parasitic capacitance on the receiver input lines. The engine includes sufficient dynamic range to cope with anticipated touchscreen self and mutual capacitances, which allows great flexibility for use with the Microchip proprietary sensor pattern designs. One- and two-layer ITO sensors are possible using glass or PET substrates.

- **Touch detection** – The mXT1664T3 allows for both mutual and self capacitance measurements, with the self capacitance measurements being used to augment the mutual capacitance measurements to produce reliable touch information.

  When self capacitance measurements are enabled, touch classification is achieved using both mutual and self capacitance touch data. This has the advantage that both types of measurement systems can work together to detect touches under a wide variety of circumstances.

  The system may be configured for different types of default measurements in both idle and active modes. For example, the device may be configured for Mutual Capacitance Touch as the default in idle mode and Self Capacitance Touch as the default in active mode. Note that other types of scans (such as other types of self capacitance scans) may also be made depending on configuration.

  Mutual capacitance touch data is used wherever possible to classify touches as this has greater granularity than self capacitance measurements and provides positional information on touches. For this reason, multiple touches can only be determined by mutual capacitance touch data. In Self Capacitance Touch Default mode, if the self capacitance touch processing detects multiple touches, touchscreen processing is skipped until mutual capacitance touch data is available.

  Self capacitance measurements allow for the detection of touches in extreme cases, such as thick glove touches, when mutual capacitance touch detection alone may miss touches.

- **Display Noise Cancellation** – A combination of analog circuitry, hardware noise processing, and firmware that combats display noise without requiring additional listening channels or synchronization to display timing. This enables the use of shieldless touch sensor stacks, including touch-on-lens.

- **Noise filtering** – Hardware noise processing in the capacitive touch engine provides enhanced autonomous filtering and allows a broad range of noise profiles to be handled. The result is good performance in the presence of charger and LCD noise.

- **Processing power** – The main CPU has two powerful microsequencer coprocessors under its control consuming low power. This system allows the signal acquisition, preprocessing, postprocessing and housekeeping to be partitioned in an efficient and flexible way.

- **Interpreting user intention** – The Microchip hybrid mutual and self capacitance method provides unambiguous multitouch performance. Algorithms in the mXT1664T3 provide optimized touchscreen position filtering for the smooth tracking of touches, responding to a user's intended touches while preventing false touches triggered by ambient noise, conductive material on the sensor surface, such as moisture, or unintentional touches from the user's resting palm or fingers.

2.0   SCHEMATICS

2.1   136-ball UFBGA – I^{2}C Mode

See Section 2.5 "Schematic Notes"

MXT1664T3 2.0
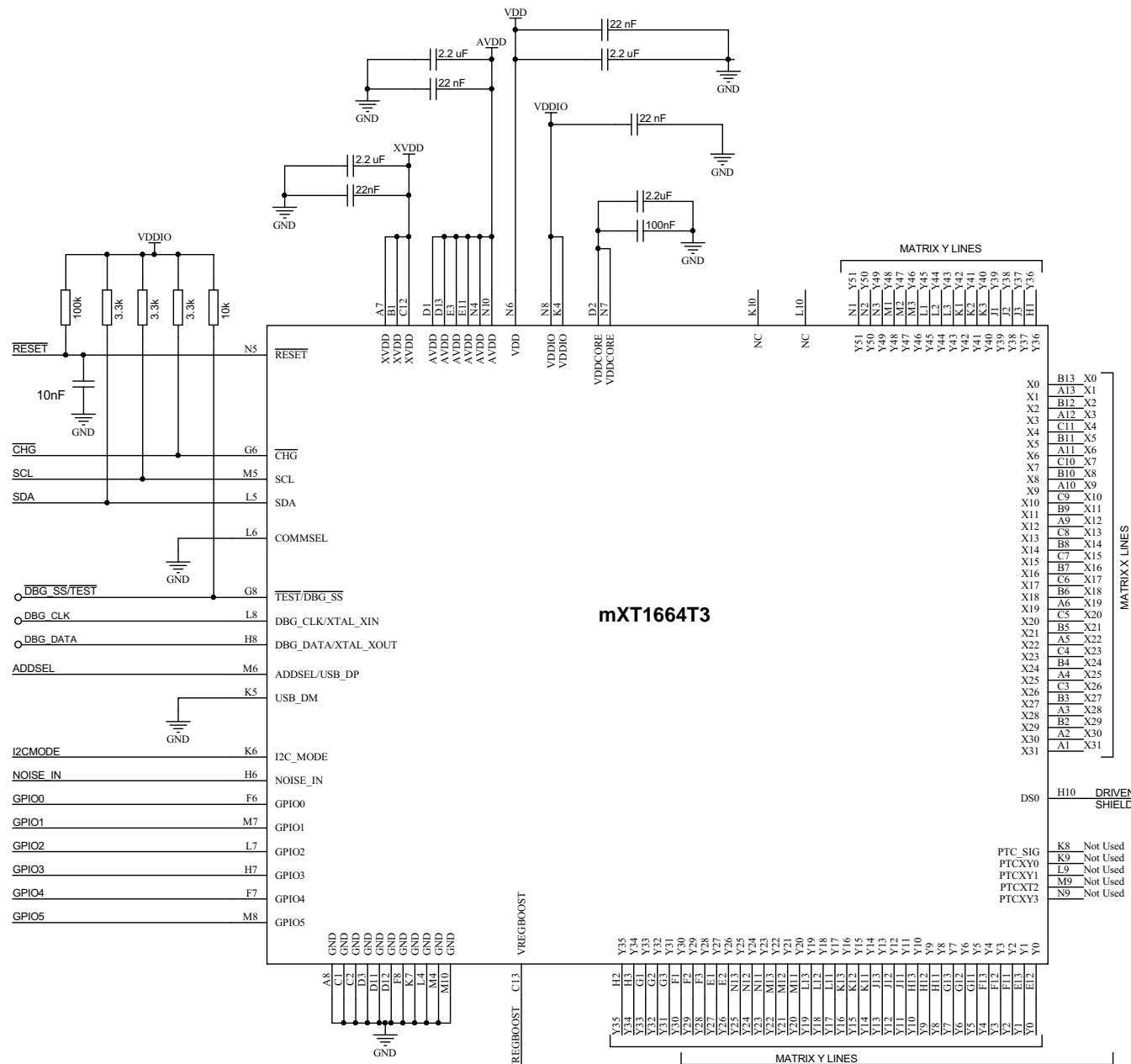
2.2   136-ball UFBGA – USB Mode
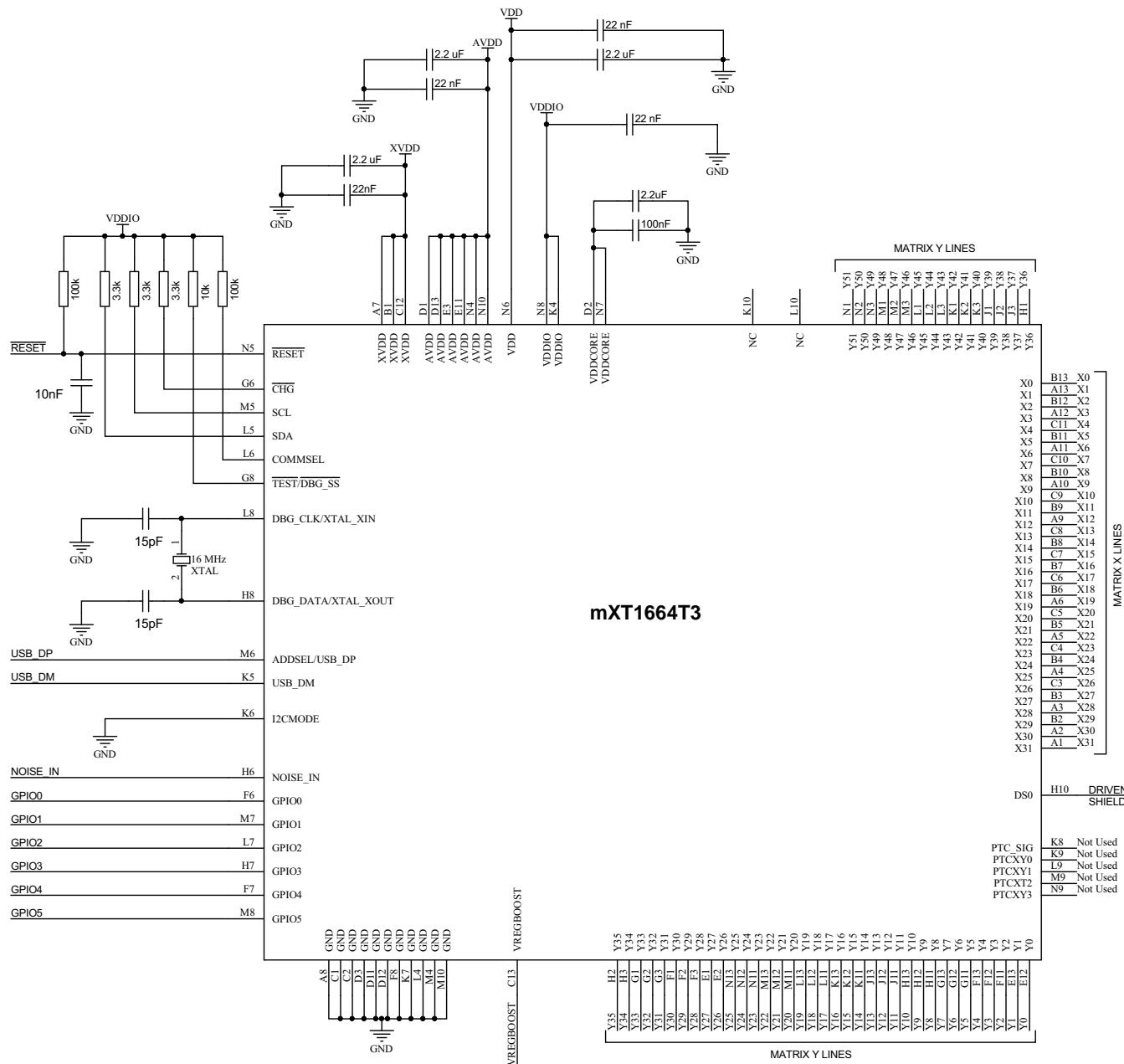
See Section 2.5 "Schematic Notes"

2.3 162-ball UFBGA – I²C Mode

mXT1664T3

MATRIX Y LINES

MATRIX X LINES

MATRIX Y LINES

DRIVEN SHIELD

See Section 2.5 "Schematic Notes"

MXT1664T3 2.0
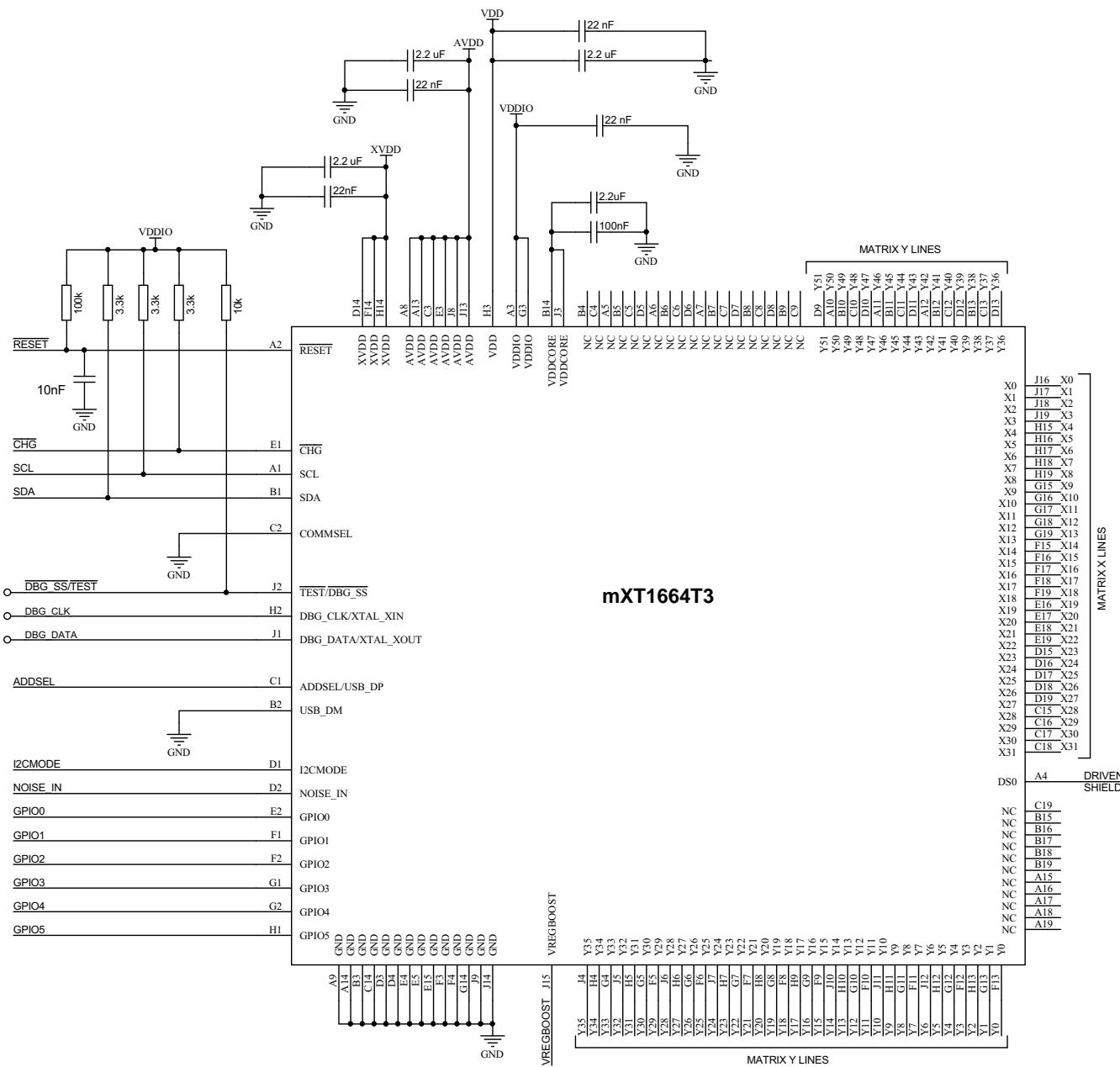
2.4   162-ball UFBGA – USB Mode
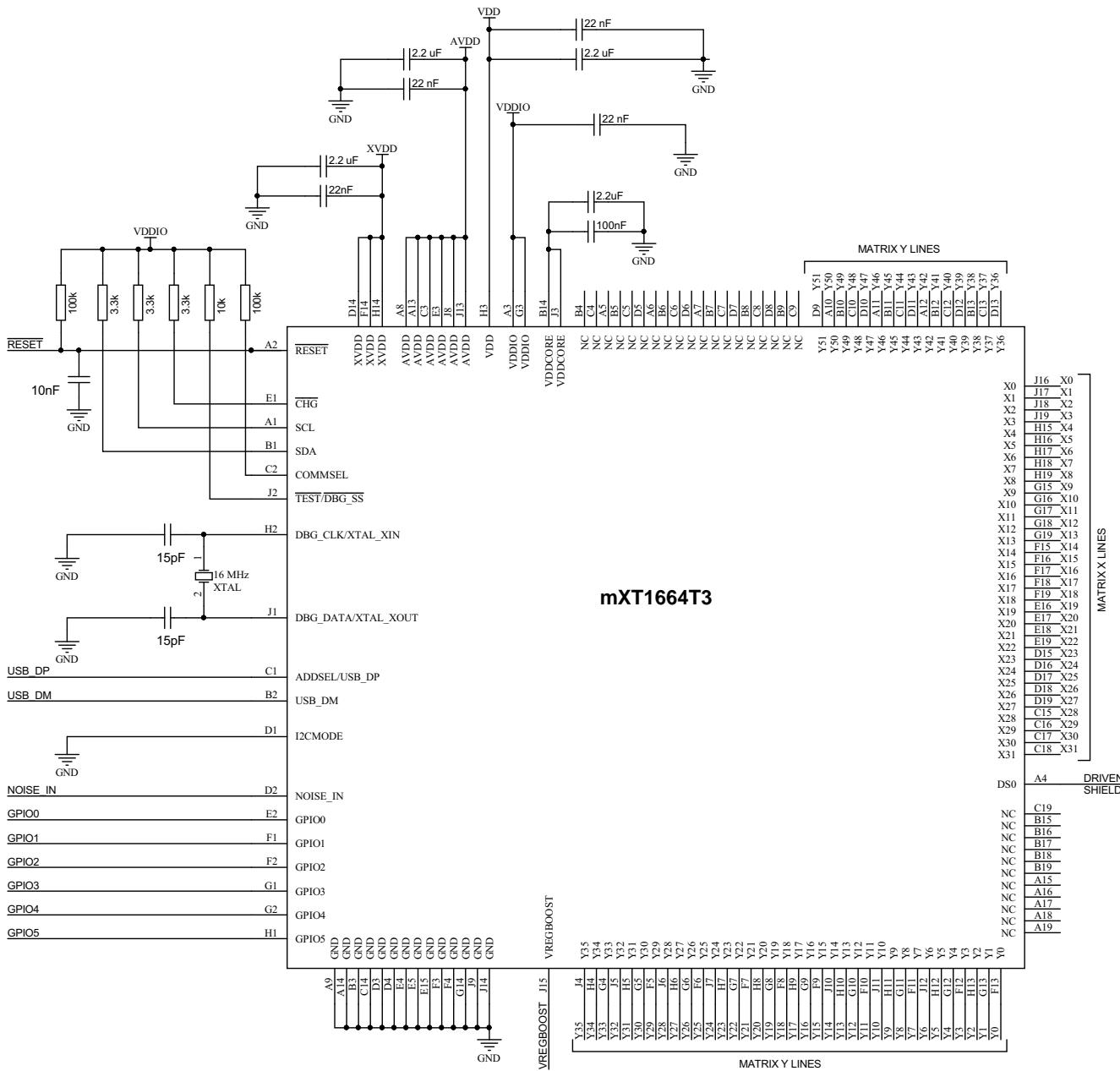
See Section 2.5 "Schematic Notes"

2.5 Schematic Notes

2.5.1 POWER SUPPLY

The sense and I/O pins are supplied by the power rails on the device as listed in Table 2-1. This information is also indicated in "Pin configuration".

TABLE 2-1: POWER SUPPLY FOR SENSE AND I/O PINS

Power Supply	Pins
XVdd	X sense pins
AVdd	Y sense pins, DS0, VREGBOOST
VddIO	RESET, COMMSEL, CHG, I2CMODE SCL, SDA, ADDSEL/USBDP, USBDM, NOISE_IN TEST/DBG_SS, DBG_DATA/XTAL_XOUT, DBG_CLK/XTAL_XIN GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5

2.5.2 DECOUPLING CAPACITORS

All decoupling capacitors must be X7R or X5R and placed less than 5 mm away from the pins for which they act as bypass capacitors. Pins of the same type can share a capacitor provided no pin is more than 10 mm from the capacitor.

The schematics on the previous pages show the capacitors required. The parallel combination of capacitors is recommended to give high and low frequency filtering, which is beneficial if the voltage regulators are likely to be some distance from the device (for example, If an active tail design is used). Note that this requires that the voltage regulator supplies for AVdd, Vdd and VddIO are clean and noise free. It also assumes that the track length between the capacitors and on-board power supplies is less than 50 mm.

The number of base capacitors can be reduced if the pinout configuration means that sharing a bypass capacitor is possible (subject to the distance between the pins satisfying the conditions above and there being no routing difficulties).

2.5.3 PULL-UP RESISTORS

The pull-up resistors shown in the schematics are suggested typical values and may be modified to meet the requirements of an individual customer design.

This applies, in particular, to the pull-up resistors on the I^{2}C SDA and SCL lines (shown on the schematic), as the values of these resistors depends on the speed of the I^{2}C interface. See Section 14.10 "I2C Specification" for details.

Note that if a VddIO supply at the low end of the allowable range is used, the I^{2}C pull-up resistor values may need to be reduced.

2.5.4 VOLTAGE BOOSTER

The XVdd power can be supplied using the Voltage Booster shown in Figure 2-1 on page 22 or an external regulated supply. See Section 14.2 "Recommended Operating Conditions" for the supply voltages possible. Two frequency modes are supported so that it is possible to avoid interference with other functions, such as Long-Term Evolution (LTE) interference. Depending on the chosen frequency mode, a different inductor has to be used. The high frequency mode requires a 10 µH inductor and a 47 µH inductor should be used in the low frequency mode.

If an external supply is used, the components in Figure 2-1 on page 22 can be omitted and VREGBOOST should be left open circuit or connected to a test point. Connection to a test point is preferred and is recommended by Microchip.

MXT1664T3 2.0

FIGURE 2-1:   **XVDD SUPPLY CIRCUIT**
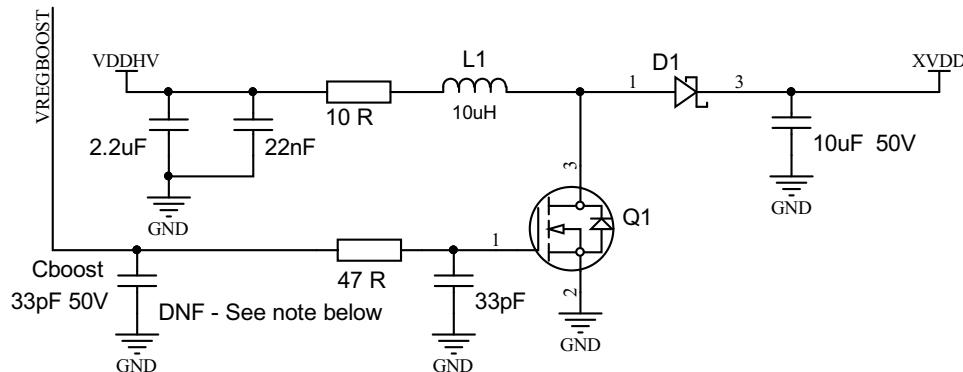
Note 1: Do not fit capacitor Cboost but make provision for it next to the VREGBOOST pin. This capacitor may be required to minimize RF noise issues.

2: See Section 2.5.4.1 "Suggested Component Suppliers" for suggested suppliers for L1 and Q1.

3: To run the Voltage Booster in low frequency mode, a 47 µH inductor (in position L1) will need to be fitted to the boost circuit.

2.5.4.1   Suggested Component Suppliers

D1 is a Schottky Diode. Possible suppliers are shown in Table 2-2.

TABLE 2-2:   **SUITABLE SCHOTTKY DIODE (D1)**

Manufacturer	Device
Various	BAT54M3T5G
Various	1N4148WX

L1 is a 10 µH inductor. Possible suppliers are shown in Table 2-3.

TABLE 2-3:   **SUITABLE 10 µH INDUCTORS (L1)**

Manufacturer	Device	Size
Panasonic	ELJFB100JF	1812
TDK	MLZ1608M100WT	1812
TDK	MLZ2012M100WT000	0805

When the Voltage Booster is run in low frequency mode, L1 is a 47 µH inductor. Possible suppliers are shown in Table 2-4.

TABLE 2-4:   **SUITABLE 47 µH INDUCTORS (L1)**

Manufacturer	Device	Size
LTE	NR3015T470M	1812
Chip1stop.com	NR3015T470M	3 x 3 mm

Q1 is an N-channel 20 V, 700 mA, MOSFET. Possible suppliers are shown in Table 2-5 on page 22.

TABLE 2-5:   **SUITABLE MOSFETS (Q1)**

Manufacturer	Device
ON Semiconductor	NTA4153NT1G
ON Semiconductor	2N7002ET1G
Toshiba	SSM3K56FS

2.5.5 VDDCORE

VddCore is internally generated from the Vdd power supply. To guarantee stability of the internal voltage regulator, one or more external decoupling capacitors are required.

2.5.6 XTAL_XOUT AND XTAL_XIN

In USB mode, the XTAL_XOUT and XTAL_XIN pins are connected to the crystal oscillator. In I^{2}C mode, the XTAL_XOUT and XTAL_XIN pins are used by the SPI Debug Interface and should be brought out to test points.

2.5.7 MULTIPLE FUNCTION PINS

Some pins may have multiple functions. In this case, only one function can be chosen and the circuit should be designed accordingly.

2.5.8 GPIO PINS

The mXT1664T3 has 6 GPIO pins. The pins can be set to be either an input or an output, as required, using the GPIO Configuration T19 object.

If a GPIO pin is unused, it can be left unconnected externally as long as it is given a defined state by the GPIO Configuration T19 object. By default the GPIO pins are set to be inputs so if a pin is not used, and is left configured as an input, it should be connected to GND through a resistor. Alternatively, it can be set as an output low using the GPIO Configuration T19 object and left open. This second option avoids any problems should the pin accidentally be configured as output high at a later date.

If the GPIO Configuration T19 object is not enabled for use, the GPIO pins cannot be used.

2.5.9 SPI DEBUG INTERFACE

In I^{2}C mode, the DBG_CLK, DBG_DATA and $\overline{\text{DBG\_SS}}$ lines form the SPI Debug Interface. These pins should be routed to test points on all designs, such that they can be connected to external hardware during system development and for debug purposes. See also Section 13.1 "SPI Debug Interface".

The DBG_CLK, DBG_DATA and $\overline{\text{DBG\_SS}}$ lines should not be connected to power or GND.

3.0   TOUCHSCREEN BASICS

3.1   Sensor Construction

A touchscreen is usually constructed from a number of transparent electrodes. These are typically on a glass or plastic substrate. They can also be made using non-transparent electrodes, such as copper or carbon. Electrodes are constructed from Indium Tin Oxide (ITO) or metal mesh. Thicker electrodes yield lower levels of resistance (perhaps tens to hundreds of Ω/square) at the expense of reduced optical clarity. Lower levels of resistance are generally more compatible with capacitive sensing. Thinner electrodes lead to higher levels of resistance (perhaps hundreds to thousands of Ω/square) with some of the best optical characteristics.

Interconnecting tracks can cause problems. The excessive RC time constants formed between the resistance of the track and the capacitance of the electrode to ground can inhibit the capacitive sensing function. In such cases, the tracks should be replaced by screen printed conductive inks (non-transparent) outside the touchscreen viewing area.

3.2   Electrode Configuration

The specific electrode designs used in Microchip touchscreens are the subject of various patents and patent applications. Further information is available on request.

The device supports various configurations of electrodes as summarized in Section 4.0 "Sensor Layout".

3.3   Scanning Sequence

All nodes are scanned in sequence by the device. There is a full parallelism in the scanning sequence to improve overall response time. The nodes are scanned by measuring capacitive changes at the intersections formed between the first X line and all the Y lines. Then the intersections between the next X line and all the Y lines are scanned, and so on, until all X and Y combinations have been measured.

The device can be configured in various ways. It is possible to disable some nodes so that they are not scanned at all. This can be used to improve overall scanning time.

3.4   Touchscreen Sensitivity

3.4.1   ADJUSTMENT

Sensitivity of touchscreens can vary across the extents of the electrode pattern due to natural differences in the parasitic capacitance of the interconnections, control chip, and so on. An important factor in the uniformity of sensitivity is the electrode design itself. It is a natural consequence of a touchscreen pattern that the edges form a discontinuity and hence tend to have a different sensitivity. The electrodes at the far edges do not have a neighboring electrode on one side and this affects the electric field distribution in that region.

A sensitivity adjustment is available for the whole touchscreen. This adjustment is a basic algorithmic threshold that defines when a node is considered to have enough signal change to qualify as being in detect.

3.4.2   MECHANICAL STACKUP

The mechanical stackup refers to the arrangement of material layers that exist above and below a touchscreen. The arrangement of the touchscreen in relation to other parts of the mechanical stackup has an effect on the overall sensitivity of the screen. QMatrix technology has an excellent ability to operate in the presence of ground planes close to the sensor. QMatrix sensitivity is attributed more to the interaction of the electric fields between the transmitting (X) and receiving (Y) electrodes than to the surface area of these electrodes. For this reason, stray capacitance on the X or Y electrodes does not strongly reduce sensitivity.

Front panel dielectric material has a direct bearing on sensitivity. Plastic front panels are usually suitable up to about 2.2 mm, and glass up to about 4.5 mm (dependent upon the screen size and layout). The thicker the front panel, the lower the signal-to-noise ratio of the measured capacitive changes and hence the lower the resolution of the touchscreen. In general, glass front panels are near optimal because they conduct electric fields almost twice as easily as plastic panels.

NOTE	Care should be taken using ultra-thin glass panels as retransmission effects can occur, which can significantly degrade performance.

4.0   SENSOR LAYOUT

The specific electrode designs used in Microchip touchscreens are the subject of various patents and patent applications. Further information is available on request.

The device supports various configurations of electrodes as summarized below:

- Touchscreen: 32 X × 52 Y maximum (subject to other configurations)

When designing the physical layout of the touch panel, the following rules must be obeyed:

- The Touchscreen object should be a regular rectangular shape in terms of the lines it uses.
- It is recommended that the Touchscreen should start at X0, Y0; if self-capacitance measurements are enabled, the Touchscreen **must** start at X0, Y0. If a design requires the touchscreen to be located in a region that does not start at X0, Y0, seek advice from Microchip first.

4.1   Screen Size

Table 4-1 lists some typical screen size and electrode pitch combinations to achieve various aspect ratios.

TABLE 4-1:   TYPICAL SCREEN SIZES

Aspect Ratio	Matrix Size	Node Count	Screen Diagonal (Inches)			
			3.8 mm Pitch [1]	5 mm Pitch	6 mm Pitch	6.5 mm Pitch
16:10	X = 32, Y = 52	1664	9.13	12.02	14.42	15.62
16:9	X = 29, Y = 52	1508	8.91	11.72	14.06	15.24
4:3	X = 32, Y = 43	1376	8.02	10.55	12.66	13.72
2:1	X = 26, Y = 52	1352	8.7	11.44	13.73	14.88

Note   1:   Recommended sensor pitch for 1.5 mm passive stylus tip diameter
2:   The figures given in the table are for a Touchscreen and show the largest node count possible to achieve the desired aspect ratio.

5.0   POWER-UP / RESET REQUIREMENTS

5.1   Power-on Reset

There is an internal Power-on Reset (POR) in the device.

If an external reset is to be used the device must be held in $\overline{\text{RESET}}$ (active low) while the digital (Vdd), analog (AVdd) and digital I/O (VddIO) power supplies are powering up. The supplies must have reached their nominal values before the $\overline{\text{RESET}}$ signal is deasserted (that is, goes high). This is shown in Figure 5-1. See Section 14.2 "Recommended Operating Conditions" for nominal values for the power supplies to the device.

FIGURE 5-1:   POWER SEQUENCING ON THE MXT1664T3
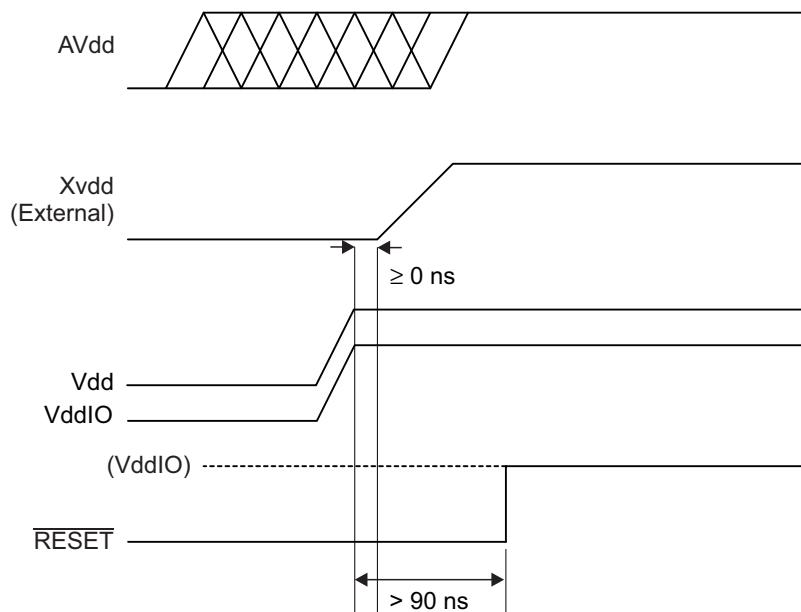
Note: 1) When using external $\overline{\text{RESET}}$ at power-up, VddIO must not be enabled after Vdd.
2) If Xvdd is powered from an external supply (not connected to Vdd), XVdd should be powered up after Vdd and must obey the rate-of-rise specification. If XVdd is connected directly to Vdd (3.3V), the two supplies can be brought up together.

CAUTION!   XVdd must not be grounded when Vdd is active as damage to the device may result.

When using a boosted external XVdd power supply, Vdd must be applied to the device before the external XVdd supply to ensure that the different power domains in the device are initialized correctly. Typically this can be done by connecting the enable pin of the Switched-Mode Power Supply (SMPS) supplying XVdd to a 10 kΩ pull-up resistor connected to the Vdd, but the XVdd can be controlled separately by the host, if required.

If XVdd is not boosted, XVdd can be connected directly to Vdd to supply 3.3 V, in which case the two supplies can be brought up together.

It is recommended that customer designs include the capability for the host to control all the maXTouch power supplies and pull the $\overline{\text{RESET}}$ line low.

After power-up, the device typically takes 79 ms before it is ready to start communications.

If the $\overline{\text{RESET}}$ line is released before the AVdd or external XVDD supply has reached its nominal voltage (see Figure 5-2 on page 27), then some additional operations need to be carried out by the host. There are two options open to the host controller:

• Start the part in deep sleep mode and then send the command sequence to set the cycle time to wake the part and allow it to run normally. Note that in this case a calibration command is also needed.
• Send a RESET command.

FIGURE 5-2: **POWER SEQUENCING ON THE MXT1664T3 – LATE RISE ON AVDD OR XVDD**
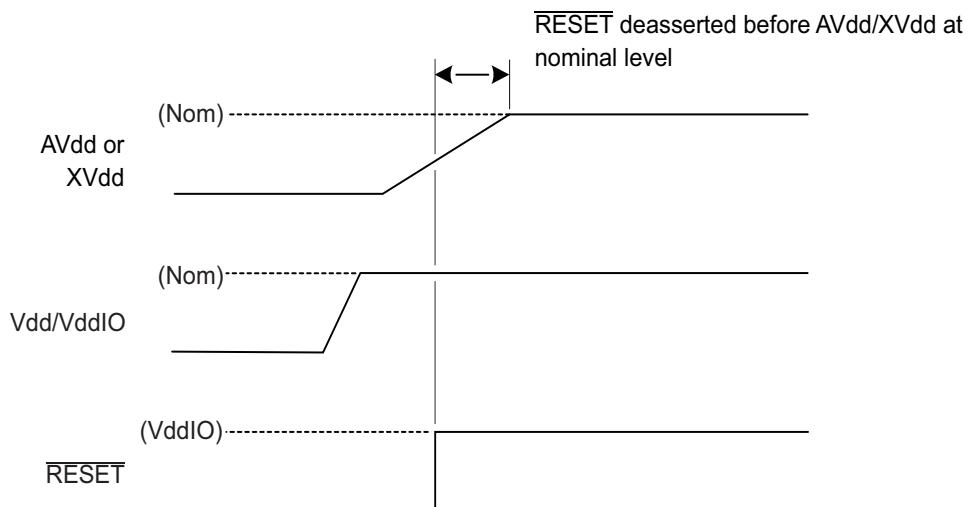
The $\overline{\text{RESET}}$ pin can be used to reset the device whenever necessary. The $\overline{\text{RESET}}$ pin must be asserted low for at least 90 ns to cause a reset. After releasing the $\overline{\text{RESET}}$ pin the device typically takes 81 ms before it is ready to start communications. It is recommended to connect the $\overline{\text{RESET}}$ pin to a host controller to allow it to initiate a full hardware reset without requiring a power-down.

WARNING	The device should be reset only by using the $\overline{\text{RESET}}$ line. If an attempt is made to reset by removing the power from the device without also sending the signal lines low, power will be drawn from the interface lines and the device will not reset correctly.

Make sure that any lines connected to the device are below or equal to Vdd during power-up. For example, if $\overline{\text{RESET}}$ is supplied from a different power domain to the VDDIO pin, make sure that it is held low when Vdd is off. If this is not done, the $\overline{\text{RESET}}$ signal could parasitically couple power via the $\overline{\text{RESET}}$ pin into the Vdd supply.

NOTE	The voltage level on the $\overline{\text{RESET}}$ pin of the device must never exceed VddIO (digital supply voltage).

A software RESET command (using the Command Processor T6 object) can be used to reset the chip. A software reset typically takes 104 ms. After the chip has finished it asserts the $\overline{\text{CHG}}$ line to signal to the host that a message is available. The reset flag is set in the Command Processor T6 object message data to indicate to the host that it has just completed a reset cycle. This bit can be used by the host to detect any unexpected brownout events. This allows the host to take any necessary corrective actions, such as reconfiguration.

NOTE	The $\overline{\text{CHG}}$ line is briefly set (~100 ms) as an input during power-up or reset. It is therefore particularly important that the line should be allowed to float high via the $\overline{\text{CHG}}$ line pull-up resistor during this period. It should never be driven by the host (see Section 14.7.3 "Reset Timings").

At power-on, the device performs a self-test routine (using the Self Test T25 object) to check for shorts that might cause damage to the device.

5.2 Power-up and Reset Sequence – VddIO Enabled after Vdd

The power-up sequence that can be used in applications where VddIO must be powered up after Vdd, is shown in Figure 5-3 on page 28.

In this case the communication interface to the maXTouch device is not driven by the host system. The $\overline{\text{RESET}}$ and $\overline{\text{CHG}}$ pins are connected to VddIO using suitable pull-up resistors. Vdd is powered up, followed by VddIO, no more than 10 ms after Vdd. Due to the pull-up resistors, $\overline{\text{RESET}}$ and $\overline{\text{CHG}}$ will rise with VddIO. The internal POR system ensures reliable boot up of the device and the $\overline{\text{CHG}}$ line will go low approximately 79 ms after Vdd to notify the host that the device is ready to start communication.

FIGURE 5-3: **POWER-UP SEQUENCE**
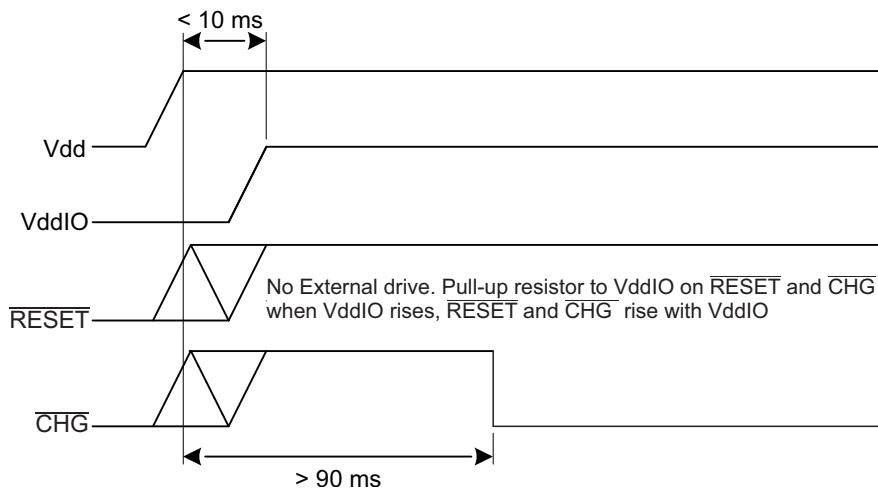
5.3 Power-up and Initialization

The device uses a number of different power domains for optimum performance and contains circuitry to interface internal signals crossing between the different domains. There is also circuitry to ensure that the device interface logic will be initialized correctly as the device powers on. Note, however, that this does not negate specific instructions elsewhere in this section about the order that the different supplies should power up. Also, as previously mentioned, $\overline{\text{RESET}}$ should be held low until after all power rails are stable. In addition, the device will not initialize until all the voltage rails have powered up and are present.

If one domain loses power, however (for example, due to a fault or an ESD event), the device should be power-cycled to ensure that the interface logic is once again initialized. It is therefore recommended that customer designs include the capability for the host to control all the maXTouch power supplies and pull the $\overline{\text{RESET}}$ line low.

5.4 Summary

The power-up and reset requirements for the maXTouch devices are summarized in Table 5-1.

TABLE 5-1: **POWER-UP AND RESET REQUIREMENTS**

Condition	External $\overline{\text{RESET}}$	VddIO Delay (After Vdd)	AVdd Power-Up	Comments
1	Low at Power-up	0 ms	Before $\overline{\text{RESET}}$ is released	If AVdd bring-up is delayed, then additional actions will be required by the host (see Section 5.1 "Power-on Reset"
2	Not driven	<10 ms	Before VddIO	

6.0   DETAILED OPERATION

6.1   Touch Detection

The mXT1664T3 allows for both mutual and self capacitance measurements, with the self capacitance measurements being used to augment the mutual capacitance measurements to produce reliable touch information.

When self capacitance measurements are enabled, touch classification is achieved using both mutual and self capacitance touch data. This has the advantage that both types of measurement systems can work together to detect touches under a wide variety of circumstances.

Mutual capacitance touch data is used wherever possible to classify touches as this has greater granularity than self capacitance measurements and provides positional information on touches.

Self capacitance measurements, on the other hand, allow for the detection of single touches in extreme cases, such as single thick glove touches, when touches can only be detected by self capacitance data and may be missed by mutual capacitance touch detection.

6.2   Operational Modes

The device operates in two modes: **Active** (touch detected) and **Idle** (no touches detected). Both modes operate as a series of burst cycles. Each cycle consists of a short burst (during which measurements are taken) followed by an inactive sleep period. The difference between these modes is the length of the cycles. Those in idle mode typically have longer sleep periods. The cycle length is configured using the IDLEACQINT and ACTVACQINT settings in the Power Configuration T7. In addition, an *Active to Idle Timeout* setting is provided.

6.3   Detection Integrator

The device features a touch detection integration mechanism. This acts to confirm a detection in a robust fashion. A counter is incremented each time a touch has exceeded its threshold and has remained above the threshold for the current acquisition. When this counter reaches a preset limit the sensor is finally declared to be touched. If, on any acquisition, the signal is not seen to exceed the threshold level, the counter is cleared and the process has to start from the beginning.

The detection integrator is configured using the appropriate touch objects (Multiple Touch Touchscreen T100).

6.4   Sensor Acquisition

The charge time is set using the Acquisition Configuration T8 object.

A number of factors influence the acquisition time for a single drive line and the total acquisition time for the sensor as a whole must not exceed 250 ms. If this condition is not met, a SIGERR will be reported.

Care should be taken to configure all the objects that can affect the measurement timing, for example, Acquisition Configuration T8, CTE Configuration T46 and Self Capacitance Configuration T111, so that these limits are not exceeded.

6.5   Calibration

Calibration is the process by which a sensor chip assesses the background capacitance on each node. Nodes are only calibrated on reset and when:

• The node is enabled (that is, activated)

or

• The node is already enabled and one of the following applies:
   - The node is held in detect for longer than the Touch Automatic Calibration setting (TCHAUTOCAL in the Acquisition Configuration T8 object)
   - The signal delta on a node is at least the touch threshold (TCHTHR – TCHHYST) in the anti-touch direction, while it meets the criteria in the Touch Recovery Processes that results in a recalibration
   - The host issues a recalibrate command
   - Certain configuration settings are changed

A status message is generated on the start and completion of a calibration.

Note that the device performs a global calibration; that is, all the nodes are calibrated together.

6.6 Digital Filtering and Noise Suppression

The mXT1664T3 supports on-chip filtering of the acquisition data received from the sensor. Specifically, the Noise Suppression T72 object provides an algorithm to suppress the effects of noise (for example, from a noisy charger plugged into the user's product). This algorithm can automatically adjust some of the acquisition parameters on-the-fly to filter the analog-to-digital conversions (ADCs) received from the sensor.

Additional noise suppression is provided by the Self Capacitance Noise Suppression T108 object. Similar in both design and configuration to the Noise Suppression T72 object, the Self Capacitance Noise Suppression T108 object is the noise suppression interface for self capacitance touch measurements.

Noise suppression is triggered when a noise source is detected.

- A hardware trigger can be implemented using the NOISE_IN pin.
- The host driver code can indicate when a noise source is present.
- The noise suppression is also triggered based on the noise levels detected using internal line measurements.The Noise Suppression T72 and Self Capacitance Noise Suppression T108 object selects the appropriate controls to suppress the noise present in the system.

6.7 Shieldless Support and Display Noise Suppression

The mXT1664T3 can support shieldless sensor design even with a noisy LCD.

The Optimal Integration feature is not filtering as such, but enables the user to use a shorter integration window. The integration window optimizes the amount of charge collected against the amount of noise collected, to ensure an optimal SNR. This feature also benefits the system in the presence of an external noise source. This feature is configured using the Shieldless T56 object.

Display noise suppression allows the device to overcome display noise simultaneously with external noise. This feature is based on filtering provided by the Lens Bending T65 object (see Section 6.10 "Lens Bending").

6.8 Retransmission Compensation

The device can limit the undesirable effects on the mutual capacitance touch signals caused by poor device coupling to ground, such as poor sensitivity and touch break-up. This is achieved using the Retransmission Compensation T80 object. This object can be configured to allow the touchscreen to compensate for signal degradation due to these undesirable effects. If self capacitance measurements are also scheduled, the Retransmission Compensation T80 object will use the resultant data to enhance the compensation process.

The Retransmission Compensation T80 object is also capable of compensating for water presence on the sensor if self capacitance measurements are scheduled. In this case, both mutual capacitance and self capacitance measurements are used to detect moisture and then, once moisture is detected, self capacitance measurements are used to detect single touches in the presence of moisture.

6.9 Grip Suppression

The device has grip suppression functionality to suppress false detections from a user's grip.

Mutual capacitance grip suppression works by specifying a boundary around a touchscreen, within which touches can be suppressed whilst still allowing touches in the center of the touchscreen. This ensures that an accidental hand touch on the edge is suppressed while still allowing a "real" (finger) touch towards the center of the screen. Mutual capacitance grip suppression is configured using the Grip Suppression T40 object.

Self Capacitance grip suppression works by looking for characteristic shapes in the self capacitance measurement along the touchscreen boundary, and thereby distinguishing between a grip and a touch further into the sensor. Self capacitance grip suppression is configured using the Self Capacitance Grip Suppression T112 object.

6.10 Lens Bending

The device supports algorithms to eliminate disturbances from the measured signal.

When the sensor suffers from the screen deformation (lens bending) the signal values acquired by normal procedure are corrupted by the disturbance component (bend). The amount of bend depends on:

- The mechanical and electrical characteristics of the sensor
- The amount and location of the force applied by the user touch to the sensor

The Lens Bending T65 object measures the bend component and compensates for any distortion caused by the bend. As the bend component is primarily influenced by the user touch force, it can be used as a secondary source to identify the presence of a touch. The additional benefit of the Lens Bending T65 object is that it will eliminate LCD noise as well.

6.11 Glove Detection

The device has glove detection algorithms that process the measurement data received from the touchscreen classifying touches as potential gloved touches.

The Glove Detection T78 object is used to detect glove touches. In Normal Mode the Glove Detection T78 object applies vigorous glove classification to small signal touches to minimize the effect of unintentional hovering finger reporting. Once a gloved touch is found, the Glove Detection T78 object enters Glove Confidence Mode. In this mode the device expects the user to be wearing gloves so the classification process is much less stringent.

6.12 Stylus Support

The mXT1664T3 allows for the particular characteristics of passive stylus touches, whilst still allowing conventional finger touches to be detected. The touch sensitivity and threshold controls for stylus touches are configured separately from those for conventional finger touches so that both types of touches can be accommodated.

Stylus support ensures that the small touch area of a stylus registers as a touch, as this would otherwise be considered too small for the touchscreen. Additionally, there are controls to distinguish a stylus touch from an unwanted approaching finger (such as on the hand holding the stylus).

Passive stylus touches are configured by the Passive Stylus T47 object. There is one instance of the Passive Stylus T47 object for each Multiple Touch Touchscreen T100 object present on the device.

6.13 Unintentional Touch Suppression

The Touch Suppression T42 object provides a mechanism to suppress false detections from unintentional touches from a large body area, such as from a face, ear or palm. The Touch Suppression T42 object also provides Maximum Touch Suppression to suppress all touches if more than a specified number of touches has been detected. There is one instance of the Touch Suppression T42 object for each Multiple Touch Touchscreen T100 object present on the device.

7.0   HOST COMMUNICATIONS

Communication between the mXT1664T3 and the host is achieved using one of the following interfaces:

- I^2C (see Section 8.0 "I2C Communications")
- HID-I^2C (see Section 9.0 "HID-I^2C Communications")
- USB (see Section 10.0 "USB Communications")

Any host interface can be used, depending on the needs of the user's project, but only one interface can be used in any one design.

7.1   Host Communication Mode Selection – COMMSEL Pin

The selection of the host I^2C or USB interface is determined by connecting the COMMSEL pin according to Table 7-1.

TABLE 7-1:   HOST INTERFACE SELECTION

COMMSEL	Interface Selected
Connected to GND	I^2C
Pulled up to VddIO [(1)]	USB

Note   1:   Requires a pull-up resistor; see Section 2.0 "Schematics"

7.2 I^2C Mode Selection – I2CMODE Pin

> **NOTE**   In USB mode, the I2CMODE pin is unused and should be connected to GND.

The selection of the I^2C or the HID-I^2C mode is determined by connecting the I2CMODE pin according to Table 7-2.

TABLE 7-2: I^2C MODE SELECTION

I2CMODE	Interface Selected
Connected to GND	HID-I^2C
Pulled up to VddIO [(1)]	I^2C
Floating	Mode is selected according to the I^2C address (as determined by the ADDSEL pin). See Section 7.2.1 "Automatic Selection of I^2C and HID-I^2C Modes" for more information.

Note   1:   Requires a pull-up resistor; see Section 2.0 "Schematics"

7.2.1   AUTOMATIC SELECTION OF I^2C AND HID-I^2C MODES

If the I2CMODE pin is left floating (that is, automatic mode selection), the device will listen on both I^2C addresses and automatically select the protocol to be used depending on the first message received. In this case the ADDSEL pin determines the primary and secondary I^2C addresses, and these in turn determine the communications mode to be used. If the primary I^2C address is detected, I^2C is used for communications; if the I^2C secondary address is detected, HID-I^2C is used.

The selection of both the communications mode and the I^2C addresses is summarized in Table 7-3.

TABLE 7-3: COMMUNICATIONS MODE SELECTION

I2CMODE	ADDSEL	Mode
0 (HID-I^{2}C selected)	0 (Address = 0x4A)	HID-I^{2}C communications at 0x4A
	1 (Address = 0x4B)	HID-I^{2}C communications at 0x4B
1 (I^{2}C selected)	0 (Address = 0x4A)	I^{2}C communications at 0x4A
	1 (Address = 0x4B)	I^{2}C communications at 0x4B
No input or input floating (auto selection)	0 (Primary address = 0x4A, secondary address = 0x4B)	I^{2}C communications at 0x4A (primary address) HID-I^{2}C communications at 0x4B (secondary address)
	1 (Primary address = 0x4B, secondary address = 0x4A)	I^{2}C communications at 0x4B (primary address) HID-I^{2}C communications at 0x4A (secondary address)

7.3 I^{2}C Address Selection – ADDSEL Pin

If the I2CMODE pin is not floating (that is, a particular mode is chosen), the I^{2}C address is selected by connecting the ADDSEL pin according to Table 7-4.

TABLE 7-4: I^{2}C ADDRESS SELECTION

ADDSEL	I^{2}C Address
Connected to GND	0x4A
Pulled up to VddIO [1]	0x4B

Note 1: Requires a pull-up resistor; see Section 2.0 "Schematics"

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8.0 I²C COMMUNICATIONS

Communication with the device can be carried out over the I²C interface.

The I²C interface is used in conjunction with the $\overline{\text{CHG}}$ line. The $\overline{\text{CHG}}$ line going active signifies that a new data packet is available. This provides an interrupt-style interface and allows the device to present data packets when internal changes have occurred. See Section 8.6 "CHG Line" for more information.

See Section 7.0 "Host Communications" for information on selecting I²C mode.

8.1 I²C Addresses

The device supports two I²C device addresses that are selected using the ADDSEL line at start up. The two internal I²C device addresses are 0x4A and 0x4B. The selection of the address (and the communication mode) is described in Section 7.3 "I²C Address Selection – ADDSEL Pin".

The I²C address is shifted left to form the SLA+W or SLA+R address when transmitted over the I²C interface, as shown in Table 8-1.

TABLE 8-1: FORMAT OF AN I²C ADDRESS

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0x4A or 0x4B							Read/write

8.2 Writing To the Device

A WRITE cycle to the device consists of a START condition followed by the I²C address of the device (SLA+W). The next two bytes are the address of the location into which the writing starts. The first byte is the Least Significant Byte (LSByte) of the address, and the second byte is the Most Significant Byte (MSByte). This address is then stored as the address pointer.

Subsequent bytes in a multi-byte transfer form the actual data. These are written to the location of the address pointer, location of the address pointer + 1, location of the address pointer + 2, and so on. The address pointer returns to its starting value when the WRITE cycle STOP condition is detected.

Figure 8-1 shows an example of writing four bytes of data to contiguous addresses starting at 0x1234.

FIGURE 8-1: EXAMPLE OF A FOUR-BYTE WRITE STARTING AT ADDRESS 0x1234

START | SLA+W | 0x34 | 0x12 | 0x96 | 0x9B | 0xA0 | 0xA5 | STOP

Write Address
(LSB MSB)
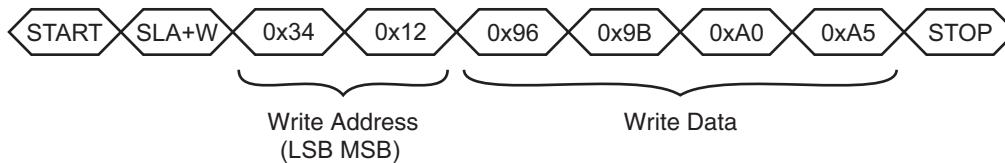
Write Data

8.3 I²C Writes in Checksum Mode

In I²C checksum mode an 8-bit CRC is added to all I²C writes. The CRC is sent at the end of the data write as the last byte before the STOP condition. All the bytes sent are included in the CRC, including the two address bytes. Any command or data sent to the device is processed even if the CRC fails.

To indicate that a checksum is to be sent in the write, the most significant bit of the MSByte of the address is set to 1. For example, the I²C command shown in Figure 8-2 writes a value of 150 (0x96) to address 0x1234 with a checksum. The address is changed to 0x**9**234 to indicate checksum mode.

FIGURE 8-2: EXAMPLE OF A WRITE TO ADDRESS 0x1234 WITH A CHECKSUM

START | SLA+W | 0x34 | 0x92 | 0x96 | Checksum | STOP

Write Address
(LSB, MSB)
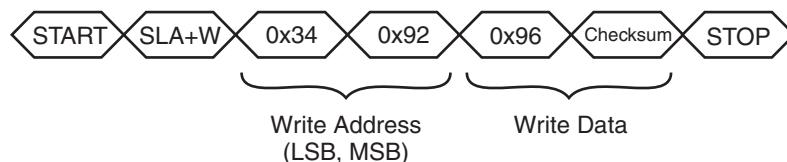
Write Data

8.4 Reading From the Device

Two I^{2}C bus activities must take place to read from the device. The first activity is an I^{2}C write to set the address pointer (LSByte then MSByte). The second activity is the actual I^{2}C read to receive the data. The address pointer returns to its starting value when the read cycle NACK is detected.

It is not necessary to set the address pointer before every read. The address pointer is updated automatically after every read operation. The address pointer will be correct if the reads occur in order. In particular, when reading multiple messages from the Message Processor T5 object, the address pointer is automatically reset to allow continuous reads (see Section 8.5 "Reading Status Messages with DMA").

The WRITE and READ cycles consist of a START condition followed by the I^{2}C address of the device (SLA+W or SLA+R respectively). Note that in this mode, calculating a checksum of the data packets is not supported.

Figure 8-3 shows the I^{2}C commands to read four bytes starting at address 0x1234.

FIGURE 8-3:   **EXAMPLE OF A FOUR-BYTE READ STARTING AT ADDRESS 0x1234**

Set Address Pointer

START — SLA+W — 0x34 — 0x12 — STOP

Read Address
(LSB, MSB)

Read Data

START — SLA+R — 0x96 — 0x9B — 0xA0 — 0xA5 — STOP
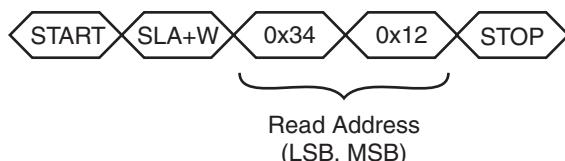
Read Data
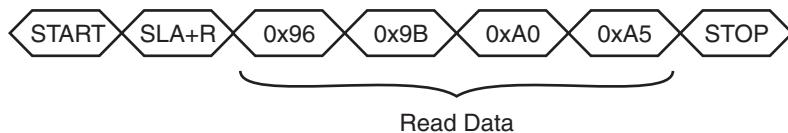
8.5 Reading Status Messages with DMA

The device facilitates the easy reading of multiple messages using a single continuous read operation. This allows the host hardware to use a direct memory access (DMA) controller for the fast reading of messages, as follows:

1. The host uses a write operation to set the address pointer to the start of the Message Count T44 object, if necessary. Note that the STOP condition at the end of the read resets the address pointer to its initial location, so it may already be pointing at the Message Count T44 object following a previous message read. If a checksum is required on each message, the most significant bit of the MSByte of the read address must be set to 1.

2. The host starts the read operation of the message by sending a START condition.

3. The host reads the Message Count T44 object (one byte) to retrieve a count of the pending messages.

4. The host calculates the number of bytes to read by multiplying the message count by the size of the Message Processor T5 object. Note that the host should have already read the size of the Message Processor T5 object in its initialization code.

   Note that the size of the Message Processor T5 object as recorded in the Object Table includes a checksum byte. If a checksum has not been requested, one byte should be deducted from the size of the object.
   That is: number of bytes = count × (size – 1).

5. The host reads the calculated number of message bytes. It is important that the host does *not* send a STOP condition during the message reads, as this will terminate the continuous read operation and reset the address pointer. No START and STOP conditions must be sent between the messages.

6. The host sends a STOP condition at the end of the read operation after the last message has been read. The NACK condition immediately before the STOP condition resets the address pointer to the start of the Message Count T44 object.

Figure 8-4 shows an example of using a continuous read operation to read three messages from the device without a checksum. Figure 8-5 on page 37 shows the same example with a checksum.

FIGURE 8-4: **CONTINUOUS MESSAGE READ EXAMPLE – NO CHECKSUM**

Set Address Pointer

START SLA+W LSB MSB STOP

Start Address of
Message Count Object

Continuous
Read

Read Message Count

START SLA+R Count = 3

Message Count Object

Read Message Data

($size$ – 1) bytes

Report ID Data • • • Data

Message Processor Object – Message # 1

Report ID Data • • • Data

Message Processor Object – Message # 2

Report ID Data • • • Data STOP

Message Processor Object – Message # 3
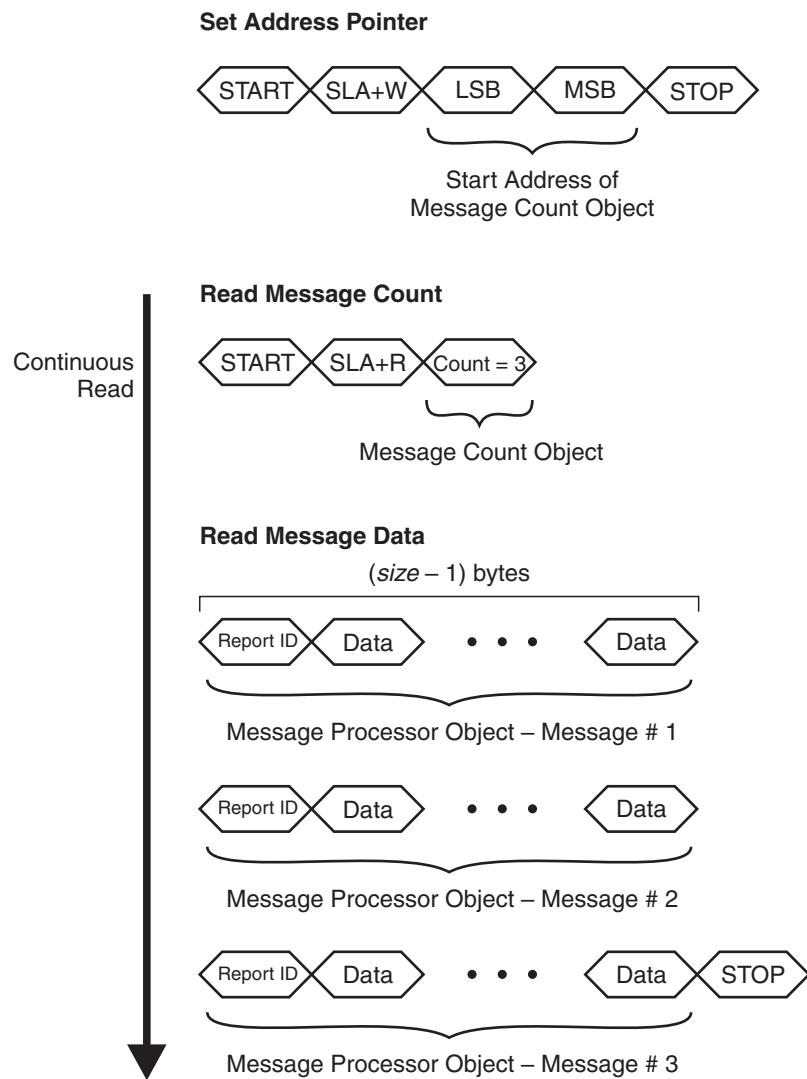
FIGURE 8-5:   **CONTINUOUS MESSAGE READ EXAMPLE – I^{2}C CHECKSUM MODE**
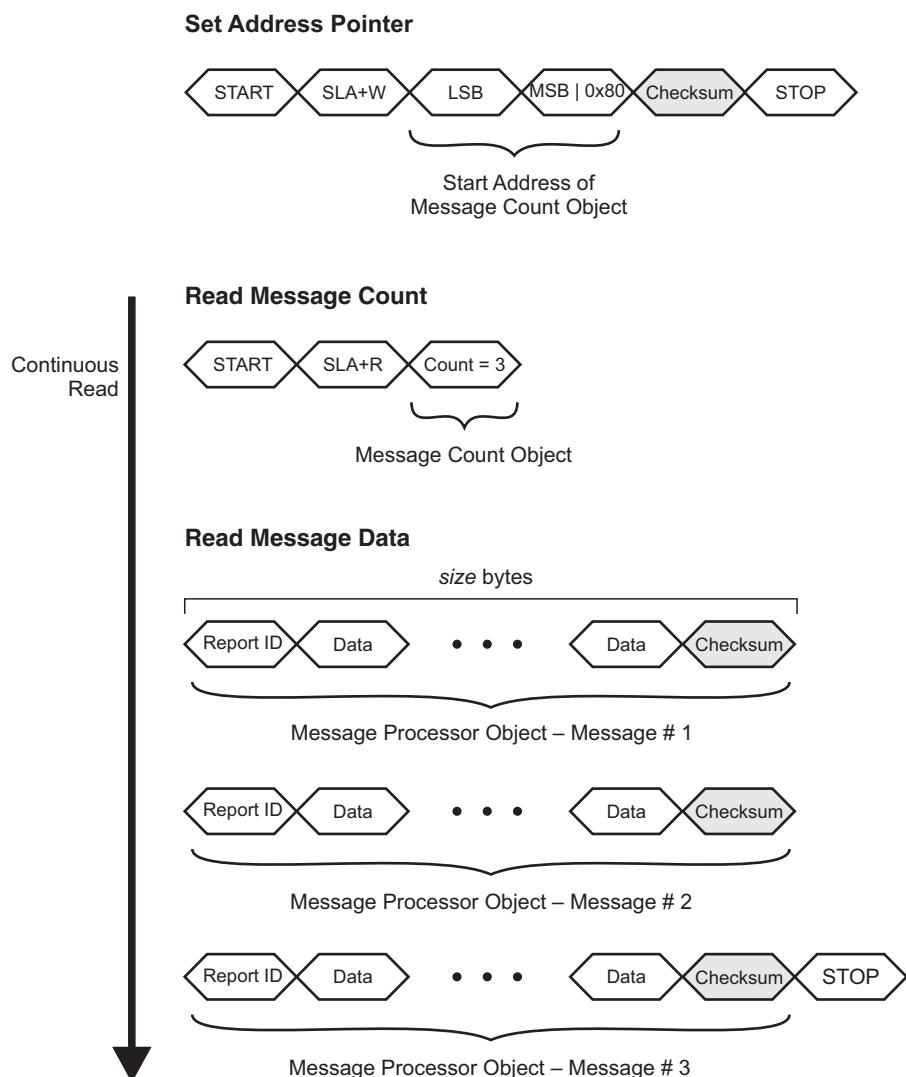
There are no checksums added on any other I^{2}C reads. An 8-bit CRC can be added, however, to all I^{2}C writes, as described in Section 8.3 "I^{2}C Writes in Checksum Mode".

An alternative method of reading messages using the $\overline{\text{CHG}}$ line is given in Section 8.6 "CHG Line".

8.6 $\overline{\text{CHG}}$ Line

The $\overline{\text{CHG}}$ line is an active-low, open-drain output that is used to alert the host that a new message is available in the Message Processor T5 object. This provides the host with an interrupt-style interface with the potential for fast response times. It reduces the need for wasteful I^{2}C communications.

The $\overline{\text{CHG}}$ line should always be configured as an input on the host during normal usage. This is particularly important after power-up or reset (see Section 5.0 "Power-up / Reset Requirements").

A pull-up resistor is required to VddIO (see Section 2.0 "Schematics").

The $\overline{\text{CHG}}$ line operates in two modes when it is used with I^{2}C communications, as defined by the Communications Configuration T18 object.

FIGURE 8-6: CHG LINE MODES FOR I²C-COMPATIBLE TRANSFERS
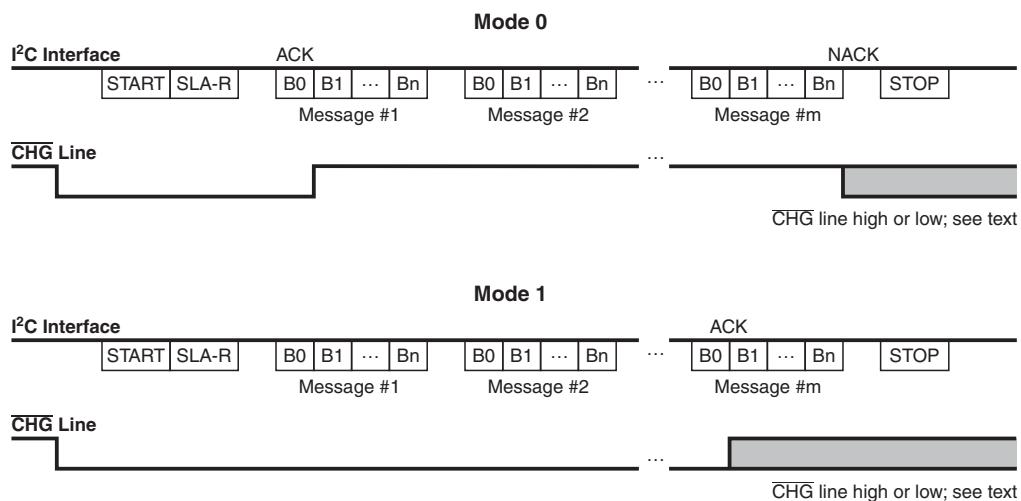
In Mode 0 (edge-triggered operation):

1. The CHG line goes low to indicate that a message is present.
2. The CHG line goes high when the first byte of the first message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the buffer.
3. The STOP condition at the end of an I²C transfer causes the CHG line to stay high if there are no more messages. Otherwise the CHG line goes low to indicate a further message.

Note that Mode 0 also allows the host to continually read messages by simply continuing to read bytes back without issuing a STOP condition. Message reading should end when a report ID of 255 ("invalid message") is received. Alternatively the host ends the transfer by sending a NACK after receiving the last byte of a message, followed by a STOP condition. If there is another message present, the CHG line goes low again, as in step 1. In this mode the state of the CHG line does not need to be checked during the I²C read.

In Mode 1 (level-triggered operation):

1. The CHG line goes low to indicate that a message is present.
2. The CHG line remains low while there are further messages to be sent after the current message.
3. The CHG line goes high again only once the first byte of the last message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the output buffer.

Mode 1 allows the host to continually read the messages until the CHG line goes high, and the state of the CHG line determines whether or not the host should continue receiving messages from the device.

NOTE	The state of the CHG line should be checked only between messages and not between the bytes of a message. The precise point at which the CHG line changes state cannot be predicted and so the state of the CHG line cannot be guaranteed between bytes.

The Communications Configuration T18 object can be used to configure the behavior of the CHG line. In addition to the CHG line operation modes described above, this object allows direct control over the state of the CHG line.

8.7   SDA and SCL

The I²C bus transmits data and clock with SDA and SCL, respectively. These are open-drain. The device can only drive these lines low or leave them open. The termination resistors (Rp) pull the line up to VddIO if no I²C device is pulling it down.

The termination resistors should be chosen so that the rise times on SDA and SCL meet the I²C specifications for the interface speed being used, bearing in mind other loads on the bus. For best latency performance, it is recommended that no other devices share the I²C bus with the maXTouch controller.

8.8   Clock Stretching

The device supports clock stretching in accordance with the I^{2}C specification. It may also instigate a clock stretch if a communications event happens during a period when the device is busy internally. The maximum clock stretch is 2 ms and typically less than 350 µs.

9.0   HID-I^{2}C COMMUNICATIONS

The device is an HID-I^{2}C device presenting two Top-level Collections (TLCs):

- **Generic HID-I^{2}C** – Provides a generic HID-I^{2}C interface that allows the host to communicate with the device using the object-based protocol (OBP).
- **Digitizer HID-I^{2}C** – Supplies touch information to the host. This interface is supported by Microsoft Windows without the need for additional software.

See Section 7.0 "Host Communications" for information on selecting HID-I^{2}C mode.

Other features are identical to standard I^{2}C communication described in Section 8.0 "I2C Communications".

Refer to the Microsoft HID-I^{2}C documentation, *HID Over I^{2}C Protocol Specification – Device Side*, for information on the HID-I^{2}C specification.

9.1   I^{2}C Addresses

See Section 8.1 "I2C Addresses".

9.2   Device Specification

The device is compliant with HID-I^{2}C specification V1.0. It has the specification shown in Table 9-1.

TABLE 9-1:   DEVICE SPECIFICATION

Parameter	Value
Vendor ID	0x03EB (Microchip)
Product ID	0x215D (mXT1664T3)
Version ID	16-bit Version & Build Identifier in the form 0xVVBB, where: VV = Version Major (Upper 4 bits) / Minor (Lower 4 bits) BB = Build number in BCD format
HID Descriptor Address	0x0000

9.3   HID Descriptor

The host should read the HID descriptor on initialization to ascertain the key attribute of the HID device. These include the report description and the report ID to be used for communication with the HID device. The HID descriptor address is 0x0000.

Note that the host driver must not make any assumptions about the report packet formats, data locations or report IDs. These must be read from the HID descriptor as they may change in future versions of the firmware.

For more information on how to read the HID descriptor, refer to the Microsoft HID-I^{2}C documentation.

9.4   HID-I^{2}C Report IDs

Table 9-2 describes the HID-I^{2}C report IDs used in reports sent to the host.

> **NOTE**   The term HID-I^{2}C report ID should not be confused with the term report Id as used in the Object Protocol; the two are entirely different concepts. Refer to the *mXT1664T3 2.0 Protocol Guide* for more information on the use of Object Protocol report IDs.

TABLE 9-2:   HID-I^{2}C REPORT IDS

Report ID	Description	Top-level Collection
0x06	Object Protocol (OBP) command and response (see Section 9.5 "Generic HID-I^{2}C TLC")	Generic HID-I^{2}C
0x01	Touch report (see Section 9.6.1 "Touch Report")	Digitizer HID-I^{2}C
0x02	Maximum Touches (Surface Contacts) report (see Section 9.6.3 "Maximum Touches Report")	Digitizer HID-I^{2}C

TABLE 9-2: HID-I²C REPORT IDS (CONTINUED)

Report ID	Description	Top-level Collection
0x05	Touch Hardware Quality Assurance (THQA) report (see Section 9.6.4 "Touch Hardware Quality Assurance (THQA) Report")	Digitizer HID-I²C

9.5   Generic HID-I²C TLC

The Generic HID-I²C TLC supports an input report for receiving data from the device and an output report for sending data to the device.

Commands are sent by the host using the output reports. Responses from the device are sent using input reports.

Supported commands are:

- Read/Write Memory Map
- Send Auto-return Messages

The HID-I²C report ID used is that for Object Protocol commands and responses; see Table 9-2 on page 40 for the value.

9.5.1   READ/WRITE MEMORY MAP COMMAND

This command is used to carry out a write/read operation on the memory map of the device.

The data packet for a read/write command consists of 18 bytes, made up of a 1-byte HID-I²C report ID followed by 17 bytes of data (see Figure 9-1).

FIGURE 9-1:   READ/WRITE MEMORY MAP – GENERIC PACKET FORMAT
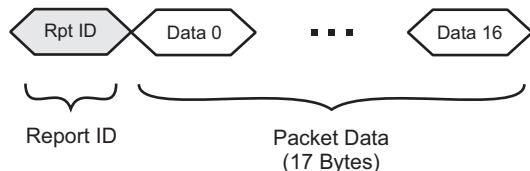
9.5.1.1   Command and Response Packets

The command packet has the generic format given in Figure 9-2. The following sections give examples on using the command to write to the memory map and to read from the memory map.

FIGURE 9-2:   READ/WRITE MEMORY MAP – COMMAND PACKET FORMAT
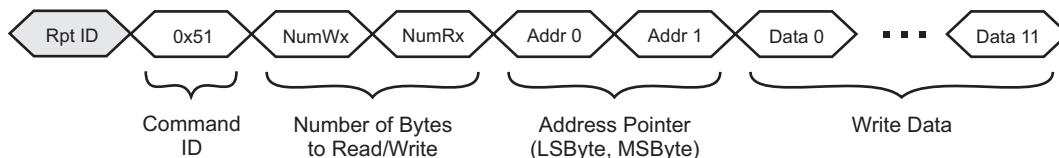
In Figure 9-2:

- **Rpt ID** is the HID-I²C report ID used for Object Protocol commands and responses (see Table 9-2 on page 40).
- **Command ID** is the command ID for the write/read operation (0x51)
- **NumWx** is the number of data bytes to write to the memory map (may be zero). If the address pointer is being sent, this must include the size of the address pointer.
- **NumRx** is the number of data bytes to read from the memory map (may be zero).
- **Addr 0** and **Addr 1** form the address pointer to the memory map (where necessary; may be zero if not needed). This is typically an address of an object within the device.
- **Data 0** to **Data 11** are the bytes of data to be written (in the case of a write). Note that data locations beyond the number specified by NumWx will be ignored.

The response packet has the generic format given in Figure 9-3.

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FIGURE 9-3: **READ/WRITE MEMORY MAP – RESPONSE PACKET FORMAT**

FIGURE 9-3: **READ/WRITE MEMORY MAP – RESPONSE PACKET FORMAT**
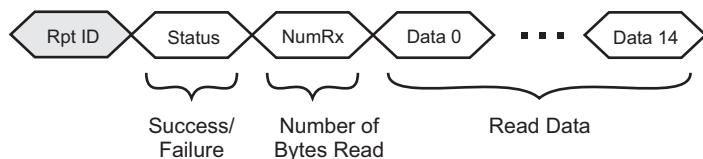
In Figure 9-3:

- **Rpt ID** is the HID-I^{2}C report ID used for Object Protocol commands and responses (see Table 9-2 on page 40).
- **Status** indicates the result of the command:
  - 0x00 = read and write completed; read data returned
  - 0x04 = write completed; no read data requested
- **NumRx** is the number of bytes following that have been read from the memory map (in the case of a read). This will be the same value as NumRx in the command packet.
- **Data 0** to **Data 14** are the data bytes read from the memory map.

9.5.1.2 Writing To the Device

A write operation cycle to the device consists of sending a packet that contains six header bytes. These specify the HID-I^{2}C report ID, the Command ID, the number of bytes to read, the number of bytes to write, and the 16-bit address pointer.

Subsequent bytes in a multi-byte transfer form the actual data. These are written to the location of the address pointer, location of the address pointer +1, location of the address pointer + 2, and so on.

Figure 9-4 shows an example command packet to write four bytes of data to contiguous addresses starting at 0x1234.

FIGURE 9-4: **EXAMPLE OF A FOUR-BYTE WRITE COMMAND STARTING AT ADDRESS 0x1234**
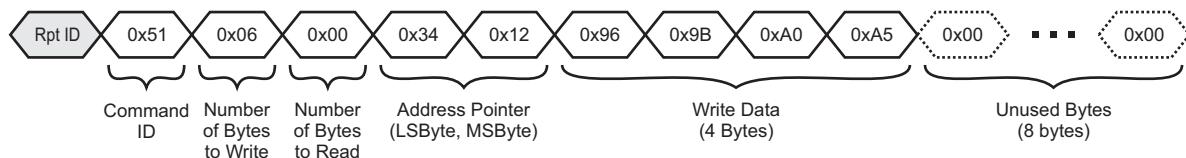
In Figure 9-4:

- **Rpt ID** is the HID-I^{2}C report ID used for Object Protocol commands and responses (see Table 9-2 on page 40).
- **Number of Bytes to Read** is set to zero as this is a write-only operation.
- **Number of Bytes to Write** is six (that is, four data bytes plus the two address pointer bytes).

Figure 9-5 shows the response to this command. In this case, the result status returned is 0x04 (that is, the write operation was completed but no read data was requested). Note that the report ID will be the same one used in the command packet.

FIGURE 9-5: **RESPONSE TO EXAMPLE FOUR-BYTE WRITE**
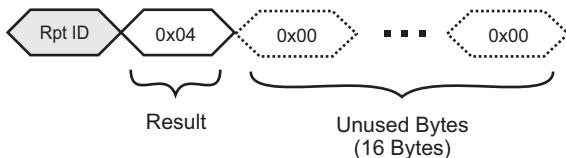
9.5.1.3 Reading From the Device

A read operation consists of sending a packet that contains the six header bytes only and no write data.

Figure 9-6 on page 43 shows an example command packet to read four bytes starting at address 0x1234. Note that the address pointer is included in the number of bytes to write, so the number of bytes to write is set to 2 as there are no other data bytes to be written.

FIGURE 9-6: **EXAMPLE OF A FOUR-BYTE READ COMMAND STARTING AT ADDRESS 0x1234**
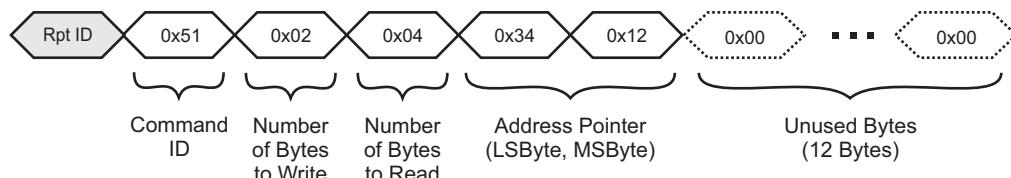
| Rpt ID | 0x51 | 0x02 | 0x04 | 0x34 | 0x12 | 0x00 | ▪ ▪ ▪ | 0x00 |

Command ID · Number of Bytes to Write · Number of Bytes to Read · Address Pointer (LSByte, MSByte) · Unused Bytes (12 Bytes)

It is not necessary to set the address pointer before every read. The address pointer is updated automatically after every read operation, so the address pointer will be correct if the reads occur in order.

Figure 9-7 shows the response to this command. The result status returned is 0x00 (that is the write operation was completed and the data was returned). The number of bytes returned will be the same as the number requested (4 in this case).

FIGURE 9-7: **RESPONSE TO EXAMPLE FOUR-BYTE READ**

| Rpt ID | 0x00 | 0x04 | 0x96 | 0x9B | 0xA0 | 0xA5 | 0x00 | ▪ ▪ ▪ | 0x00 |

Result · Number of Bytes Read · Read Data (4 Bytes) · Unused Bytes (11 Bytes)
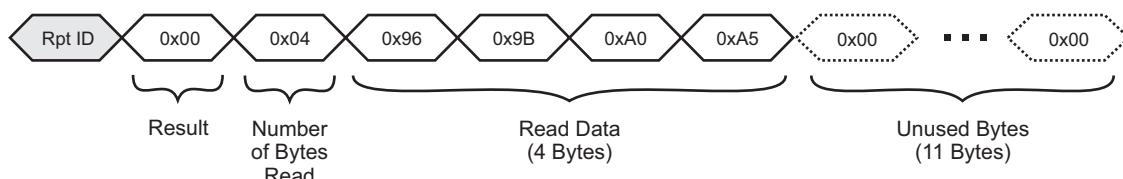
9.5.2   SEND AUTO-RETURN COMMAND

With this command the device can be configured to return new messages from the Message Processor T5 object autonomously.

The packet sequence to do this is shown in Figure 9-8.

FIGURE 9-8: **SEND AUTO-RETURN – PACKET SEQUENCE**

Host · Device

Send Auto-return Command Packet

Response Packet

Message Data Packet

Message Data Packet

⋮

Message Data Packet

Null Packet to Terminate
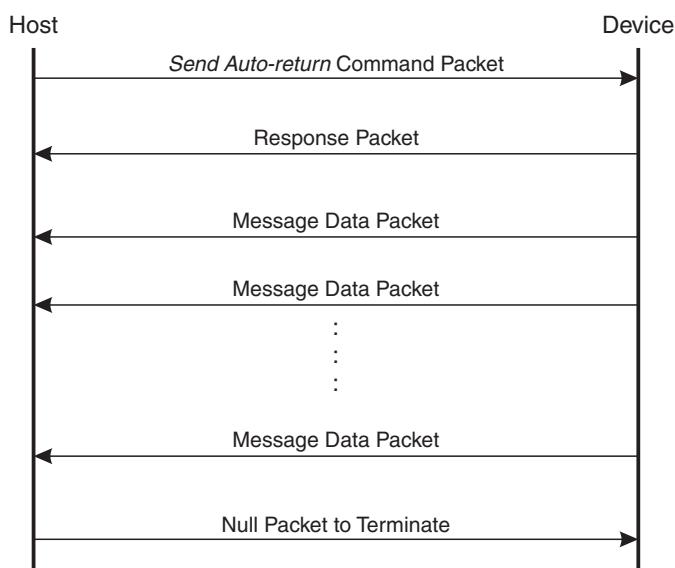
The data packet for Send Auto-return commands consists of 14 bytes, made up of a 1-byte HID-I²C report ID followed by 13 bytes of data. Note that this is different to the packet for standard read/write operations described in Section 9.5.1 "Read/Write Memory Map Command".

The command packet has the format given in Figure 9-9.

FIGURE 9-9:   **SEND AUTO-RETURN – COMMAND PACKET FORMAT**
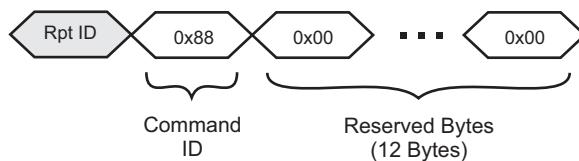
In Figure 9-9:

- **Rpt ID** is the HID-I^{2}C report ID used for Object Protocol commands and responses (see Table 9-2 on page 40).
- **Command ID** is the command ID for the Send Auto-return command (0x88)
- **Reserved Bytes** are reserved bytes with a value of 0x00.

Note that with this command, the command packet does not include an address pointer as the device already knows the address of the Message Processor T5 object.

The response packet has the format given in Figure 9-10.

FIGURE 9-10:   **SEND AUTO-RETURN – RESPONSE PACKET FORMAT**
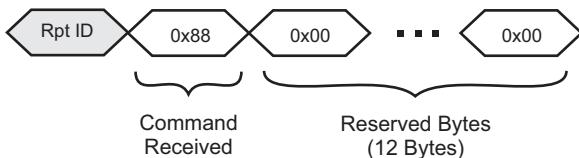
Once the device has responded to the command, it starts sending message data. Each time a message is generated in the Message Processor T5 object, the device automatically sends a message packet to the host with the data. The message packets have the format given in Figure 9-11.

FIGURE 9-11:   **SEND AUTO-RETURN – MESSAGE PACKET FORMAT**
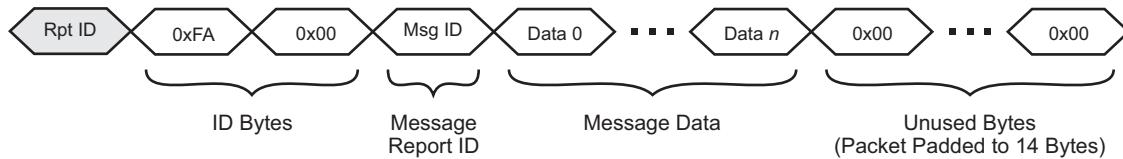
In Figure 9-11:

- **Rpt ID** is the HID-I^{2}C report ID used for Object Protocol commands and responses (see Table 9-2 on page 40).
- **ID Bytes** identify the packet as an auto-return message packet.
- **Message Report ID** is the report ID returned by the Message Processor T5 object. Note that this is the report ID used in the Object Protocol and should not be confused with the HID-I^{2}C report ID. Refer to the *mXT1664T3 2.0 Protocol Guide* for more information on the use of Object Protocol report IDs.
- **Message Data** bytes are the bytes of data returned by the Message Processor T5 object. The size of the data depends on the source object for which this is the message data. Any unused bytes are padded with zeros. Refer to the *mXT1664T3 2.0 Protocol Guide* for more information on the messages from the various objects.

To stop the sending of the messages, the host can send a null command packet. This consists of two bytes: the HID-I^{2}C report ID for Object Protocol commands and responses (see Table 9-2 on page 40) and a null command byte of 0x00 (see Figure 9-12).

FIGURE 9-12:   **SEND AUTO-RETURN – NULL COMMAND PACKET FORMAT**
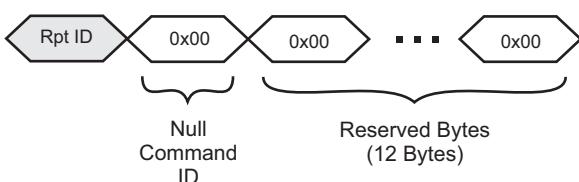
Note that any standard read or write operation will also terminate any currently enabled auto-return mode (see Section 9.5.1 "Read/Write Memory Map Command").

Figure 9-13 shows an example sequence of packets to receive messages from the Message Processor T5 object using the Send Auto-return command.

FIGURE 9-13: **SEND AUTO-RETURN – EXAMPLE SEQUENCE**
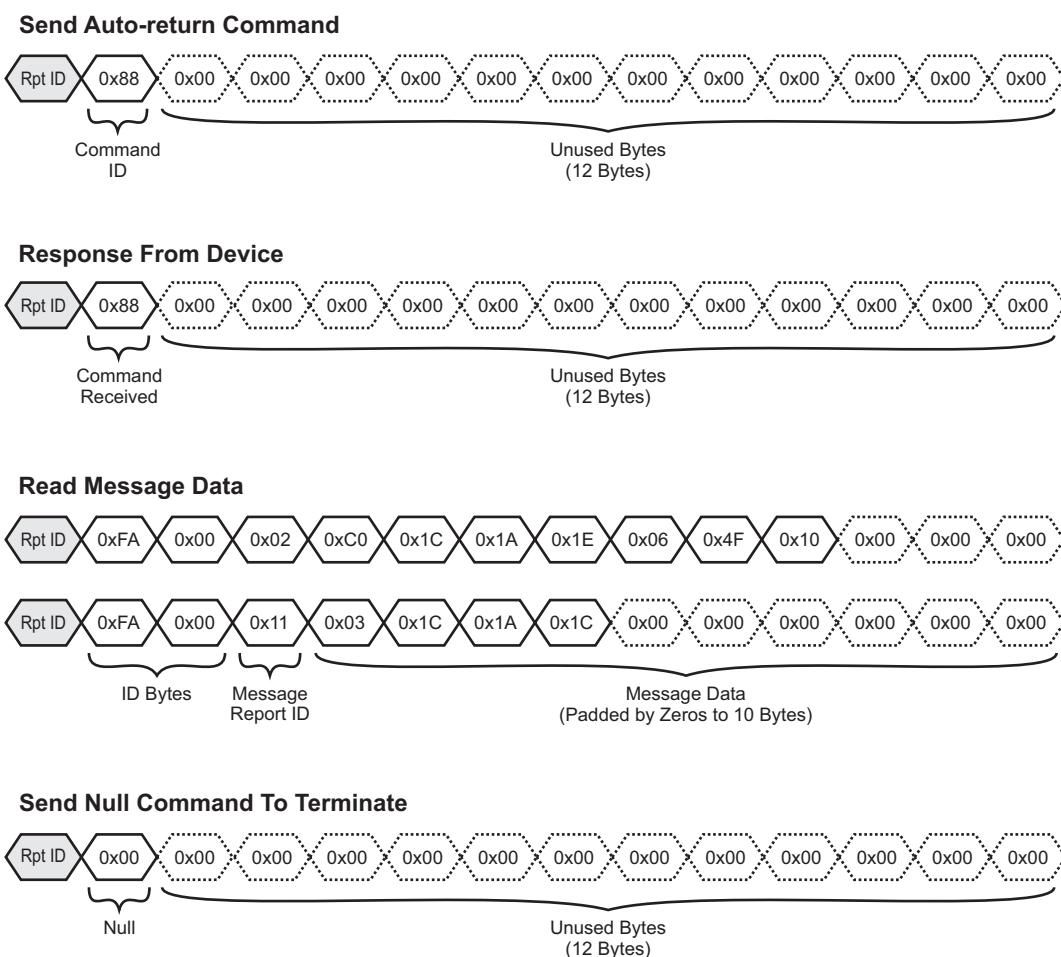
9.6 Digitizer HID-I²C

This is a digitizer class HID.

9.6.1 TOUCH REPORT

The format of a Touch report is shown in Figure 9.6.2. Each Touch report is 18 bytes long and contains the data for one touch.

9.6.2 TOUCH REPORT PACKET FORMAT
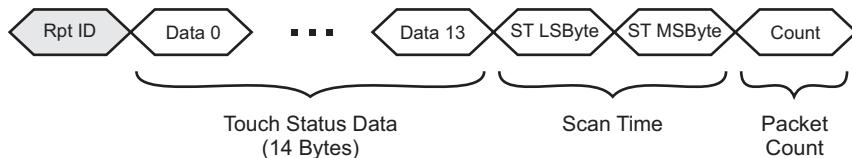
In Figure 9.6.2:

- **Rpt ID** is the HID-I²C report ID used for Touch reports (see Table 9-2 on page 40).
- **Touch** is the data for the touch.
- **Scan Time** is the Timestamp for the report packet
- **Count** is used to identify the report packets for current active touches that are to be reported as a single package. The Count in the first packet for the first touch is set to the number of active touches to be sent in one package (that is, the number of packets). Subsequent packets for subsequent active touches have a Count of 0.

An example of the Touch report packets for 3 active touches is shown in Figure 9-14.

FIGURE 9-14: **EXAMPLE TOUCH REPORT PACKETS FOR 3 ACTIVE TOUCHES**
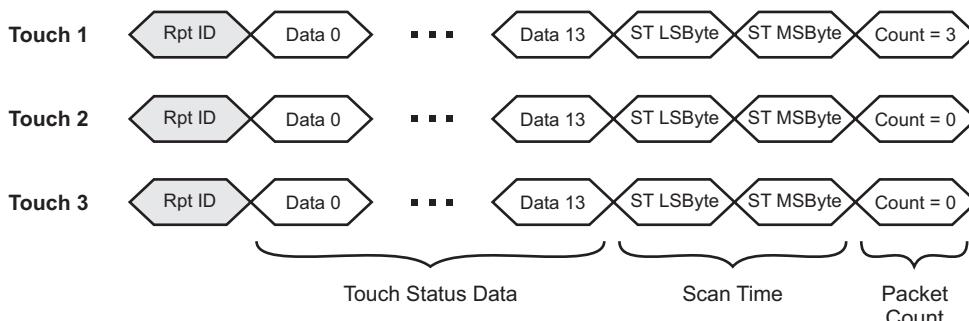
Each input report consists of a HID-I²C report ID followed by 17 bytes that describe the status of one active touch. The input report format depends on the geometry calculation control (TCHGEOMEN) of the Digitizer HID Configuration T43 object. Table 9-3 and Table 9-4 on page 47 give the detailed format of a touch report packet.

TABLE 9-3: **TOUCH REPORT FORMAT WHEN TCHGEOMEN = 1**

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	HID-I²C Touch Report ID							
1	Reserved							Status
2	Touch ID							
3	Touch X Position LSByte (first touch)							
4	Reserved				Touch X Position MSBits (first touch)			
5	Touch Center X Position LSByte (first touch)							
6	Reserved				Touch Center X Position MSBits (first touch)			
7	Touch Y Position LSByte (first touch)							
8	Reserved				Touch Y Position MSBits (first touch)			
9	Touch Center Y Position LSByte (first touch)							
10	Reserved				Touch Center Y Position MSBits (first touch)			

TABLE 9-3:   TOUCH REPORT FORMAT WHEN TCHGEOMEN = 1 (CONTINUED)

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
11	Touch Width							
12	Reserved							
13	Touch Height							
14	Reserved							
15	Scan Time LSByte							
16	Scan Time MSByte							
17	Packet Count							

TABLE 9-4:   TOUCH REPORT FORMAT WHEN TCHGEOMEN = 0

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	HID-I^{2}C Touch Report ID							
1	Reserved							Status
2	Touch ID							
3	Touch X Position LSByte (first touch)							
4	Reserved				Touch X Position MSBits (first touch)			
5	Reserved							
6	Reserved							
7	Touch Y Position LSByte (first touch)							
8	Reserved				Touch Y Position MSBits (first touch)			
9	Reserved							
10	Reserved							
11	Reserved							
12	Reserved							
13	Reserved							
14	Reserved							
15	Scan Time LSByte							
16	Scan Time MSByte							
17	Packet Count							

- Byte 0:

  The HID-I^{2}C report ID (see Table 9-2 on page 40 for Touch reports).

- Byte 1:

  Status is the status of the touch detection. This bit is set to 1 if touch is detected, and set to 0, if no touches are detected.

- Byte 2:

  Touch ID identifies the touch for which this is a status report (starting from 0).

- Bytes 3 to 10:

  X and Y positions identify the touch position. These are scaled to 12-bit resolution. This means that the upper four bits of the MSByte will always be zero. Bytes 5, 6, 9 and 10 are reserved when TCHGEOMEN field is set to 0.

- Byte 11:

  Touch Width reports the width of the detected touch when TCHGEOMEN is set to 1.
  Reserved when TCHGEOMEN is set to 0

- Byte 13:

  Touch Height reports the height of the detected touch when TCHGEOMEN is set to 1.
  Reserved when TCHGEOMEN is set to 0

- Byte 15 to 16:

  Scan Time is the timestamp associated with the current report packet (10 kHz resolution).

- Byte 17:

  Count is the number of active touches to be sent in one package, for the first touch only. Subsequent packets for subsequent active touches have a Count of 0.

9.6.3   MAXIMUM TOUCHES REPORT

Read this report to receive the maximum number of touches (surface contacts) that can currently be reported.

Write this report to set the maximum number of touches to be reported.

The format of the Maximum Touches report packet is shown in Figure 9-15. Each Maximum Touch report is 18 bytes long and contains a single byte giving the maximum number of touches to be reported.

FIGURE 9-15:   **MAXIMUM TOUCHES REPORT FORMAT**
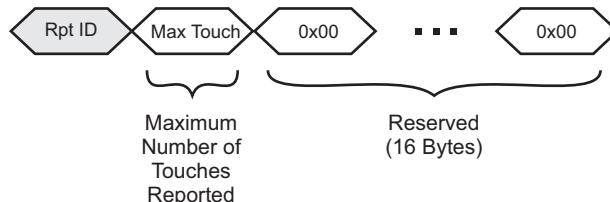
In Figure 9-15:

- **Rpt ID** is the HID-I^{2}C report ID used for Maximum Touches reports (see Table 9-2 on page 40).
- **Max Touch** is the maximum number of touches to be reported by the device.

NOTE	The number of touches cannot be set to more than the maximum number of touches configured in the device by the Multiple Touch Touchscreen T100 object.

9.6.4   TOUCH HARDWARE QUALITY ASSURANCE (THQA) REPORT

The THQA data is reported to Microsoft Windows using the THQA report ID (see Table 9-2 on page 40 for the value). The content of this data is defined by Microsoft.

9.7 $\overline{CHG}$ Line

The $\overline{CHG}$ line is used to implement the HID-I^{2}C interrupt line. It provides a level triggered interrupt to the host to indicate when there is one or more reports to be read. The $\overline{CHG}$ line will be pulled low when a report is ready and will remain low as long as there are further reports to be read. Once the last report is read the $\overline{CHG}$ line will go high.

NOTE	In order to comply with the HID-I^{2}C specification, Communications Configuration T18 MODE should be set to 0.

9.8   SDA, SCL

Identical to standard I^{2}C operation. See Section 8.7 "SDA and SCL".

9.9   Clock Stretching

Identical to standard I^{2}C operation. See Section 8.8 "Clock Stretching".

9.10   Power Control

The mXT1664T3 supports the use of the HID-I^{2}C *SET POWER* commands to put the device into a low power state.

9.11   Microsoft Windows Compliance

The mXT1664T3 has algorithms within the Multiple Touch Touchscreen T100 object specifically to ensure compliance with Microsoft Windows 8.x and later versions.

The device also supports Microsoft Touch Hardware Quality Assurance (THQA) in the Serial Data Command T68 object. Refer to the Microsoft whitepaper *How to Design and Test Multitouch Hardware Solutions for Windows 8*.

These, and other device features, may need specific tuning.

10.0 USB COMMUNICATIONS

The device is a composite USB device with two Human Interface Device (HID) interfaces:

- **Interface 0** – This interface provides a Generic HID that allows the host to communicate with the device using the Object Protocol. The HID identifier string is "Atmel maXTouch Control". See Section 10.4 "Interface 0 (Generic HID)" for more details.

- **Interface 1** – This interface provides a Digitizer HID that supplies touch information to the Host for passing on to a PC operating system. This interface is supported by Microsoft Windows without the need for additional software. The HID identifier string is "Atmel maXTouch Digitizer". See Section 10.5 "Interface 1 (Digitizer HID)" for more details.

The topography of the USB device is shown in Figure 10-1.

FIGURE 10-1:   USB TOPOGRAPHY
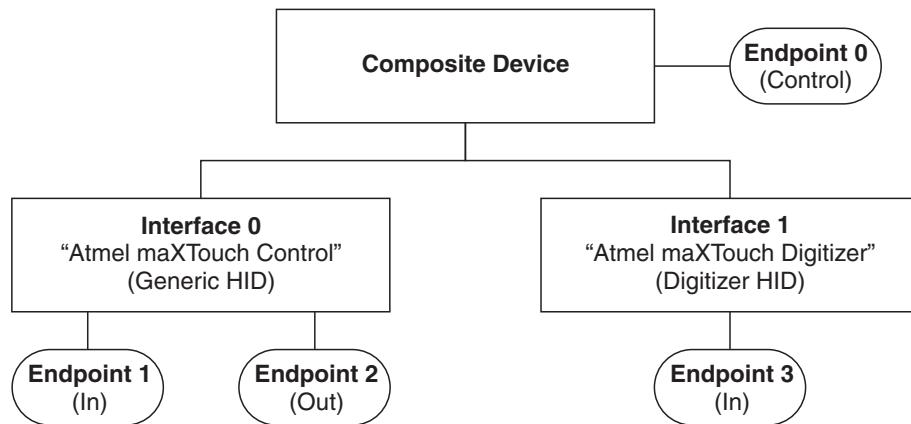
Communication takes place using Full-speed USB at 12 Mbps.

For more information on the USB HID specifications visit www.usb.org.

10.1 Endpoint Addresses

The endpoint addresses are listed in Table 10-1.

TABLE 10-1:   ENDPOINT ADDRESSES

Endpoint	Direction	Address
Endpoint 0	Bidirectional (control)	–
Endpoint 1	In	0x81
Endpoint 2	Out	0x02
Endpoint 3	In	0x83

10.2 Composite Device

The composite device is a USB 2.0-compliant USB composite device running at full speed (12 Mbps). It has the specification shown in Table 10-2 on page 49.

TABLE 10-2:   DEVICE SPECIFICATION

Parameter	Value
Vendor ID	0x03EB (Microchip Atmel)
Product ID	0x215D (mXT1664T3)
Version ID	16-bit Version & Build Identifier in the form 0xVVBB, where: VV = Version Major (Upper 4 bits) / Minor (Lower 4 bits) BB = Build number in BCD format

The composite device has one bidirectional endpoint: the Control Endpoint (Endpoint 0). It is used by the USB Host to interrogate the USB device for details on its configurations, interfaces and report structures. It is also used to apply general device settings relating to USB Implementation.

10.3 USB Report IDs

Table 10-3 describes the USB report IDs used in reports sent to the host.

NOTE	The term USB report ID should not be confused with the term report Id as used in the Object Protocol; the two are entirely different concepts. Refer to the *mXT1664T3 2.0 Protocol Guide* for more information on the use of Object Protocol report IDs.

TABLE 10-3:   USB REPORT IDS

Report ID	Description	HID Interface
0x01	Object Protocol (OBP) command and response (see Section 10.4 "Interface 0 (Generic HID)")	Generic HID
0x02	Additional OBP report ID for debug data (see Section 10.4.3 "Start Debug Monitoring")	Generic HID
0x01	Touch report (see Section 10.5.1 "Touch Report")	Digitizer HID
0x02	Maximum Touches (Surface Contacts) report (see Section 10.5.2 "Maximum Touches Report")	Digitizer HID
0x05	Touch Hardware Quality Assurance (THQA) report (see Section 10.5.3 "Touch Hardware Quality Assurance (THQA) Report")	Digitizer HID

10.4 Interface 0 (Generic HID)

Interface 0 is a Generic Human Interface Device, compliant with HID specification 1.11 with amendments (an implementation of Microsoft's USB HID specification for multitouch digitizers).

Interface 0 consists of two endpoints: an interrupt-In endpoint (Endpoint 1) and an interrupt-out endpoint (Endpoint 2). The data packet in each case contains a 1-byte USB report ID followed by 63 bytes of data, totaling 64 bytes (see Figure 10-2).

FIGURE 10-2:   GENERIC HID – DATA PACKET FORMAT

Commands are sent by the application software over the Interrupt-out endpoint, Endpoint 2. The command is sent as the first data byte of the packet data (data byte 0), followed by conditions and/or data.

The supported commands are as follows:

- Read/write Memory Map
- Send Auto-return messages
- Start debug monitoring
- End debug monitoring

Responses from the device are sent via the Interrupt-In endpoint, Endpoint 1.

The USB report ID used is that for Object Protocol commands and responses; see Table 10-3 for the value.

10.4.1   READ/WRITE MEMORY MAP

This command is used to carry out a write/read operation on the memory map of the device.

10.4.1.1   Command and Response Packets

The command packet has the generic format given in Figure 10-3. The following sections give examples on using the command to write to the memory map and to read from the memory map.

**FIGURE 10-3:   READ/WRITE MEMORY MAP – COMMAND PACKET FORM**
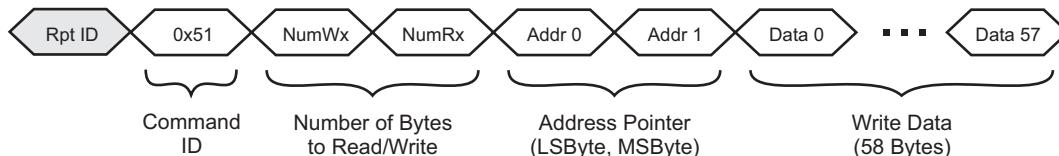
In Figure 10-3:

- **Rpt ID** is the USB report ID used for Object Protocol commands and responses (see Table 10-3 on page 50).
- **Command ID** is the command ID for the write/read operation (0x51)
- **NumWx** is the number of data bytes to write to the memory map (may be zero). If the address pointer is being sent, this must include the size of the address pointer.
- **NumRx** is the number of data bytes to read from the memory map (may be zero).
- **Addr 0** and **Addr 1** form the address pointer to the memory map (where necessary; may be zero if not needed). This is typically an address of an object within the device.
- **Data 0** to **Data 57** are the bytes of data to be written (in the case of a write). Note that data locations beyond the number specified by NumWx will be ignored.

The response packet has the generic format given in Figure 10-4.

FIGURE 10-4:   READ/WRITE MEMORY MAP – RESPONSE PACKET FORMAT
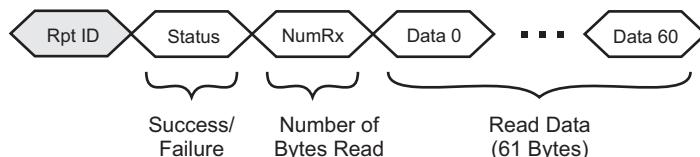
In Figure 10-4:

- **Status** indicates the result of the command:
  - 0x00 = read and write completed; read data returned
  - 0x04 = write completed; no read data requested
- **NumRx** is the number of bytes following that have been read from the memory map (in the case of a read). This will be the same value as NumRx in the command packet.
- **Data 0** to **Data 60** are the data bytes read from the memory map.

10.4.1.2   Writing To the Device

A write operation cycle to the device consists of sending a packet that contains six header bytes (see Section 10.4.1.1 "Command and Response Packets"). These specify the USB report ID, the Command ID, the number of bytes to read, the number of bytes to write, and the 16-bit address pointer.

Subsequent bytes in a multibyte transfer form the actual data. These are written to the location of the address pointer, location of the address pointer +1, location of the address pointer + 2, and so on.

Figure 10-5 shows an example command packet to write four bytes of data to contiguous addresses starting at 0x1234.

FIGURE 10-5:   EXAMPLE OF A FOUR-BYTE WRITE STARTING AT ADDRESS 0x1234
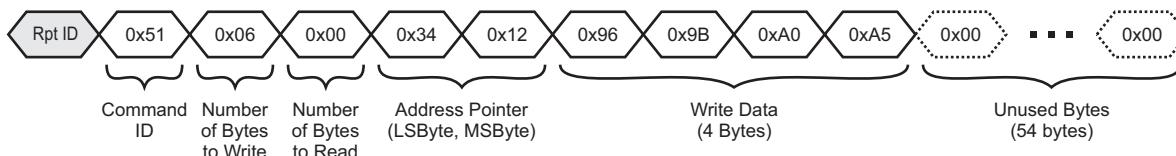
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- **Number of Bytes to Read** is set to zero as this is a write-only operation.
- **Number of Bytes to Write** is six (that is, four data bytes plus the two address pointer bytes).

Figure 10-6 shows the response to this command. Note that the result status returned is 0x04 (that is, the write operation was completed but no read data was requested).

FIGURE 10-6: **RESPONSE TO EXAMPLE FOUR-BYTE WRITE**
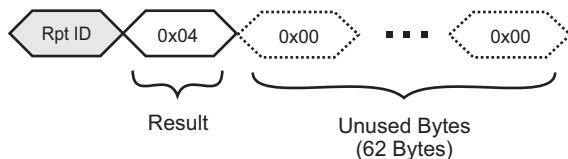
10.4.1.3   Reading From the Device

A read operation consists of sending a packet that contains the six header bytes only and no write data.

Figure 10-7 shows an example command packet to read four bytes starting at address 0x1234. Note that the address pointer is included in the number of bytes to write, so the number of bytes to write is set to 2 as there are no other data bytes to be written.

FIGURE 10-7: **EXAMPLE OF A FOUR-BYTE READ STARTING AT ADDRESS 0x1234**
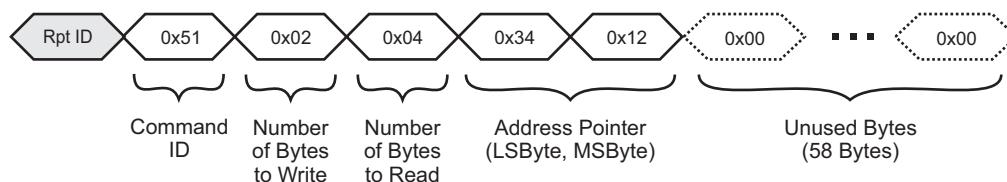
It is not necessary to set the address pointer before every read. The address pointer is updated automatically after every read operation, so the address pointer will be correct if the reads occur in order.

Figure 10-8 shows the response to this command. The result status returned is 0x00 (that is the write operation was completed and the data was returned). The number of bytes returned will be the same as the number requested (4 in this case).

FIGURE 10-8: **RESPONSE TO EXAMPLE FOUR-BYTE READ**
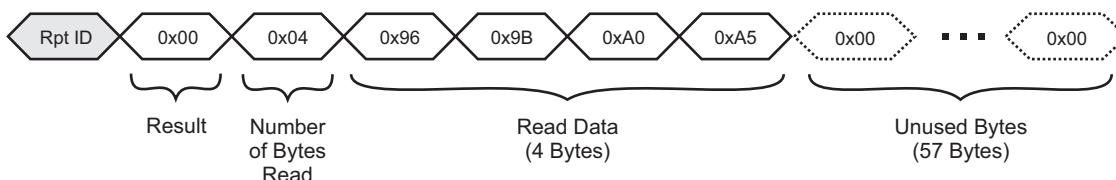
10.4.2   SEND AUTO-RETURN MESSAGES

With this command the device can be configured to return new messages from the Message Processor T5 object autonomously. The packet sequence to do this is shown in Figure 10-9.

FIGURE 10-9: **SEND AUTO-RETURN – PACKET SEQUENCE**
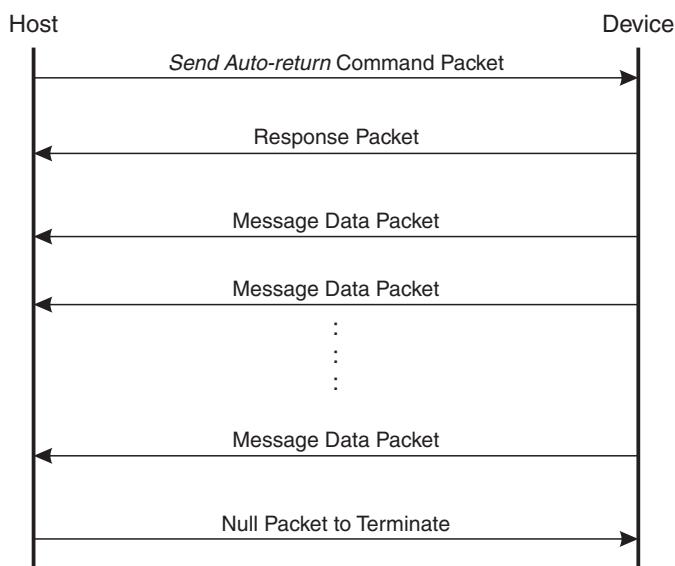
The USB report ID used is that for Object Protocol commands and responses; see Table 10-3 on page 50 for the value.

The command packet has the format given in Figure 10-10.

FIGURE 10-10: **SEND AUTO-RETURN – COMMAND PACKET FORMAT**
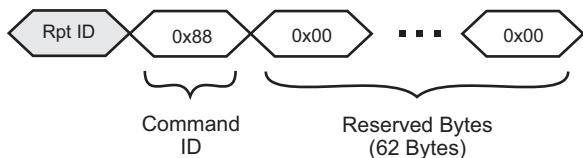
In Figure 10-10:

- **Rpt ID** is the USB report ID used is that for Object Protocol commands and responses (see Table 10-3 on page 50 for the value).
- **Command ID** is the command ID for the Send Auto-return command (0x88).
- **Reserved Bytes** are reserved bytes with a value of 0x00.

The response packet has the format given in Figure 10-11. Note that with this command, the command packet does not include an address pointer as the device already knows the address of the Message Processor T5 object.

FIGURE 10-11: **SEND AUTO-RETURN – RESPONSE PACKET FORMAT**
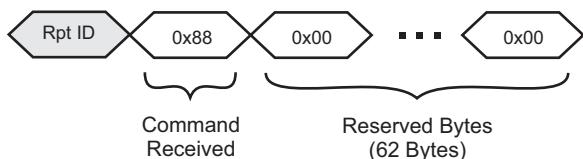
Once the device has responded to the command, it starts sending message data. Each time a message is generated in the Message Processor T5 object, the device automatically sends a message packet to the host with the data. The message packets have the format given in Figure 10-12.

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FIGURE 10-12: SEND AUTO-RETURN – MESSAGE PACKET FORMAT
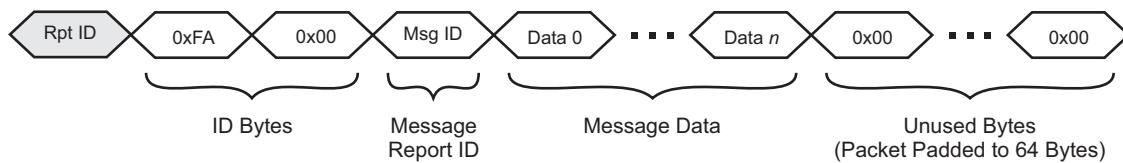
In Figure 10-12:

- **Rpt ID** is the USB report ID used is that for Object Protocol commands and responses (see Table 10-3 on page 50 for the value).
- **ID Bytes** identify the packet as an auto-return message packet.
- **Message Report ID** is the report ID returned by the Message Processor T5 object. Note that this is the report ID used in the Object Protocol and should not be confused with the USB report ID. Refer to the *mXT1664T3 2.0 Protocol Guide* for more information on the use of Object Protocol report IDs.
- **Message Data** bytes are the bytes of data returned by the Message Processor T5 object. The size of the data depends on the source object for which this is the message data. Any unused bytes are padded with zeros. Refer to the *mXT1664T3 2.0 Protocol Guide* for more information on the messages from the various objects.

To stop the sending of the messages, the host can send a null command packet. This consists of two bytes: the report ID for Object Protocol commands and responses (0x01) and a command byte of 0x00 (see Figure 10-13).

FIGURE 10-13: SEND AUTO-RETURN – NULL COMMAND PACKET FORMAT
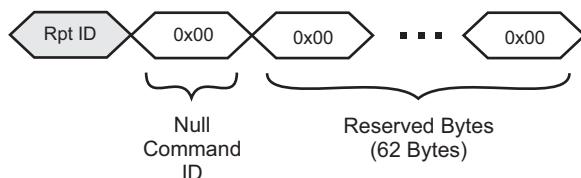
Note that any standard read/write operation (see Section 9.5.1 "Read/Write Memory Map Command") or Start Debug Monitoring (see Section 10.4.3 "Start Debug Monitoring") command will also terminate any currently enabled auto-return mode.

Figure 10-14 on page 55 shows an example sequence of packets to receive messages from the Message Processor T5 object using the Send Auto-return command.

FIGURE 10-14:   SEND AUTO-RETURN – EXAMPLE SEQUENCE

Send Auto-return Command

Command ID — 0x88

Reserved Bytes (62 Bytes)

Response From Device

Command Received — 0x88

Reserved Bytes (62 Bytes)

Read Message Data

| Rpt ID | 0xFA | 0x00 | 0x02 | 0xC0 | 0x1C | 0x1A | 0x1E | 0x06 | 0x4F | 0x10 | 0x00 | ... | 0x00 |

| Rpt ID | 0xFA | 0x00 | 0x11 | 0x03 | 0x1C | 0x1A | 0x1C | 0x00 | 0x00 | 0x00 | 0x00 | ... | 0x00 |

ID Bytes   Message Report ID   Message Data (Padded by Zeros to 60 Bytes)

Send Null Command To Terminate

Null — 0x00

Reserved Bytes (62 Bytes)
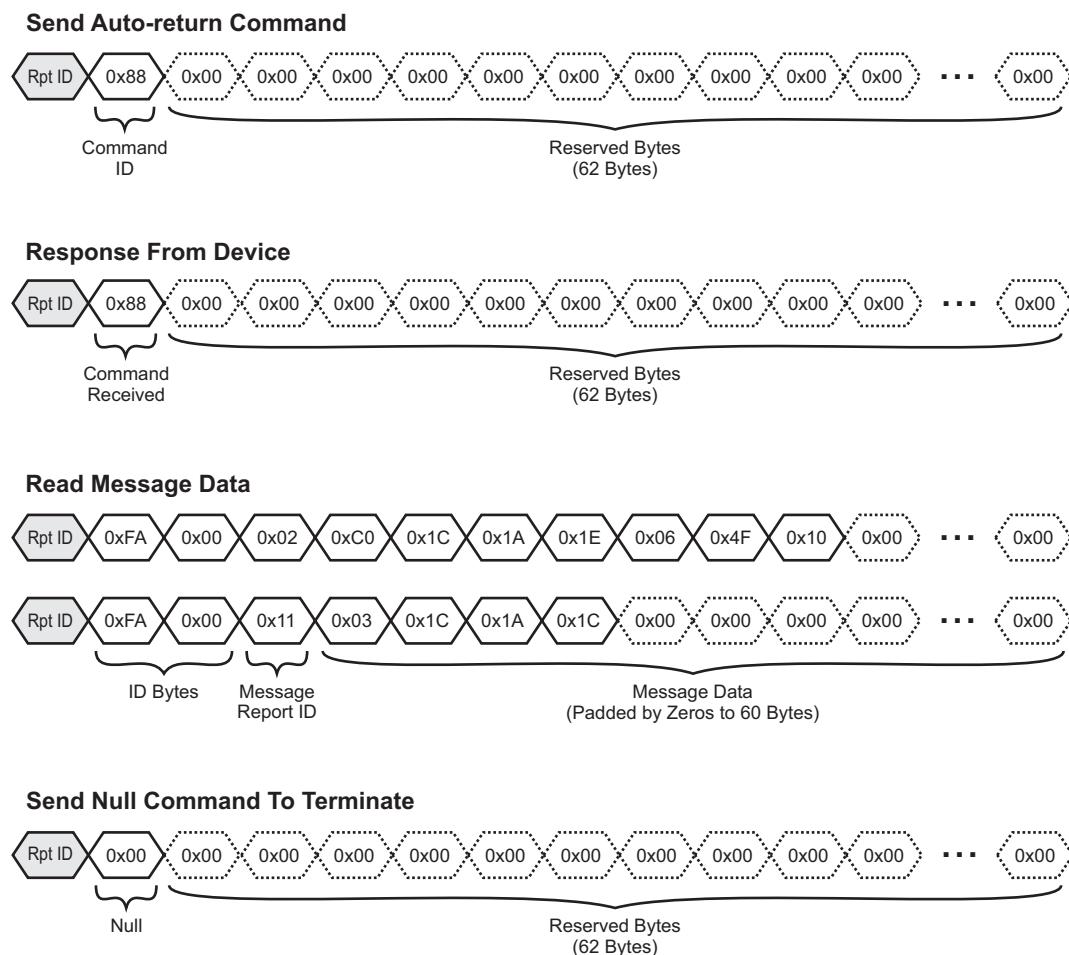
10.4.3   START DEBUG MONITORING

This command instructs the device to return debug-monitoring data packets using the debug port, if this feature has been enabled in the Command Processor T6 object.

The command packet has the format given in Figure 10-15.

FIGURE 10-15:   START DEBUG MONITORING – COMMAND PACKET FORMAT

Command ID — 0xE1

Reserved Bytes (62 Bytes)
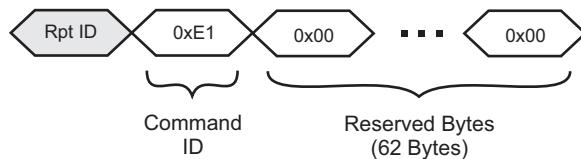
In Figure 10-15:

- **Rpt ID** can be either 0x01 or 0x02 (see Table 10-3 on page 50). The main difference is that a USB report ID of 0x01 will terminate any currently enabled auto-return mode (see Section 10.4.2 "Send Auto-return Messages").
- **Command ID** is the command ID to start debug monitoring (0xE1).

The response packet has the format given in Figure 10-16 on page 56. Note that the USB report ID will be the same as that used in the command packet.

FIGURE 10-16:   **START DEBUG MONITORING – RESPONSE PACKET FORMAT**
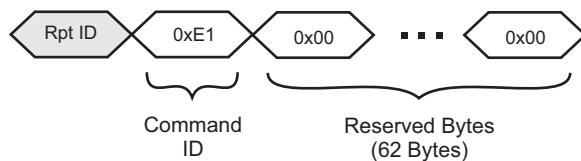
In Figure 10-16:

- **Rpt ID** is the same as that used in the command packet (either 0x01 or 0x02, as appropriate).
- **Command ID** is always 0xE1 (start debug monitoring command).

The debug data packet has the format given in Figure 10-17.

FIGURE 10-17:   **DEBUG DATA PACKET FORMAT**
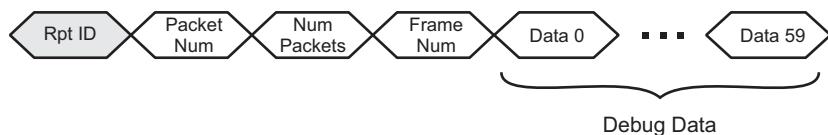
In Figure 10-17:

- **Packet Num** is the number of this USB packet in the debug data frame (full set of debug data). Refer to QTAN0050, *Using the maXTouch Debug Port*, for more information on the format of the debug data.
- **Num Packets** is the total number of USB packets that make up a debug data frame.
- **Frame Num** is the ID number of this frame.
- **Data 0** to **Data 59** are 59 bytes of debug data.

10.4.4 STOP DEBUG MONITORING

This command instructs the device to cease returning debug-monitoring data packets.

The command packet has the format given in Figure 10-18.

FIGURE 10-18:   **STOP DEBUG MONITORING – COMMAND PACKET FORMAT**
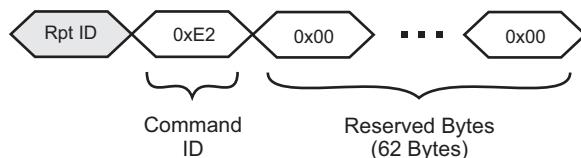
In Figure 10-18:

- **Rpt ID** can be either 0x01 or 0x02 (see Table 10-3 on page 50).
- **Command ID** is the command ID to stop debug monitoring (0xE2).

The response packet has the format given in Figure 10-19.

FIGURE 10-19:   **STOP DEBUG MONITORING – RESPONSE PACKET FORMAT**
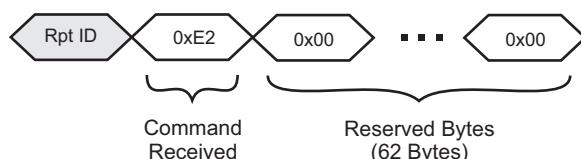
In Figure 10-19:

- **Rpt ID** is the same as that used in the command packet (either 0x01 or 0x02, as appropriate).
- **Command ID** is always 0xE2 (stop debug monitoring command).

10.5 Interface 1 (Digitizer HID)

Interface 1 is a Digitizer-class HID, compliant with HID specification 1.11 with amendments (an implementation of Microsoft's USB HID specification for multitouch digitizers).

This interface consists of a single interrupt-In endpoint (Endpoint 3).

10.5.1 TOUCH REPORT

The format of a Touch report is shown in Figure 10-20.

FIGURE 10-20: TOUCH REPORT PACKET
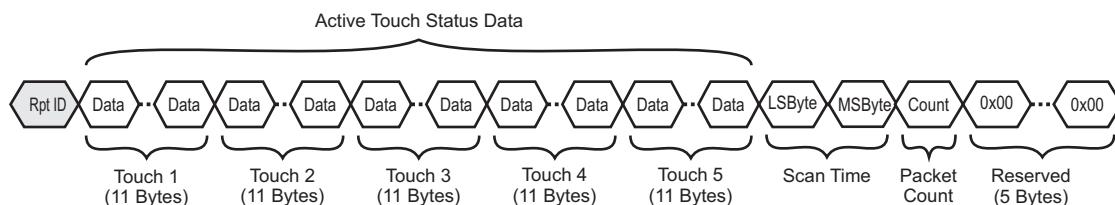
In Figure 10-20:

- **Rpt ID** is the report ID for Touch reports (see Table 10-3 on page 50).
- **Active Touch Status Data** are 5 sets of data (11 bytes each) that describe the status of up to 5 active touches. Any unused touch data bytes are set to zero.
- **Scan Time** is the timestamp associated with the report frame (in units of 100 μs).
- **Count** is the number of active touches in this Touch report.

  If there are more than five active touches to be reported, a further report is sent with the remaining touch data. In this case, the count (for all touches) is sent in the first count byte and the count byte in the last report is zero.

An example of the input report packets for 7 active touches is shown in Figure 10-21.

FIGURE 10-21: EXAMPLE TOUCH REPORT PACKETS FOR 7 ACTIVE TOUCHES
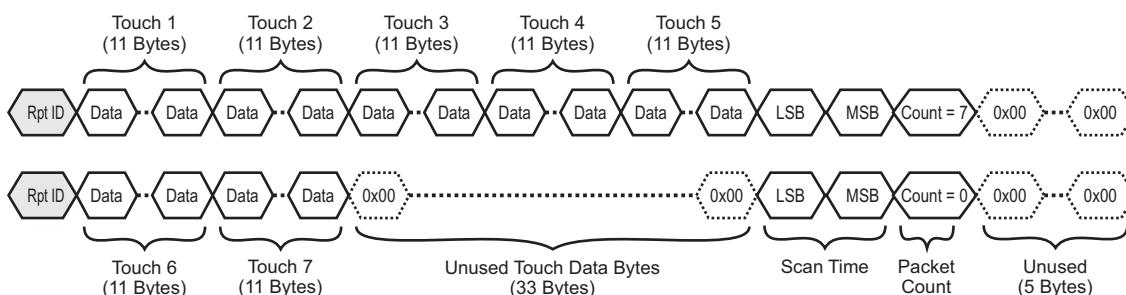
The Touch report format depends on the geometry calculation field (TCHGEOMEN) of the Digitizer HID Configuration T43 object. Table 10-4 and Table 10-5 on page 58 give the detailed format of an Touch report packet.

TABLE 10-4: TOUCH REPORT FORMAT WHEN TCHGEOMEN IS ENABLED

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	USB Report ID							
1	Touch ID (first touch)					Reserved		Status
2	Touch X Position LSByte (first touch)							
3	0	0	0	0	Touch X Position MSBits (first touch)			
4	Touch Center X Position LSByte (first touch)							
5	0	0	0	0	Touch Center X Position MSBits (first touch)			
6	Touch Y Position LSByte (first touch)							
7	0	0	0	0	Touch Y Position MSBits (first touch)			
8	Touch Center Y Position LSByte (first touch)							
9	0	0	0	0	Touch Center Y Position MSBits (first touch)			

TABLE 10-4: TOUCH REPORT FORMAT WHEN TCHGEOMEN IS ENABLED (CONTINUED)

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10	Touch width							
11	Touch height							
12 – 22	Touch data for second touch – same format as bytes 1 – 11							
23 – 33	Touch data for third touch – same format as bytes 1 – 11							
34 – 44	Touch data for fourth touch – same format as bytes 1 – 11							
45 – 55	Touch data for fifth touch – same format as bytes 1 – 11							
56 – 57	Scan time							
58	Contact count							

TABLE 10-5: TOUCH REPORT FORMAT WHEN TCHGEOMEN IS DISABLED

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	USB Report ID							
1	Touch ID (first touch)					Reserved		Status
2	Touch ID							
3	Touch X Position LSByte (first touch)							
4	0	0	0	0	Touch X Position MSBits (first touch)			
5	Reserved							
6	Reserved							
7	Touch Y Position LSByte (first touch)							
8	0	0	0	0	Touch Y Position MSBits (first touch)			
9	Reserved							
10	Reserved							
11	Reserved							
12 – 22	Touch data for second touch – same format as bytes 1 – 11							
23 – 33	Touch data for third touch – same format as bytes 1 – 11							
34 – 44	Touch data for fourth touch – same format as bytes 1 – 11							
45 – 55	Touch data for fifth touch – same format as bytes 1 – 11							
56 – 57	Scan time							
58	Contact count							

In and Table 10-5:

• Byte 1:

  Status is the status of the touch detection. This bit is set to 1 if touch is detected, and set to 0, if no touches are detected.

  Touch ID identifies the touch for which this is a status report (starting from 1).

• Bytes 2 to 9:

  X and Y positions are the X and Y coordinates. These are scaled to 12-bit resolution. This means that the upper four bits of the MSByte will always be zero. Bytes 4, 5, 8 and 9 are reserved when TCHGEOMEN field is set to 0.

• Byte 10:

  Touch Width reports the width of the detected touch when TCHGEOMEN is set to 1.
  Reserved when TCHGEOMEN is set to 0

• Byte 11:

  Touch Height reports the height of the detected touch when TCHGEOMEN is set to 0.
  Reserved when TCHGEOMEN is set to 0

• Byte 56 to 57:

  Scan Time is the timestamp associated with the current report frame (in units of 100 μs).

• Byte 58:

  Contact Count is the number of active touches to be sent in one package, for the first touch only. Subsequent packets for subsequent active touches have a Count of 0.

10.5.2 MAXIMUM TOUCHES REPORT

Read this report to receive the maximum number of touches (surface contacts) that can currently be reported.

Write this report to set the maximum number of touches to be reported.

The format of the Maximum Touches report packet is shown in Figure 10-22.

FIGURE 10-22: **MAXIMUM TOUCHES REPORT PACKET FORMAT**
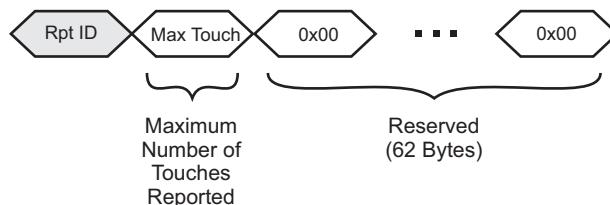
In Figure 10-22.

- **Rpt ID** is the report ID for the Maximum Touches reports (see Table 10-3 on page 50).
- **Max Touch** is the maximum number of touches to be reported by the device.

| NOTE | The number of touches cannot be set to more than the maximum number of touches configured in the device by the Multiple Touch Touchscreen T100 object. |

10.5.3 TOUCH HARDWARE QUALITY ASSURANCE (THQA) REPORT

The THQA data is reported to Microsoft Windows using the THQA report ID (see Table 10-3 on page 50 for the value). The content of this data is defined by Microsoft.

10.6 USB Suspend Mode

When the device is used in USB configuration, the USB "System Suspend" event can be used to minimize current consumption. Note that it is possible to put the device into deep sleep mode without also sending a "System Suspend" event on the USB bus, but the current consumption is not as low. The USB controller must send a USB "System Wakeup" event on the bus to bring the device out of suspend mode.

The device can also be configured to respond to USB "Remote Wakeup" requests. In this case, if the operating system enables remote wakeup and the device is suspended, the device will continue to scan at a preset sensor refresh rate. Use of the remote wake up feature and the sensor refresh rate are configured using the Digitizer HID Configuration T43 object (refer to the *mXT1664T3 2.0 Protocol Guide* for more information).

11.0 PCB DESIGN CONSIDERATIONS

11.1 Introduction

The following sections give the design considerations that should be adhered to when designing a PCB layout for use with the mXT1664T3. Of these, power supply and ground tracking considerations are the most critical.

By observing the following design rules, and with careful preparation for the PCB layout exercise, designers will be assured of a far better chance of success and a correctly functioning product.

11.2 Printed Circuit Board

Microchip recommends the use of a four-layer printed circuit board for mXT1664T3 applications. This, together with careful layout, will ensure that the board meets relevant EMC requirements for both noise radiation and susceptibility, as laid down by the various national and international standards agencies.

11.2.1 PCB CLEANLINESS

Modern no-clean-flux is generally compatible with capacitive sensing circuits.

> **CAUTION!** If a PCB is reworked to correct soldering faults relating to any device, or to any associated traces or components, be sure that you fully understand the nature of the flux used during the rework process. Leakage currents from hygroscopic ionic residues can stop capacitive sensors from functioning. If you have any doubts, a thorough cleaning after rework may be the only safe option.

11.3 Power Supply

11.3.1 SUPPLY QUALITY

While the device has good Power Supply Rejection Ratio properties, poorly regulated and/or noisy power supplies can significantly reduce performance.

Particular care should be taken of the AVdd supply, as it supplies the sensitive analog stages in the device.

11.3.2 SUPPLY RAILS AND GROUND TRACKING

Power supply and clock distribution are the most critical parts of any board layout. Because of this, it is advisable that these be completed before any other tracking is undertaken. After these, supply decoupling, and analog and high speed digital signals should be addressed. Track widths for all signals, especially power rails should be kept as wide as possible in order to reduce inductance.

The Power and Ground planes themselves can form a useful capacitor. Flood filling for either or both of these supply rails, therefore, should be used where possible. It is important to ensure that there are no floating copper areas remaining on the board: all such areas should be connected to the ground plane. The flood filling should be done on the outside layers of the board.

In applications where the USB bus supplies power to the board, care should be taken to ensure that suitable capacitive decoupling is provided close to the USB connector. The tracking to the on-board regulators should also be kept as short as possible.

It should also be remembered that the screen of the USB cable is not intended to be connected to the ground or 0V supply of a remote device. It should either be left open circuit (being connected only at the host computer end) or decoupled with a suitable high voltage capacitor (typically 4.7 nF, 250 V) and a parallel resistor (typically 1 MΩ). Note that these components may not be required when the USB cabling is internal and permanently wired, and is routed away from the noisier parts of the system.

11.3.3 POWER SUPPLY DECOUPLING

Decoupling capacitors should be fitted as specified in Section 2.5 "Schematic Notes".

The decoupling capacitors must be placed as close as possible to the pin being decoupled. The traces from these capacitors to the respective device pins should be wide and take a straight route. They should be routed over a ground plane as much as possible. The capacitor ground pins should also be connected directly to a ground plane.

Surface mounting capacitors are preferred over wire-leaded types due to their lower ESR and ESL. It is often possible to fit these decoupling capacitors underneath and on the opposite side of the PCB to the digital ICs. This will provide the shortest tracking, and most effective decoupling possible.

11.4 Voltage Regulators

Each supply rail requires a Low Drop-Out (LDO) voltage regulator, although an LDO can be shared where supply rails share the same voltage level.

Figure 11-1 shows an example circuit for an LDO.

FIGURE 11-1: **EXAMPLE LDO CIRCUIT**
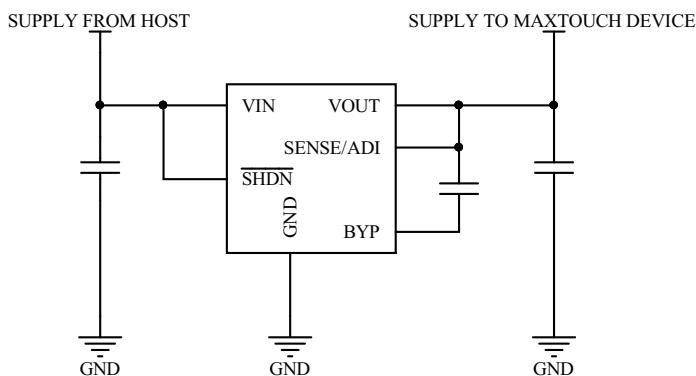
An LDO regulator should be chosen that provides adequate output capability, low noise, good load regulation and step response. The voltage regulators listed in Table 11-1 have been tested and found to work well with maXTouch devices. If it is desired to use an alternative LDO, however, certain performance criteria should be verified before using the device. These are:

- Stable with high value multi-layer ceramic capacitors on the output
- Low output noise – ideally less than 100 μV_{RMS} over the range 10 Hz to 1 MHz
- Good load transient response – this should be less than 35 mV peak when a load step change of 100 mA is applied at the device output terminal
- No-load stable – Some LDOs become unstable if the output current falls below a certain minimum. If this is the case, then this minimum must be lower than the minimum current consumed by the mXT1664T3 (for example, in deep sleep).

TABLE 11-1: **SUITABLE LDO REGULATORS**

Manufacturer	Device	Current Rating (mA)
Microchip Technology Inc.	MCP1824	300
Microchip Technology Inc.	MCP1824S	300
Microchip Technology Inc.	MAQ5300	300
Microchip Technology Inc.	MCP1725	500
Microchip Technology Inc.	MIC5323	300
Analog Devices	ADP122/ADP123	300
Diodes Inc.	AP2125	300
Diodes Inc.	AP7335	300
Linear Technology	LT1763CS8-3.3	500
NXP	LD6836	300
Texas Instruments	LP3981	300

Note 1: Some manufacturers claim that minimal or no capacitance is required for correct regulator operation. However, in all cases, a minimum of a 1.0 µF ceramic, low ESR capacitor at the input and output of these devices should be used. The manufacturer's datasheets should always be referred to when selecting capacitors for these devices and the typical recommended values, types and dielectrics adhered to.

2: A "soft-start" regulator with excellent noise and load step regulation will be needed to satisfy the XVdd supply requirements. 1% resistors should be used to define the nominal output voltage. If 5% resistors are used, the nominal XVdd voltage must be reduced accordingly to ensure that the recommended voltage range is adhered to.

11.4.1   SINGLE SUPPLY OPERATION

When designing a PCB for an application using a single LDO, extra care should be taken to ensure short, low inductance traces between the supply and the touch controller supply input pins. Ideally, tracking for the individual supplies should be arranged in a star configuration, with the LDO at the junction of the star. This will ensure that supply current variations or noise in one supply rail will have minimum effect on the other supplies. In applications where a ground plane is not practical, this same star layout should also apply to the power supply ground returns.

Only regulators with a 300 mA or greater rating can be used in a single-supply design.

Refer to the following application note for more information on routing with a single LDO:

• Application Note: MXTAN0208 – *Design Guide for PCB Layouts for maXTouch Touch Controllers*

11.4.2   MULTIPLE VOLTAGE REGULATOR SUPPLY

The AVdd supply stability is critical for the device because this supply interacts directly with the analog front end. If noise problems exist when using a single LDO regulator, Microchip recommends that AVdd is supplied by a regulator that is separate from the digital supply and high voltage regulators. This reduces the amount of noise injected into the sensitive, low signal level parts of the design.

11.5   Crystal Oscillator

> **NOTE**   The oscillator is not needed in I^2C mode.

The internal 16 MHz oscillator must be used when the device is operating in USB mode. An external crystal with a minimum accuracy of 100 ppm must be used.

The crystal placement is critical to the performance of the design. The connecting leads between the device and the crystal should be as short as possible. These tracks, together with the crystal itself, should be placed above a suitable ground plane. It is also important that no other signal tracks are placed close to, or under, these tracks. The crystal input pins are at a relatively high impedance and cross-talk from other signals will seriously affect oscillator stability and accuracy. The crystal case should also be connected to ground if possible.

If an external oscillator module is used, care still needs to be taken when tracking to the device. The clock signal should be kept as short as possible, with a solid ground return underneath the clock output.

11.6   Analog I/O

In general, tracking for the analog I/O signals from the device should be kept as short as possible. These normally go to a connector which interfaces directly to the touchscreen.

Ensure that adequate ground-planes are used. An analog ground plane should be used in addition to a digital one. Care should be taken to ensure that both ground planes are kept separate and are connected together only at the point of entry for the power to the PCB. This is usually at the input connector.

11.7   Component Placement and Tracking

It is important to orient all devices so that the tracking for important signals (such as power and clocks) are kept as short as possible.

11.7.1   DIGITAL SIGNALS

In general, when tracking digital signals, it is advisable to avoid sharp directional changes on sensitive signal tracks (such as analog I/O) and any clock or crystal tracking.

A good ground return path for all signals should be provided, where possible, to ensure that there are no discontinuities.

11.8   EMC and Other Observations

The following recommendations are not mandatory, but may help in situations where particularly difficult EMC or other problems are present:

• A small common mode choke is recommended on the differential USB data pair. This should be placed directly at the USB connector, between the connector and the relevant pins. Tracking lengths for the USB data pair should be kept as short as possible.

- Try to keep as many signals as possible on the inside layers of the board. If suitable ground flood fills are used on the top and bottom layers, these will provide a good level of screening for noisy signals, both into and out of the PCB.
- Ensure that the on-board regulators have sufficient tracking around and underneath the devices to act as a heatsink. This heatsink will normally be connected to the 0 V or ground supply pin. Increasing the width of the copper tracking to any of the device pins will aid in removing heat. There should be no solder mask over the copper track underneath the body of the regulators.
- Ensure that the decoupling capacitors, especially high capacity ceramic type, have the requisite low ESR, ESL and good stability/temperature properties. Refer to the regulator manufacturer's datasheet for more information.

12.0 GETTING STARTED WITH MXT1664T3

12.1 Establishing Contact

12.1.1 COMMUNICATION WITH THE HOST

The host can use any of the following interfaces to communicate with the device (See Section 7.0 "Host Communications"):

- I^2C interface (see Section 8.0 "I2C Communications")
- HID-I^2C interface (see Section 9.0 "HID-I^2C Communications")
- USB interface (see Section 10.0 "USB Communications")

12.1.2 POWER-UP SEQUENCE

On power-up, the $\overline{CHG}$ line goes low to indicate that there is new data to be read from the device. If the $\overline{CHG}$ line does not go low, there is a problem with the device.

Once the $\overline{CHG}$ line goes low, the host should attempt to read the first 7 bytes of memory from location 0x00 to establish that the device is present and running following power-up.

A checksum check is performed on the configuration settings held in the non-volatile memory. If the checksum does not match a stored copy of the last checksum, then this indicates that the settings have become corrupted. The host should write a correct configuration to the device if the read checksum does not match the expected checksum, or if the configuration error bit in the message data from the Command Processor T6 object is set.

12.2 Using the Object Protocol

The device has an object-based protocol that is used to communicate with the device. Typical communication includes configuring the device, sending commands to the device, and receiving messages from the device.

The host must perform the following initialization so that it can communicate with the device:

1. Read the start positions of all the objects in the device from the Object Table and build up a list of these addresses.
2. Use the Object Table to calculate the report IDs so that messages from the device can be correctly interpreted.

12.2.1 CLASSES OF OBJECTS

The mXT1664T3 contains the following classes of objects:

- **Debug objects** – provide a raw data output method for development and testing.
- **General objects** – required for global configuration, transmitting messages and receiving commands.
- **Touch objects** – operate on measured signals from the touch sensor and report touch data.
- **Signal processing objects** – process data from other objects (typically signal filtering operations).
- **Support objects** – provide additional functionality on the device.

12.2.2 OBJECT INSTANCES

TABLE 12-1: OBJECTS ON THE MXT1664T3

Object	Description	Number of Instances	Usage
Debug Objects			
Diagnostic Debug T37	Allows access to diagnostic debug data to aid development.	1	Debug commands only. No configuration/tuning necessary. Not for use in production.
General Objects			
Message Processor T5	Handles the transmission of messages. This object holds a message in its memory space for the host to read.	1	No configuration necessary.
Command Processor T6	Performs a command when written to. Commands include reset, calibrate and backup settings.	1	No configuration necessary.

TABLE 12-1:   OBJECTS ON THE MXT1664T3 (CONTINUED)

Object	Description	Number of Instances	Usage
Power Configuration T7	Controls the sleep mode of the device. Power consumption can be lowered by controlling the acquisition frequency and the sleep time between acquisitions.	1	Must be configured before use.
Acquisition Configuration T8	Controls how the device takes each capacitive measurement.	1	Must be configured before use.
Touch Objects			
Multiple Touch Touchscreen T100	Creates a Touchscreen that supports the tracking of more than one touch.	1	Enable and configure as required.
Signal Processing Objects			
Grip Suppression T40	Suppresses false detections caused, for example, by the user gripping the edge of a touchscreen.	1	Enable and configure as required.
Touch Suppression T42	Suppresses false detections caused by unintentional large touches by the user.	1	Enable and configure as required.
Passive Stylus T47	Processes passive stylus input.	1	Enable and configure as required.
Shieldless T56	Allows a sensor to use true single-layer co-planar construction.	1	Enable and configure as required.
Lens Bending T65	Compensates for lens deformation (lens bending) by attempting to eliminate the disturbance signal from the reported deltas.	3	Enable and configure as required.
Noise Suppression T72	Performs various noise reduction techniques during sensor signal acquisition.	1	Enable and configure as required.
Glove Detection T78	Allows for the reporting of glove touches.	1	Enable and configure as required.
Retransmission Compensation T80	Limits the negative effects on touch signals caused by poor device coupling to ground or moisture on the sensor.	1	Enable and configure as required.
Self Capacitance Noise Suppression T108	Suppresses the effects of external noise within the context of self capacitance touch measurements.	1	Enable and configure as required.
Self Capacitance Grip Suppression T112	Allows touches to be reported from the self capacitance measurements while the device is being gripped.	1	Enable and configure as required.
Support Objects			
Communications Configuration T18	Configures additional communications behavior for the device.	1	Check and configure as necessary.
GPIO Configuration T19	Allows the host controller to configure and use the general purpose I/O pins on the device.	1	Enable and configure as required.
Self Test T25	Configures and performs self-test routines to find faults on a touch sensor.	1	Configure as required for pin test commands.
User Data T38	Provides a data storage area for user data.	1	Configure as required.
Digitizer HID Configuration T43	Configures the Digitizer HID interface and the Descriptors associated with it.	1	Enable and configure as required.
Message Count T44	Provides a count of pending messages.	1	Read-only object.
CTE Configuration T46	Controls the capacitive touch engine for the device.	1	Must be configured.

TABLE 12-1:   OBJECTS ON THE MXT1664T3 (CONTINUED)

Object	Description	Number of Instances	Usage
Timer T61	Provides control of a timer.	6	Enable and configure as required.
Serial Data Command T68	Provides an interface for the host driver to deliver various data sets to the device.	1	Enable and configure as required.
Dynamic Configuration Controller T70	Allows rules to be defined that respond to system events.	20	Enable and configure as required.
Dynamic Configuration Container T71	Allows the storage of user configuration on the device that can be selected at runtime based on rules defined in the Dynamic Configuration Controller T70 object.	1	Configure if Dynamic Configuration Controller T70 is in use.
CTE Scan Configuration T77	Configures enhanced X line scanning features.	1	Enable and configure as required.
Touch Event Trigger T79	Configures touch triggers for use with the event handler.	3	Enable and configure as required.
Auxiliary Touch Configuration T104	Allows the setting of self capacitance gain and thresholds for a particular measurement to generate auxiliary touch data for use by other objects.	1	Enable and configure if using self capacitance measurements
Self Capacitance Global Configuration T109	Provides configuration for self capacitance measurements employed on the device.	1	Check and configure as required (if using self capacitance measurements).
Self Capacitance Tuning Parameters T110	Provides configuration space for a generic set of settings for self capacitance measurements.	6	Use under the guidance of Microchip field engineers only.
Self Capacitance Configuration T111	Provides configuration for self capacitance measurements employed on the device.	2	Check and configure as required (if using self capacitance measurements).
Self Capacitance Measurement Configuration T113	Configures self capacitance measurements to generate data for use by other objects.	1	Enable and configure as required.

12.2.3   CONFIGURING AND TUNING THE DEVICE

The objects are designed such that a default value of zero in their fields is a "safe" value that typically disables functionality. The objects must be configured before use and the settings written to the non-volatile memory using the Command Processor T6 object.

Perform the following actions for each object:

1. Enable the object, if the object requires it.
2. Configure the fields in the object, as required.
3. Enable reporting, if the object supports messages, to receive messages from the object.

12.3   Writing to the Device

The following mechanisms can be used to write to the device:

- Using an I^{2}C write operation (see Section 8.2 "Writing To the Device").
- Using the USB Generic HID write operation (see Section 10.4.1.2 "Writing To the Device").
- Using the Generic HID-I^{2}C write operation (see Section 9.5.1.2 "Writing To the Device").

Communication with the device is achieved by writing to the appropriate object:

- To send a command to the device, an appropriate command is written to the Command Processor T6 object.

- To configure the device, a configuration parameter is written to the appropriate object. For example, writing to the Power Configuration T7 configures the power consumption for the device and writing to the touchscreen Multiple Touch Touchscreen T100 object sets up the touchscreen. Some objects are optional and need to be enabled before use.

IMPORTANT!	When the host issues any command within an object that results in a flash write to the device Non-Volatile Memory (NVM), that object should have its CTRL RPTEN bit set to 1, if it has one. This ensures that a message from the object writing to the NVM is generated at the completion of the process and an assertion of the CHG line is executed.
	The host must also ensure that the assertion of the CHG line refers to the expected object report ID before asserting the RESET line to perform a reset. Failure to follow this guidance may result in a corruption of device configuration area and the generation of a CFGERR.

12.4 Reading from the Device

Status information is stored in the Message Processor T5 object. This object can be read to receive any status information from the device. The following mechanisms provide an interrupt-style interface for reading messages in the Message Processor T5 object:

- The CHG line is asserted whenever a new message is available in the Message Processor T5 object (see Section 8.6 "CHG Line"). See Section 8.4 "Reading From the Device" for information on the format of the I^2C read operation.
- When using the USB interface, the interface provides an interrupt-driven interface that sends the messages automatically (see Section 10.4.1.3 "Reading From the Device").
- When using the HID-I^2C interface, the interface provides an interrupt-driven interface that sends the messages automatically (see Section 9.5.1.3 "Reading From the Device")

Note that the host should always wait to be notified of messages. The host should not poll the device for messages.

13.0   DEBUGGING AND TUNING

13.1   SPI Debug Interface

The SPI Debug Interface is used for tuning and debugging when running the system and allows the development engineer to use Microchip maXTouch Studio to read the real-time raw data. This uses the low-level debug port.

The SPI Debug Interface consists of the $\overline{\text{DBG\_SS}}$, DBG_CLK, and DBG_DATA lines. It is recommended that these pins are routed to test points on all designs such that they can be connected to external hardware during system development. These lines should not be connected to power or GND. See Section 2.5.9 "SPI Debug Interface" for more details.

The SPI Debug Interface is enabled by the Command Processor T6 object and by default will be off.

NOTE	The touch controller will take care of the pin configuration. When the $\overline{\text{DBG\_SS}}$, DBG_CLK, and DBG_DATA lines are in use for debugging, any alternative function for the pins cannot be used.

13.2   USB Debug Interface

If the USB interface is in use on the device, this can be used as the hardware debug interface instead of the SPI Debug Interface.

The USB hardware debugging interface is enabled by the Command Processor T6 object and by default will be off.

13.3   Object-based Protocol

The device provides a mechanism for obtaining debug data for development and testing purposes by reading data from the Diagnostic Debug T37 object.

NOTE	The Diagnostic Debug T37 object is of most use for simple tuning purposes. When debugging a design, it is preferable to use the SPI Debug Interface, as this will have a much higher bandwidth and can provide real-time data.

13.4   Self Test

There is a Self Test T25 object that runs self-test routines in the device to find hardware faults on the sense lines and the electrodes. This object also performs an initial pin fault test on power-up to ensure that there is no pin short (X-to-Y, or sense pin to power or GND) before the high-voltage supply is enabled inside the chip. A high-voltage short on the sense lines could damage the device.

14.0 SPECIFICATIONS

14.1 Absolute Maximum Specifications

Vdd	3.6 V
VddIO	3.6 V
AVdd	3.6 V
XVdd (external)	10 V
Maximum continuous combined pin current, all GPIO*n* pins	80 mA
Voltage forced onto any pin	−0.3 V to Vdd/VddIO/AVdd + 0.3 V
Configuration parameters maximum writes	10,000
Maximum junction temperature	125°C

> **CAUTION!** Stresses beyond those listed under *Absolute Maximum Specifications* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum specification conditions for extended periods may affect device reliability.

14.2 Recommended Operating Conditions

Operating temperature	−40°C to +85°C
Storage temperature	−60°C to +150°C
Vdd	3.3V ±5%
VddIO	1.8V to 3.3V ±5% (I^2C mode) 3.3 V ±5% (USB mode)
AVdd	3.3V ±5%
External XVdd – Static	6.1V to 9.5V (8.5 V recommended)
XVdd – With Voltage Booster enabled	6.2V Nominal, Band Gap Referenced 7.4V Nominal, Band Gap Referenced 8.5V Nominal, Band Gap Referenced (Recommended) 9.21V Nominal, Band Gap Referenced
Temperature slew rate	10°C/min

14.2.1   DC CHARACTERISTICS

14.2.1.1   Analog Voltage Supply – AVdd

Parameter	Min	Typ	Max	Units	Notes
AVdd					
Operating limits	3.14	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage must not rise in less than 92 µs

14.2.1.2   Digital Voltage Supply – VddIO, Vdd

Parameter	Min	Typ	Max	Units	Notes
VddIO					
Operating limits, I^{2}C	1.71	3.3	3.47	V	I^{2}C
Operating limits, USB	3.14	3.3	3.47	V	USB
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage must not rise in less than 92 µs
Vdd					
Operating limits	3.14	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage must not rise in less than 92 µs
Supply Fall Rate	–	–	0.05	V/µs	For example, for a 3.3 V rail, the voltage must not fall in less than 66 µs

14.2.1.3   XVdd Voltage Supply – XVdd

Parameter	Min	Typ	Max	Units	Notes
XVdd					
Operating limits	6.1	8.5	9.5	V	External XVdd supply
Supply Rise Rate	–	–	0.1	V/µs	For example, for a 10 V rail, the voltage must not rise in less than 85 µs

14.2.2   POWER SUPPLY RIPPLE AND NOISE

Parameter	Min	Typ	Max	Units	Notes
Vdd	–	–	±50	mV	Across frequency range 1 Hz to 1 MHz
AVdd	–	–	±40	mV	Across frequency range 1 Hz to 1 MHz, with Noise Suppression enabled

14.3   Test Configuration

The configuration values listed below were used in the reference unit to validate the interfaces and derive the characterization data provided in the following sections.

TABLE 14-1:   TEST CONFIGURATION

Object/Parameter	Description/Setting
Acquisition Configuration T8	
CHRGTIME	50
MEASALLOW	11
MEASIDLEDEF	2
MEASACTVDEF	2
GPIO Configuration T19	Object Enabled
Self Test T25	Object Enabled
CTE Configuration T46	
IDLESYNCSPERX	16
ACTVSYNCSPERX	16
Passive Stylus T47	Object Enabled
Shieldless T56	Object Enabled
INTTIME	29
Lens Bending T65	Object Enabled
Noise Suppression T72	Object Enabled
CTE Scan Configuration T77	Object Enabled
Glove Detection T78	Object Enabled
Retransmission Compensation T80	Object Enabled
Multiple Touch Touchscreen T100	Object Enabled
XSIZE	32
YSIZE	52
Auxiliary Touch Configuration T104	Object Enabled
Self Capacitance Noise Suppression T108	Object Enabled
Self Capacitance Configuration T111 Instance 0	
INTTIME	45
IDLESYNCSPERL	24
ACTVSYNCSPERL	24
Self Capacitance Configuration T111 Instance 1	
INTTIME	55
IDLESYNCSPERL	32
ACTVSYNCSPERL	32

14.4 Current Consumption – I^{2}C Interface

> **NOTE** The characterization charts show typical values based on the configuration in . Actual power consumption in the user's application will depend on the circumstances of that particular project and will vary from that shown here. Further tuning will be required to achieve an optimal performance.

14.4.1   ANALOG SUPPLY

Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	5 Touches (mA)	10 Touches (mA)	15 Touches (mA)
Free-run	16.82	15.59	17.84	18.42	11.28
10	6.23	5.88	14.94	14.90	9.90
16	3.99	3.91	9.80	9.73	9.76
32	2.11	2.49	5.74	4.65	6.59
64	1.14	1.70	3.03	2.33	2.91
128	0.61	0.80	1.45	1.12	1.99
254	0.39	0.70	0.69	0.58	1.03
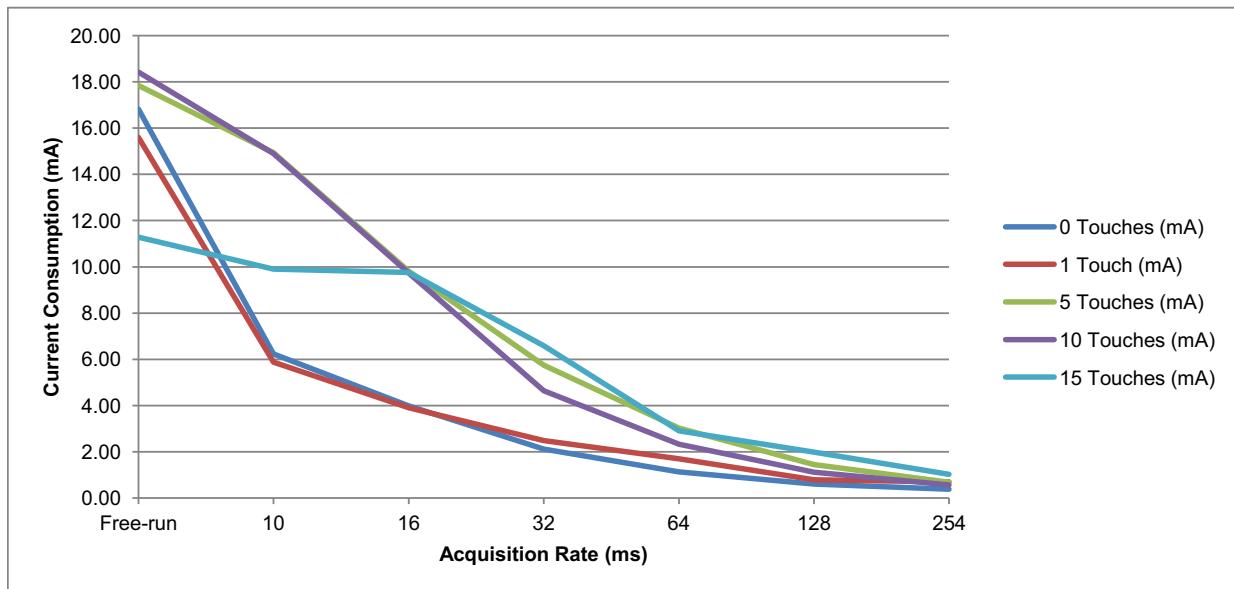
14.4.2 DIGITAL SUPPLY

14.4.2.1 Vdd

Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	5 Touches (mA)	10 Touches (mA)	15 Touches (mA)
Free-run	10.91	12.27	15.74	16.50	14.48
10	4.51	4.68	13.60	13.75	14.47
16	2.92	3.22	8.57	8.87	12.19
32	1.72	2.02	6.69	4.12	7.87
64	1.18	1.51	2.32	2.31	3.86
128	0.69	0.98	2.68	0.91	4.92
254	0.66	0.75	0.70	0.77	2.77
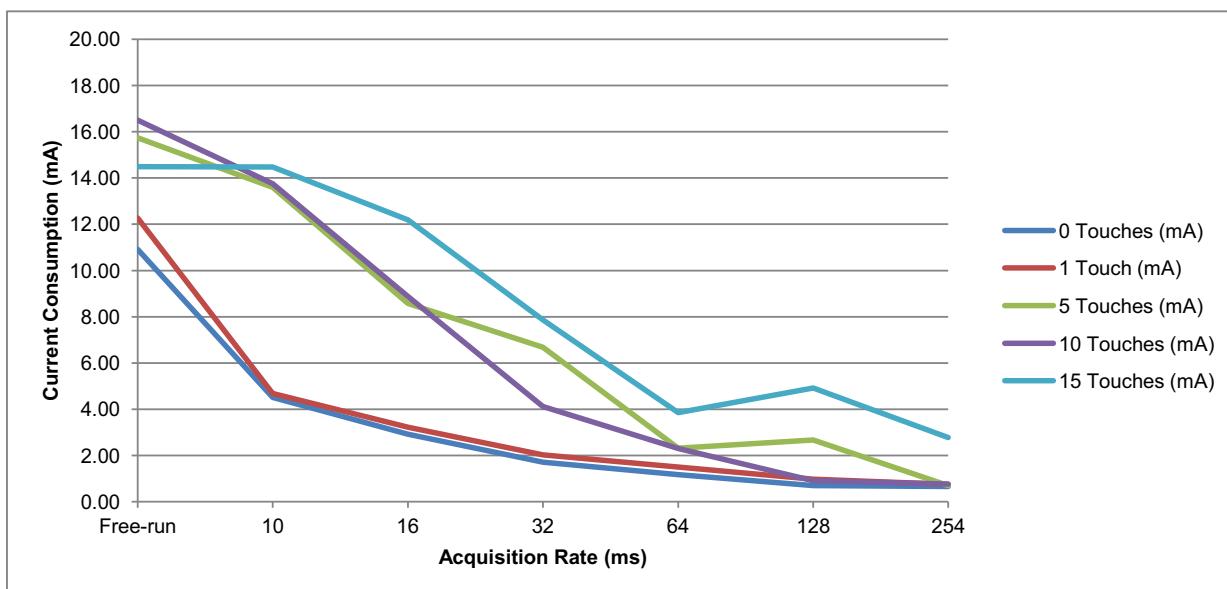
14.4.2.2   VddIO

Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	5 Touches (mA)	10 Touches (mA)	15 Touches (mA)
Free-run	0.15	1.18	1.16	1.15	1.16
10	0.17	1.21	1.17	1.16	1.16
16	0.17	1.19	1.18	1.17	1.17
32	0.18	1.19	1.20	1.18	1.18
64	0.19	1.21	1.20	1.19	1.19
128	0.19	1.21	1.21	1.19	1.19
254	0.18	1.20	1.20	1.20	1.19
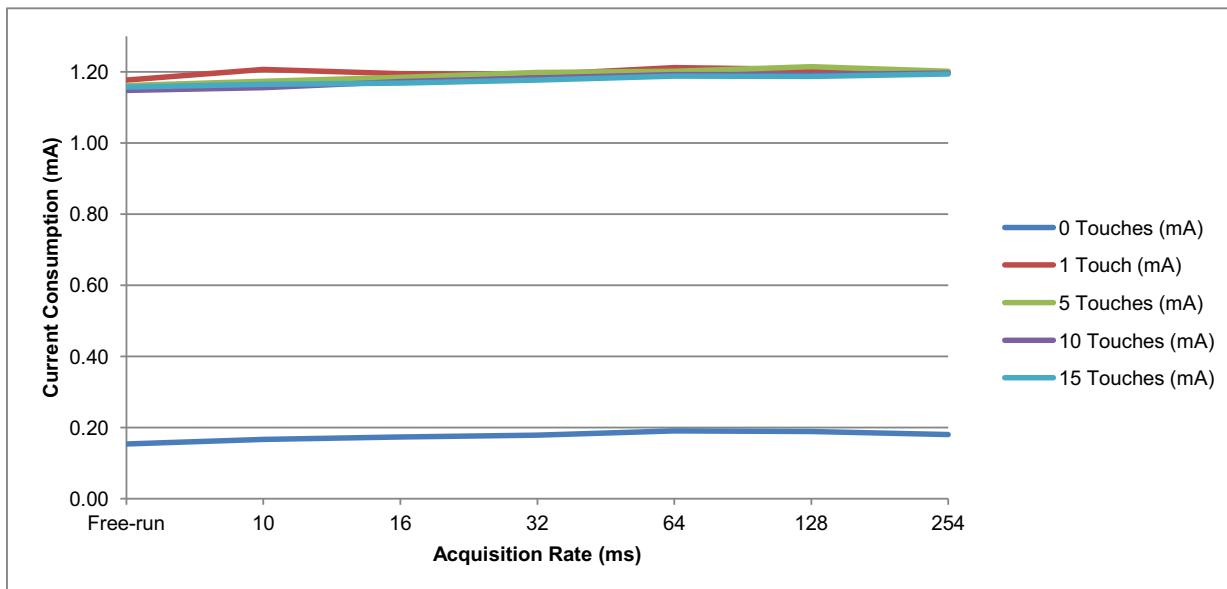
14.4.3   XVDD SUPPLY

Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	5 Touches (mA)	10 Touches (mA)	15 Touches (mA)
Free-run	0.63	0.63	0.77	0.77	0.70
10	0.25	0.24	0.67	0.64	0.70
16	0.16	0.17	0.40	0.40	0.60
32	0.09	0.11	0.25	0.18	0.49
64	0.05	0.06	0.07	0.09	0.17
128	0.02	0.03	0.03	0.06	0.28
254	0.02	0.03	0.02	0.02	0.12
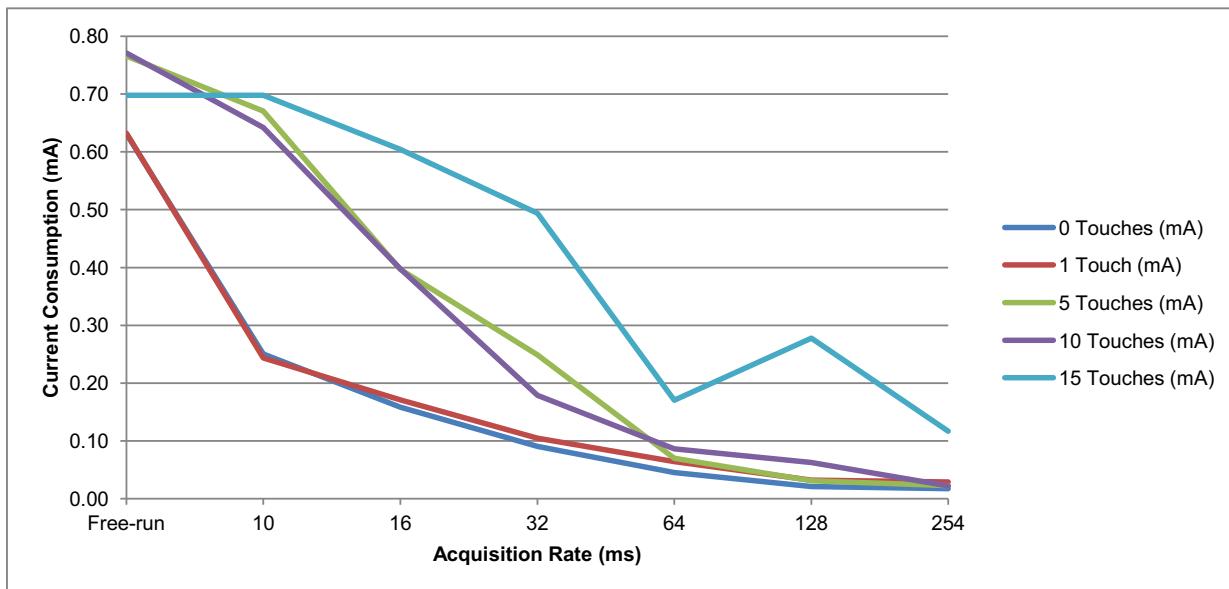
14.5 Current Consumption – USB Interface

NOTE The characterization charts show typical values based on the configuration in Table 14-1 on page 71. Actual power consumption in the user's application will depend on the circumstances of that particular project and will vary from that shown here. Further tuning will be required to achieve an optimal performance.

14.5.1 ANALOG SUPPLY

Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	5 Touches (mA)	10 Touches (mA)	15 Touches (mA)
Free-run	17.13	15.78	18.43	20.43	11.22
10	7.05	6.45	15.48	15.14	9.45
16	4.95	4.98	9.95	9.93	9.99
32	3.17	3.57	5.72	5.48	6.97
64	2.22	2.85	3.31	3.45	5.38
128	1.86	2.03	2.68	2.21	3.91
254	1.65	1.57	1.58	1.78	2.86
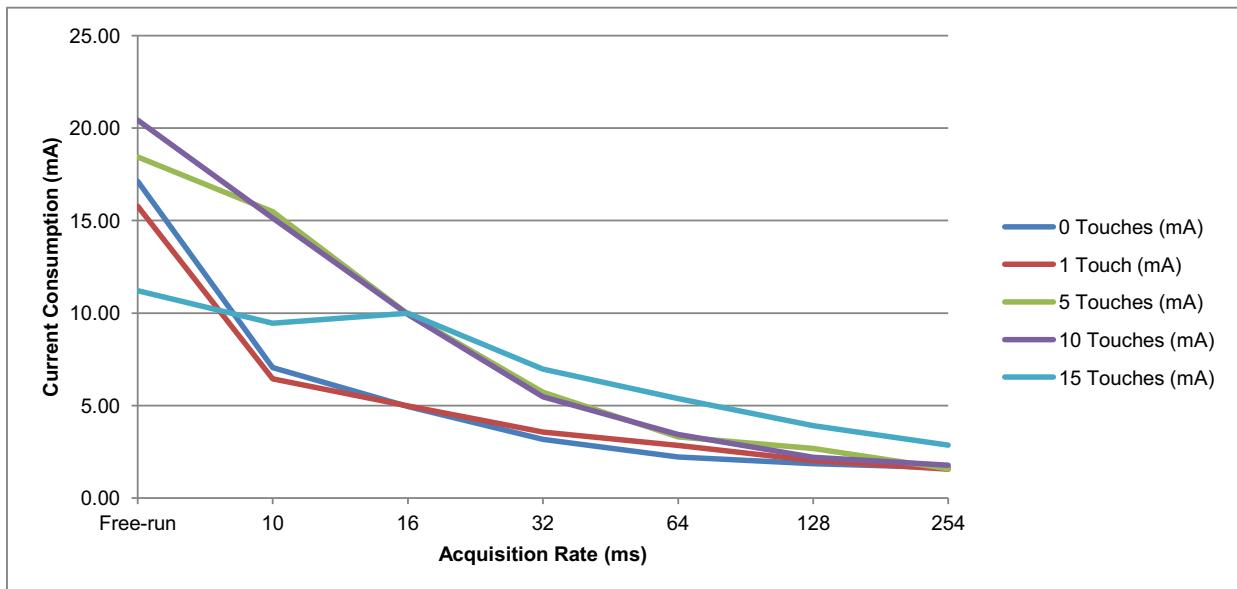
14.5.2   DIGITAL SUPPLY

14.5.2.1   Vdd

Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	5 Touches (mA)	10 Touches (mA)	15 Touches (mA)
Free-run	11.57	12.96	15.23	18.09	15.12
10	8.29	8.72	14.51	14.68	14.97
16	7.56	7.80	11.08	11.46	14.69
32	6.84	7.20	8.62	8.77	13.12
64	6.56	6.81	7.74	7.37	10.49
128	6.40	6.49	6.66	6.93	8.56
254	6.30	6.34	6.45	6.59	8.12
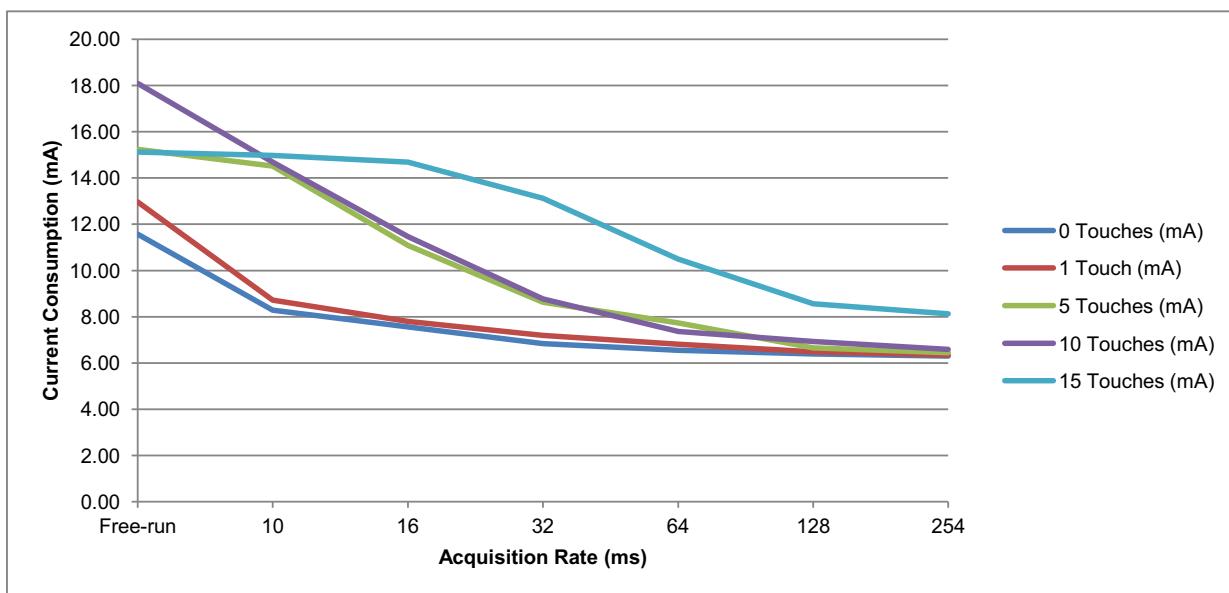
14.5.2.2   VddIO

Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	5 Touches (mA)	10 Touches (mA)	15 Touches (mA)
Free-run	1.97	2.96	2.97	2.97	2.96
10	1.97	2.96	2.96	2.96	2.96
16	1.96	2.96	2.96	2.96	2.96
32	1.96	2.95	2.96	2.96	2.96
64	1.96	2.95	2.95	2.95	2.95
128	1.96	2.94	2.94	2.95	2.95
254	1.96	2.94	2.94	2.94	2.94
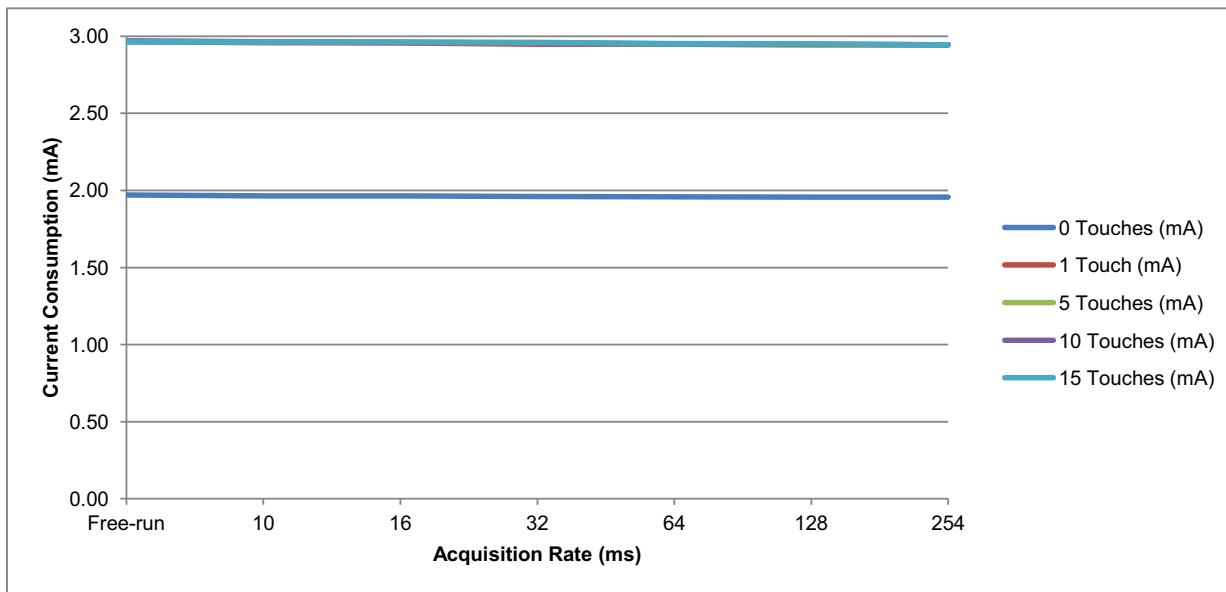
14.5.3   XVDD SUPPLY

Acquisition Rate (ms)	0 Touches (mA)	1 Touch (mA)	5 Touches (mA)	10 Touches (mA)	15 Touches (mA)
Free-run	0.63	0.63	0.75	0.79	0.69
10	0.61	0.62	0.73	0.73	0.68
16	0.61	0.61	0.68	0.68	0.68
32	0.60	0.61	0.65	0.64	0.66
64	0.60	0.61	0.62	0.62	0.64
128	0.60	0.60	0.61	0.61	0.63
254	0.60	0.60	0.60	0.61	0.61
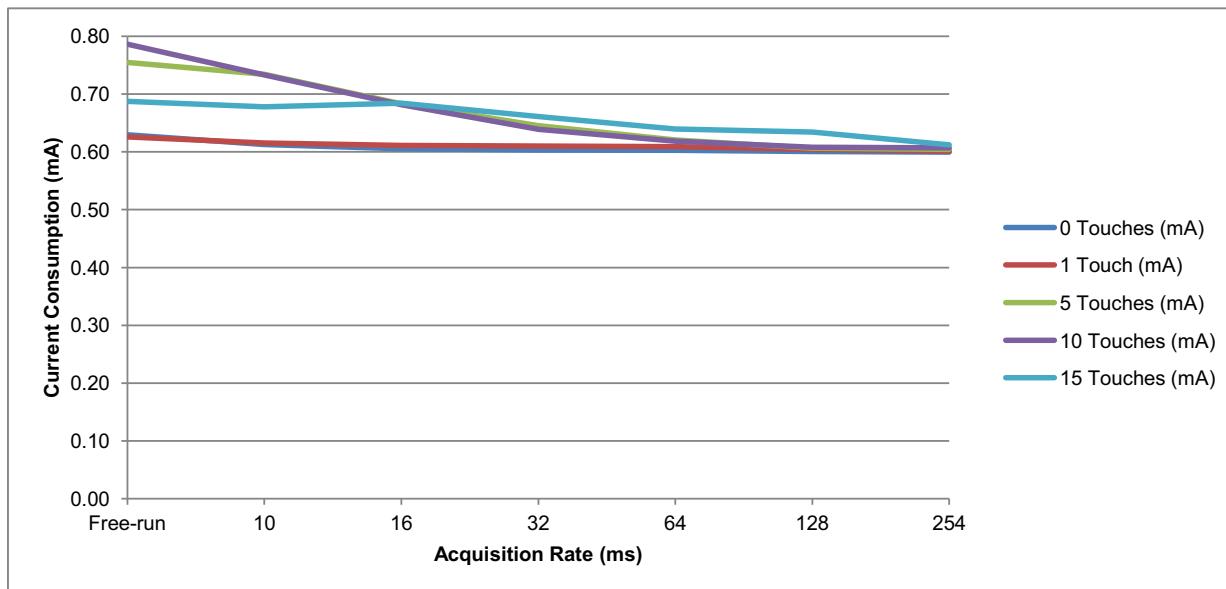
14.6   Deep Sleep Current

$T_A = 25°C$

Parameter	Min	Typ	Max	Units	Notes
Deep Sleep Current	–	360	–	µA	Vdd = 3.3 V, AVdd = 3.3 V
Deep Sleep Power	–	1188	–	µW	Vdd = 3.3 V, AVdd = 3.3 V

14.7   Timing Specifications

> **NOTE**   The figures below show typical values based on the test configuration. Actual timings in the user's
> application will depend on the circumstances of that particular project and will vary from those shown
> below. Further tuning will be required to achieve an optimal performance.

14.7.1   TOUCH LATENCY
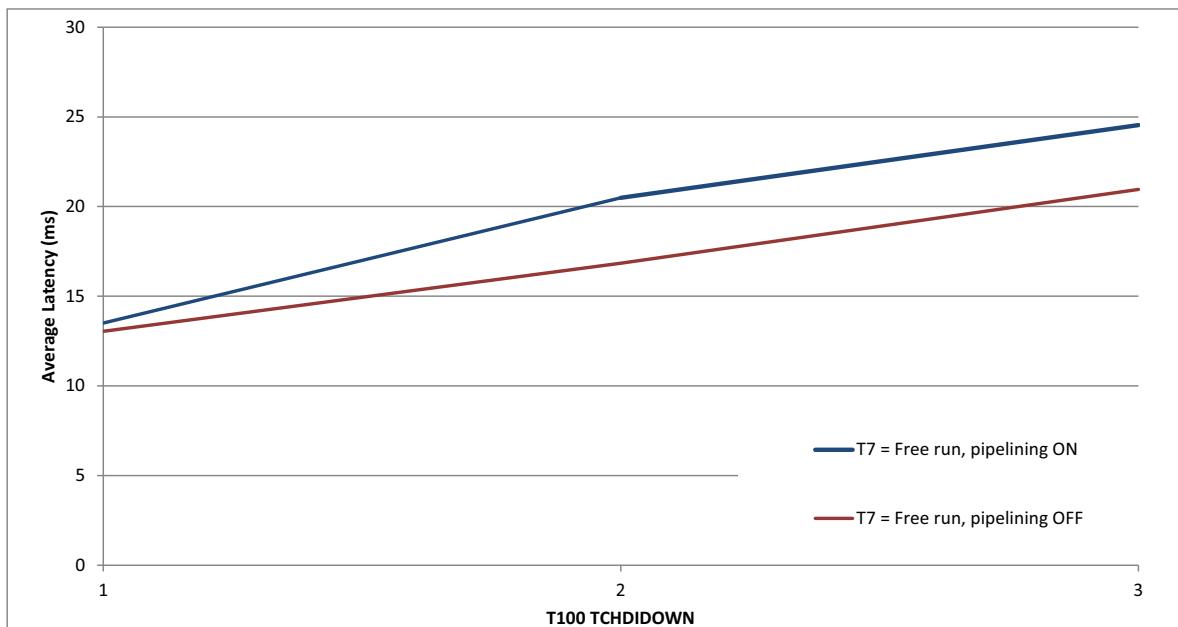

> **NOTE**   T7 Idle pipelining OFF during latency testing

14.7.2   SPEED
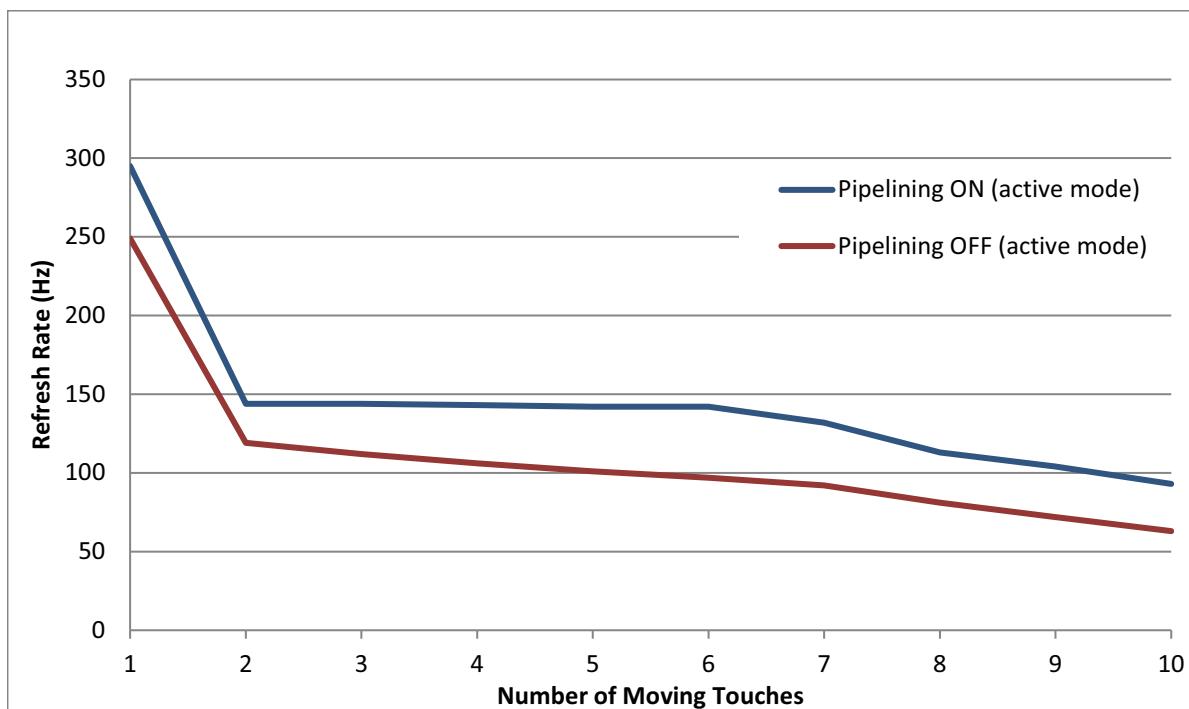
14.7.3   RESET TIMINGS

Parameter	Min	Typ	Max	Units	Notes
Power on to $\overline{CHG}$ line low	–	79	–	ms	Vdd supply for POR VddIO supply for external reset
Hardware reset to $\overline{CHG}$ line low	–	81	–	ms	
Software reset to $\overline{CHG}$ line low	–	104	–	ms	

Note 1: Any $\overline{CHG}$ line activity before the power-on or reset period has expired should be ignored by the host. Operation of this signal cannot be guaranteed before the power-on/reset periods have expired.

**2:** The mXT1664T3 meets the requirements of Microsoft Windows 8.x and later versions.

14.8   Touchscreen Sensor Characteristics

Parameter	Description	
Cm	Mutual capacitance	Typical value is between 0.15 pF and 10 pF on a single node.
Cpx	Mutual capacitance load to X	Microchip recommends a maximum load of 300 pF on each X or Y line. [1]
Cpy	Mutual capacitance load to Y	
Cpx	Self capacitance load to X	Microchip recommends a maximum load of 100 pF on each X or Y line. [1]
Cpy	Self capacitance load to Y	
∆Cpx	Self capacitance imbalance on X	Nominal value is 20.9 pF. Value increases by 1 pF for every 45 pF reduction in Cpx/Cpy (based on 100 pF load)
∆Cpy	Self capacitance imbalance on Y	
Cpds0	Self capacitance load to Driven Shield	Microchip recommends a maximum load of 100 pF on the Driven Shield line. [1]

Note 1: Please contact your Microchip representative for advice if you intend to use higher values.

14.9 Input/Output Characteristics

Parameter	Description	Min	Typ	Max	Units	Notes
Input (All input pins connected to the VddIO power rail)						
Vil	Low input logic level	−0.3	–	0.3 × VddIO	V	VddIO = 1.8V to Vdd
Vih	High input logic level	0.7 × VddIO	–	VddIO	V	VddIO = 1.8V to Vdd
Iil	Input leakage current	–	–	1	µA	Pull-up resistors disabled
RESET	Internal pull-up resistor	20	40	60	kΩ	
GPIOs	Internal pull-up/pull-down resistor					
Output (All output pins connected to the VddIO power rail)						
Vol	Low output voltage	0	–	0.2 × VddIO	V	VddIO = 1.8V to Vdd Iol = −2 mA
Voh	High output voltage	0.8 × VddIO	–	VddIO	V	VddIO = 1.8V to Vdd Ioh = 2 mA

14.10 I^{2}C Specification

Parameter	Value
Addresses	0x4A or 0x4B
I^{2}C specification [1]	Revision 6.0
Maximum bus speed (SCL) [2]	1 MHz
Standard Mode [3]	100 kHz
Fast Mode [3]	400 kHz
Fast Mode Plus [3]	1 MHz
High Speed Mode [3]	3.4 MHz

Note **1:** More detailed information on I^{2}C operation is available from www.nxp.com/documents/user_manual/UM10204.pdf.

2: In systems with heavily laden I^{2}C lines, even with minimum pull-up resistor values, bus speed may be limited by capacitive loading to less than the theoretical maximum.

3: The values of pull-up resistors should be chosen to ensure SCL and SDA rise and fall times meet the I^{2}C specification. The value required will depend on the amount of capacitance loading on the lines.

14.11 HID-I^{2}C Specification

Parameter	Value
Vendor ID	0x03EB (Microchip)
Product ID	0x215D (mXT1664T3)
HID-I^{2}C specification	1.0

14.12 USB Specification

Parameter	Value
Endpoint Addresses	0x81 (Endpoint 1) 0x02 (Endpoint 2) 0x83 (Endpoint 3)
Maximum bus speed	12 Mbps
Vendor ID	0x03EB (Microchip)
Product ID	0x215D (mXT1664T3)
USB specification	USB 2.0 HID specification 1.11 with amendments for multitouch digitizers

14.13 Touch Accuracy and Repeatability

Parameter	Min	Typ	Max	Units	Notes
Linearity (touch only; 5.4 mm electrode pitch)	–	±1	–	mm	8 mm or greater finger
Linearity (touch only; 4.2 mm electrode pitch)	–	±0.5	–	mm	4 mm or greater finger
Accuracy	–	±1	–	mm	
Accuracy at edge	–	±2	–	mm	
Repeatability	–	±0.25	–	%	X axis with 12-bit resolution

14.14 Thermal Packaging

14.14.1 THERMAL DATA

Parameter	Description	Typ	Unit	Condition	Package
θ_{JA}	Junction to ambient thermal resistance	42.1	°C/W	Still air	136-ball UFBGA 7 × 7 × 0.6 mm
θ_{JC}	Junction to case thermal resistance	6.2	°C/W		136-ball UFBGA 7 × 7 × 0.6 mm
θ_{JA}	Junction to ambient thermal resistance	28.2	°C/W	Still air	162-ball UFBGA 10 × 5 × 0.6 mm
θ_{JC}	Junction to case thermal resistance	2.4	°C/W		162-ball UFBGA 10 × 5 × 0.6 mm

14.14.2 JUNCTION TEMPERATURE

The maximum junction temperature allowed on this device is 125°C.

The average junction temperature in °C (T_J) for this device can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA})$$

If a cooling device is required, use this equation:

$$T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$$

where:

- θ_{JA} = package thermal resistance, Junction to ambient (°C/W) (see Section 14.14.1 "Thermal Data")
- θ_{JC} = package thermal resistance, Junction to case thermal resistance (°C/W) (see Section 14.14.1 "Thermal Data")
- $\theta_{HEATSINK}$ = cooling device thermal resistance (°C/W), provided in the cooling device datasheet
- P_D = device power consumption (W)
- T_A is the ambient temperature (°C)

14.15 ESD Information

Parameter	Value	Reference standard
Human Body Model (HBM)	±2000 V	JEDEC JS–001
Charge Device Model (CDM)	±250 V	JEDEC JS–001

14.16 Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	150 – 200°C
Time Maintained Above 217°C	60 – 150 s
Time within 5°C of Actual Peak Temperature	30 s
Peak Temperature Range	260°C
Ramp down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max

14.17 Moisture Sensitivity Level (MSL)

MSL Rating	Package Type(s)	Peak Body Temperature	Specifications
MSL3	BGA	260°C	IPC/JEDEC J-STD-020

15.0 PACKAGING INFORMATION

15.1 Package Marking Information

15.1.1 136-BALL UFBGA
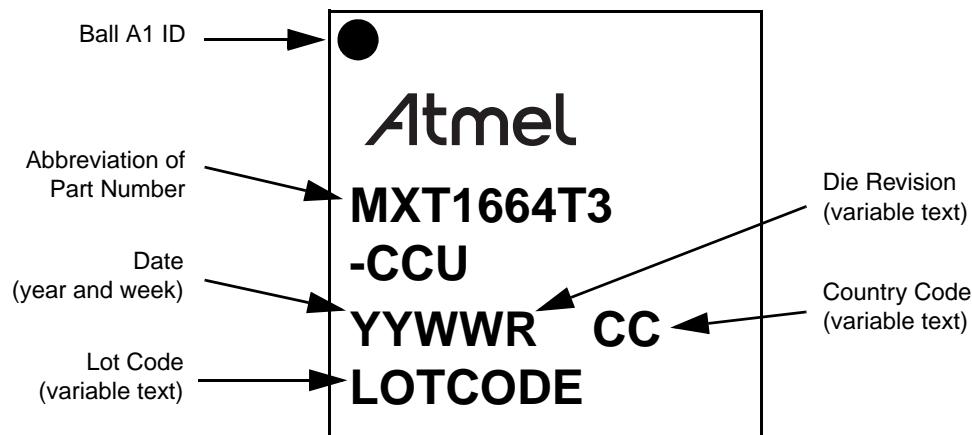
15.1.2 162-BALL UFBGA
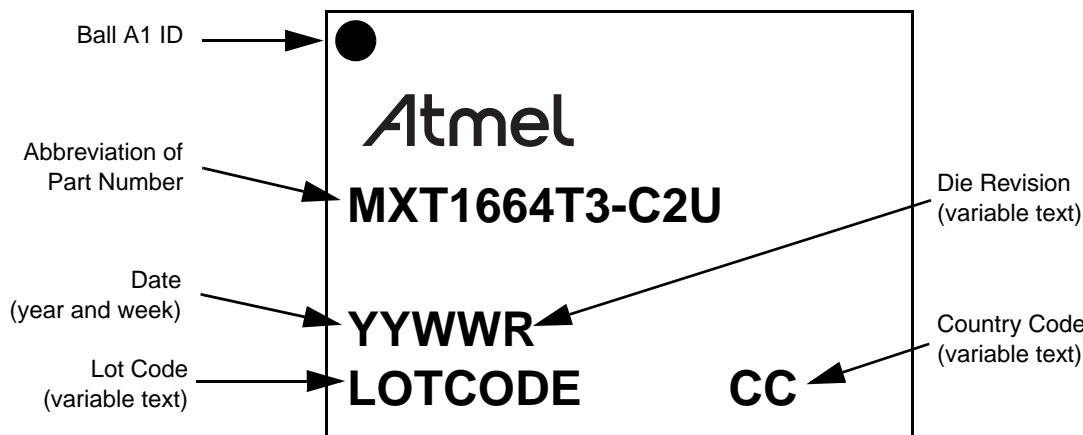
15.1.3 ORDERABLE PART NUMBERS

The product identification system for maXTouch devices is described in "Product Identification System". That section also lists example part numbers for the device.

15.2   Package Details

15.2.1   136-BALL UFBGA 7 × 7 × 0.6 MM

NOTE   For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

DRAWINGS NOT SCALED

PIN A1 CORNER

TOP VIEW

SIDE VIEW

SEATING PLANE

BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	0.600	3
A1	0.110	0.160	0.210	
E/D	7.00 / 7.00			
E1/D1	6.00 / 6.00			
ball width	0.220	-----	0.280	4
e	Ball pitch : 0.500			
M	Mold thickness : 0.250 ref			
S	Subst thickness : 0.136 ref			
aaa	Pack edge tolerance : 0.100			
bbb	Mold flatness : 0.100			
ddd	Coplanarity : 0.080			
ball diam	0.250			
n	136			

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-280, Variation UGCBA for proper dimensions, tolerances, datums, etc.
2. Array as seen from the bottom of the package.
3. Dimension A includes stand-off height A1, package body thickness, and lid height, but does not include attached features.
4. Dimension b is measured at the maximum ball diameter, parallel to primary datum C.

27/10/2014

	TITLE	GPC	DRAWING NO.	REV.
	7Y, 136-ball (13x13 3P Array + 7 Balls, + 3x3 1P Array), 0.5mm pitch, 7x7x0.6mm Ultra Thin Fine-Pitch Ball Grid Array Package (UFBGA)	CDK	7Y	C

## 15.2.2 162-BALL UFBGA 10 × 5 × 0.6 MM

NOTE For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

DRAWINGS NOT SCALED

TOP VIEW

SIDE VIEW

BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.488	0.546	0.600	3
A1	0.120	0.155	0.190	
E	9.90	10.00	10.10	
D	4.90	5.00	5.10	
E1	8.90	9.00	9.10	
D1	3.90	4.00	4.10	
ball width	0.250	-----	0.350	4
eD/eE	Ball pitch : 0.500			
aaa	Package edge tolerance : 0.100			
bbb	Mold flatness : 0.100			
ddd	Coplanarity : 0.080			
ball diam	0.250			
n	162			

Notes : 1. No JEDEC Drawing Reference.
2. Array as seen from the bottom of the package.
3. Dimension A includes stand-off height A1, package body thickness, and lid height, but does not include attached features.
4. Dimension b is measured at the maximum ball diameter, parallel to primary datum C.

02/13/2015

TITLE	GPC	DRAWING NO.	REV.
7M, 162-ball - 19x9 4P array (+ 2 balls), 0.5mm pitch, 10x5x0.6mm Ultra Thin Fine-Pitch Ball Grid Array Package (UFBGA)	CAK	7M	D

APPENDIX A: ASSOCIATED DOCUMENTS

NOTE	Some of the documents listed below are available under NDA only.

The following documents are available by contacting your Microchip representative:

Product Documentation

• Application Note: MXTAN0213 – *Interfacing with maXTouch Touchscreen Controllers*

Touchscreen design and PCB/FPCB layout guidelines

• Application Note: QTAN0054 – *Getting Started with maXTouch Touchscreen Designs*
• Application Note: MXTAN0208 – *Design Guide for PCB Layouts for maXTouch Touch Controllers*
• Application Note: QTAN0080 – *Touchscreens Sensor Design Guide*
• Application note: AN2683 – *Edge Wiring for Self Capacitance maXTouch Touchscreens*

Miscellaneous

• Application Note: QTAN0050 – *Using the maXTouch Debug Port*
• Application Note: QTAN0058 – *Rejecting Unintentional Touches with the maXTouch Touchscreen Controllers*

Tools

• *maXTouch Studio User Guide* (distributed as on-line help with maXTouch Studio)

APPENDIX B: REVISION HISTORY

Revision AX (January 2015)

Final edition for firmware revision 2.0 – Atmel Release version

Revision A (August 2018)

Reformatted edition for firmware revision 2.0 – Microchip Release version

This revision incorporates the following updates:

- Updated to Microchip datasheet format:
  - "Pin configuration" moved to start of datasheet
  - "To Our Valued Customers" added
  - Section 15.0 "Packaging Information" updated with new headings. Part numbers moved to "Product Identification System"
  - Associated Documents moved to Appendix A "Associated Documents"
  - Revision History moved to this appendix
  - Index added
  - "Product Identification System" added
  - "The Microchip Web Site", "Customer Change Notification Service" and "Customer Support" sections added
  - Front and back covers updated
- Features:
  - Typical touchscreen size updated
  - Touch Sensor Technology section added
  - Panel / cover glass support section replaced by Front Panel Material. Recommended panel thickness for glass and plastic revised
  - Advanced Touch Handling section merged into Touch Performance section. Burst Frequency and Scan Speed one finger reporting rate added
  - Application Interfaces: SPI Debug Interface added
  - Design Services section added
  - Other feature points rearranged
- "Pin configuration":
  - DBG_SS/TEST pin now recommends pull up to VddIO
  - Pin listing tables updated to show power rail information
- Section 1.0 "Overview of mXT1664T3":
  - Touch detection description updated
- Section 2.0 "Schematics":
  - Schematic drawing modified to show the maximum number of decoupling capacitors required. Pull-up resistors added for completeness to COMMSEL (USB mode) and $\overline{TEST}$ lines. Some pins rearranged
  - Section 2.5.1 "Power Supply": New section added
  - Section 2.5.2 "Decoupling capacitors": Advice on decoupling capacitors modified to recommend maximum number of decoupling capacitors
  - Section 2.5.3 "Pull-up Resistors": New section added
  - Section $\overline{RESET}$ Line removed (capacitor to GND no longer considered optional)
  - Section 2.5.4 "Voltage Booster": Information on 47 µH inductors added for low voltage mode
  - Low Drop-Out Voltage Regulators (LDOs) section removed. Information moved to Section 11.0 "PCB Design Considerations"
  - Section I^2C Interface removed (information moved elsewhere)
  - Section 2.5.6 "XTAL_XOUT and XTAL_XIN" added
  - Section 2.5.8 "GPIO Pins": Updated with information moved from elsewhere
  - Section 2.5.9 "SPI Debug Interface": New section
- Circuit Components section removed and contents merged into Section 11.0 "PCB Design Considerations"

- Section 4.0 "Sensor Layout":
  - Section 4.1 "Screen Size" added
- *Circuit Components* section combined with Section 11.0 "PCB Design Considerations"
- Section 5.0 "Power-up / Reset Requirements":
  - Updated with minor rewording. Clarification on connection of XVdd to Vdd added. Checksum information moved to Section 12.1.2 "Power-up Sequence"
  - Section 5.3 "Power-up and Initialization": Section added
  - Section 5.4 "Summary" moved to end
- Section 6.0 "Detailed Operation":
  - Section 6.4 "Sensor Acquisition" updated
  - GPIO Pins section removed and contents moved to Section 2.5.8 "GPIO Pins"
- Section 7.0 "Host Communications"
  - Text updated and reformatted
- Section 8.0 "I2C Communications":
  - Section 8.8 "Clock Stretching" corrected
  - All footnotes incorporated into main text
- Section 11.0 "PCB Design Considerations":
  - Section 11.4 "Voltage Regulators": updated to include additional recommended LDOs
  - I^2C Line Pull-up Resistor section removed; information included elsewhere
- Section 12.0 "Getting Started with mXT1664T3":
  - Section 12.1.2 "Power-up Sequence": Information and advice corrected. Checksum information moved from Section 5.0 "Power-up / Reset Requirements"
- Section 14.0 "Specifications":
  - Section 14.2 "Recommended Operating Conditions": Cx removed; information now in Section 14.8 "Touchscreen Sensor Characteristics"
  - Section 14.2.1 "DC Characteristics": Tables in sub-sections updated to show rise/fall rates correctly with explanatory notes
  - Section 14.2.2 "Power Supply Ripple and Noise" moved and now quotes single AVdd value
  - Section 14.4 "Current Consumption – I^2C Interface": Note added to say characterization charts show typical values
  - Section 14.5 "Current Consumption – USB Interface": Note added to say characterization charts show typical values
  - Section 14.7.3 "Reset Timings": Hardware reset figure updated
  - Section 14.8 "Touchscreen Sensor Characteristics" added
  - Section 14.9 "Input/Output Characteristics": All I/O pins are listed in the table
  - Section 14.10 "I2C Specification": Specific resistor values removed
- Appendix A "Associated Documents":
  - Referenced documents updated
- maXCharger T72 object renamed to Noise Suppression T72
- Self Capacitance maXCharger T108 object renamed to Self Capacitance Noise Suppression T108
- References to restricted documents removed throughout
- References to Atmel Corporation removed or changed to Microchip Technology Inc, where appropriate
- New documentation number assigned

INDEX

PRODUCT IDENTIFICATION SYSTEM

The table below gives details on the product identification system for maXTouch devices. See "Orderable Part Numbers" below for example part numbers for the mXT1664T3.

To order or obtain information, for example on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–XXX	[X]	[XX]	[X]	[XXX]
Device	Package	Temperature Range	Sample Type	Tape and Reel Option	Pattern

Device:		Base device name	
Package:	A	=	QFP (Plastic Quad Flatpack)
	CC	=	UFBGA (Ultra Thin Fine-pitch Ball Grid Array)
	C2	=	UFBGA (Ultra Thin Fine-pitch Ball Grid Array)
	NH	=	UFBGA (Ultra Thin Fine-pitch Ball Grid Array)
	C4	=	X1FBGA (Extra Thin Fine-pitch Ball Grid Array)
	MA	=	XQFN (Super Thin Quad Flat No Lead Sawn)
	MA5	=	XQFN (Super Thin Quad Flat No Lead Sawn)
Temperature Range:	U	=	–40°C to +85°C (Grade 3)
	T	=	–40°C to +85°C (Grade 3)
	B	=	–40°C to +105°C (Grade 2)
Sample Type:	Blank	=	Release Sample
	ES	=	Pre-release (Engineering) Sample
Tape and Reel Option:	Blank	=	Standard Packaging (Tube or Tray)
	R	=	Tape and Reel [1]
Pattern:			QTP, SQTP, Code or Special Requirements (Blank Otherwise)

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. See "Orderable Part Numbers" below or check with your Microchip Sales Office for package availability with the Tape and Reel option.

Orderable Part Numbers

Orderable Part Number	Firmware Revision	Description
ATMXT1664T3-CCU035 (Supplied in trays)	2.0.AA	136-ball UFBGA 7 × 7 × 0.6 mm, RoHS compliant Industrial grade; not suitable for automotive characterization
ATMXT1664T3-CCUR035 (Supplied in tape and reel)		
ATMXT1664T3-C2U035 (Supplied in trays)	2.0.AA	162-ball UFBGA 10 × 5 × 0.6 mm, RoHS compliant Industrial grade; not suitable for automotive characterization
ATMXT1664T3-C2UR035 (Supplied in tape and reel)		

Atmel SL Code

An SL (QS) code was required on Atmel purchase orders, but is no longer used by Microchip. The SL code has been replaced by the 3-digit QTP code suffix on all Microchip industrial grade orderable part numbers.

The legacy Atmel SL (QS) code for mXT1664T3 2.0.AA is QS976.

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- Technical Support

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