mXT2113TG-AT/mXT2113TG-AB 1.0

maXTouch 2048-node Touchscreen Controller

Automotive Applications

- AEC-Q100 Qualified
- Developed following Automotive SPICE® Level 3 certified processes
- CISPR 25 compliant (for both mutual and self capacitance measurements)

maXTouch® Adaptive Sensing Touchscreen Technology

- Up to 32 X (transmit) lines and 64 Y (receive) lines for use by a touchscreen and 2 key arrays
- A maximum of 2048 nodes can be allocated to the touch sensor
- Touchscreen size of 16.9 inches (2:1 aspect ratio), assuming a sensor electrode pitch of 6 mm. Other sizes are possible with different electrode pitches and appropriate sensor material
- Multiple touch support with up to 16 concurrent touches tracked in real time

Keys

- Up to 32 nodes can be allocated as mutual capacitance sensor keys in addition to the touchscreen, defined as 2 key arrays (subject to availability of X and Y lines and other configurations)
- Adjacent Key Suppression (AKS) technology is supported for false key touch prevention

Touch Sensor Technology

- Discrete/out-cell support including glass and PET film-based sensors
- On-cell/touch-on display support including TFT, LCD (ITPS, IPS) and OLED
- Synchronization with display refresh timing capability
- 3D (air) gestures supported with additional electrodes
- Support for standard (for example, Diamond) and proprietary sensor patterns (review of designs by Microchip or a Microchip-qualified touch sensor module partner is recommended)

Front Panel Material

- Works with PET or glass, including curved profiles (configuration and stack-up to be approved by Microchip or a Microchip-qualified touch sensor module partner)
- 10 mm glass (or 5 mm PMMA) with bare finger (dependent on screen size, touch size, configuration and stack-up)
- 6 mm glass (or 3 mm PMMA) with multi-finger 5 mm glove (2.7 mm PMMA equivalent) (dependent on screen size, touch size, configuration and stack-up)

Touch Performance

- Moisture/Water Compensation
  - No false touch with condensation or water drop up to 22 mm diameter
  - One-finger tracking with condensation or water drop up to 22 mm diameter
- Mutual capacitance and self capacitance measurements supported for robust touch detection
- P2P mutual capacitance measurements supported for extra sensitive multi-touch sensing
- Noise suppression technology to combat ambient and power-line noise
  - Up to 240 V_{PP} between 1 Hz and 1 kHz sinusoidal waveform
  - Up to 20 V_{PP} between 1 kHz and 1 MHz sinusoidal waveform
- Burst Frequency
  - Flexible and dynamic Tx burst frequency selection to reduce EMC disturbance
  - Controlled Tx burst frequency drift over process and temperature range
  - Configurable Tx waveform shaping to reduce emissions
- Scan Speed
  - Typical report rate for 10 touches ≥100 Hz (subject to configuration)
  - Initial touch latency <20 ms for first touch from idle (subject to configuration)
  - Configurable to allow for power and speed optimization

- Touch panel failure detection
  - Automatic touch sensor diagnostics during run time to support the implementation of safety critical features
  - Diagnostics reported using dedicated output pin or by standard Object Protocol messages
  - Configurable test limits

On-chip Gestures

- 3D (air) gestures supported in conjunction with the MXG3141 3D gesture device
- Reports one-touch and two-touch 2D gestures, processed natively by the mXT2113TG-Ax touch controller

Enhanced Algorithms

- Lens bending algorithms to remove display noise
- Touch suppression algorithms to remove unintentional large touches, such as palm
- Palm Recovery Algorithm for quick restoration to normal state

Data Store

- 60-byte CRC-checksummed data area for use as a run-time Product Data Store Area
- Up to 64 bytes of user's custom data (not CRC checksummed)

Power Saving

- Programmable timeout for automatic transition from Active to Idle state
- Pipelined analog sensing detection and digital processing to optimize system power efficiency

Application Interfaces

- I^2C client interface with support for Standard mode (up to 100 kHz), Fast mode (up to 400 kHz), Fast-mode Plus (up to 1 MHz)
- SPI client interface (up to 8 MHz)
- Interrupt to indicate when a message is available
- Additional SPI Debug Interface to read the raw data for tuning and debugging purposes

Power Supply

- Digital (Vdd) 3.3V nominal
- Digital I/O (VddIO) 3.3V nominal
- Analog (AVdd) 3.3V nominal
- High voltage external X line drive (XVdd) up to 8.5V

Package

- 144-lead LQFP 20 × 20 × 1.4 mm, 0.5 mm pitch

Operating Temperature

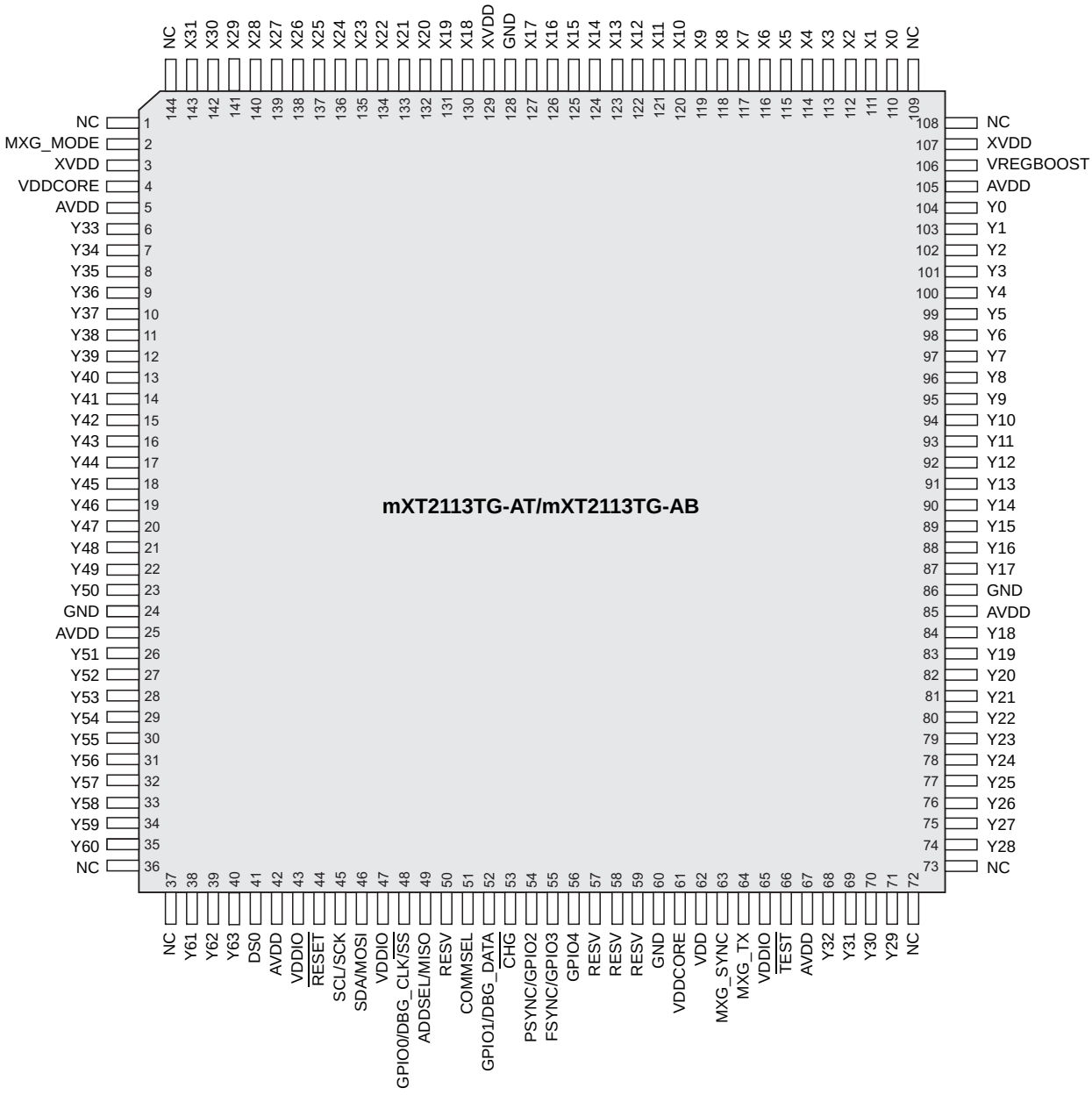
- mXT2113TG-AT: –40°C to +85°C (Grade 3)
- mXT2113TG-AB: –40°C to +105°C (Grade 2)

Design Services

- Review of device configuration, stack-up and sensor patterns
- Custom firmware versions can be considered
- Contact your Microchip representative for more information

PIN CONFIGURATION

144-lead LQFP



Top view

TABLE 1: PIN LISTING – 144-LEAD LQFP

Pin	Name	Type	Supply	Description	If Unused...
1	NC	–	–	No connection	–
2	MXG_MODE	O	AVdd	3D Gesture device scan mode: High: 2D touch measuring Low: 3D gesture measuring	–
3	XVDD	P	–	X line drive power	–
4	VDDCORE	P	–	Digital core power	–
5	AVDD	P	–	Analog power	–
6	Y33	S	AVdd	Y line connection	Leave open
7	Y34	S	AVdd	Y line connection	Leave open
8	Y35	S	AVdd	Y line connection	Leave open
9	Y36	S	AVdd	Y line connection	Leave open
10	Y37	S	AVdd	Y line connection	Leave open
11	Y38	S	AVdd	Y line connection	Leave open
12	Y39	S	AVdd	Y line connection	Leave open
13	Y40	S	AVdd	Y line connection	Leave open
14	Y41	S	AVdd	Y line connection	Leave open
15	Y42	S	AVdd	Y line connection	Leave open
16	Y43	S	AVdd	Y line connection	Leave open
17	Y44	S	AVdd	Y line connection	Leave open
18	Y45	S	AVdd	Y line connection	Leave open
19	Y46	S	AVdd	Y line connection	Leave open
20	Y47	S	AVdd	Y line connection	Leave open
21	Y48	S	AVdd	Y line connection	Leave open
22	Y49	S	AVdd	Y line connection	Leave open
23	Y50	S	AVdd	Y line connection	Leave open
24	GND	P	–	Ground	–
25	AVDD	P	–	Analog power	–
26	Y51	S	AVdd	Y line connection	Leave open
27	Y52	S	AVdd	Y line connection	Leave open
28	Y53	S	AVdd	Y line connection	Leave open
29	Y54	S	AVdd	Y line connection	Leave open
30	Y55	S	AVdd	Y line connection	Leave open
31	Y56	S	AVdd	Y line connection	Leave open
32	Y57	S	AVdd	Y line connection	Leave open
33	Y58	S	AVdd	Y line connection	Leave open
34	Y59	S	AVdd	Y line connection	Leave open
35	Y60	S	AVdd	Y line connection	Leave open
36	NC	–	–	No connection	–
37	NC	–	–	No connection	–
38	Y61	S	AVdd	Y line connection	Leave open
39	Y62	S	AVdd	Y line connection	Leave open
40	Y63	S	AVdd	Y line connection	Leave open

TABLE 1: PIN LISTING – 144-LEAD LQFP (CONTINUED)

Pin	Name	Type	Supply	Description	If Unused...
41	DS0	O	AVdd	Driven Shield signal; used as guard track between X/Y signals and ground	Leave open
42	AVDD	P	–	Analog power	–
43	VDDIO	P	–	Digital power	–
44	$\overline{\text{RESET}}$	I	VddIO	Reset low. Connection to host system is recommended	Pull up to VddIO
45	SCL	OD	VddIO	I^2C Mode: Serial clock	–
	SCK	I		SPI Mode: Serial clock	
46	SDA	OD	VddIO	I^2C Mode: Serial Data	–
	MOSI	I		SPI Mode: Serial Data – Host Output Client Input	
47	VDDIO	P	–	Digital power	–
48	GPIO0	I/O	VddIO	I^2C Mode: General purpose I/O; see Section 2.3.10 “GPIO Pins”	Connect to test point Leave open
	DBG_CLK	O		I^2C Mode: Debug clock; see Section 2.3.11 “SPI Debug Interface”	
	$\overline{\text{SS}}$	I		SPI Mode: Chip Select line (active low)	
49	ADDSEL	I	VddIO	I^2C Mode: I^2C address select; see Section 8.2 “I^2C Address Selection – ADDSEL Pin”	–
	MISO	O		SPI Mode: Serial Data – Host Input Client Output	
50	RESV	–	–	Reserved for future use	Leave open
51	COMMSEL	I	VddIO	Communications interface selection; see Section 8.1 “Host Communication Mode Selection – COMMSEL Pin”	–
52	GPIO1	I/O	VddIO	General purpose I/O; see Section 2.3.10 “GPIO Pins”	Connect to test point Leave open
	DBG_DATA	O		I^2C Mode: Debug data; see Section 2.3.11 “SPI Debug Interface”	
53	$\overline{\text{CHG}}$	OD	VddIO	State change interrupt	Pull up to VddIO
54	PSYNC	I	VddIO	External pulse synchronization (usually HSYNC)	Input: Connect to GND Output: Leave open
	GPIO2	I/O		General purpose I/O; see Section 2.3.10 “GPIO Pins”	
55	FSYNC	I	VddIO	External frame synchronization (usually VSYNC)	Input: Connect to GND Output: Leave open
	GPIO3	I/O		General purpose I/O; see Section 2.3.10 “GPIO Pins”	
56	GPIO4	I/O	VddIO	General purpose IO; see Section 2.3.10 “GPIO Pins”	Input: Connect to GND Output: Leave open
57	RESV	–	–	Reserved for future use	Leave open
58	RESV	–	–	Reserved for future use	Leave open
59	RESV	–	–	Reserved for future use	Leave open
60	GND	P	–	Ground	–
61	VDDCORE	P	–	Digital core power	–
62	VDD	P	–	Digital power	–
63	MXG_SYNC	I	VddIO	3D Gesture device synchronization pulse (approximately every 1 ms)	–
64	MXG_TX	I	VddIO	3D Gesture device transmit; touch controller routes signal to touch sensor	–
65	VDDIO	P	–	Digital power	–
66	$\overline{\text{TEST}}$	–	VddIO	Reserved; must be pulled up to VddIO	–

TABLE 1: PIN LISTING – 144-LEAD LQFP (CONTINUED)

Pin	Name	Type	Supply	Description	If Unused...
67	AVDD	P	–	Analog power	–
68	Y32	S	AVdd	Y line connection	Leave open
69	Y31	S	AVdd	Y line connection	Leave open
70	Y30	S	AVdd	Y line connection	Leave open
71	Y29	S	AVdd	Y line connection	Leave open
72	NC	–	–	No connection	–
73	NC	–	–	No connection	–
74	Y28	S	AVdd	Y line connection	Leave open
75	Y27	S	AVdd	Y line connection	Leave open
76	Y26	S	AVdd	Y line connection	Leave open
77	Y25	S	AVdd	Y line connection	Leave open
78	Y24	S	AVdd	Y line connection	Leave open
79	Y23	S	AVdd	Y line connection	Leave open
80	Y22	S	AVdd	Y line connection	Leave open
81	Y21	S	AVdd	Y line connection	Leave open
82	Y20	S	AVdd	Y line connection	Leave open
83	Y19	S	AVdd	Y line connection	Leave open
84	Y18	S	AVdd	Y line connection	Leave open
85	AVDD	P	–	Analog power	–
86	GND	P	–	Ground	–
87	Y17	S	AVdd	Y line connection	Leave open
88	Y16	S	AVdd	Y line connection	Leave open
89	Y15	S	AVdd	Y line connection	Leave open
90	Y14	S	AVdd	Y line connection	Leave open
91	Y13	S	AVdd	Y line connection	Leave open
92	Y12	S	AVdd	Y line connection	Leave open
93	Y11	S	AVdd	Y line connection	Leave open
94	Y10	S	AVdd	Y line connection	Leave open
95	Y9	S	AVdd	Y line connection	Leave open
96	Y8	S	AVdd	Y line connection	Leave open
97	Y7	S	AVdd	Y line connection	Leave open
98	Y6	S	AVdd	Y line connection	Leave open
99	Y5	S	AVdd	Y line connection	Leave open
100	Y4	S	AVdd	Y line connection	Leave open
101	Y3	S	AVdd	Y line connection	Leave open
102	Y2	S	AVdd	Y line connection	Leave open
103	Y1	S	AVdd	Y line connection	Leave open
104	Y0	S	AVdd	Y line connection	Leave open
105	AVDD	P	–	Analog power	–
106	VREGBOOST	O	AVdd	Voltage booster control	Connect to test point Leave open
107	XVDD	P	–	X line drive power	–

TABLE 1: PIN LISTING – 144-LEAD LQFP (CONTINUED)

Pin	Name	Type	Supply	Description	If Unused...
108	NC	–	–	No connection	–
109	NC	–	–	No connection	–
110	X0	S	XVdd	X line connection	Leave open
111	X1	S	XVdd	X line connection	Leave open
112	X2	S	XVdd	X line connection	Leave open
113	X3	S	XVdd	X line connection	Leave open
114	X4	S	XVdd	X line connection	Leave open
115	X5	S	XVdd	X line connection	Leave open
116	X6	S	XVdd	X line connection	Leave open
117	X7	S	XVdd	X line connection	Leave open
118	X8	S	XVdd	X line connection	Leave open
119	X9	S	XVdd	X line connection	Leave open
120	X10	S	XVdd	X line connection	Leave open
121	X11	S	XVdd	X line connection	Leave open
122	X12	S	XVdd	X line connection	Leave open
123	X13	S	XVdd	X line connection	Leave open
124	X14	S	XVdd	X line connection	Leave open
125	X15	S	XVdd	X line connection	Leave open
126	X16	S	XVdd	X line connection	Leave open
127	X17	S	XVdd	X line connection	Leave open
128	GND	P	–	Ground	–
129	XVDD	P	–	X line drive power	–
130	X18	S	XVdd	X line connection	Leave open
131	X19	S	XVdd	X line connection	Leave open
132	X20	S	XVdd	X line connection	Leave open
133	X21	S	XVdd	X line connection	Leave open
134	X22	S	XVdd	X line connection	Leave open
135	X23	S	XVdd	X line connection	Leave open
136	X24	S	XVdd	X line connection	Leave open
137	X25	S	XVdd	X line connection	Leave open
138	X26	S	XVdd	X line connection	Leave open
139	X27	S	XVdd	X line connection	Leave open
140	X28	S	XVdd	X line connection	Leave open
141	X29	S	XVdd	X line connection	Leave open
142	X30	S	XVdd	X line connection	Leave open
143	X31	S	XVdd	X line connection	Leave open
144	NC	–	–	No connection	–

Key:

I	Input only	O	Output only	I/O	Input or output
OD	Open drain output	P	Ground or power	S	Sense pin

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1.0 OVERVIEW OF MXT2113TG-AT/MXT2113TG-AB

1.1 Introduction

The Microchip maXTouch family of touch controllers brings industry-leading capacitive touch performance to customer automotive applications. The mXT2113TG-AT/mXT2113TG-AB (known as mXT2113TG-Ax) features the latest generation of Microchip adaptive sensing technology that utilizes a hybrid mutual and self capacitive sensing system in order to deliver unparalleled touch features and a robust user experience.

- **Patented capacitive sensing method** – The mXT2113TG-Ax uses a unique charge-transfer acquisition engine to implement Microchip's patented capacitive sensing method. Coupled with a state-of-the-art CPU, the entire touchscreen sensing solution can measure, classify and track a number of individual finger touches with a high degree of accuracy in the shortest response time.
- **Capacitive Touch Engine (CTE)** – The mXT2113TG-Ax features an acquisition engine that uses an optimal measurement approach to ensure almost complete immunity from parasitic capacitance on the receiver input lines. The engine includes sufficient dynamic range to cope with anticipated touchscreen self and mutual capacitances, which allows great flexibility for use with the Microchip proprietary sensor pattern designs. One- and two-layer ITO sensors are possible using glass or PET substrates.
- **Touch detection** – The mXT2113TG-Ax allows for both mutual and self capacitance measurements, with the self capacitance measurements being used to augment the mutual capacitance measurements to produce reliable touch information.

  When self capacitance measurements are enabled, touch classification is achieved using both mutual and self capacitance touch data. This has the advantage that both types of measurement systems can work together to detect touches under a wide variety of circumstances.

  The system may be configured for different types of default measurements in both idle and active modes. For example, the device may be configured for Mutual Capacitance Touch as the default in active mode and Self Capacitance Touch as the default in idle mode. Note that other types of scans (such as P2P mutual capacitance scans and other types of self capacitance scans) may also be made depending on configuration.

  Mutual capacitance touch data is used wherever possible to classify touches as this has a greater resolution than self capacitance measurements and provides positional information on touches. For this reason, multiple touches can only be determined by mutual capacitance touch data. In Self Capacitance Touch Default mode, if the self capacitance touch processing detects multiple touches, touchscreen processing is skipped until mutual capacitance touch data is available.

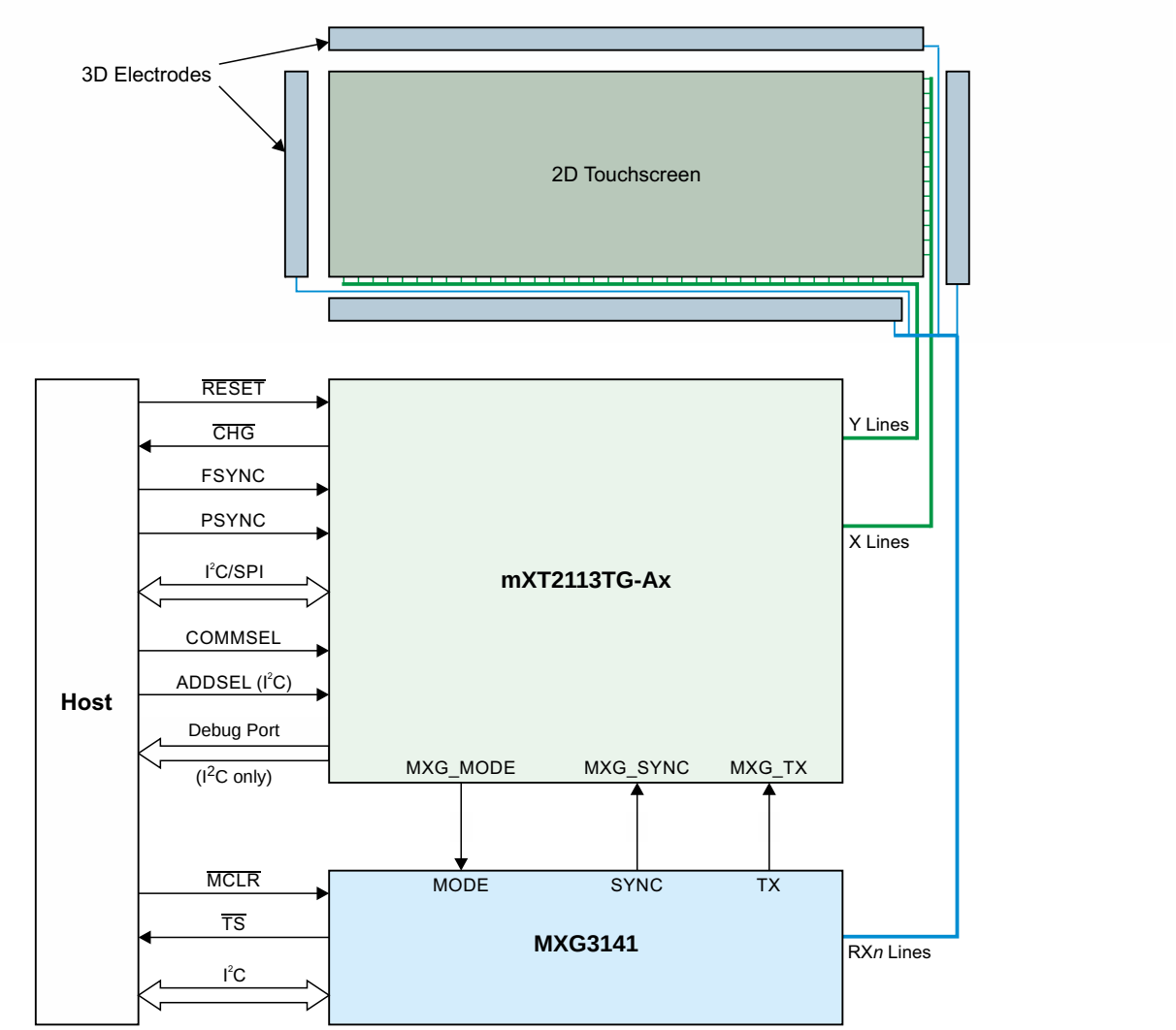
  Self capacitance and P2P mutual capacitance measurements allow for the detection of touches in extreme scenarios, such as thick glove touches, when mutual capacitance touch detection alone may miss touches.
- **2D and 3D Gestures** – The mXT2113TG-Ax touch controller operates seamlessly with the MXG3141 3D gesture device to provide both 2-dimensional (2D) gestures on the touchscreen surface and 3-dimensional (3D) gestures in the 3-dimensional space above the touchscreen. Full multiplexing allows the total system to process both 3D gestures from an approaching hand and 2D touch gestures once a surface touch has been detected. See Section 1.2 "mXT2113TG-Ax System Architecture" for more information.
- **Display Noise Cancellation** – A combination of analog circuitry, hardware noise processing, and firmware combats display noise without requiring additional listening channels or synchronization to display timing. This enables the use of shieldless touch sensor stacks, including touch-on-lens.
- **Noise filtering** – Hardware noise processing in the capacitive touch engine provides enhanced autonomous filtering and allows a broad range of noise profiles to be handled. The result is good performance in the presence of LCD noise.
- **Processing power** – The main CPU has two companion microsequencer coprocessors under its control consuming low power. This system allows the signal acquisition, preprocessing and postprocessing to be partitioned in an efficient and flexible way.
- **Interpreting user intention** – The Microchip hybrid mutual and self capacitance method provides unambiguous multitouch performance. Algorithms in the mXT2113TG-Ax provide optimized touchscreen position filtering for the smooth tracking of touches, responding to a user's intended touches while preventing false touches triggered by ambient noise, conductive material on the sensor surface, such as moisture, or unintentional touches from the user's resting palm or fingers.

1.2 mXT2113TG-Ax System Architecture

The maXTouch capacitive touch technology is a 2D system that detects the X and Y position of a touch on the surface of a capacitive touchscreen. The MXG3141 3D gesture device is a 3D system that uses near-field sensing to detect the position of a hand in the space above the surface of the touchscreen. The mXT2113TG-Ax allows these two technologies to be combined into one seamless system without a deterioration in the performance of either technology.

Figure 1-1 shows the mXT2113TG-Ax system architecture.

FIGURE 1-1: SYSTEM ARCHITECTURE



The MXG_MODE line allows the mXT2113TG-Ax to schedule 2D and 3D processing, while the MXG_SYNC line is used by the MXG3141 to send a synchronization pulse approximately every 1 ms.

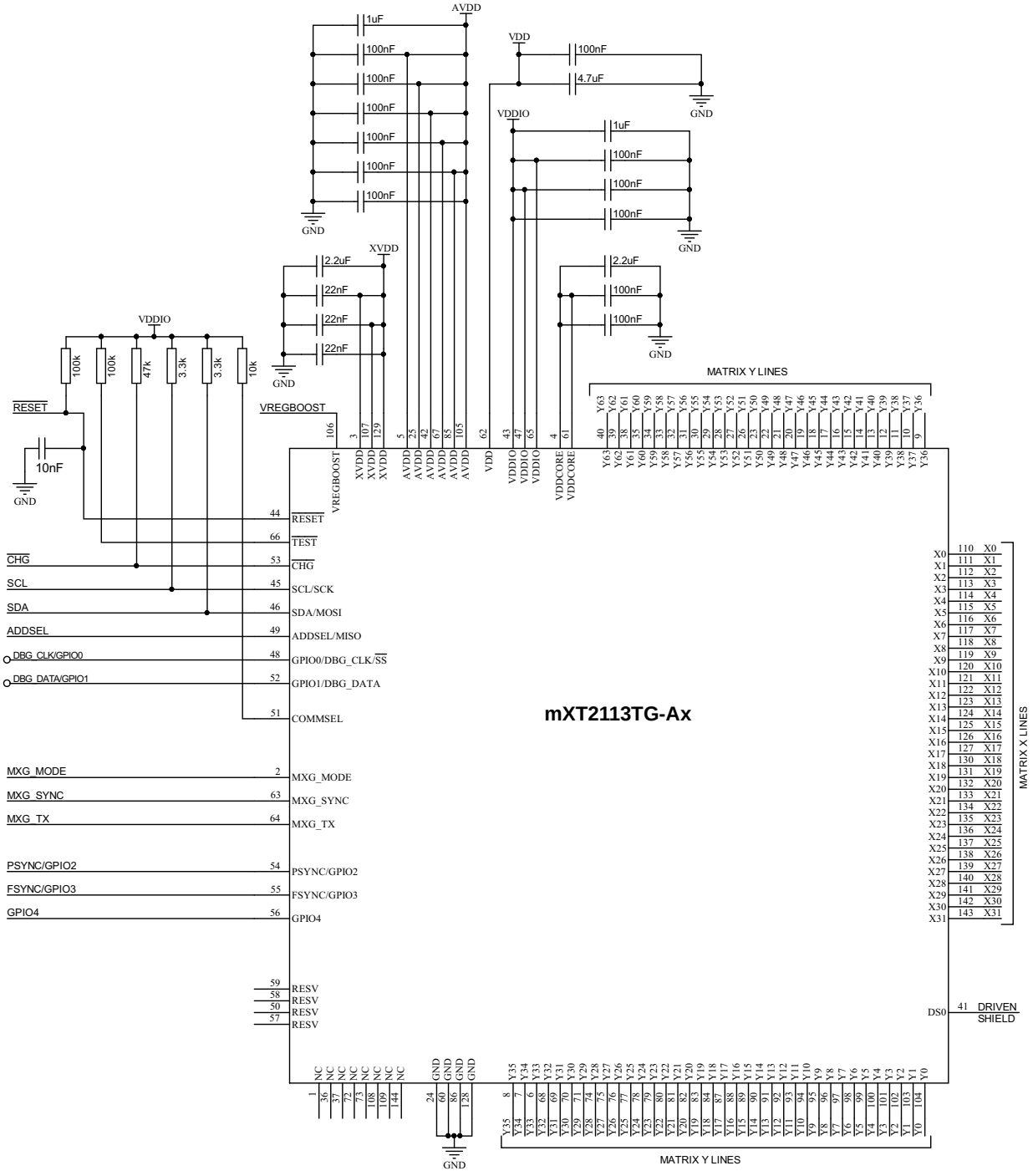
All MXG3141 status and event reporting messages are sent directly to the host.

The two devices process hand and touch detections as follows:

1. The system is in 2D/3D Multiplexed mode so that both 3D gestures and 2D touches can be detected. In this mode, the mXT2113TG-Ax allows both the 2D and 3D section processes some time to operate by setting the MXG_MODE pin both high (2D processing) and low (3D processing) during each Idle acquisition cycle.
2. If the MXG3141 3D processing detects the presence of a hand, it processes any 3D gestures.
3. If the mXT2113TG-Ax 2D processing detects a touch on the touchscreen, the mXT2113TG-Ax sets the MXG_MODE pin high and the MXG3141 stops monitoring the MXG_RX lines.
4. The mXT2113TG-Ax processes the 2D touches until the last touch is released and a configurable timeout has expired, at which point the system enters 2D/3D Multiplexed mode once again.

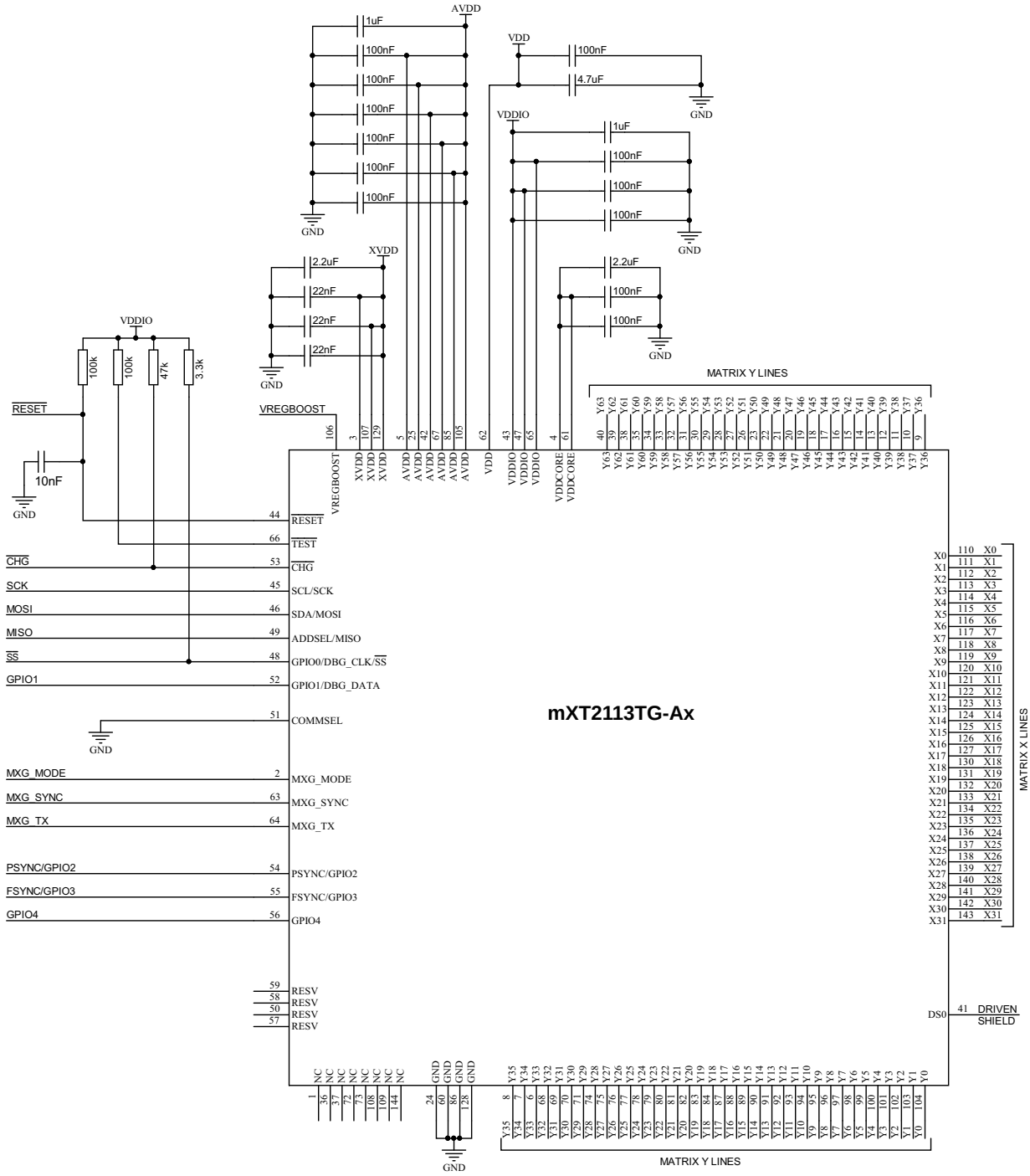
2.0 SCHEMATICS

2.1 144-lead LQFP – I²C Mode



See Section 2.3 “Schematic Notes”

2.2 144-lead LQFP – SPI Mode



See Section 2.3 “Schematic Notes”

2.3 Schematic Notes

2.3.1 POWER SUPPLY

The sense and I/O pins are supplied by the different power rails on the device as listed in "Pin configuration".

2.3.2 DECOUPLING CAPACITORS

All decoupling capacitors must be X7R or X5R and placed less than 5 mm away from the pins for which they act as bypass capacitors. Pins of the same type can share a capacitor provided no pin is more than 10 mm from the capacitor.

The schematics on the previous pages show the capacitors required. The parallel combination of capacitors is recommended to give high and low frequency filtering, which is beneficial if the voltage regulators are likely to be some distance from the device (for example, If an active tail design is used). Note that this requires that the voltage regulator supplies for AVdd, Vdd and VddIO are clean and noise free. It also assumes that the track length between the capacitors and on-board power supplies is less than 50 mm.

The number of base capacitors can be reduced if the pinout configuration means that sharing a bypass capacitor is possible (subject to the distance between the pins satisfying the conditions above and there being no routing difficulties).

2.3.3 PULL-UP RESISTORS

The pull-up resistors shown in the schematics are suggested typical values and may be modified to meet the requirements of an individual customer design.

This applies, in particular, to the pull-up resistors on the I^2C SDA and SCL lines (shown on the schematic), as the values of these resistors depend on the speed of the I^2C interface. See Section 14.10 "Host I2C Specification" for details.

2.3.4 VDDCORE

VddCore is internally generated from the Vdd power supply. To guarantee stability of the internal voltage regulator, one or more external decoupling capacitors are required.

2.3.5 XVDD

XVdd power can be supplied using one of the following methods:

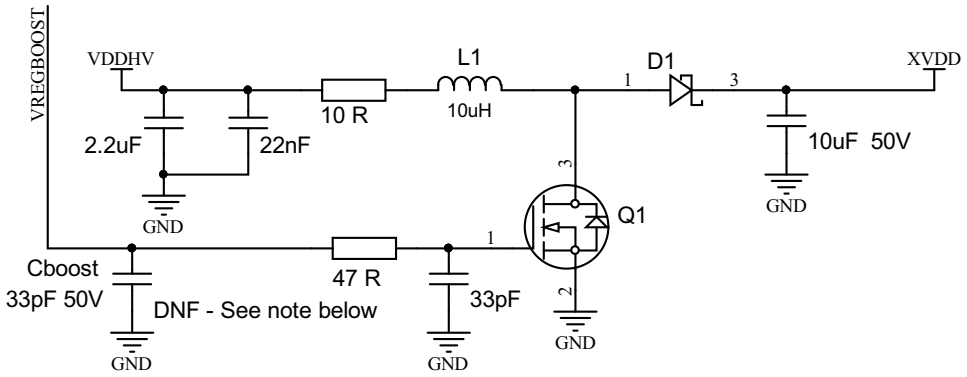
- From an external regulated XVdd supply (see Section 14.2.1.3 "XVdd Voltage Supply – XVdd")
- Using an external Voltage Booster (See Section 2.3.6 "Voltage Booster"). See Section 14.2 "Recommended Operating Conditions" for the supply voltages possible
- From the same regulator as the Vdd supply

2.3.6 VOLTAGE BOOSTER

The XVdd power can be supplied using the Voltage Booster shown in Figure 2-1. Two frequency modes are supported so that it is possible to avoid interference with other functions, such as Long-Term Evolution (LTE) technology. Depending on the chosen frequency mode, a different inductor has to be used. The high frequency mode requires a 10 µH inductor and a 47 µH inductor should be used in the low frequency mode.

If an external supply is used, the components in Figure 2-1 can be omitted and VREGBOOST should be left open circuit or connected to a test point. Connection to a test point is preferred and is recommended by Microchip.

FIGURE 2-1: XVDD SUPPLY CIRCUIT



Note 1: Do not fit capacitor Cboost but make provision for it next to the VREGBOOST pin. This capacitor may be required to minimize RF noise issues.

2: See Section 2.3.6.1 “Suggested Component Suppliers” for suggested suppliers for L1 and Q1.

3: To run the Voltage Booster in low frequency mode, a 47 µH inductor (in position L1) will need to be fitted to the boost circuit.

2.3.6.1 Suggested Component Suppliers

D1 is a Schottky Diode. Possible suppliers are shown in Table 2-1.

TABLE 2-1: SUITABLE SCHOTTKY DIODE (D1)

Manufacturer	Device
ON Semiconductor	BAT54M3T5G
Micro Commercial Co	1N4148WX

L1 is a 10 µH inductor. Possible suppliers are shown in Table 2-2.

TABLE 2-2: SUITABLE 10 µH INDUCTORS (L1)

Manufacturer	Device	Size
Panasonic	ELJFB100JF	1812 (4532 metric)
TDK	MLZ1608M100WT	1812 (4532 metric)
TDK	MLZ2012M100WT	0805 (2012 metric)

When the Voltage Booster is run in low frequency mode, L1 is a 47 µH inductor. Possible suppliers are shown in Table 2-3.

TABLE 2-3: SUITABLE 47 µH INDUCTORS (L1)

Manufacturer	Device	Size
Taiyo Yuden	NR3015T470M	1212 (3 × 3 mm)

Q1 is an N-channel 20 V, 700 mA, MOSFET. Possible suppliers are shown in Table 2-4.

TABLE 2-4: SUITABLE MOSFETS (Q1)

Manufacturer	Device
Microchip	2N7002-G
Toshiba	SSM3K56FS

2.3.7 DRIVEN SHIELD LINE

The driven shield line (DS0) should be used to shield the X/Y sense lines. Specifically, it acts as a driven shield in self capacitance operation. See Section 11.4 “Driven Shield Line” for more details.

2.3.8 MULTIPLE FUNCTION PINS

Some pins may have multiple functions. In this case, only one function can be chosen and the circuit should be designed accordingly.

2.3.9 FSYNC AND PSYNC PIN

The mXT2113TG-Ax has two synchronization pins: FSYNC for frame synchronization (typically connected to VSYNC) and PSYNC for pulse synchronization (typically connected to HSYNC).

2.3.10 GPIO PINS

The mXT2113TG-Ax has 5 GPIO pins. The pins can be set to be either an input or an output, as required, using the GPIO Configuration T19 object.

If a GPIO pin is unused, it can be left unconnected externally as long as it is given a defined state by the GPIO Configuration T19 object.

By default the GPIO pins are set to be inputs so if a pin is not used, and is left configured as an input, it should be connected to GND through a resistor. Alternatively, the internal pull-up resistor should be enabled (in the GPIO Configuration T19 object) to pull up the pin. Note that this does not apply if the GPIO pin is shared with a debug line; see Section 2.3.11 “SPI Debug Interface” for advice on how to treat an unused GPIO pin in this case.

Alternatively, the GPIO pin can be set as an output low using the GPIO Configuration T19 object and left open. This second option avoids any problems should the pin accidentally be configured as output high at a later date.

If the GPIO Configuration T19 object is not enabled for use, the GPIO pins cannot be used for GPIO purposes, although any alternative function can still be used.

Some GPIO pins have alternative functions. If an alternative function is used then this takes precedence over the GPIO function and the pin cannot be used as a GPIO pin. In particular:

- GPIO3 cannot be used if the FSYNC function is in use.
- GPIO2 cannot be used if the PSYNC function is in use.
- GPIO0 cannot be used if the $\overline{SS}$ function is in use. This means that if the SPI interface is in use, GPIO0 is not available for use.
- The SPI Debug Interface functionality is shared with some of the GPIO pins. See Section 2.3.11 “SPI Debug Interface” for more details on the SPI Debug Interface and how to handle these pins if they are totally unused.

2.3.11 SPI DEBUG INTERFACE

The DBG_CLK, DBG_DATA and $\overline{DBG\_SS}$ lines form the SPI Debug Interface. These pins should be routed to test points on all designs, such that they can be connected to external hardware during system development and for debug purposes. See also Section 13.1 “SPI Debug Interface”.

The debug lines may share pins with other functionality. If the circuit is designed to use the SPI Debug Interface, then any alternative functionality cannot be used. Specifically:

- The DBG_CLK line shares functionality with $\overline{SS}$ and GPIO0; therefore $\overline{SS}$ and GPIO0 cannot be used if the SPI Debug Interface is in use.
- The DBG_DATA line shares functionality with GPIO1; therefore GPIO1 cannot be used if the SPI Debug Interface is in use.

The DBG_CLK, DBG_DATA and $\overline{DBG\_SS}$ lines should not be connected to power or GND. For this reason, where these pins are shared with GPIO pins and they are totally unused (that is, they are not being used as debug or GPIO pins), they should be set as outputs using the GPIO Configuration T19 object.

NOTE	The SPI Debug Interface is not available if the SPI interface is being used for communications with the host.

3.0 TOUCHSCREEN BASICS

3.1 Sensor Construction

A touchscreen is usually constructed from a number of transparent electrodes. These are typically on a glass or plastic substrate. They can also be made using non-transparent electrodes, such as copper or carbon. Electrodes are constructed from Indium Tin Oxide (ITO) or metal mesh. Thicker electrodes yield lower levels of resistance (perhaps tens to hundreds of Ω/square) at the expense of reduced optical clarity. Lower levels of resistance are generally more compatible with capacitive sensing. Thinner electrodes lead to higher levels of resistance (perhaps hundreds of Ω/square) with some of the best optical characteristics.

Interconnecting tracks in ITO can cause problems. The excessive RC time constants formed between the resistance of the track and the capacitance of the electrode to ground can inhibit the capacitive sensing function. In such cases, the tracks should be replaced by screen printed conductive inks (non-transparent) outside the touchscreen viewing area.

3.2 Electrode Configuration

The specific electrode designs used in Microchip touchscreens are the subject of various patents and patent applications. Further information is available on request.

The device supports various configurations of electrodes as summarized in Section 4.0 “2D Sensor Layout”.

3.3 Scanning Sequence

All nodes are scanned in sequence by the device. Where possible, there is a parallelism in the scanning sequence to improve overall response time. The nodes are scanned by measuring capacitive changes at the intersections formed between the first drive (X) line and all the receive (Y) lines. Then the intersections between the next drive line and all the receive lines are scanned, and so on, until all X and Y combinations have been measured.

The device can be configured in various ways. It is possible to disable some nodes so that they are not scanned at all. This can be used to improve overall scanning time.

3.4 Touchscreen Sensitivity

3.4.1 ADJUSTMENT

Sensitivity of touchscreens can vary across the extents of the electrode pattern due to natural differences in the parasitic capacitance of the interconnections, control chip, and so on. An important factor in the uniformity of sensitivity is the electrode design itself. It is a natural consequence of a touchscreen pattern that the edges form a discontinuity and hence tend to have a different sensitivity. The electrodes at the edges do not have a neighboring electrode on one side and this affects the electric field distribution in that region.

A sensitivity adjustment is available for the whole touchscreen. This adjustment is a basic algorithmic threshold that defines when a node is considered to have enough signal change to qualify as being in detect.

3.4.2 MECHANICAL STACKUP

The mechanical stackup refers to the arrangement of material layers that exist above and below a touchscreen. The arrangement of the touchscreen in relation to other parts of the mechanical stackup has an effect on the overall sensitivity of the screen. The maXTouch technology has an excellent ability to operate in the presence of ground planes close to the sensor. The sensitivity of the maXTouch technology is attributed more to the interaction of the electric fields between the transmitting (X) and receiving (Y) electrodes than to the surface area of these electrodes. For this reason, stray capacitance on the X or Y electrodes does not strongly reduce sensitivity.

Front panel dielectric material has a direct bearing on sensitivity. Plastic front panels are usually suitable up to about 5 mm, and glass up to about 10 mm (dependent upon the screen size and layout). The thicker the front panel, the lower the signal-to-noise ratio of the measured capacitive changes and hence the lower the resolution of the touchscreen. In general, glass front panels are near optimal because they conduct electric fields almost twice as easily as plastic panels.

NOTE	Care should be taken using ultra-thin glass panels as retransmission effects can occur, which can significantly degrade performance.

4.0 2D SENSOR LAYOUT

NOTE	The specific electrode designs used in Microchip touchscreens may be the subject of various patents and patent applications. Further information is available on request.

This section describes the sensor layout of the 2D touchscreen. For information on the 3D electrodes, see Section 5.0 “3D Sensor Layout”.

4.1 Electrodes

The device supports various configurations of touch electrodes on the 2D touchscreen as summarized below:

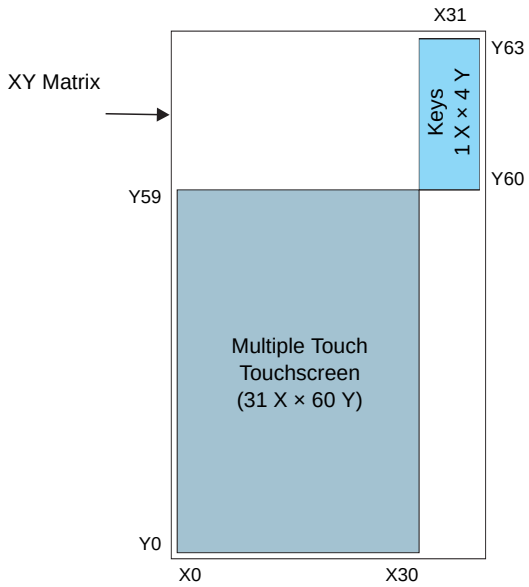
- Touchscreen: 1 touchscreen panel occupies a rectangular matrix of up to 32 X × 64 Y lines maximum (subject to other configurations).
- Keys: Up to 32 keys in an X/Y grid (consisting of 2 Key Arrays of up to 16 keys each), with each node (X/Y intersection) forming a key within each array.

The physical sensor matrix is configured using one or more touch objects. It is not mandatory to have all the allowable touch objects on the device enabled, nor is it mandatory to use all the rows and columns on the matrix, so objects that are not required can be left disabled (default).

4.2 Sensor Matrix Layout

An example layout is shown in Figure 4-1.

FIGURE 4-1: EXAMPLE LAYOUT



When designing the physical layout of the touch panel, the following rules must be obeyed:

- **General layout rules:**
  - Each touch object should be a regular rectangular shape in terms of the lines it uses.
  - Although each touch object must use a contiguous block of X or Y lines, there can be gaps between the blocks of X and Y lines used for the different touch objects (or different instances of the touch objects)
- **Additional layout rules for Multiple Touch Touchscreen T100:**
  - The Multiple Touch Touchscreen T100 object ***must*** start at (X0, Y0)
  - The Multiple Touch Touchscreen T100 object cannot share an X or Y line with another touch object (for example, a Key Array T15).

- The touchscreen must contain a minimum of 3 X lines. If Dual X Drive is enabled for use in the Noise Suppression T72 object, the minimum is 4 X lines.
- The touchscreen must contain a minimum of 3 Y lines.

- **Additional layout rules for Key Array T15:**
  - An instance of the Key Array must occupy higher X and Y lines than those used by the Multiple Touch Touchscreen T100 object.
  - An instance of the Key Array T15 object cannot share an X or Y line with the Multiple Touch Touchscreen T100 object. However, an instance of the Key Array T15 object can share any number of X or Y lines with another instance of the Key Array T15 object.

4.3 Screen Size

Table 4-1 lists some typical screen size and electrode pitch combinations to achieve various aspect ratios.

TABLE 4-1: TYPICAL SCREEN SIZES

Aspect Ratio	Matrix Size	Node Count	Screen Diagonal (Inches)			
			5 mm Pitch	5.5 mm Pitch	6 mm Pitch	6.5 mm Pitch
Single Touchscreen (1)						
16:10	X = 32, Y = 52	1664	12.02	13.22	14.42	15.62
16:9	X = 32, Y = 57	1824	12.87	14.15	15.44	16.73
8:3	X = 24, Y = 64	1536	13.46	14.8	16.15	17.49
2:1	X = 32, Y = 64	2048	14.09	15.49	16.9	18.31

Note 1: The figures given in the table are for a Touchscreen and show the largest node count possible to achieve the desired aspect ratio. No provision has been made for a Key Array.

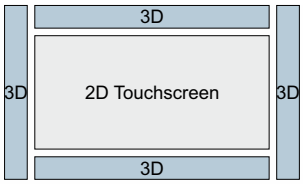
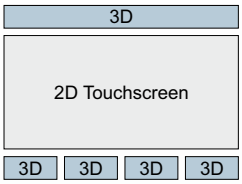
5.0 3D SENSOR LAYOUT

In order to process 3D gestures, the two-dimensional touchscreen needs to be extended with three-dimensional electrodes. The MXG3141 3D gesture device typically uses four or five receiver (RX) electrodes to detect 3D gestures, arranged in one of the layouts shown in Table 5-1.

Note that full gesture detection is only possible on a particular axis if there is an electrode on either end of the axis. With a frame style layout, therefore, gesture detection is possible in both X (West-East) and Y (South-North) directions.

With a Single Edge Plus One arrangement, the electrode arrangement along the main edge means that there is high precision along this axis. In addition, by adding an additional fifth electrode along the opposite edge to the single edge, full gesture detection is possible.

TABLE 5-1: 3D ELECTRODE STYLES

Feature	Electrode Arrangement	
	Frame	**Single Edge Plus One**
Layout	 1 × 3D electrode per side of 2D touchscreen	 4 × 3D electrodes + 1 × 3D electrode along far side of 2D touchscreen
Space Requirement in X Direction	Touchscreen width + 2 × border + 2 × 3D electrode width	Touchscreen width + 3D feed line allowance (track and gap)
Space Requirement in Y Direction	Touchscreen height + 2 × border + 2 × 3D electrode height	Touchscreen height + 2 × border + 2 × 3D electrode height
X Position Indication	Normal	High precision
Y Position Indication	Normal	Normal (1)
3D Gesture Recognition	West-East Flicks North-South Flicks Proximity detection	West-East Flicks North-South Flicks Proximity detection

Note 1: Assumes electrodes are positioned on South and North edges. If electrodes are along the West and East edges, then high precision Y position with normal X position indication is possible instead.

For details on designing 3D electrodes, see the following document:

- Application Note AN2574: *2D/3D Electrode Design Guide*

5.1 Driven Shield Line

A driven shield trace is recommended to run between the groups of X tracks and the groups of Y tracks, as well as between the combined group of X/Y tracks and Ground. See Section 11.4 “Driven Shield Line” for more information.

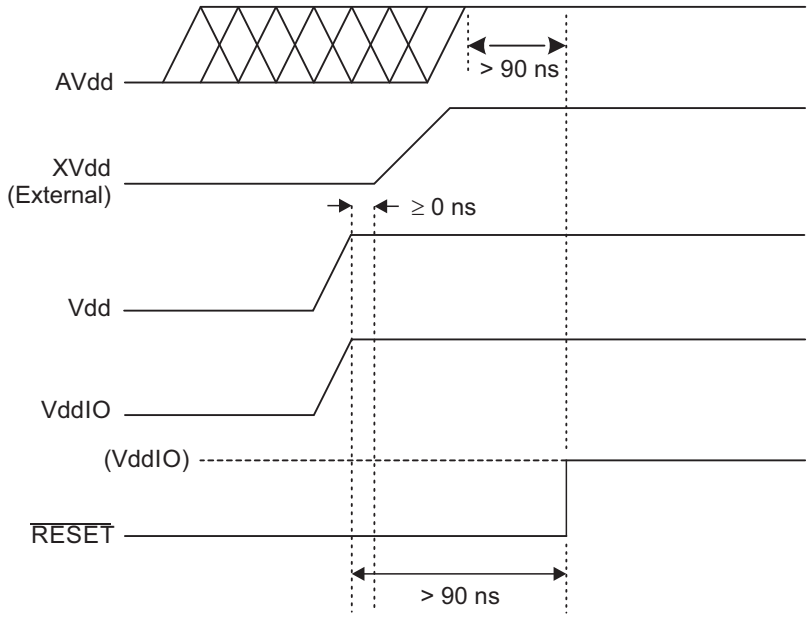
6.0 POWER-UP / RESET REQUIREMENTS

6.1 Power-on Reset

There is an internal Power-on Reset (POR) in the device.

If an external reset is to be used the device must be held in $\overline{\text{RESET}}$ (active low) while the digital (Vdd), analog (AVdd) and digital I/O (VddIO) power supplies are powering up. The supplies must have reached their nominal values before the $\overline{\text{RESET}}$ signal is deasserted (that is, goes high). This is shown in Figure 6-1. See Section 14.2 “Recommended Operating Conditions” for nominal values for the power supplies to the device.

FIGURE 6-1: POWER SEQUENCING ON THE MXT2113TG-Ax



Note: 1) When using external $\overline{\text{RESET}}$ at power-up, VddIO must not be enabled after Vdd.
2) If XVdd is powered from an external supply (not connected to Vdd), XVdd should be powered up after Vdd and must obey the rate-of-rise specification. If XVdd is connected directly to Vdd (3.3V), the two supplies can be brought up together.

CAUTION! XVdd must not be grounded when Vdd is active as damage to the device may result.

When using a boosted external XVdd power supply, Vdd must be applied to the device before the external XVdd supply to ensure that the different power domains in the device are initialized correctly. Typically this can be done by connecting the enable pin of the Switched-Mode Power Supply (SMPS) supplying XVdd to a 10 kΩ pull-up resistor connected to the Vdd, but the XVdd can be controlled separately by the host, if required.

If XVdd is not boosted, XVdd can be connected directly to Vdd to supply 3.3 V, in which case the two supplies can be brought up together.

It is recommended that customer designs include the capability for the host to control all the maXTouch power supplies and pull the $\overline{\text{RESET}}$ line low.

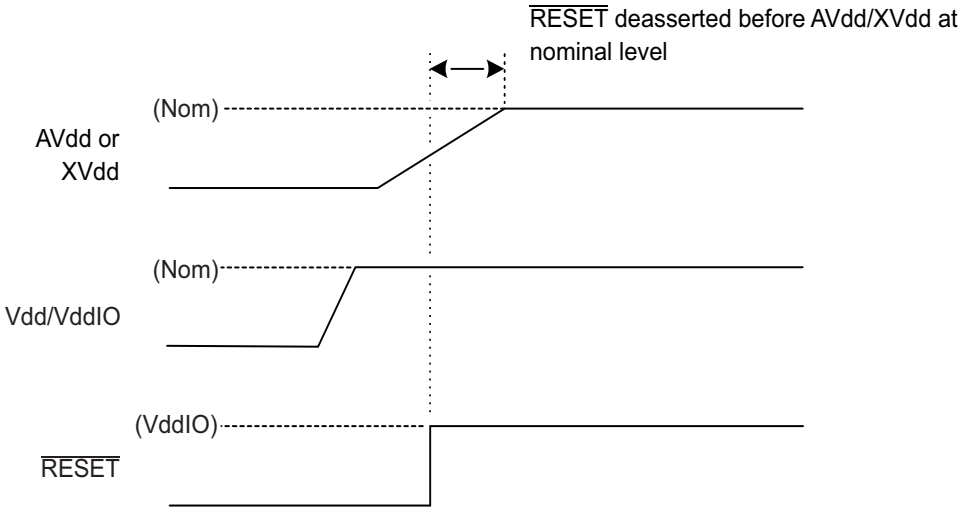
After power-up, the device typically takes 90 ms before it is ready to start communications.

NOTE Device initialization will not complete until after all the power supplies are present. If any power supply is not present, internal initialization stalls and the device will not communicate with the host.

If the RESET line is released before the AVdd or external XVDD supply has reached its nominal voltage (see Figure 6-2), then some additional operations need to be carried out by the host. There are two options open to the host controller:

- Start the part in Deep Sleep mode and then send the command sequence to set the cycle time to wake the part and allow it to run normally. Note that in this case a calibration command is also needed.
- Send a RESET command.

FIGURE 6-2: POWER SEQUENCING ON THE MXT2113TG-Ax – LATE RISE ON AVDD OR XVDD



The RESET pin can be used to reset the device whenever necessary. The RESET pin must be asserted low for at least 90 ns to cause a reset. After the host has released the RESET pin, the device typically takes 90 ms before it is ready to start communications. It is recommended to connect the RESET pin to a host controller to allow the host to initiate a full hardware reset without requiring the mXT2113TG-Ax to be powered down.

WARNING	The device should be reset only by using the RESET line. If an attempt is made to reset by removing the power from the device without also sending the signal lines low, power will be drawn from the communication and I/O lines and the device will not reset correctly.

Make sure that any lines connected to the device are below or equal to Vdd during power-up and power-down. For example, if RESET is supplied from a different power domain to the VDDIO pin, make sure that it is held low when Vdd is off. If this is not done, the RESET signal could parasitically couple power via the RESET pin into the Vdd supply.

NOTE	The voltage level on the RESET pin of the device must never exceed VddIO (digital supply voltage).

A software RESET command (using the Command Processor T6 object) can be used to reset the chip. A software reset typically takes 110 ms before it is ready to start communications. After the chip has finished it asserts the CHG line to signal to the host that a message is available. The reset flag is set in the Command Processor T6 object message data to indicate to the host that it has just completed a reset cycle. This bit can be used by the host to detect any unexpected brownout events. This allows the host to take any necessary corrective actions, such as reconfiguration.

NOTE	The CHG line is briefly set (~100 ms) as an input during power-up or reset. It is therefore particularly important that the line should be allowed to float high via the CHG line pull-up resistor during this period. It should never be driven by the host (see Section 14.6.4 “Reset Timings”).

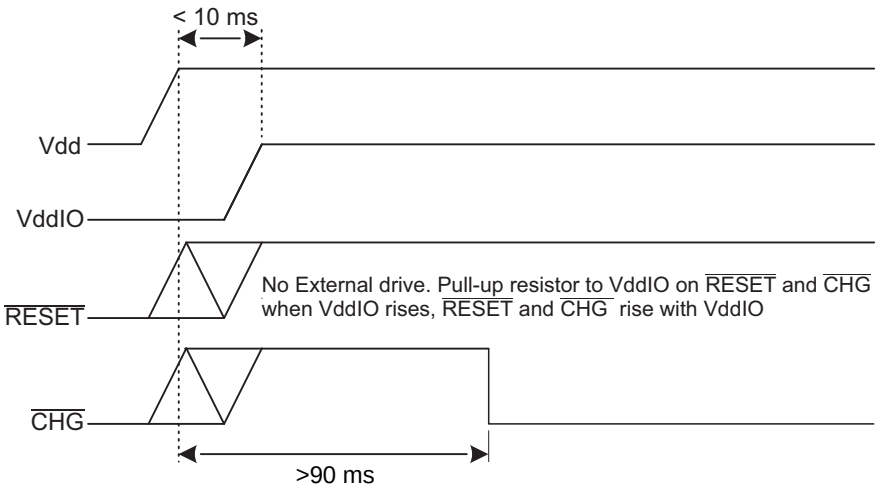
At power-on, the device performs a self-test routine (using the Self Test T25 object) to check for shorts that might cause damage to the device.

6.2 Power-up and Reset Sequence – VddIO Enabled after Vdd

The power-up sequence that can be used in applications where VddIO must be powered up after Vdd, is shown in Figure 6-3.

In this case the communication interface to the maXTouch device is not driven by the host system. The $\overline{\text{RESET}}$ and $\overline{\text{CHG}}$ pins are connected to VddIO using suitable pull-up resistors. Vdd is powered up, followed by VddIO, no more than 10 ms after Vdd. Due to the pull-up resistors, $\overline{\text{RESET}}$ and $\overline{\text{CHG}}$ will rise with VddIO. The internal POR system ensures reliable boot up of the device and the $\overline{\text{CHG}}$ line will go low approximately 90 ms after Vdd to notify the host that the device is ready to start communication.

FIGURE 6-3: POWER-UP SEQUENCE



7.0 DETAILED OPERATION

7.1 Touch Detection

The mXT2113TG-Ax allows for both mutual and self capacitance measurements, with the self capacitance measurements being used to augment the mutual capacitance measurements to produce reliable touch information.

When self capacitance measurements are enabled, touch classification is achieved using both mutual and self capacitance touch data. This has the advantage that both types of measurement systems can work together to detect touches under a wide variety of circumstances.

Mutual capacitance touch data is used wherever possible to classify touches as this has greater granularity than self capacitance measurements and provides positional information on touches.

Self capacitance measurements, on the other hand, allow for the detection of single touches in extreme cases, such as single thick glove touches, when touches can only be detected by self capacitance data and may be missed by mutual capacitance touch detection.

7.2 Operational Modes

The device operates in two modes: **Active** (touch detected) and **Idle** (no touches detected). Both modes operate as a series of burst cycles. Each cycle consists of a short burst (during which measurements are taken) followed by an inactive sleep period. The difference between these modes is the length of the cycles. Those in idle mode typically have longer sleep periods. The cycle length is configured using the IDLEACQINT and ACTVACQINT settings in the Power Configuration T7. In addition, an *Active to Idle Timeout* setting is provided.

7.3 Detection Integrator

The device features a touch detection integration mechanism. This acts to confirm a detection in a robust fashion. A counter is incremented each time a touch has exceeded its threshold and has remained above the threshold for the current acquisition. When this counter reaches a preset limit the sensor is finally declared to be touched. If, on any acquisition, the signal is not seen to exceed the threshold level, the counter is cleared and the process has to start from the beginning.

The detection integrator is configured using the appropriate touch objects (Multiple Touch Touchscreen T100, Key Array T15).

7.4 Sensor Acquisition

The charge time for mutual capacitance measurements is set using the Acquisition Configuration T8 object. The device combines a number of factors together to arrive at the total acquisition time for one drive line (that is, one X line for mutual capacitance acquisitions or one axis for self capacitance acquisitions).

The following constraints apply on the mXT2113TG-Ax:

- The per X line mutual capacitance touch measurement and the per axis self capacitance measurement should not normally exceed 2 ms. Furthermore, the total acquisition time for the sensor as a whole must not exceed 250 ms. In the event of a timeout, a SIGERR may be reported.
- The high and low pulse periods must not exceed 18.63 µs each. This means that the maximum possible burst period is 37.26 µs (that is, a minimum frequency of 26.84 kHz). In addition, the burst period must not be less than 4 µs (that is, a maximum frequency of 250 kHz).

Unpredictable system behavior might occur if any of the above constraints are not met.

Care should be taken to configure all the objects that can affect the measurement timing (for example, 2D drift and noise measurement interval settings) so that these limits are not exceeded.

7.5 Calibration

Calibration is the process by which a sensor chip assesses the background capacitance on each node. Calibration occurs in a variety of circumstances, for example:

- When determined by the mutual capacitance recalibration process, as controlled by the Acquisition Configuration T8 object
- When determined by the self capacitance recalibration process, as controlled by the Self Capacitance Configuration T111 object
- When the Retransmission Compensation T80 object detects calibrated-in moisture has been removed
- Following a Self Capacitance Global Configuration T109 Tune command
- When the host issues a recalibrate command
- When certain configuration settings are changed

7.6 Digital Filtering and Noise Suppression

The mXT2113TG-Ax supports on-chip filtering of the acquisition data received from the sensor. Specifically, the Noise Suppression T72 object provides an algorithm to suppress the effects of noise. This algorithm can automatically adjust some of the acquisition parameters on-the-fly to filter the Analog-to-Digital Conversions (ADCs) received from the sensor.

Additional noise suppression is provided by the Self Capacitance Noise Suppression T108 object. Similar in both design and configuration to the Noise Suppression T72 object, the Self Capacitance Noise Suppression T108 object is the noise suppression interface for self capacitance touch measurements.

Noise suppression is triggered when a noise source is detected.

- The host driver code can indicate when a noise source is present.
- The noise suppression is also triggered based on the noise levels detected using internal line measurements.The Noise Suppression T72 and Self Capacitance Noise Suppression T108 object selects the appropriate controls to suppress the noise present in the system.

7.7 EMC Reduction

The mXT2113TG-Ax has the following mechanisms to help reduce EMC emissions and ensure that the user's product operates within the desired EMC limits:

Spread Spectrum – Varies the burst frequency on each measurement pulse to spread the EMC energy over the frequency domain. This feature is configured by the CTE Configuration T46 object.

- **Configurable Voltage Reference Mode** – Allows for the selection of voltage swing of the self capacitance measurements.This feature is configured by the Self Capacitance Global Configuration T109 object.
- **Input Buffer Power Configuration** – Controls the positive/negative drive strength of the Input Buffer for self capacitance measurements. This feature is configured by the Self Capacitance Global Configuration T109 object.
- **Configurable Input Amplifier Bias** – Controls the Input Amplifier Bias. This feature is configured by the Self Capacitance Global Configuration T109 object.
- **Configurable Wave Shaping** – Controls the voltage modulation on self capacitance scans allows wave shaping of the edge for EMC harmonic control.

7.8 Shieldless Support and Display Noise Suppression

The mXT2113TG-Ax can support shieldless sensor design even with a noisy LCD.

The Optimal Integration feature is not filtering as such, but enables the user to use a shorter integration window. The integration window optimizes the amount of charge collected against the amount of noise collected, to ensure an optimal SNR. This feature also benefits the system in the presence of an external noise source. This feature is configured using the Shieldless T56 object.

Display noise suppression allows the device to overcome display noise simultaneously with external noise. This feature is based on filtering provided by the Lens Bending T65 object (see Section 7.11 "Lens Bending").

7.9 Retransmission Compensation

The device can limit the undesirable effects on the mutual capacitance touch signals caused by poor device coupling to ground, such as poor sensitivity and touch break-up. This is achieved using the Retransmission Compensation T80 object. This object can be configured to allow the touchscreen to compensate for signal degradation due to these undesirable effects. If self capacitance measurements are also scheduled, the Retransmission Compensation T80 object will use the resultant data to enhance the compensation process.

The Retransmission Compensation T80 object is also capable of compensating for water presence on the sensor if self capacitance measurements are scheduled. In this case, both mutual capacitance and self capacitance measurements are used to detect moisture and then, once moisture is detected, self capacitance measurements are used to detect single touches in the presence of moisture.

7.10 Grip Suppression

The device has grip suppression functionality to suppress false detections from a user's grip.

Mutual capacitance grip suppression works by specifying a boundary around a touchscreen, within which touches can be suppressed whilst still allowing touches in the center of the touchscreen. This ensures that an accidental hand touch on the edge is suppressed while still allowing a "real" (finger) touch towards the center of the screen. Mutual capacitance grip suppression is configured using the Grip Suppression T40 object.

Self Capacitance grip suppression works by looking for characteristic shapes in the self capacitance measurement along the touchscreen boundary, and thereby distinguishing between a grip and a touch further into the sensor. Self capacitance grip suppression is configured using the Self Capacitance Grip Suppression T112 object.

7.11 Lens Bending

The device supports algorithms to eliminate disturbances from the measured signal.

When the sensor suffers from the screen deformation (lens bending) the signal values acquired by normal procedure are corrupted by the disturbance component (bend). The amount of bend depends on:

- The mechanical and electrical characteristics of the sensor
- The amount and location of the force applied by the user touch to the sensor

The Lens Bending T65 object measures the bend component and compensates for any distortion caused by the bend. As the bend component is primarily influenced by the user touch force, it can be used as a secondary source to identify the presence of a touch. The additional benefit of the Lens Bending T65 object is that it will eliminate LCD noise as well.

7.12 Glove Detection

The device has glove detection algorithms that process the measurement data received from the touchscreen classifying touches as potential gloved touches.

The Glove Detection T78 object is used to detect glove touches. In Normal Mode the Glove Detection T78 object applies vigorous glove classification to small signal touches to minimize the effect of unintentional hovering finger reporting. Once a gloved touch is found, the Glove Detection T78 object enters Glove Confidence Mode. In this mode the device expects the user to be wearing gloves so the classification process is much less stringent.

7.13 Unintentional Touch Suppression

The Touch Suppression T42 object provides a mechanism to suppress false detections from unintentional touches from a large body area, such as from a face, ear or palm. The Touch Suppression T42 object also provides Maximum Touch Suppression to suppress all touches if more than a specified number of touches has been detected.

7.14 Adjacent Key Suppression Technology

Adjacent Key Suppression (AKS) technology is a patented method used to detect which touch object (Multiple Touch Touchscreen T100 or Key Array T15) is touched, and to suppress touches on the other touch objects, when touch objects are located close together.

The device has two levels of AKS:

- The first level works between the touch objects (Multiple Touch Touchscreen T100 and Key Array T15). The touch objects are assigned to AKS groups. If a touch occurs within one of the touch objects in a group, then touches within other objects inside that group are suppressed. For example, if a touchscreen and a Key Array are placed in the same AKS group, then a touch in the touchscreen will suppress touches in the Key Array, and vice versa. Objects can be in more than one AKS group.
- The second level of AKS is internal AKS within an individual Key Array object. If internal AKS is enabled, then when one key is touched, touches on all the other keys within the Key Array are suppressed. Note that internal AKS is not present on other types of touch objects.

8.0 HOST COMMUNICATIONS

Communication between the mXT2113TG-Ax and the host is achieved using one of the following interfaces:

- I^2C (see Section 9.0 “I2C Communications”)
- SPI (see Section 10.0 “SPI Communications”)

Either host interface can be used, depending on the needs of the user’s project, but only one host interface can be used in any one design.

An I^2C connection is also required between the host and the MXG3141 3D gesture device.

8.1 Host Communication Mode Selection – COMMSEL Pin

The selection of the mXT2113TG-Ax host interface is determined by connecting the COMMSEL pin according to Table 8-1.

TABLE 8-1: HOST INTERFACE SELECTION

COMMSEL	Interface Selected
Connected to GND	SPI
Pulled up to VddIO (1)	I^2C

Note 1: Requires an external pull-up resistor; see Section 2.0 “Schematics” for details

8.2 I^2C Address Selection – ADDSEL Pin

The mXT2113TG-Ax I^2C address is selected by connecting the ADDSEL pin according to Table 8-2.

TABLE 8-2: I^2C ADDRESS SELECTION

ADDSEL	I^2C Address
Connected to GND	0x4A
Pulled up to VddIO (1)	0x4B

Note 1: Requires an external pull-up resistor.

9.0 I²C COMMUNICATIONS

Communication with the mXT2113TG-Ax can be carried out over the I²C interface.

The I²C interface is used in conjunction with the $\overline{\text{CHG}}$ line. The $\overline{\text{CHG}}$ line going active signifies that a new data packet is available. This provides an interrupt-style interface and allows the device to present data packets when internal changes have occurred. See Section 9.5 “CHG Line” for more information.

9.1 I²C Addresses

The mXT2113TG-Ax supports two I²C device addresses that are selected using the ADDSEL line at startup. The two I²C device addresses are 0x4A and 0x4B. The selection of the address (and the communication mode) is described in Section 8.2 “I²C Address Selection – ADDSEL Pin”.

The I²C address is shifted left to form the SLA+W or SLA+R address when transmitted over the I²C interface, as shown in Table 9-1.

TABLE 9-1: FORMAT OF SLA+W/SLA+R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0x4A or 0x4B							Read/write

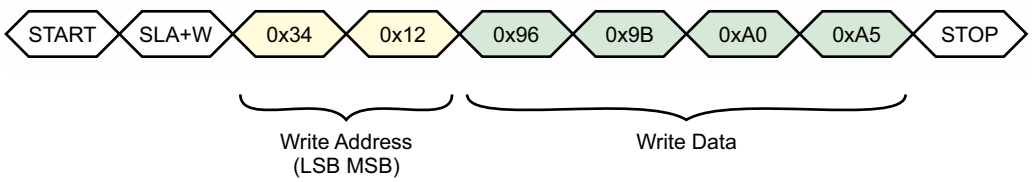
9.2 Writing To the Device

An I²C WRITE cycle consists of the following bytes:

START	1 bit	I²C START condition
SLA+W	1 byte	I²C address of the device (see Section 9.1 “I2C Addresses”)
Address (LSByte, MSByte)	2 bytes	Address of the location at which the data writing starts. This address is stored as the address pointer.
Data	0 or more bytes	The actual data to be written. The data is written to the device, starting at the location of the address pointer. The address pointer returns to its starting value when the I²C STOP condition is detected.
CRC (optional)	1 byte	An optional 8-bit CRC that includes all the bytes that have been sent, including the two address bytes, but not the SLA+W byte. If the device detects an error in the CRC during a write transfer, a COMSERR fault is reported by the Command Processor T6 object. See Section 9.3 “I²C Writes in Checksum Mode” for more details
STOP	1 bit	I²C STOP condition

Figure 9-1 shows an example of writing four bytes of data to contiguous addresses starting at 0x1234.

FIGURE 9-1: EXAMPLE OF A FOUR-BYTE WRITE STARTING AT ADDRESS 0x1234

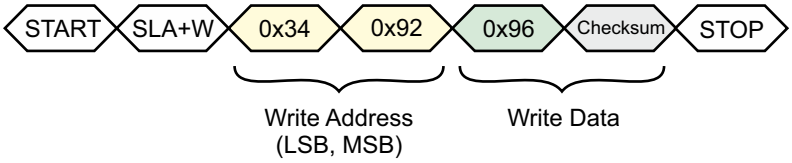


9.3 I²C Writes in Checksum Mode

In I²C checksum mode an 8-bit CRC is added to all I²C writes. The CRC is sent at the end of the data write as the last byte before the STOP condition. All the bytes sent are included in the CRC, including the two address bytes. Any command or data sent to the device is processed even if the CRC fails.

To indicate that a checksum is to be sent in the write, the most significant bit of the MSByte of the write address is set to 1. For example, the I²C command shown in Figure 9-2 writes a value of 150 (0x96) to address 0x1234 with a checksum. The address is changed to 0x**9**234 to indicate checksum mode.

FIGURE 9-2: EXAMPLE OF A WRITE TO ADDRESS 0x1234 WITH A CHECKSUM



9.4 Reading From the Device

Two I^2C bus activities must take place to read from the device. The first activity is an I^2C write to set the address pointer (LSByte then MSByte). The second activity is the actual I^2C read to receive the data. The address pointer returns to its starting value when the read cycle NACK or STOP is detected.

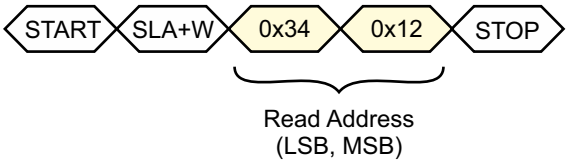
It is not necessary to set the address pointer before every read. The address pointer is updated automatically after every read operation. The address pointer will be correct if the reads occur in order. In particular, when reading multiple messages from the Message Processor T5 object, the address pointer is automatically reset to the address of the Message Processor T5 object, in order to allow continuous reads (see Section 9.4.2 “Reading Status Messages with DMA”).

The WRITE and READ cycles consist of a START condition followed by the I^2C address of the device (SLA+W or SLA+R respectively).

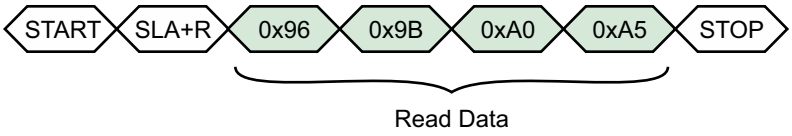
Figure 9-3 shows the I^2C commands to read four bytes starting at address 0x1234.

FIGURE 9-3: EXAMPLE OF A FOUR-BYTE READ STARTING AT ADDRESS 0x1234

Set Address Pointer



Read Data



NOTE	At least one data byte must be read during an I^2C READ transaction; it is illegal to abort the transaction with an I^2C STOP condition without reading any data.

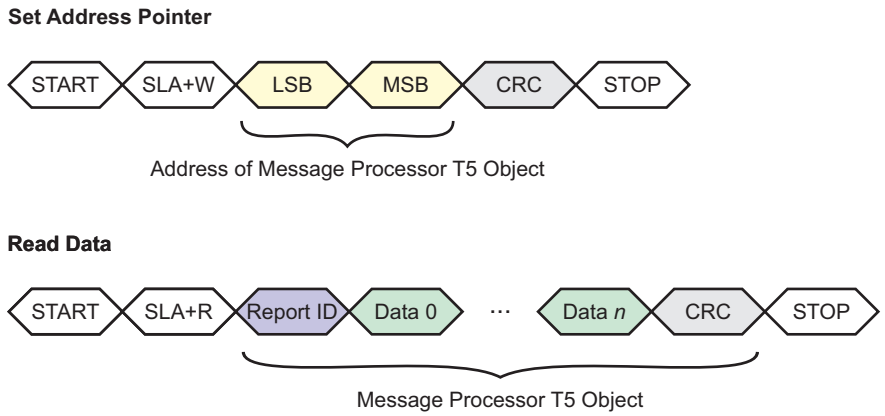
9.4.1 READING A MESSAGE FROM THE MESSAGE PROCESSOR T5 OBJECT

An I^2C read of the Message Processor T5 object contains the following bytes:

START	1 bit	I^2C START condition
SLA+R	1 byte	I^2C address of the device (see Section 9.1 “I2C Addresses”)
Report ID	1 byte	Message report ID
Data	1 or more bytes	The message data (size = size of Message Processor T5 MESSAGE field)
CRC (optional)	1 byte	An 8-bit CRC (if requested) for the Message Processor T5 report ID and message data See Section 9.3 “I^2C Writes in Checksum Mode” for more details on how to request a checksum
STOP	1 bit	I^2C STOP condition

Figure 9-4 shows an example read from the Message Processor T5 object. To read multiple messages using Direct Memory Access, see Section 9.4.2 “Reading Status Messages with DMA”.

FIGURE 9-4: EXAMPLE READ FROM MESSAGE PROCESSOR T5 WITH A CHECKSUM



9.4.2 READING STATUS MESSAGES WITH DMA

The device facilitates the easy reading of multiple messages using a single continuous read operation. This allows the host hardware to use a Direct Memory Access (DMA) controller for the fast reading of messages, as follows:

1. The host uses a write operation to set the address pointer to the start of the Message Count T44 object, if necessary. Note that the STOP condition at the end of the read resets the address pointer to its initial location, so it may already be pointing at the Message Count T44 object following a previous message read. If a checksum is required on each message, the most significant bit of the MSByte of the read address must be set to 1.
2. The host starts the read operation of the message by sending a START condition.
3. The host reads the Message Count T44 object (one byte) to retrieve a count of the pending messages.
4. The host calculates the number of bytes to read by multiplying the message count by the size of the Message Processor T5 object. Note that the host should have already read the size of the Message Processor T5 object in its initialization code.

   Note that the size of the Message Processor T5 object as recorded in the Object Table includes a checksum byte. If a checksum has not been requested, one byte should be deducted from the size of the object. That is: number of bytes = count × (size – 1).
5. The host reads the calculated number of message bytes. It is important that the host does *not* send a STOP condition during the message reads, as this will terminate the continuous read operation and reset the address pointer. No START and STOP conditions must be sent between the messages.
6. The host sends a STOP condition at the end of the read operation after the last message has been read. The NACK condition immediately before the STOP condition resets the address pointer to the start of the Message Count T44 object.

Figure 9-5 shows an example of using a continuous read operation to read three messages from the device without a checksum. Figure 9-6 shows the same example with a checksum.

FIGURE 9-5: CONTINUOUS MESSAGE READ EXAMPLE – NO CHECKSUM

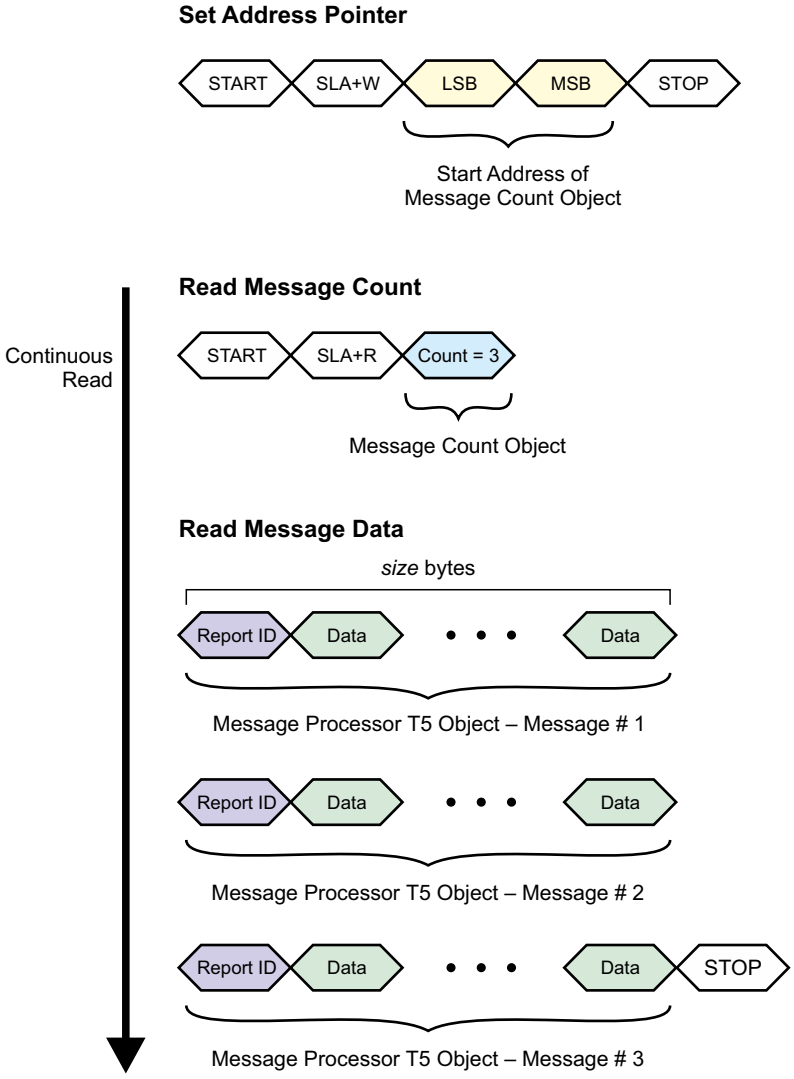
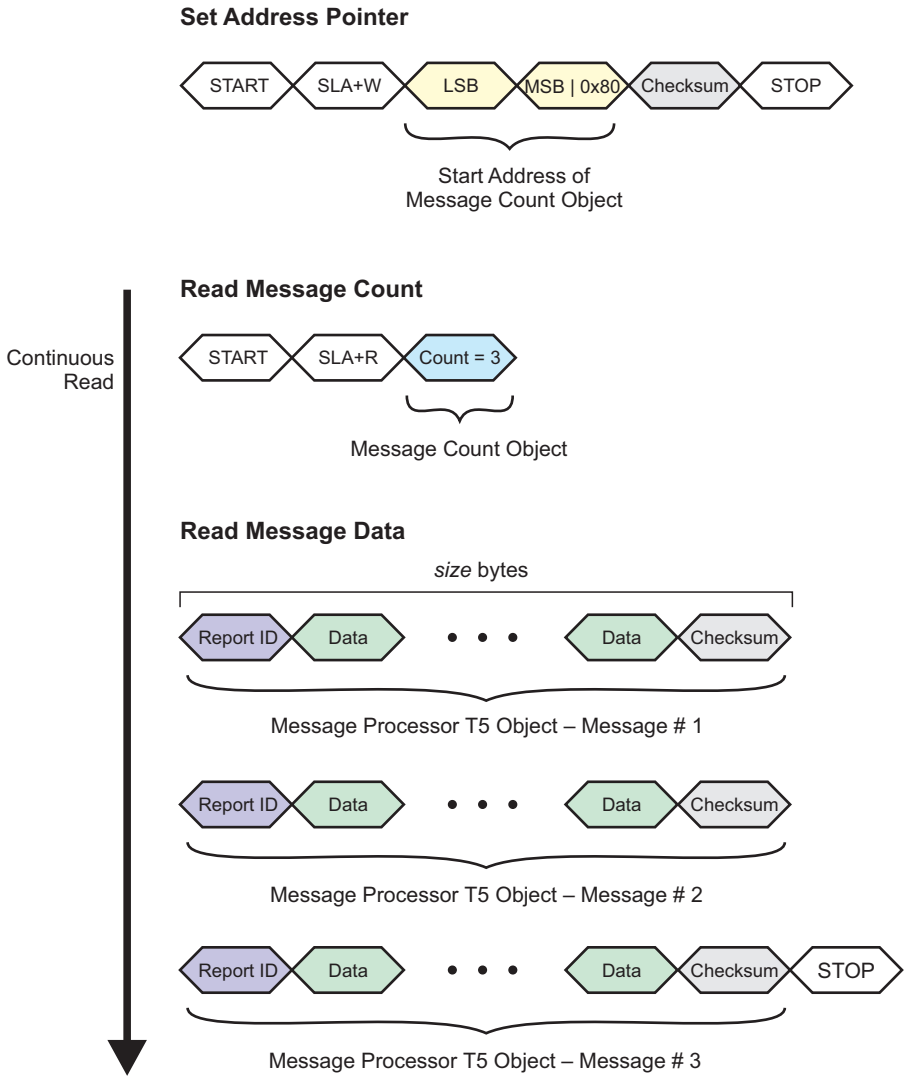


FIGURE 9-6: CONTINUOUS MESSAGE READ EXAMPLE – I²C CHECKSUM MODE



9.5 $\overline{\text{CHG}}$ Line

The $\overline{\text{CHG}}$ line is an active-low, open-drain output that is used to alert the host that a new message is available in the Message Processor T5 object. This provides the host with an interrupt-style interface with the potential for fast response times. It reduces the need for wasteful I²C communications.

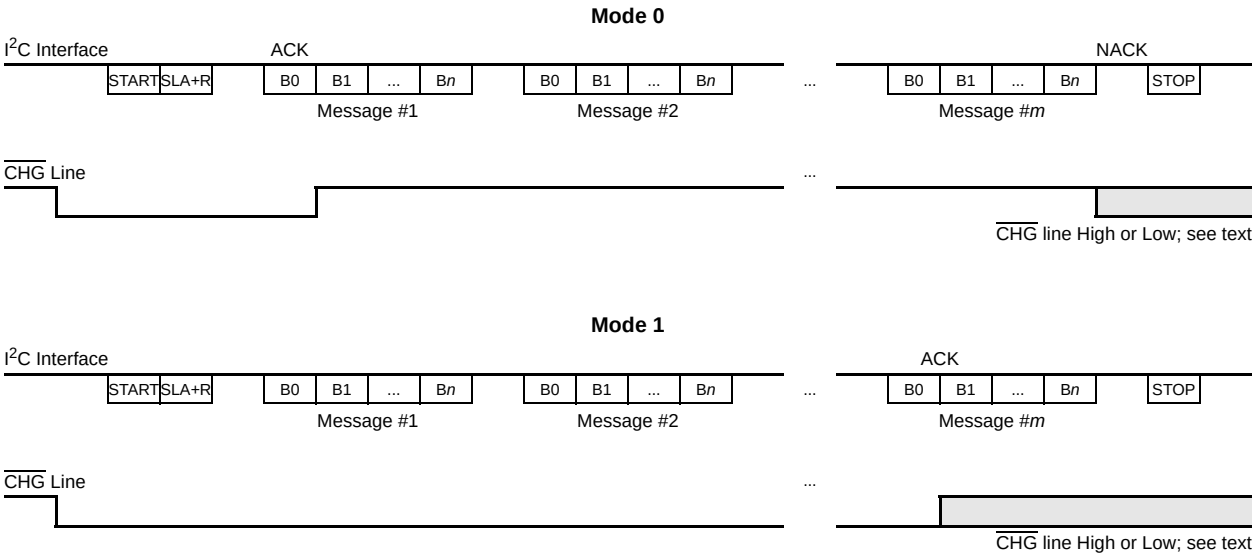
NOTE	The host should always use the $\overline{\text{CHG}}$ line as an indication that a message is ready to be read from the Message Processor T5 object; the host should never poll the device for messages.

The $\overline{\text{CHG}}$ line should always be configured as an input on the host during normal usage. This is particularly important after power-up or reset (see Section 6.0 “Power-up / Reset Requirements”).

A pull-up resistor is required to VddIO (see Section 2.0 “Schematics”).

The $\overline{\text{CHG}}$ line operates in two modes when it is used with I²C communications, as defined by the Communications Configuration T18 object.

FIGURE 9-7: $\overline{\text{CHG}}$ LINE MODES FOR I²C-COMPATIBLE TRANSFERS



In Mode 0 (edge-triggered operation):

1. The $\overline{\text{CHG}}$ line goes low to indicate that a message is present.
2. The $\overline{\text{CHG}}$ line goes high when the first byte of the first message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the buffer.
3. The STOP condition at the end of an I²C transfer causes the $\overline{\text{CHG}}$ line to stay high if there are no more messages. Otherwise the $\overline{\text{CHG}}$ line goes low to indicate a further message.

Note that Mode 0 also allows the host to continually read messages by simply continuing to read bytes back without issuing a STOP condition. Message reading should end when a report ID of 255 (“invalid message”) is received. Alternatively the host ends the transfer by sending a NACK after receiving the last byte of a message, followed by a STOP condition. If there is another message present, the $\overline{\text{CHG}}$ line goes low again, as in step 1. In this mode the state of the $\overline{\text{CHG}}$ line does not need to be checked during the I²C read.

In Mode 1 (level-triggered operation):

1. The $\overline{\text{CHG}}$ line goes low to indicate that a message is present.
2. The $\overline{\text{CHG}}$ line remains low while there are further messages to be sent after the current message.
3. The $\overline{\text{CHG}}$ line goes high again only once the first byte of the last message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the output buffer.

Mode 1 allows the host to continually read the messages until the $\overline{\text{CHG}}$ line goes high, and the state of the $\overline{\text{CHG}}$ line determines whether or not the host should continue receiving messages from the device.

NOTE	The state of the $\overline{\text{CHG}}$ line should be checked only between messages and not between the bytes of a message. The precise point at which the $\overline{\text{CHG}}$ line changes state cannot be predicted and so the state of the $\overline{\text{CHG}}$ line cannot be guaranteed between bytes.

The Communications Configuration T18 object can be used to configure the behavior of the $\overline{\text{CHG}}$ line. In addition to the $\overline{\text{CHG}}$ line operation modes described above, this object allows direct control over the state of the $\overline{\text{CHG}}$ line.

9.6 SDA and SCL

The I²C bus transmits data and clock with SDA and SCL, respectively. These are open-drain. The device can only drive these lines low or leave them open. The termination resistors (Rp) pull the line up to VddIO if no I²C device is pulling it down.

The termination resistors should be chosen so that the rise times on SDA and SCL meet the I²C specifications for the interface speed being used, bearing in mind other loads on the bus. For best latency performance, it is recommended that no other devices share the I²C bus with the maXTouch controller.

9.7 Clock Stretching

The device supports clock stretching in accordance with the I^2C specification. It may also instigate a clock stretch if a communications event happens during a period when the device is busy internally. The maximum clock stretch is 2 ms and typically less than 350 µs.

The device has an internal bus monitor that can reset the internal I^2C hardware if either SDA or SCL is stuck low for more than 200 ms. This means that if a prolonged clock stretch of more than 200 ms is seen by the device, then any ongoing transfers with the device may be corrupted.

The bus monitor is enabled or disabled using the Communications Configuration T18 object.

10.0 SPI COMMUNICATIONS

10.1 Communications Protocol

Communication with the mXT2113TG-Ax can be carried out over the Serial Peripheral Interface (SPI). The host communicates with the mXT2113TG-Ax over the SPI using a host-client relationship, with the mXT2113TG-Ax acting in client mode.

10.2 SPI Operation

The SPI uses four logic signals:

- **Serial Clock (SCK)** – output from the host.
- **Host Output, Client Input (MOSI)** – output from the host, input to the mXT2113TG-Ax. Used by the host to send data to the mXT2113TG-Ax.
- **Host Input, Client Output (MISO)** – input to the host, output from the mXT2113TG-Ax. Used by the mXT2113TG-Ax to send data to the host.
- **Chip Select ($\overline{SS}$)** – active low output from the host.

In addition the following pin is used:

- **Change Line ($\overline{CHG}$ line)** – active low input to the host, output from the mXT2113TG-Ax. Used by the mXT2113TG-Ax to indicate that a response is ready for transmission (see Section 10.2.1 “CHG Line”) or that an OBP message is ready to be read.

The host pulls $\overline{SS}$ low at the start of the SPI transaction and it remains low until the end of it.

At each byte, the host generates 8 clock pulses on SCK. With these 8 clock pulses, a byte of data is transmitted from the host to the client over MOSI, most significant bit first.

Simultaneously a byte of data is transmitted from the client to the host over MISO, also most significant bit first.

The mXT2113TG-Ax requires that the clock idles “high” (CPOL=1). The data on MOSI and MISO pins are set at the falling edges and sampled at the rising edges (CPHA=1). This is known as SPI Mode 3.

The mXT2113TG-Ax SPI interface can operate at a SCK frequency of up to 8 MHz.

NOTE	**The SPI interface is used in half duplex mode, even though it is a full duplex communication bus by its nature.** This simplifies the protocol, minimizes the CPU processing required and avoids possible timing critical scenarios. This means that only one of the two in/out data lines (MOSI/MISO) will be meaningful at a time. During a read operation, therefore, the host must transmit 0xFF bytes on the MOSI line while it is reading data from the device. Similarly, during a write operation, the host must ignore the data on the MISO line.

An SPI transaction is considered as initiated when the $\overline{SS}$ line is asserted (active low) by the host and terminated when it is deasserted. The host can abort a transfer at any time by deasserting the $\overline{SS}$ line.

10.2.1 $\overline{CHG}$ LINE

The $\overline{CHG}$ line line is an active-low, open-drain output that is used as an interrupt to alert the host that the client is ready to send a response or that an OBP message is pending and ready to be read from the host.

The change line must be handled by the host as a falling edge triggered line. It must not be used a level triggered line. This avoids the situation in which the host initiates a new read/write operation (because the interrupt line is still asserted following a previous SPI transaction) but the target is not yet ready to handle it.

To prevent the host missing an interrupt, the target device can use a retriggering mechanism for the interrupt line. This guarantees that any pending message is always delivered. This mechanism must be enabled in the Communications Configuration T18 object.

10.2.2 SPI PROTOCOL OPCODES

The allowed operations and responses codes used by the SPI protocol are shown in Table 10-1.

TABLE 10-1: SPI OPCODES

Name	Value	Operation
Write Operation and Responses (see Section 10.3 “Write Operation and Responses”)		
SPI_WRITE_REQ	0x01	Write operation request
SPI_WRITE_OK	0x81	Write operation succeeded (response)
SPI_WRITE_FAIL	0x41	Write operation failed (response)
Read Operation and Responses (see Section 10.4 “Read Operation and Responses”)		
SPI_READ_REQ	0x02	Read operation request
SPI_READ_OK	0x82	Read operation succeeded (response)
SPI_READ_FAIL	0x42	Read operation failed (response)
General Responses (see Section 10.5 “General Operations”)		
SPI_INVALID_REQ	0x04	Invalid operation (response)
SPI_INVALID_CRC	0x08	Invalid CRC (response)

All the responses reported in Table 10-1 require the Interrupt line to go from inactive (deasserted) to active (asserted) before the host can read a response following an SPI_READ_REQ or SPI_WRITE_REQ operation.

10.2.3 SPI TRANSACTION HEADER

Every SPI transaction includes a 6-byte HEADER that has the format shown in Table 10-2.

TABLE 10-2: HEADER FORMAT

Byte	Field	Description
0	Opcode	Op code for the transaction
1	Address LSByte	The memory address of the client device where the host wants to write to or read from.
2	Address MSByte	
3	Length LSByte	The number of bytes that the host wants to write to or read from the client device.
4	Length MSByte	
5	CRC	8-bit CRC

An 8-bit CRC is used to detect errors on the 5 bytes of the header (that is: Opcode, Address LSB, Address MSB, Length LSByte, Length MSByte) in order to prevent the writing to or reading from unwanted objects if the header gets corrupted during the SPI transfer. The 8-bit CRC algorithm is the same as that used to calculate the CRC for Message Processor T5 messages.

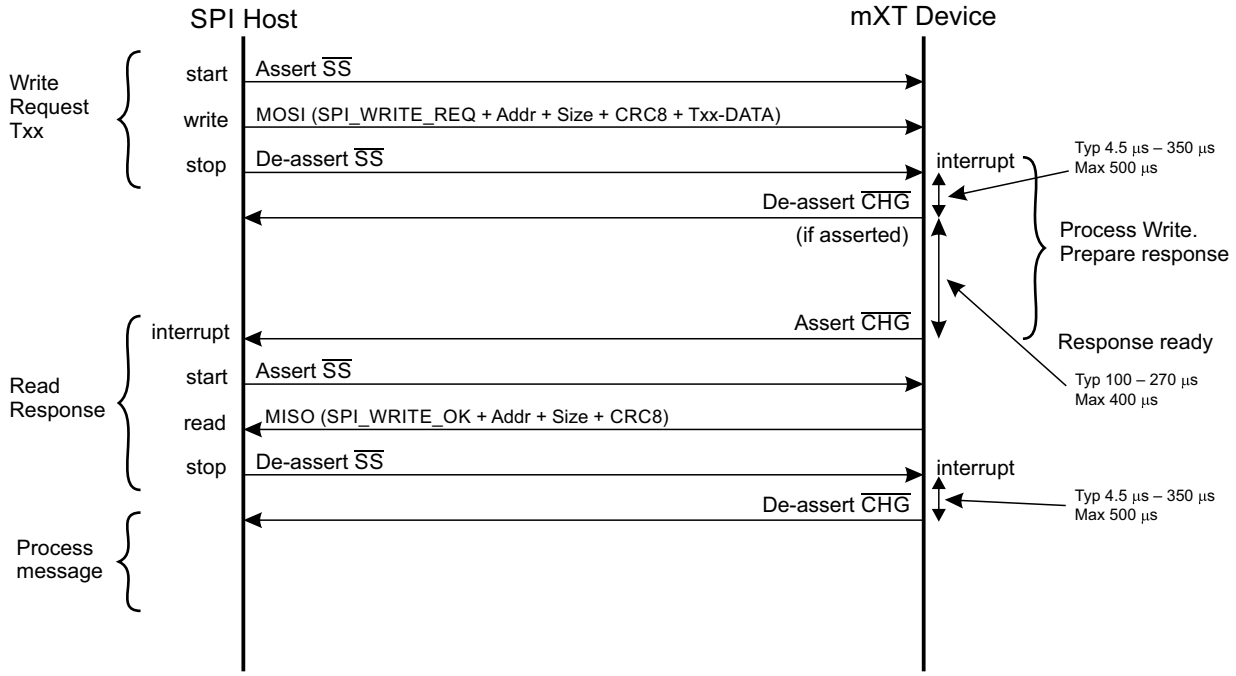
10.3 Write Operation and Responses

The write operation and its responses allows the host to write to an object configuration area.

The flow and timing are shown in Figure 10-1.

Note that no detection mechanism is provided at the SPI network layer level on the data written, but the host can check the correctness of the data that is read back by using a checksum. This allows the host to detect whether the payload of the write operation was corrupted or not during the SPI transaction (see Figure 10-5 on page 40).

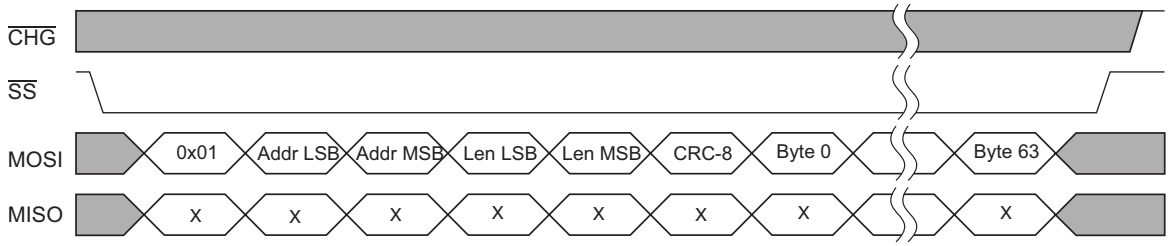
FIGURE 10-1: SPI WRITE CONFIGURATION MESSAGE FLOW AND TIMING



10.3.1 SPI_WRITE_REQ

Figure 10-2 shows the message format used for the write request operation.

FIGURE 10-2: SPI_WRITE_REQ



In Figure 10-2:

- **0x01** is the opcode
- **Addr LSB and Addr MSB** together specify the address to which the host wishes to write
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the host wishes to write to the device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC
- **Byte 0 .. Byte 63** contain the data that is to be written (64 bytes maximum).

If the host needs to write more than 64 bytes of data then multiple SPI_WRITE_REQ operations are required.

Following an SPI_WRITE_REQ operation, the host must wait for a response from the device before accessing the SPI bus again. If the client system does not assert the interrupt line within 10 ms, a hardware reset or a retry from the host is necessary. When the response is ready to be sent, the target device asserts the interrupt line to notify the host that a message is ready to be read. Only at this point is the host allowed to initiate a new SPI transaction to read back the response related to the previous write operation.

This means that an object message will be blocked during the time that a response related to a previous read or write request is pending and has not yet been read back by the host.

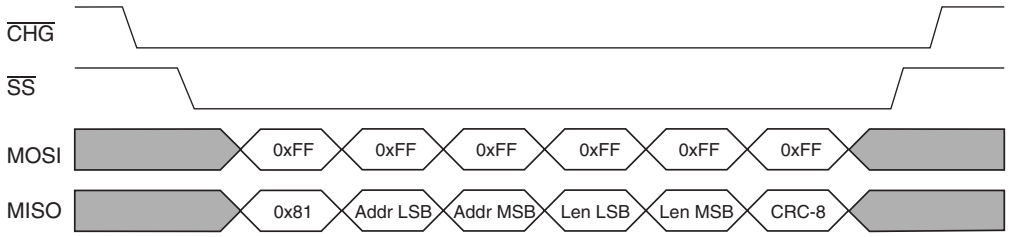
The following responses are possible following an SPI_WRITE_REQ operation:

- **SPI_WRITE_OK** – Generated if the write operation was successfully completed (the memory address and length specified by the host were within the allowed accessible memory map regions). See Section 10.3.2 “SPI_WRITE_OK”
- **SPI_WRITE_FAIL** – Generated if the write operation failed, for example if the host tries to write to an address outside the available memory map. See Section 10.3.3 “SPI_WRITE_FAIL”
- **SPI_INVALID_REQ** – See Section 10.5.1 “SPI_INVALID_REQ”
- **SPI_INVALID_CRC** – See Section 10.5.2 “SPI_INVALID_CRC”

10.3.2 SPI_WRITE_OK

Figure 10-3 shows the message format used for the write OK response.

FIGURE 10-3: SPI_WRITE_OK



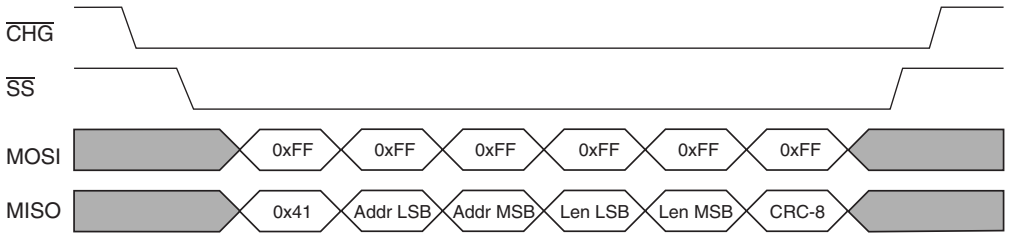
In Figure 10-3:

- **0x81** is the opcode
- **Addr LSB and Addr MSB** together specify the address to which the data was written
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that was written to the device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC

10.3.3 SPI_WRITE_FAIL

Figure 10-4 shows the message format used for the write fail response.

FIGURE 10-4: SPI_WRITE_FAIL



In Figure 10-4:

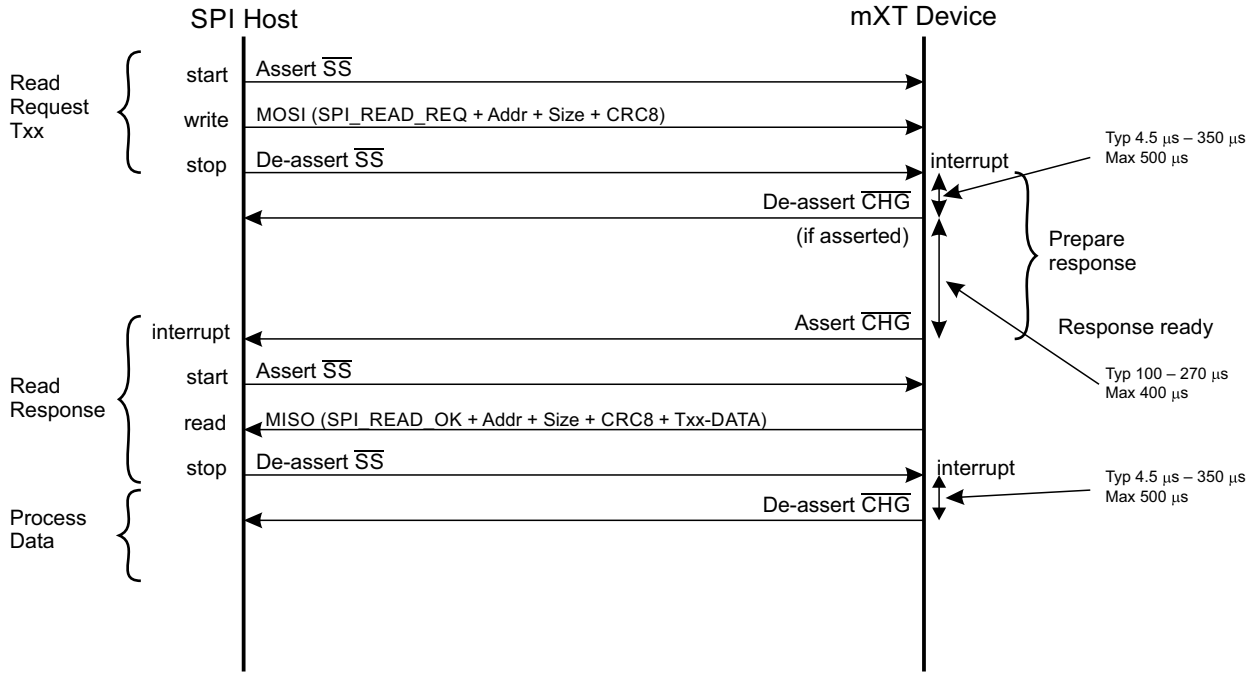
- **0x41** is the opcode
- **Addr LSB and Addr MSB** together specify the address to which the host requested the write
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the host attempted to write to the device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC

10.4 Read Operation and Responses

The read request operation allows the host to read from the object memory map for the device. This allows the host to read a message from the Message Processor T5 object or read from an object configuration area.

The flow and timing are shown in Figure 10-5.

FIGURE 10-5: SPI READ CONFIGURATION MESSAGE FLOW AND TIMING



Normally a limit of 64 bytes is allowed for data reads. If the host tries to read more than 64 bytes, the client returns SPI_READ_FAIL (see Section 10.4.3 “SPI_READ_FAIL”). A mechanism is provided, however, that supports the DMA transfer of a large block of data that exceeds this limit. This is achieved by the provision of multiple instances of the Data Container T117 object within the device that allow up to 5832 bytes of data to be read in a contiguous manner.

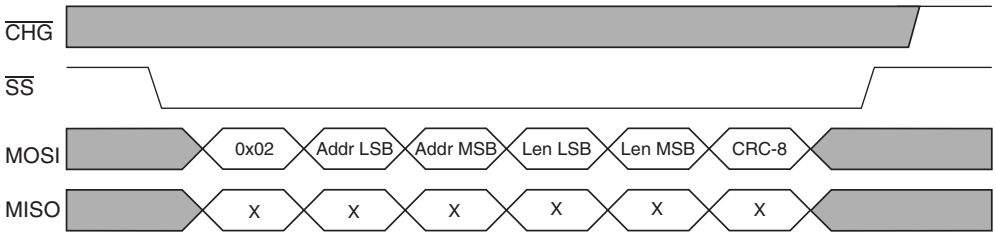
Under certain circumstances, a CRC can be used as an error detection mechanism when reading an object:

- Message Processor T5 – When reading a message from the Message Processor T5 object, an optional CRC as an error detection mechanism is provided. This is enabled in the Message Processor T5 object.
- Data Container T117 – When performing a block data transfer from Data Container T117 instances, the header bytes within the data can be configured to provide a CRC for some types of data.
- All other objects – When reading from any other object configuration area, no error detection mechanism is provided, as this operation is typically performed only at system startup. It is possible, however, to verify a read operation by performing it twice and comparing the results.

10.4.1 SPI_READ_REQ

Figure 10-6 shows the message format used for the read request operation.

FIGURE 10-6: SPI_READ_REQ



The SPI_READ_REQ operation can be initiated by the host at any time, regardless of the state of the interrupt line. The device will assert the interrupt line when there are object messages pending. When the host asserts $\overline{SS}$ (whether to respond to the client asserting the interrupt line or because the host wants to initiate a transaction), the interrupt line is deasserted until the message from the host has been received and processed.

In Figure 10-6:

- **0x02** is the opcode
- **Addr LSB and Addr MSB** together specify the address from which the host wishes to read
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes (excluding the header bytes) that the host wishes to read from the device. The limit is 64 bytes for normal reads, and 5832 maximum for a block data transfer from Data Container T117 instances
- **CRC-8** is the 8-bit CRC

The actual data is sent in the subsequent SPI_READ_OK operation.

Following an SPI_READ_REQ operation, the host must wait for a response to be ready from the device before accessing the SPI bus again. If the client system does not assert the interrupt line within 10 ms, a HW reset or a retry from the host is necessary. When the response is ready to be sent, the target device asserts the interrupt line to notify the host that a message is ready to be read. Only at this point is the host allowed to initiate a new SPI transaction to read back the response related to the previous write operation.

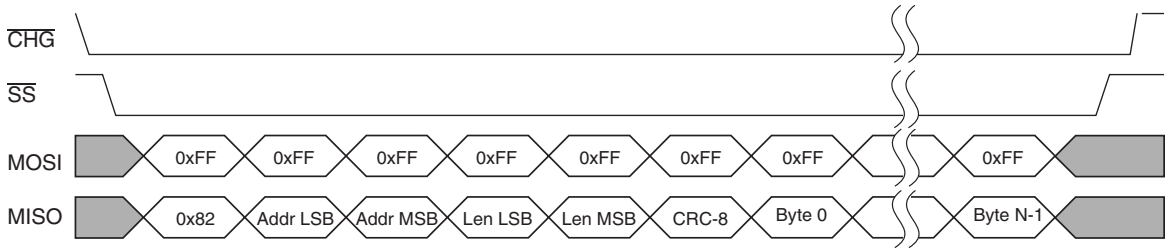
The following responses are possible following an SPI_READ_REQ operation:

- **SPI_READ_OK** – Generated if the read operation was successfully completed (the memory address and length specified by the host were within the allowed accessible memory map regions). See Section 10.4.2 “SPI_READ_OK”
- **SPI_READ_FAIL** – Generated if the read operation failed, for example if the host tries to read from an address outside the available memory map. See Section 10.4.3 “SPI_READ_FAIL”
- **SPI_INVALID_REQ** – See Section 10.5.1 “SPI_INVALID_REQ”
- **SPI_INVALID_CRC** – See Section 10.5.2 “SPI_INVALID_CRC”

10.4.2 SPI_READ_OK

Figure 10-7 shows the message format used for the read OK response.

FIGURE 10-7: SPI_READ_OK



In Figure 10-7:

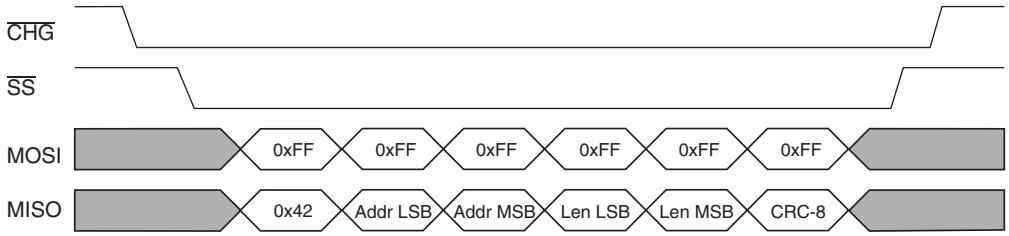
- **0x82** is the opcode
- **Addr LSB and Addr MSB** together specify the address from which the host requested the data should be read
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the host requested to read from the device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC
- **Byte 0 .. Byte N-1** contain the data that is to be written, where *N* the number of bytes (maximum 64 bytes for normal reads, and 5832 for block data transfers from Data Container T117 instances)

Note that, although the device flushes the transmit buffer when the host performs a read operation, any attempt by the host to read more data than expected (that is, greater than Len bytes) could cause the device to transmit junk data on the MISO line.

10.4.3 SPI_READ_FAIL

Figure 10-8 shows the message format used for the read fail response.

FIGURE 10-8: SPI_READ_FAIL



In Figure 10-8:

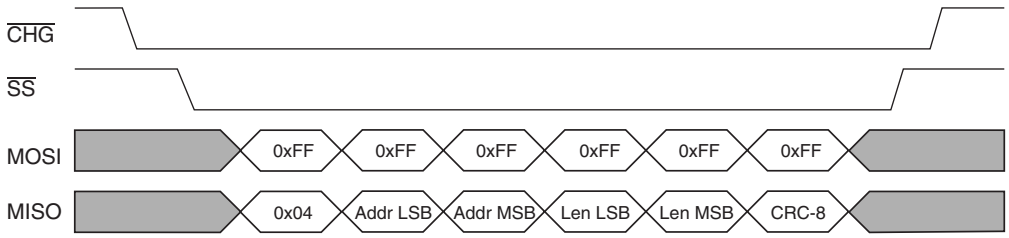
- **0x42** is the opcode
- **Addr LSB and Addr MSB** together specify the address from which the host requested the data should be read
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the host attempted to read from the device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC

10.5 General Operations

10.5.1 SPI_INVALID_REQ

Figure 10-9 shows the message format used for the Invalid Request response. The purpose of this opcode is to report to the host that the opcode of the last request was not recognized or that the host has tried to perform another read or write operation without waiting for the response from the previous request.

FIGURE 10-9: SPI_INVALID_REQ



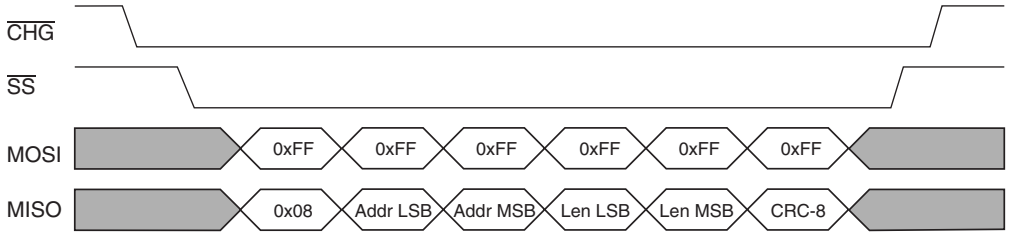
In Figure 10-9:

- **0x04** is the opcode
- **Addr LSB and Addr MSB** together specify the address received in the invalid request
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the host attempted to read from or write to from the device (excluding the header bytes)
- **CRC-8** is the 8-bit CRC

10.5.2 SPI_INVALID_CRC

Figure 10-10 shows the message format used for the Invalid CRC response. The purpose of this opcode is to report an error in the CRC check performed on the received data.

FIGURE 10-10: SPI_INVALID_CRC



In Figure 10-10:

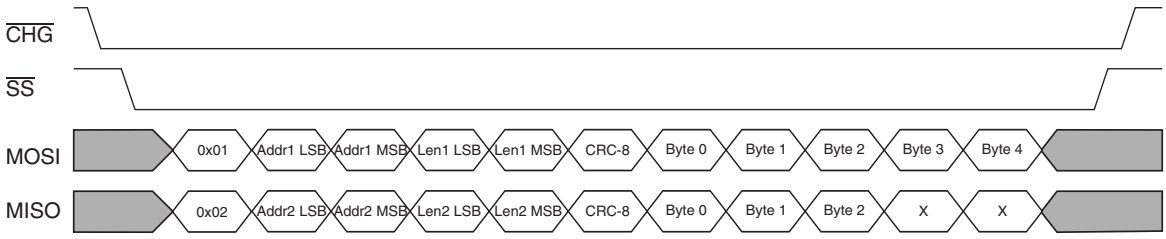
- **0x08** is the opcode
- **Addr LSB and Addr MSB** together specify the address received in the last request
- **Len LSB and Len MSB** together specify the length of the data in bytes. This is the total number of bytes that the host attempted to read from or write to from the device in the last request (excluding the header bytes)
- **CRC-8** is the 8-bit CRC

10.6 Example of a Failed Transaction

In order to prevent unpredictable system behavior, the host *must* always wait for the response of the last request issued to be ready before initiating a new SPI request transaction. If the host does not comply with the protocol specification, clashes can occur.

For example, Figure 10-11 shows the situation in which an SPI_READ_OK (0x82) response with a payload of 3 bytes is expected, but the host performs an SPI_WRITE_ REQ (0x01) operation instead to write 5 bytes to address *Addr1*. In this case, the device outputs the SPI_READ_OK data on the MISO line (this will have been prepared in advance before the interrupt line was asserted) and ignores the new host request received on the MOSI line. The device will send the host an SPI_INVALID_REQ response, in response to the following read or write request, to indicate a violation of the SPI protocol.

FIGURE 10-11: EXAMPLE CLASH – SPI_WRITE_REQ WHEN SPI_READ_OK IS EXPECTED



11.0 PCB DESIGN CONSIDERATIONS

11.1 Introduction

The following sections give the design considerations that should be adhered to when designing a PCB layout for use with the mXT2113TG-Ax. Of these, power supply and ground tracking considerations are the most critical.

By observing the following design rules, and with careful preparation for the PCB layout exercise, designers will be assured of a far better chance of success and a correctly functioning product.

11.2 Printed Circuit Board

Microchip recommends the use of a four-layer printed circuit board for mXT2113TG-Ax applications. This, together with careful layout, will ensure that the board meets relevant EMC requirements for both noise radiation and susceptibility, as laid down by the various national and international standards agencies.

11.2.1 PCB CLEANLINESS

Modern no-clean-flux is generally compatible with capacitive sensing circuits.

CAUTION!	If a PCB is reworked to correct soldering faults relating to any device, or to any associated traces or components, be sure that you fully understand the nature of the flux used during the rework process. Leakage currents from hygroscopic ionic residues can stop capacitive sensors from functioning. If you have any doubts, a thorough cleaning after rework may be the only safe option.

11.3 Power Supply

11.3.1 SUPPLY QUALITY

While the device has good Power Supply Rejection Ratio properties, poorly regulated and/or noisy power supplies can significantly reduce performance.

Particular care should be taken of the AVdd supply, as it supplies the sensitive analog stages in the device.

11.3.2 SUPPLY RAILS AND GROUND TRACKING

Power supply and clock distribution are the most critical parts of any board layout. Because of this, it is advisable that these be completed before any other tracking is undertaken. After these, supply decoupling, and analog and high speed digital signals should be addressed. Track widths for all signals, especially power rails should be kept as wide as possible in order to reduce inductance.

The Power and Ground planes themselves can form a useful capacitor. Flood filling for either or both of these supply rails, therefore, should be used where possible. It is important to ensure that there are no floating copper areas remaining on the board: all such areas should be connected to the ground plane. The flood filling should be done on the outside layers of the board.

11.3.3 POWER SUPPLY DECOUPLING

Decoupling capacitors should be fitted as specified in Section 2.3 “Schematic Notes”.

The decoupling capacitors must be placed as close as possible to the pin being decoupled. The traces from these capacitors to the respective device pins should be wide and take a straight route. They should be routed over a ground plane as much as possible. The capacitor ground pins should also be connected directly to a ground plane.

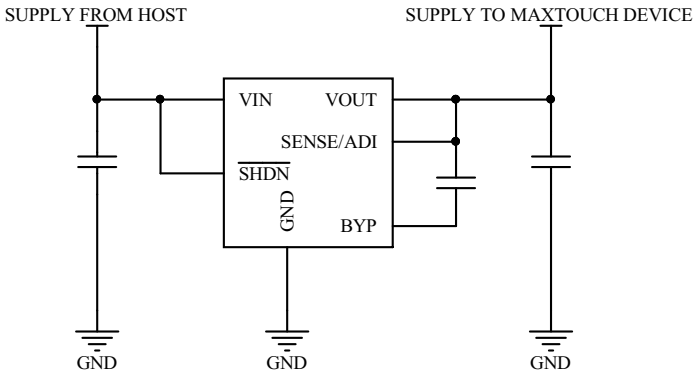
Surface mounting capacitors are preferred over wire-leaded types due to their lower ESR and ESL. It is often possible to fit these decoupling capacitors underneath and on the opposite side of the PCB to the digital ICs. This will provide the shortest tracking, and most effective decoupling possible.

11.3.4 VOLTAGE REGULATORS

Each supply rail requires a Low Drop-Out (LDO) voltage regulator, although an LDO can be shared where supply rails share the same voltage level.

Figure 11-1 shows an example circuit for an LDO.

FIGURE 11-1: EXAMPLE LDO CIRCUIT



An LDO regulator should be chosen that provides adequate output capability, low noise, no-load stability, good load regulation and step response. The mXT2113TG-Ax has been qualified for use only with the Microchip LDOs listed in Table 11-1 and Microchip cannot guarantee the functionality or performance of this maXTouch controller with any other LDO. If an alternative LDO is needed in the user's product, please check with your local Microchip representative concerning its suitability.

NOTE	Microchip recommends that a minimum of a 1.0 µF ceramic, low ESR capacitor at the input and output of these devices is always used. The datasheet for the device should always be referred to when selecting capacitors and the typical recommended values, types and dielectrics adhered to. A"soft-start" regulator with excellent noise and load step regulation will be needed to satisfy the XVdd supply requirements. 1% resistors should be used to define the nominal output voltage. If 5% resistors are used, the nominal XVdd voltage must be reduced accordingly to ensure that the recommended voltage range is adhered to.

TABLE 11-1: LDO REGULATORS – QUALIFIED FOR USE

Manufacturer	Device	Current Rating (mA)
Microchip Technology Inc.	MCP1824	300
Microchip Technology Inc.	MCP1824S	300
Microchip Technology Inc.	MAQ5300	300
Microchip Technology Inc.	MCP1725	500

11.3.5 SINGLE SUPPLY OPERATION

When designing a PCB for an application using a single LDO, extra care should be taken to ensure short, low inductance traces between the supply and the touch controller supply input pins. Ideally, tracking for the individual supplies should be arranged in a star configuration, with the LDO at the junction of the star. This will ensure that supply current variations or noise in one supply rail will have minimum effect on the other supplies. In applications where a ground plane is not practical, this same star layout should also apply to the power supply ground returns.

Only regulators with a 300 mA or greater rating can be used in a single-supply design.

Refer to the following application note for more information:

- Application Note: MXTAN0208 – *Design Guide for PCB Layouts for maXTouch Touch Controllers*

11.3.6 MULTIPLE VOLTAGE REGULATOR SUPPLY

The AVdd supply stability is critical for the device because this supply interacts directly with the analog front end. If noise problems exist when using a single LDO regulator, Microchip recommends that AVdd is supplied by a regulator that is separate from the digital supply and high voltage regulators. This reduces the amount of noise injected into the sensitive, low signal level parts of the design.

11.4 Driven Shield Line

The driven shield line is used to provide a guard track around the 2D touchscreen panel that serves as Ground in mutual capacitance operation and as a driven shield in self capacitance operation.

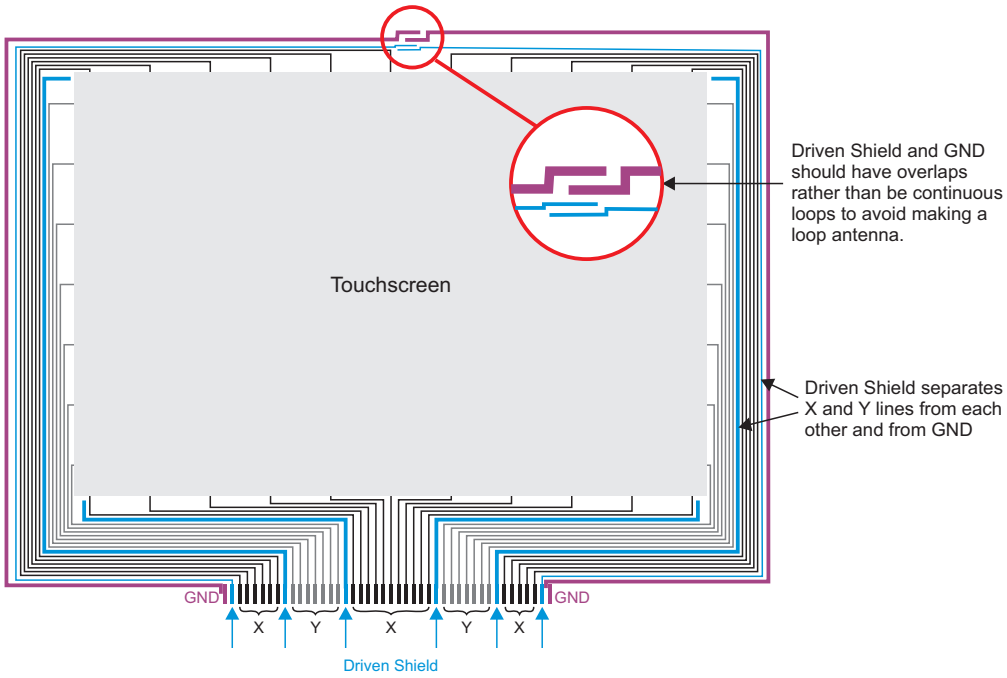
Note that the 3D electrodes will be located outside of the driven shield and sufficient clearance will be needed between the driven shield and the 3D electrodes. Refer to the following document for further details:

- Application Note: AN2574 – *2D/3D Electrode Design Guide*

The guard track must be routed between the X and Y tracks, as well as between the X/Y tracks and Ground. It should be fairly wide to avoid X-to-Y coupling in mutual capacitance operation, as the guard track will act as Ground in this circumstance.

A guard track is also needed between any self capacitance X/Y lines and mutual capacitance only X/Y lines (for example, between Multiple Touch Touchscreen T100 and Key Array T15 lines).

FIGURE 11-2: EXAMPLE DRIVEN SHIELD ROUTING



NOTE: Sample touchscreen for illustrative purposes only. The number of X/Y lines available on any given device might differ from that shown here. Similarly, the routing of the X/Y lines shown should not be taken as indicative of any preferred layout and the user's layout may vary.

11.5 ESD Ground Routing

To avoid damage due to ESD strikes, the outermost track on the sensor should be an ESD ground (see Figure 11-2). Like the driven shield, this should completely surround the sensor but with an overlap at the top rather than forming a complete loop.

To avoid electromagnetic induction of currents into the driven shield trace, a minimum separation of 0.3 mm should be maintained between the ESD GND trace and the Driven Shield.

The ESD ground traces should be connected to a dedicated ground trace in the PCB, and routed such that ESD strike currents do not flow under or close to the touch controller or the connecting wiring between it and the touchscreen array. The ESD ground should be connected in to the main system ground at a star point at the main GND connection to the PCB.

See also:

- MXTAN0208 – *Design guide for PCB Layouts for maXTouch Touch Controllers*

11.6 Analog I/O

In general, tracking for the analog I/O signals from the device should be kept as short as possible. These normally go to a connector which interfaces directly to the touchscreen.

Ensure that adequate ground-planes are used. An analog ground plane should be used in addition to a digital one. Care should be taken to ensure that both ground planes are kept separate and are connected together only at the point of entry for the power to the PCB. This is usually at the input connector.

11.7 Component Placement and Tracking

It is important to orient all devices so that the tracking for important signals (such as power and clocks) are kept as short as possible.

11.7.1 DIGITAL SIGNALS

In general, when tracking digital signals, it is advisable to avoid sharp directional changes on sensitive signal tracks (such as analog I/O) and any clock or crystal tracking.

A good ground return path for all signals should be provided, where possible, to ensure that there are no discontinuities.

11.8 EMC and Other Observations

The following recommendations are not mandatory, but may help in situations where particularly difficult EMC or other problems are present:

- Try to keep as many signals as possible on the inside layers of the board. If suitable ground flood fills are used on the top and bottom layers, these will provide a good level of screening for noisy signals, both into and out of the PCB.
- Ensure that the on-board regulators have sufficient tracking around and underneath the devices to act as a heatsink. This heatsink will normally be connected to the 0 V or ground supply pin. Increasing the width of the copper tracking to any of the device pins will aid in removing heat. There should be no solder mask over the copper track underneath the body of the regulators.
- Ensure that the decoupling capacitors, especially high capacity ceramic type, have the requisite low ESR, ESL and good stability/temperature properties. Refer to the regulator manufacturer’s datasheet for more information.

12.0 GETTING STARTED WITH MXT2113TG-AT/MXT2113TG-AB

12.1 Establishing Contact

12.1.1 COMMUNICATION WITH THE HOST

The host can use any of the following interfaces to communicate with the device (See Section 8.0 “Host Communications”):

- I^2C interface (see Section 9.0 “I2C Communications”)
- SPI interface (see Section 10.0 “SPI Communications”)

12.1.2 POWER-UP SEQUENCE

The power-up sequence is as follows:

1. On power-up, the $\overline{\text{CHG}}$ line goes low to indicate that there is new data to be read from the device. If the $\overline{\text{CHG}}$ line does not go low within a suitable timeout (for example, 200 ms), there is a problem with the device.
2. Once the $\overline{\text{CHG}}$ line goes low, the host should attempt to read the first 7 bytes of memory from location 0x0000 to establish that the device is present and running following power-up. These bytes represent the ID Information portion of the Information Block and should be recorded by the host so it can read the Object Table (see Section 12.2 “Using the Object Protocol”).
3. The device performs a checksum on the configuration settings held in the non-volatile memory. If the checksum does not match a stored copy of the last checksum, then this indicates that the settings have become corrupted. The host should write a correct configuration to the device, and issue a Command Processor T6 Backup command, if the read checksum does not match the expected checksum, or if the configuration error bit in the message data from the Command Processor T6 object is set.

Once the device has been initialized, the host must perform the following initialization so that it can communicate with the device:

1. Read the start positions of all the objects in the device from the Object Table and build up a list of these addresses. Note that the number of elements was read by the host at start-up as part of the ID Information bytes.
2. Use the Object Table to calculate the report IDs so that messages from the device can be correctly interpreted.
3. Read any pending messages generated during the start-up process.

Refer to Application Note MXTAN0213, *Interfacing with maXTouch Touchscreen Controllers*, for more information.

12.2 Using the Object Protocol

The device has an object-based protocol that is used to communicate with the device. Typical communication includes configuring the device, sending commands to the device, and receiving messages from the device.

12.2.1 CLASSES OF OBJECTS

The mXT2113TG-Ax contains the following classes of objects:

- **Debug objects** – provide a raw data output method for development and testing.
- **General objects** – required for global configuration, transmitting messages and receiving commands.
- **Touch objects** – operate on measured signals from the touch sensor and report touch data.
- **Signal processing objects** – process data from other objects (typically signal filtering operations).
- **Support objects** – provide additional functionality on the device.

12.2.2 OBJECT INSTANCES

TABLE 12-1: OBJECTS ON THE MXT2113TG-Ax

Object	Description	Number of Instances	Usage
Debug Objects			
Diagnostic Debug T37	Allows access to diagnostic debug data to aid development.	1	Debug commands only; Read-only object. No configuration or tuning necessary. Not for use in production.

TABLE 12-1: OBJECTS ON THE MXT2113TG-Ax (CONTINUED)

Object	Description	Number of Instances	Usage
General Objects			
Message Processor T5	Handles the transmission of messages. This object holds a message in its memory space for the host to read.	1	No configuration necessary.
Command Processor T6	Performs a command when written to. Commands include reset, calibrate and backup settings.	1	No configuration necessary.
Power Configuration T7	Controls the sleep mode of the device. Power consumption can be lowered by controlling the acquisition frequency and the sleep time between acquisitions.	1	Must be configured before use.
Acquisition Configuration T8	Controls how the device takes each capacitive measurement.	1	Must be configured before use.
Touch Objects			
Key Array T15	Defines a rectangular array of keys. A Key Array T15 object reports simple on/off touch information.	2	Enable and configure as required.
Multiple Touch Touchscreen T100	Creates a Touchscreen that supports the tracking of more than one touch.	1	Enable and configure as required.
Signal Processing Objects			
Key Thresholds T14	Allows different thresholds to be specified for each key in a Key Array.	2	Configure as required.
One-touch Gesture Processor T24	Operates on the data from a Touchscreen object. A One-touch Gesture Processor T24 converts touches into one-touch finger gestures (for example, taps, double taps and drags).	1	Enable and configure as required.
Two-touch Gesture Processor T27	Operates on the data from a One-touch Gesture Processor T24 object. A Two-touch Gesture Processor T27 converts touches into two-touch finger gestures (for example, pinches, stretches and rotates).	1	Enable and configure as required.
Grip Suppression T40	Suppresses false detections caused, for example, by the user gripping the edge of a touchscreen.	1	Enable and configure as required.
Touch Suppression T42	Suppresses false detections caused by unintentional large touches by the user.	1	Enable and configure as required.
Shieldless T56	Allows a sensor to use true single-layer co-planar construction.	1	Enable and configure as required.
Lens Bending T65	Compensates for lens deformation (lens bending) by attempting to eliminate the disturbance signal from the reported deltas.	3	Enable and configure as required.
Noise Suppression T72	Performs various noise reduction techniques during sensor signal acquisition.	1	Enable and configure as required.
Glove Detection T78	Allows for the reporting of glove touches.	1	Enable and configure as required.
Retransmission Compensation T80	Limits the negative effects on touch signals caused by poor device coupling to ground or moisture on the sensor.	1	Enable and configure as required.
Self Capacitance Noise Suppression T108	Suppresses the effects of external noise within the context of self capacitance touch measurements.	1	Enable and configure as required.

TABLE 12-1: OBJECTS ON THE MXT2113TG-Ax (CONTINUED)

Object	Description	Number of Instances	Usage
Self Capacitance Grip Suppression T112	Allows touches to be reported from the self capacitance measurements while the device is being gripped.	1	Enable and configure as required.
Support Objects			
Communications Configuration T18	Configures additional communications behavior for the device.	1	Check and configure as necessary.
GPIO Configuration T19	Allows the host controller to configure and use the general purpose I/O pins on the device.	1	Enable and configure as required.
Self Test T25	Configures and performs self-test routines to find faults on a touch sensor.	1	Enable and configure as required.
User Data T38	Provides a data storage area for user data.	1	Configure as required.
Message Count T44	Provides a count of pending messages.	1	Read-only object.
CTE Configuration T46	Controls the capacitive touch engine for the device.	1	Must be configured.
Timer T61	Provides control of a timer.	6	Enable and configure as required.
Serial Data Command T68	Provides an interface for the host driver to deliver various data sets to the device.	1	Enable and configure as required.
Dynamic Configuration Controller T70	Allows rules to be defined that respond to system events.	20	Enable and configure as required.
Dynamic Configuration Container T71	Allows the storage of user configuration on the device that can be selected at runtime based on rules defined in the Dynamic Configuration Controller T70 object.	1	Configure if Dynamic Configuration Controller T70 is in use.
Touch Event Trigger T79	Configures touch triggers for use with the event handler.	3	Enable and configure as required.
Auxiliary Touch Configuration T104	Allows the setting of self capacitance gain and thresholds for a particular measurement to generate auxiliary touch data for use by other objects.	1	Enable and configure if using self capacitance measurements
Self Capacitance Global Configuration T109	Provides configuration for self capacitance measurements employed on the device.	1	Check and configure as required (if using self capacitance measurements).
Self Capacitance Tuning Parameters T110	Provides configuration space for a generic set of settings for self capacitance measurements.	4	Use under the guidance of Microchip field engineers only.
Self Capacitance Configuration T111	Provides configuration for self capacitance measurements employed on the device.	2	Check and configure as required (if using self capacitance measurements).
Self Capacitance Measurement Configuration T113	Configures self capacitance measurements to generate data for use by other objects.	1	Enable and configure as required.
Data Container T117	Provides a mechanism for retrieving specific data held in the device's internal memory.	24	Read-only object. No configuration necessary.
Data Container Controller T118	Provides direct access to internal data in memory for use with the Data Container T117 objects.	1	Enable and configure as required.
Self Capacitance Voltage Modulation T133	Controls the voltage modulation on self capacitance scans.	2	Enable and configure as required.

TABLE 12-1: OBJECTS ON THE MXT2113TG-Ax (CONTINUED)

Object	Description	Number of Instances	Usage
3D Scan Configuration T140	Defines the data that is used to control the 3D scan.	2	Enable and configure as required

12.2.3 CONFIGURING AND TUNING THE DEVICE

The objects are designed such that a default value of zero in their fields is a “safe” value that typically disables functionality. The objects must be configured before use and the settings written to the non-volatile memory using the Command Processor T6 object.

Perform the following actions for each object:

1. Enable the object, if the object requires it.
2. Configure the fields in the object, as required.
3. Enable reporting, if the object supports messages, to receive messages from the object.

12.3 Writing to the Device

The following mechanisms can be used to write to the device:

- Using an I^2C write operation (see Section 9.2 “Writing To the Device”).
- Using the SPI write operation (see Section 10.3 “Write Operation and Responses”).

Communication with the device is achieved by writing to the appropriate object:

- To send a command to the device, an appropriate command is written to the Command Processor T6 object.
- To configure the device, a configuration parameter is written to the appropriate object. For example, writing to the Power Configuration T7 configures the power consumption for the device and writing to the Multiple Touch Touchscreen T100 object sets up the touchscreen. Some objects are optional and need to be enabled before use.

IMPORTANT! When the host issues any command within an object that results in a flash write to the device Non-Volatile Memory (NVM), that object should have its CTRL RPTEN bit set to 1, if it has one. This ensures that a message from the object writing to the NVM is generated at the completion of the process and an assertion of the $\overline{\text{CHG}}$ line is executed.

The host must also ensure that the assertion of the $\overline{\text{CHG}}$ line refers to the expected object report ID before asserting the $\overline{\text{RESET}}$ line to perform a reset. Failure to follow this guidance may result in a corruption of device configuration area and the generation of a CFGERR.

12.4 Reading from the Device

Status information is stored in the Message Processor T5 object. This object can be read to receive any status information from the device.

The following mechanisms provide an interrupt-style interface for reading messages in the Message Processor T5 object:

- In I^2C and SPI modes, the $\overline{\text{CHG}}$ line is asserted whenever a new message is available in the Message Processor T5 object (see Section 9.5 “CHG Line” and Section 10.2.1 “CHG Line”). See Section 9.4 “Reading From the Device” for information on the format of the I^2C read operation and Section 10.4 “Read Operation and Responses” for information on the format of the SPI read operation.

  When using the SPI interface, two SPI transactions must take place: the first is an SPI Read request which is used to set the address pointer (Address LSByte and MSByte) and to indicate to the device how many bytes (Length LSByte and MSByte) the host wants to read; the second is a response which comes with a payload that actually contains the data that was requested (see Section 10.4 “Read Operation and Responses”).

NOTE The host should always wait to be notified of messages; the host should not poll the device for messages (either by polling the Message Processor T5 object or by polling the $\overline{\text{CHG}}$ line).

13.0 DEBUGGING AND TUNING

13.1 SPI Debug Interface

NOTE	The SPI Debug Interface is not available if the SPI interface is being used for communications with the host.

The SPI Debug Interface is used for tuning and debugging when running the system and allows the development engineer to use Microchip maXTouch Studio to read the real-time raw data. This uses the low-level debug port.

The SPI Debug Interface consists of the $\overline{\text{DBG\_SS}}$, DBG_CLK, and DBG_DATA lines. These lines should be routed to test points on all designs such that they can be connected to external hardware during system development. These lines should not be connected to power or GND. See Section 2.3.11 “SPI Debug Interface” for more details.

The SPI Debug Interface is enabled by the Command Processor T6 object and by default will be off.

NOTE	When the $\overline{\text{DBG\_SS}}$, DBG_CLK, and DBG_DATA lines are in use for debugging, any alternative function for the pins cannot be used. The touch controller will take care of the pin configuration.

13.2 Object-based Protocol

The device provides a mechanism for obtaining debug data for development and testing purposes by reading data from the Diagnostic Debug T37 object.

NOTE	The Diagnostic Debug T37 object is of most use for simple tuning purposes. When debugging a design, it is preferable to use the SPI Debug Interface, as this will have a much higher bandwidth and can provide real-time data.

13.3 Self Test

There is a Self Test T25 object that runs self-test routines in the device to find hardware faults on the sense lines and the electrodes. This object also performs an initial pin fault test on power-up to ensure that there is no pin short (X to Y, or X lines to power or GND) before the high-voltage supply is enabled inside the chip. A high-voltage short on the sense lines could damage the device.

In addition to one-off hardware tests, the Self Test T25 object can also provide continuous monitoring of the health of the device while it is in operation. A periodic test can be run at a user-specified interval and reports pass and/or fail messages (as determined by the device configuration). Reporting is achieved either by standard Self Test T25 object protocol messages or by a configurable hardware GPIO pin, configured using the GPIO Configuration T19 object.

14.0 SPECIFICATIONS

14.1 Absolute Maximum Specifications

Vdd	3.6V
VddIO	3.6V
AVdd	3.6V
XVdd (external)	10.0V
Maximum continuous combined pin current, all GPIO*n* pins	60 mA
Voltage forced onto any pin	–0.3 V to Vdd/VddIO/AVdd + 0.3 V
Configuration parameters maximum writes	10,000
Maximum junction temperature	125°C

CAUTION! Stresses beyond those listed under *Absolute Maximum Specifications* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum specification conditions for extended periods may affect device reliability.

14.2 Recommended Operating Conditions

Operating temperature	mXT2113TG-AT: –40°C to +85°C (Grade 3)
	mXT2113TG-AB: –40°C to +105°C (Grade 2)
Storage temperature	–60°C to +150°C
Vdd	3.3V ±5%
VddIO	3.3 V ±5%
AVdd	3.3 V ±5%
External XVdd – Static	3.3 V to 8.5 V ±5% (3.3V recommended)
XVdd – With Voltage Booster enabled	6.2 V Nominal, Band Gap Referenced 7.4 V Nominal, Band Gap Referenced 8.5 V Nominal, Band Gap Referenced
Temperature slew rate	10°C/min

14.2.1 DC CHARACTERISTICS

14.2.1.1 Analog Voltage Supply – AVdd

Parameter	Min	Typ	Max	Units	Notes
AVdd					
Operating limits	3.14	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 µs to rise

14.2.1.2 Digital Voltage Supply – VddIO, Vdd

Parameter	Min	Typ	Max	Units	Notes
VddIO					
Operating limits	3.14	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 µs to rise
Vdd					
Operating limits	3.14	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 µs to rise
Supply Fall Rate	–	–	0.05	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 66 µs to fall

14.2.1.3 XVdd Voltage Supply – XVdd

Parameter	Min	Typ	Max	Units	Notes
XVdd					
Operating limits – external XVdd supply	3.14	3.3	9.0	V	
Supply Rise Rate	–	–	0.1	V/µs	For example, for a 8.5 V rail, the voltage should take a minimum of 85 µs to rise

14.2.2 POWER SUPPLY RIPPLE AND NOISE

Parameter	Min	Typ	Max	Units	Notes
Vdd	–	–	±50	mV	Across frequency range 1 Hz to 1 MHz
AVdd	–	–	±40	mV	Across frequency range 1 Hz to 1 MHz, with Noise Suppression enabled

14.3 Test Configuration

The configuration values listed below were used in the reference unit to validate the interfaces and derive the characterization data provided in the following sections.

TABLE 14-1: TEST CONFIGURATION

Object/Parameter	Description/Setting (Numbers in Decimal)
Acquisition Configuration T8	
CHRGTIME	75
MEASALLOW	3
GPIO Configuration T19	Object Enabled
One-touch Gesture Processor T24	Object Enabled
Self Test T25	Object Enabled
Two-touch Gesture Processor T27	Object Enabled
Touch Suppression T42	Object Enabled
CTE Configuration T46	
IDLESYNCSPERX	8
ACTVSYNCSPERX	8
Shieldless T56	Object Enabled
INTTIME	65
Timer T61 Instance 0	Object Instance Enabled
Lens Bending T65 Instance 0	Object Instance Enabled
Lens Bending T65 Instance 1	Object Instance Enabled
Lens Bending T65 Instance 2	Object Instance Enabled
Dynamic Configuration Controller T70 Instance 0	Object Instance Enabled
Dynamic Configuration Controller T70 Instance 1	Object Instance Enabled
Dynamic Configuration Controller T70 Instance 2	Object Instance Enabled
Dynamic Configuration Controller T70 Instance 4	Object Instance Enabled
Dynamic Configuration Controller T70 Instance 5	Object Instance Enabled
Noise Suppression T72	Object Enabled
Glove Detection T78	Object Enabled
Retransmission Compensation T80	Object Enabled
Multiple Touch Touchscreen T100	Object Enabled
Auxiliary Touch Configuration T104	Object Enabled
Self Capacitance Noise Suppression T108	Object Enabled
Self Capacitance Configuration T111 Instance 0	
INTTIME	100
IDLESYNCSPERL	8
ACTVSYNCSPERL	8
Self Capacitance Voltage Modulation T133 Instance 0	Object Instance Enabled
Self Capacitance Voltage Modulation T133 Instance 1	Object Instance Enabled
3D Scan Configuration T140 Instance 0	Object Instance Enabled

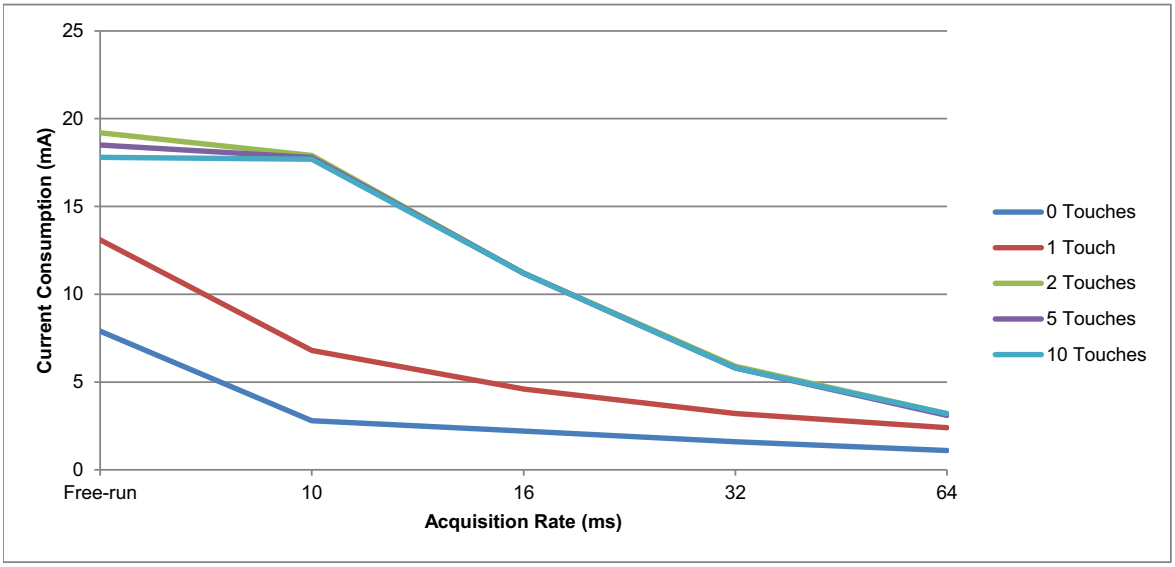
14.4 Current Consumption – I²C Interface

NOTE The characterization charts show typical values based on the configuration in Table 14-1. Actual power consumption in the user's application will depend on the circumstances of that particular project and will vary from that shown here. Further tuning will be required to achieve an optimal performance.

14.4.1 AVDD 3.3V

NOTE Figures for the MXG3141 not included

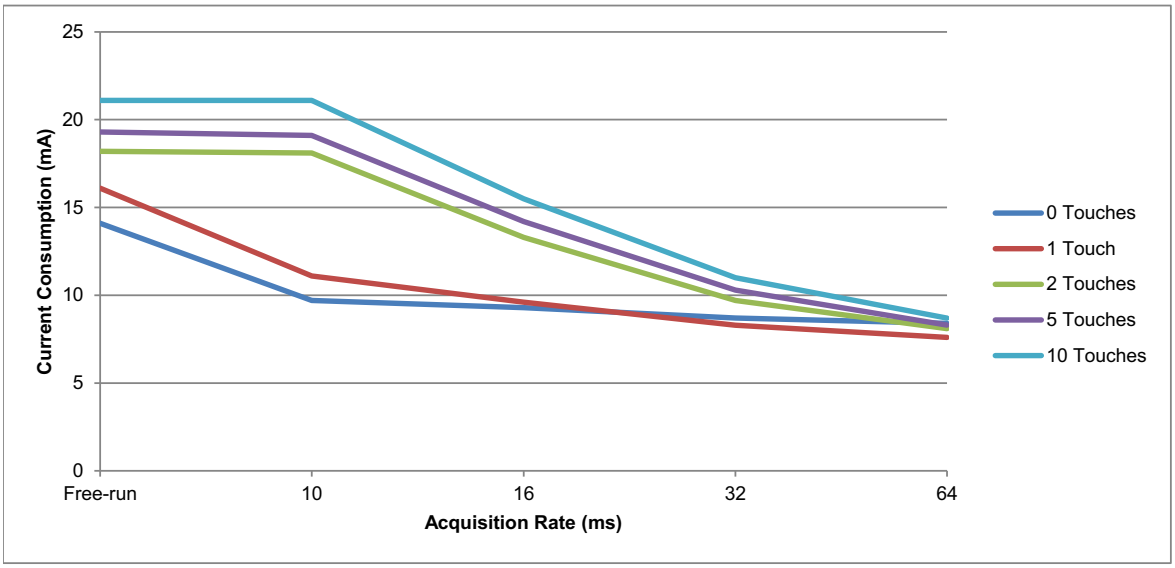
	Current Consumption (mA)				
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**	**10 Touches**
Free-run	7.9	13.1	19.2	18.5	17.8
10	2.8	6.8	17.9	17.8	17.7
16	2.2	4.6	11.2	11.2	11.2
32	1.6	3.2	5.9	5.8	5.8
64	1.1	2.4	3.2	3.1	3.2



14.4.2 VDD 3.3V

NOTE Figures for the MXG3141 not included

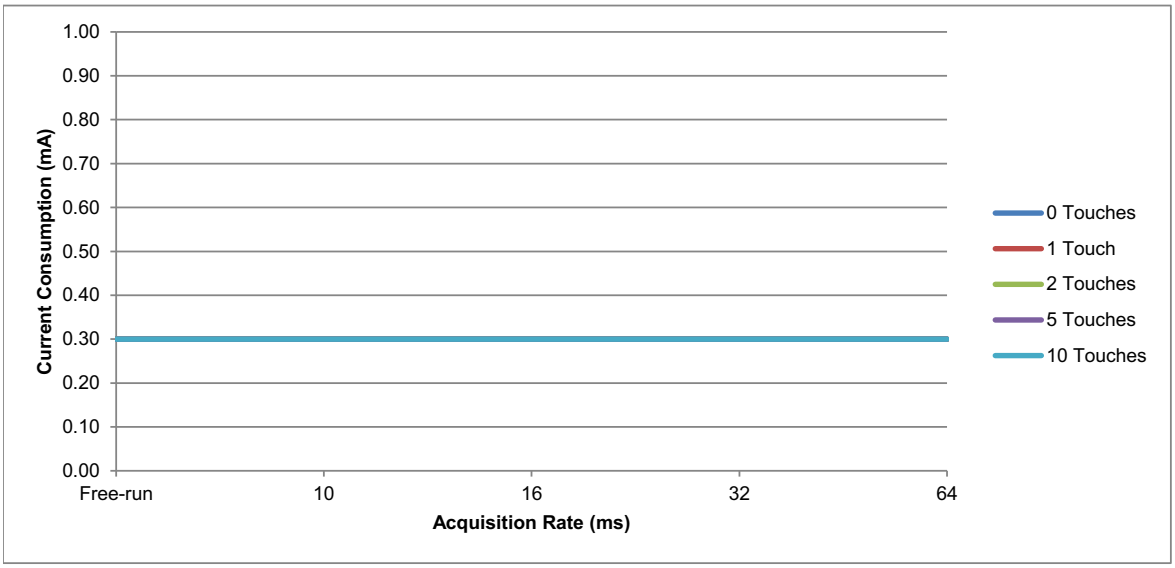
	Current Consumption (mA)				
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**	**10 Touches**
Free-run	14.1	16.1	18.2	19.3	21.1
10	9.7	11.1	18.1	19.1	21.1
16	9.3	9.6	13.3	14.2	15.5
32	8.7	8.3	9.7	10.3	11
64	8.4	7.6	8.1	8.3	8.7



14.4.3 VDDIO 3.3V

NOTE Figures for the MXG3141 not included

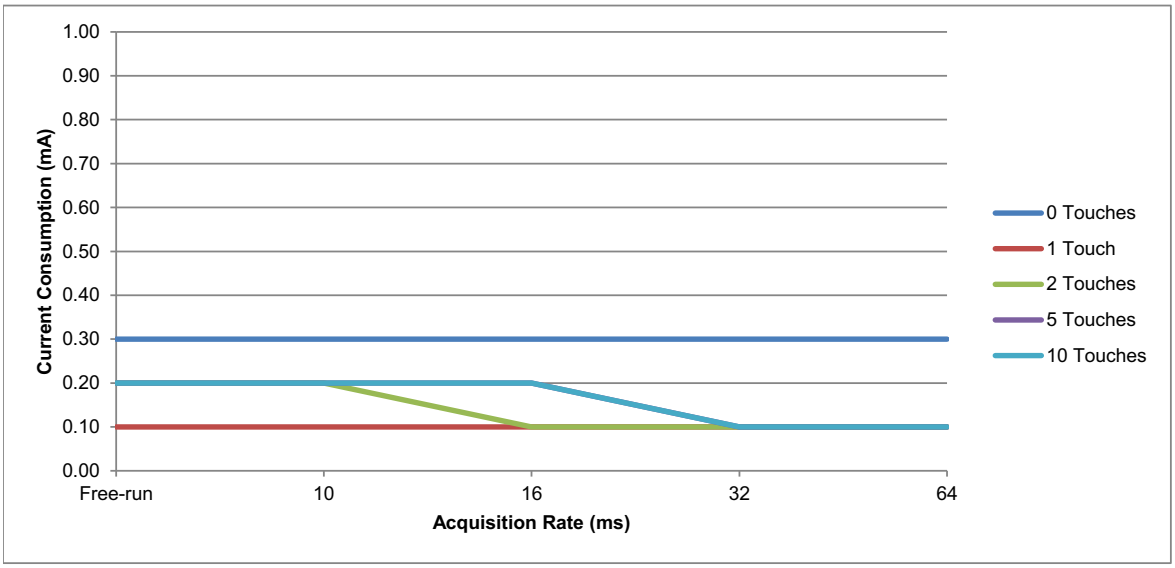
	Current Consumption (mA)				
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**	**10 Touches**
Free-run	0.30	0.30	0.30	0.30	0.30
10	0.30	0.30	0.30	0.30	0.30
16	0.30	0.30	0.30	0.30	0.30
32	0.30	0.30	0.30	0.30	0.30
64	0.30	0.30	0.30	0.30	0.30



14.4.4 XVDD 3.3V

NOTE Figures for the MXG3141 not included

	Current Consumption (mA)				
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**	**10 Touches**
Free-run	0.3	0.1	0.2	0.2	0.2
10	0.3	0.1	0.2	0.2	0.2
16	0.3	0.1	0.1	0.2	0.2
32	0.3	0.1	0.1	0.1	0.1
64	0.3	0.1	0.1	0.1	0.1



14.4.5 DEEP SLEEP

T_A = 25°C

Parameter	**Value**	**Units**	**Notes**
Deep Sleep Current	1.6	mA	Vdd = 3.3V, AVdd = 3.3V, XVdd= 3.3V, VddIO = 3.3V
Deep Sleep Power	5.28	mW	

Note: Figures for the MXG3141 not included

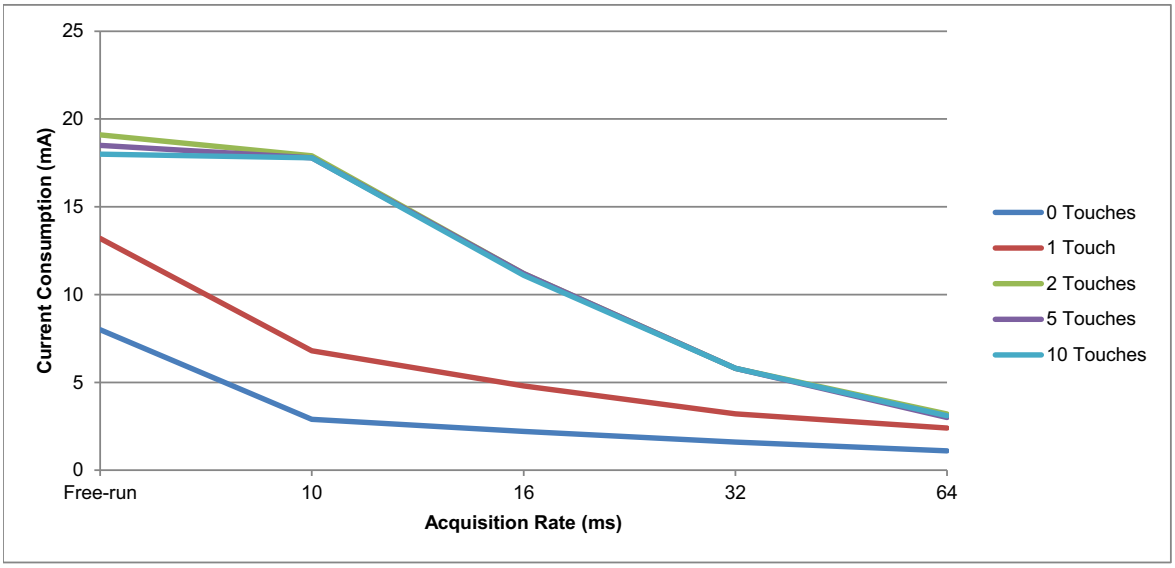
14.5 Current Consumption – SPI Interface

NOTE The characterization charts show typical values based on the configuration in Table 14-1 on page 55. Actual power consumption in the user's application will depend on the circumstances of that particular project and will vary from that shown here. Further tuning will be required to achieve an optimal performance.

14.5.1 AVDD 3.3V

NOTE Figures for the MXG3141 not included

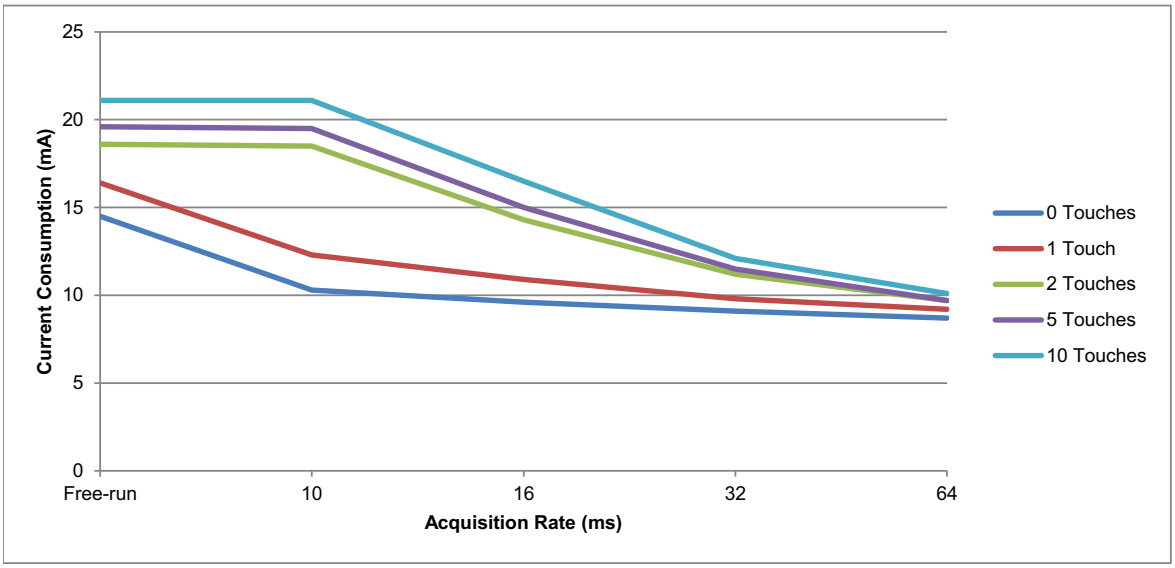
	Current Consumption (mA)				
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**	**10 Touches**
Free-run	8	13.2	19.1	18.5	18
10	2.9	6.8	17.9	17.8	17.8
16	2.2	4.8	11.2	11.2	11.1
32	1.6	3.2	5.8	5.8	5.8
64	1.1	2.4	3.2	3	3.1



14.5.2 VDD 3.3V

NOTE Figures for the MXG3141 not included

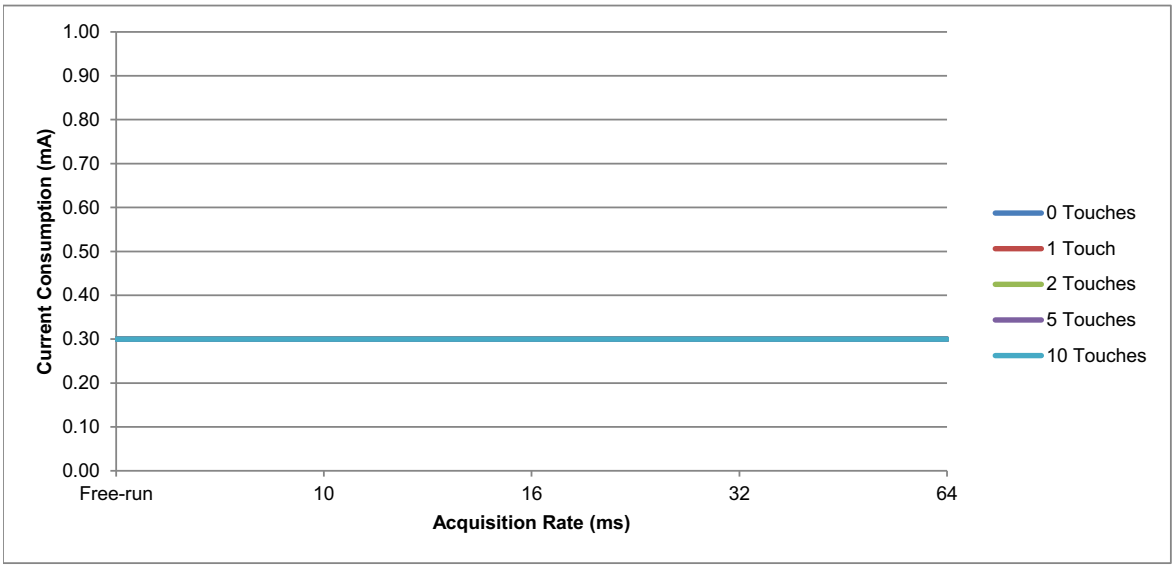
	Current Consumption (mA)				
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**	**10 Touches**
Free-run	14.5	16.4	18.6	19.6	21.1
10	10.3	12.3	18.5	19.5	21.1
16	9.6	10.9	14.3	15	16.5
32	9.1	9.8	11.2	11.5	12.1
64	8.7	9.2	9.7	9.7	10.1



14.5.3 VDDIO 3.3V

NOTE Figures for the MXG3141 not included

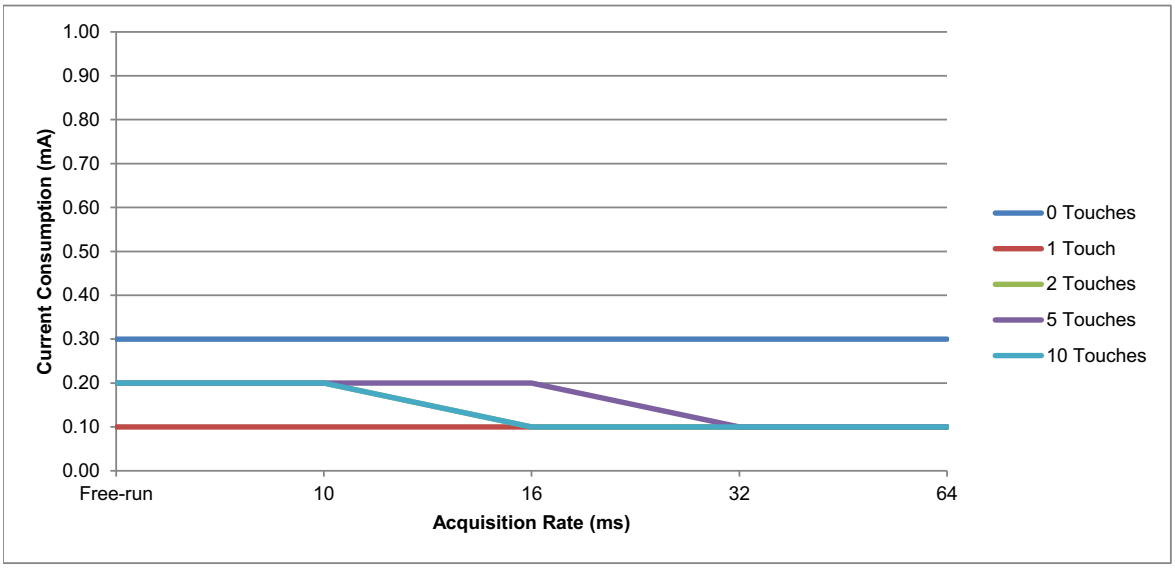
	Current Consumption (mA)				
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**	**10 Touches**
Free-run	0.30	0.30	0.30	0.30	0.30
10	0.30	0.30	0.30	0.30	0.30
16	0.30	0.30	0.30	0.30	0.30
32	0.30	0.30	0.30	0.30	0.30
64	0.30	0.30	0.30	0.30	0.30



14.5.4 XVDD 3.3V

NOTE Figures for the MXG3141 not included

	Current Consumption (mA)				
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**	**10 Touches**
Free-run	0.3	0.1	0.2	0.2	0.2
10	0.3	0.1	0.2	0.2	0.2
16	0.3	0.1	0.1	0.2	0.1
32	0.3	0.1	0.1	0.1	0.1
64	0.3	0.1	0.1	0.1	0.1



14.5.5 DEEP SLEEP

T_A = 25°C

Parameter	**Value**	**Units**	**Notes**
Deep Sleep Current	8.7	mA	Vdd = 3.3V, AVdd = 3.3V, XVdd= 3.3V, VddIO = 3.3V
Deep Sleep Power	28.71	mW	

Note: Figures for the MXG3141 not included

14.6 Timing Specifications

NOTE	The figures below show typical values based on the test configuration. Actual timings in the user's application will depend on the circumstances of that particular project and will vary from those shown below. Further tuning will be required to achieve an optimal performance.

14.6.1 TOUCH LATENCY

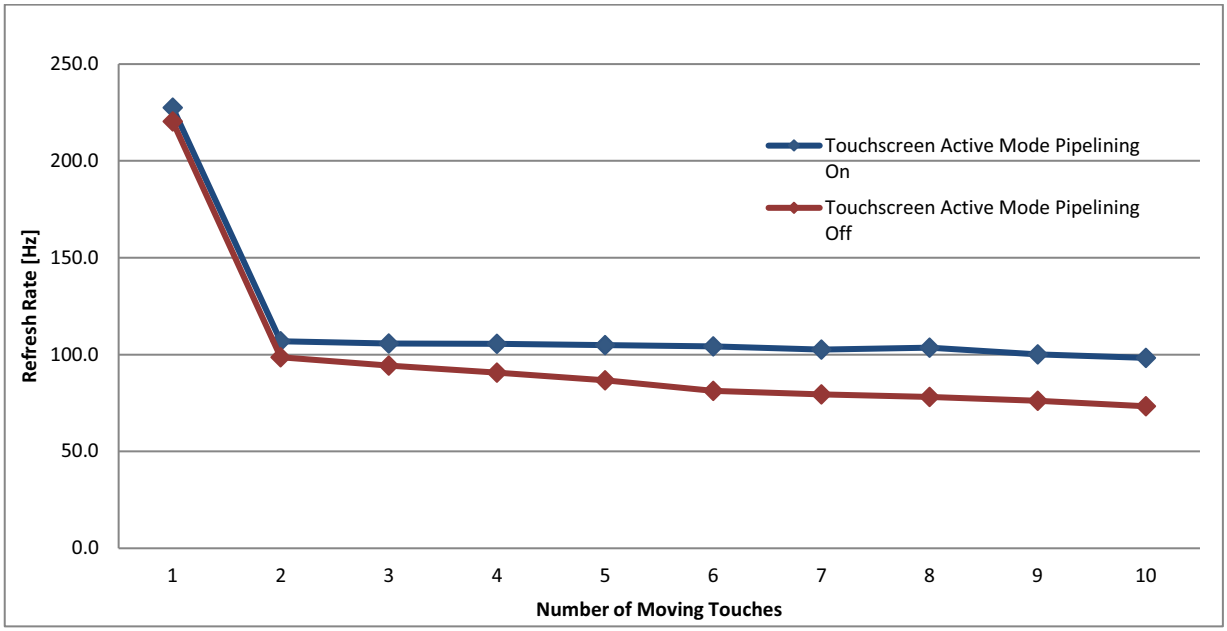
Conditions: CHRGTIME = 75; IDLESYNCSPERX = 8; ACTVSYNCSPERX = 8; T = ambient temperature; Finger center of screen; Reporting off (except T100); C_{pk} Process Capability Index calculation not applied

Idle Primary = Self Capacitance; Active Primary = Mutual Capacitance

T100 TCHDIDOWN	Pipelining Off			Pipelining On			Units
	Min	Typ	Max	Min	Typ	Max	
3	24.1	30.1	37.3	22.6	28.1	35.6	ms
2	21.2	27	34.4	19.7	24.5	32.7	ms
1	13.3	18.9	26.3	11.7	16.2	24.8	ms
Disabled (DISTCHDIDOWN = 1)	10.8	18.5	26.4	11.5	15.9	24.6	ms

14.6.2 REPORT RATE

Conditions: CHRGTIME = 75; IDLESYNCSPERX = 8; ACTVSYNCSPERX = 8; T = ambient temperature



14.6.3 BURST FREQUENCY TOLERANCE

The burst frequency is directly correlated to the system clock. The burst frequency tolerance depends on the tolerance of the system's oscillator (see Table 14-2).

TABLE 14-2: OSCILLATOR TOLERANCE

Conditions: T= –40°C, 25°C, 85°C, 105°C

Min Drift	Nominal	Max Drift	Notes
–3%	55 MHz (calibrated)	+3%	Minimum/Maximum drift over temperature is specified as percentage below/above nominal frequency

14.6.4 RESET TIMINGS

Parameter	Min	Typ	Max	Units	Notes
Power on to $\overline{\text{CHG}}$ line low	–	90	–	ms	Triggered by Vdd supply at start up
Hardware reset to $\overline{\text{CHG}}$ line low	–	90	–	ms	Triggered by $\overline{\text{RESET}}$
Software reset to $\overline{\text{CHG}}$ line low	–	110	–	ms	Triggered by Command Processor T6 Reset command

Note 1: Any $\overline{\text{CHG}}$ line activity before the power-on or reset period has expired should be ignored by the host. Operation of this signal cannot be guaranteed before the power-on/reset periods have expired.

14.7 Touch Accuracy and Repeatability

Parameter	Min	Typ	Max	Units	Notes
Linearity	–	±0.5	–	mm	Finger diameter 8 mm
Accuracy (across all areas of screen)	–	0.5	–	mm	Finger diameter 8 mm
Repeatability	–	±0.25	–	%	X axis with 12-bit resolution

14.8 Touchscreen Sensor Characteristics

Parameter	Description	Value
Cm	Mutual capacitance	Typical value is between 0.15 pF and 10 pF on a single node.
Cpx	Mutual capacitance load to X	Microchip recommends a maximum load of 300 pF on each X or Y line. (1)
Cpy	Mutual capacitance load to Y	
Cpx	Self capacitance load to X	Microchip recommends a maximum load of 150 pF on each X or Y line. (1)
Cpy	Self capacitance load to Y	
ΔCpx	Self capacitance imbalance on X	Nominal value is 37 pF. Value increases by 1 pF for every 45 pF reduction in Cpx/Cpy (based on 150 pF load)
ΔCpy	Self capacitance imbalance on Y	
Cpds0	Self capacitance load to Driven Shield	Microchip recommends a maximum load of 150 pF on the Driven Shield line. (1)

Note 1: Please contact your Microchip representative for advice if you intend to use higher values.

14.9 Input/Output Characteristics

Parameter	Description	Min	Typ	Max	Units	Notes
Input (All input pins connected to the VddIO power rail)						
Vil	Low input logic level	–0.3	–	0.3 × VddIO	V	
Vih	High input logic level	0.7 × VddIO	–	VddIO	V	
Iil	Input leakage current	–	–	1	µA	Pull-up resistors disabled
$\overline{\text{RESET}}$	Internal pull-up resistor	20	40	60	kΩ	
GPIOs	Internal pull-up/pull-down resistor					
Output (All output pins connected to the VddIO power rail)						
Vol	Low output voltage	0	–	0.2 × VddIO	V	Iol = 4 mA
Voh	High output voltage	0.8 × VddIO	–	VddIO	V	Ioh = –4 mA

14.10 Host I²C Specification

Parameter	Value
Addresses	0x4A or 0x4B
I²C specification (1)	Revision 6.0
Maximum bus speed (SCL) (2)	1 MHz
Standard Mode (3)	100 kHz
Fast Mode (3)	400 kHz
Fast Mode Plus (3)	1 MHz

Note 1: More detailed information on I²C operation is available from www.nxp.com/documents/user_manual/UM10204.pdf.

2: In systems with heavily laden I²C lines, even with minimum pull-up resistor values, bus speed may be limited by capacitive loading to less than the theoretical maximum.

3: The values of pull-up resistors should be chosen to ensure SCL and SDA rise and fall times meet the I²C specification. The value required will depend on the amount of capacitance loading on the lines.

14.11 Host SPI Bus Specification

Parameter	Specification
Mode	Mode 3 (CPOL = 1 and CPHA = 1)
Clock idle state	High
Setup on	Leading (falling) edge
Sample on	Trailing (rising) edge
Word size	8-bit
Maximum clock frequency	8 MHz

14.12 Thermal Packaging

14.12.1 THERMAL DATA

Parameter	Description	Typ	Unit	Condition	Package
θ_{JA}	Junction to ambient thermal resistance	45.4	°C/W	Still air	144-lead LQFP 20 × 20 × 1.4 mm
θ_{JC}	Junction to case thermal resistance	10.3	°C/W		144-lead LQFP 20 × 20 × 1.4 mm

14.12.2 JUNCTION TEMPERATURE

The maximum junction temperature allowed on this device is 125°C.

The average junction temperature in °C (T_J) for this device can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA})$$

If a cooling device is required, use this equation:

$$T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$$

where:

- θ_{JA}= package thermal resistance, Junction to ambient (°C/W) (see Section 14.12.1 “Thermal Data”)
- θ_{JC} = package thermal resistance, Junction to case thermal resistance (°C/W) (see Section 14.12.1 “Thermal Data”)
- $\theta_{HEATSINK}$ = cooling device thermal resistance (°C/W), provided in the cooling device datasheet
- P_D = device power consumption (W)
- T_A is the ambient temperature (°C)

14.13 ESD Information

Parameter	Value	Reference Standard	Notes
Human Body Model (HBM)	±2000V	AEC–Q100	
Charge Device Model (CDM)	±500V	AEC–Q100	Except corner pins
	±750V	AEC–Q100	Corner pins only

14.14 Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	150 – 200°C
Time Maintained Above 217°C	60 – 150 s
Time within 5°C of Actual Peak Temperature	30 s
Peak Temperature Range	260°C
Ramp down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max

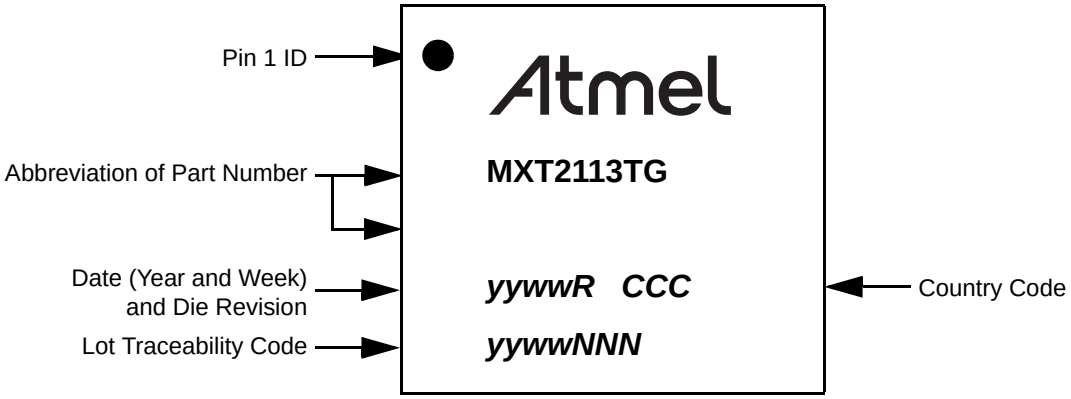
14.15 Moisture Sensitivity Level (MSL)

MSL Rating	Package Type(s)	Peak Body Temperature	Specifications
MSL3	144-lead LQFP	260°C	AEC–Q100

15.0 PACKAGING INFORMATION

15.1 Package Marking Information

15.1.1 144-LEAD LQFP



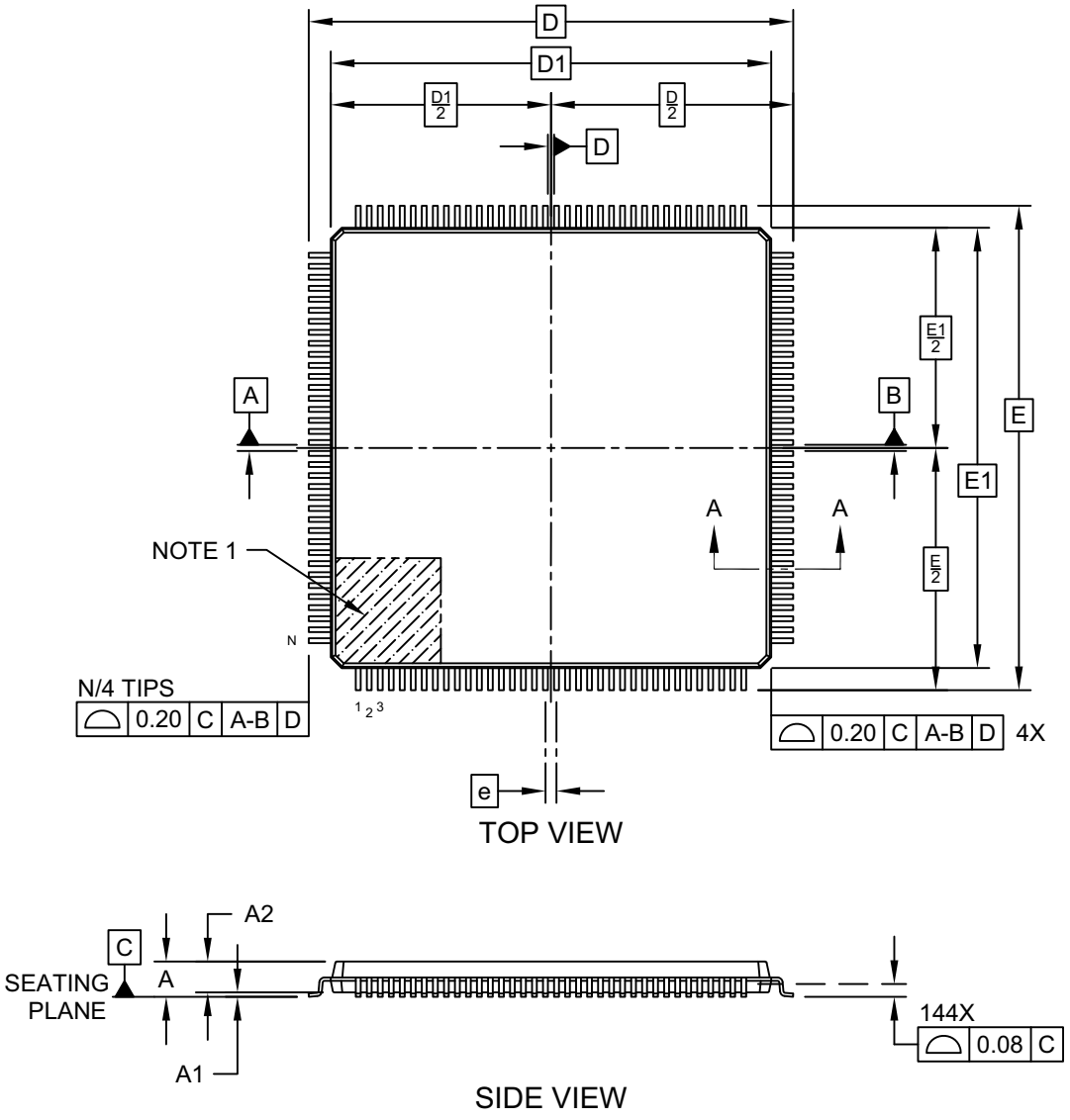
15.1.2 ORDERABLE PART NUMBERS

The product identification system for maXTouch devices is described in "Product Identification System". That section also lists example part numbers for the device.

15.2 Package Details

144-Lead Plastic Quad Flatpack (2SB) - 20x20x1.4 mm Body [LQFP]
Atmel Legacy Global Package Code AEI

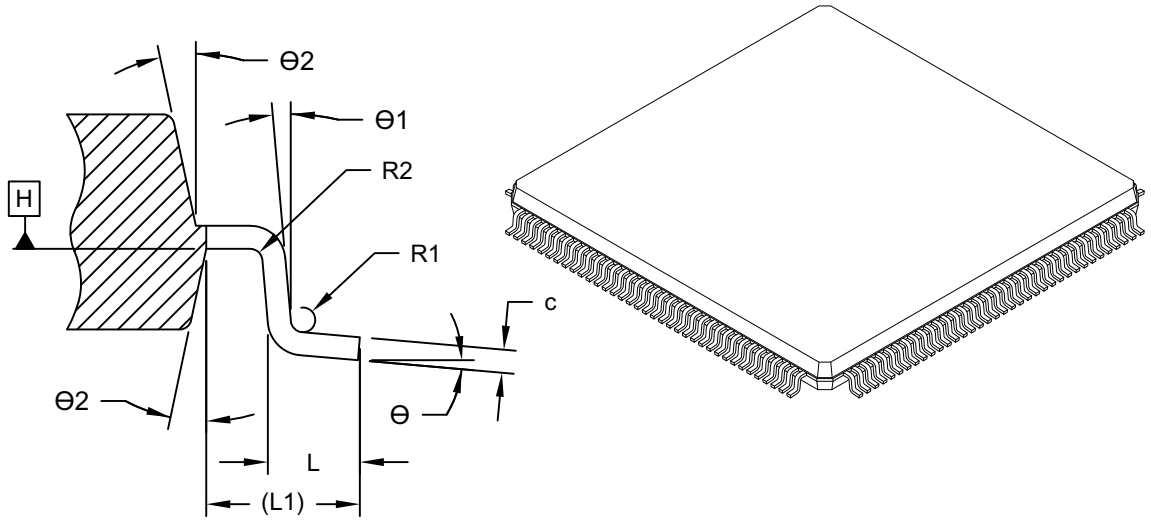
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21010 Rev A Sheet 1 of 2

144-Lead Plastic Quad Flatpack (2SB) - 20x20x1.4 mm Body [LQFP]
Atmel Legacy Global Package Code AEI

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		144	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.60
Standoff	A1	0.05	0.02	0.15
Molded Plastic Height	A2	1.35	1.40	1.45
Overall Length	D		22.00 BSC	
Exposed Pad Length	D1		20.00 BSC	
Overall Width	E		22.00 BSC	
Exposed Pad Width	E1		20.00 BSC	
Terminal Width	b	0.17	0.22	0.27
Terminal Width	c	0.09	0.15	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Terminal Bend Radius	R1	0.08	-	-
Terminal Bend Radius	R2	0.08	-	0.20
Terminal Angle	Θ	0°	3.5°	7°
Terminal Angle	Θ1	0°	-	-
Mold Draft Angle	Θ2	11°	12°	13°

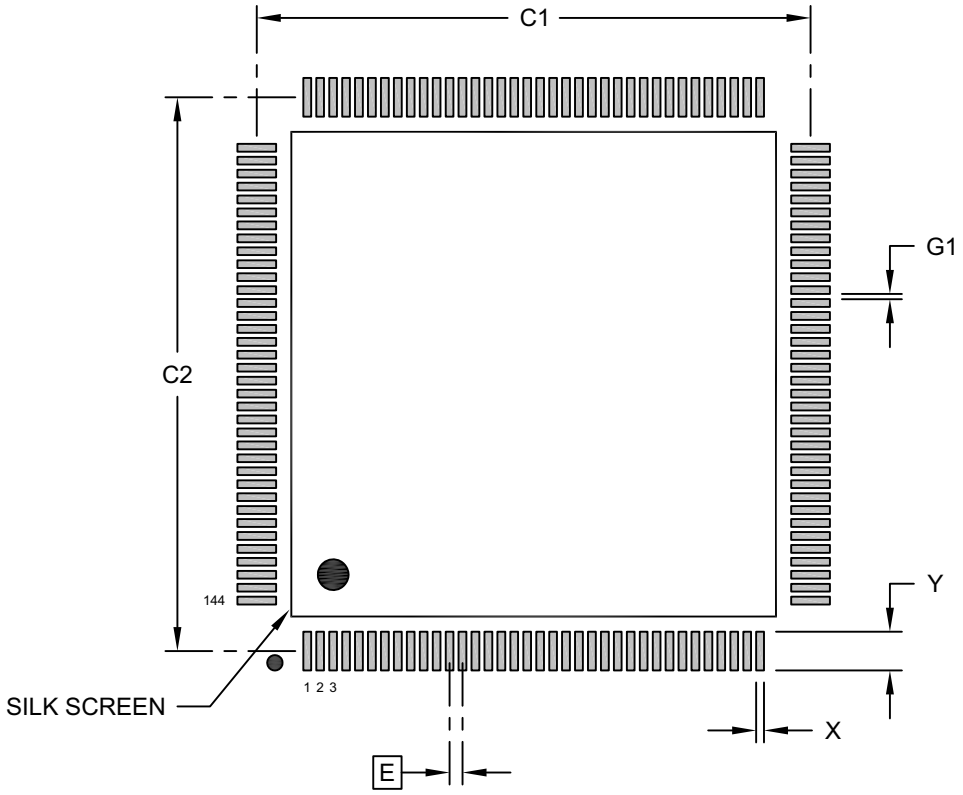
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21010 Rev A Sheet 2 of 2

144-Lead Plastic Quad Flatpack (2SB) - 20x20x1.4 mm Body [LQFP]
Atmel Legacy Global Package Code AEI

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		21.40	
Contact Pad Spacing	C2		21.40	
Contact Pad Width (X144)	X1			0.30
Contact Pad Length (X144)	Y1			1.50
Contact Pad to Contact Pad (X140)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-23010 Rev A

APPENDIX A: ASSOCIATED DOCUMENTS

Microchip maXTouch Documents

The following documents are available on the Microchip website.

Product Documentation

- *MXG3141 3D Tracking and Gesture Controller Data Sheet*

Touchscreen Design and PCB/FPCB Layout Guidelines

- Application Note: AN2574 – *2D/3D Electrode Design Guide*
- Application Note: QTAN0054 – *Getting Started with maXTouch Touchscreen Designs*
- Application Note: MXTAN0208 – *Design Guide for PCB Layouts for maXTouch Touch Controllers*
- Application Note: QTAN0080 – *Touchscreens Sensor Design Guide*
- Application Note: AN2683 – *Edge Wiring for Self Capacitance maXTouch Touchscreens*

Configuring and Tuning the Device

- Application Note: MXTAN0213 – *Interfacing with maXTouch Touchscreen Controllers*

Tools

- *maXTouch Studio User Guide* (distributed as on-line help with maXTouch Studio)

External Documents

The following documents are not supplied by Microchip. To obtain any of the following documents, please contact the relevant organization.

I^2C Interface

- UM10204, *I^2C bus specification and user manual*, Rev. 6 — 4 April 2014
  Available from NXP: www.nxp.com/documents/user_manual/UM10204.pdf

APPENDIX B: REVISION HISTORY

Revision A (September 2017)

Initial edition for firmware revision 0.5 – Advance Information

Revision B (June 2019)

Updated for firmware revision 0.5.06 – Pre-Alpha

- Section 5.0 “3D Sensor Layout”: 3D gestures support Air Wheel and Flick gestures only

Revision C (February 2021)

Updated for firmware revision 1.0.AA – Release

This revision incorporates the following updates:

- $\overline{\text{MXG\_MCLR}}$, $\overline{\text{MXG\_TS}}$, MXG_SDA and MXG_SCL pins no longer used; marked as RESV
- Single Edge layout removed
- Additional sections added:
  - Section 3.0 “Touchscreen Basics”
  - Section 7.0 “Detailed Operation”
  - Section 9.0 “I2C Communications”
  - Section 10.0 “SPI Communications”
  - Section 12.0 “Getting Started with mXT2113TG-AT/mXT2113TG-AB”
  - Section 13.0 “Debugging and Tuning”
- Section 14.0 “Specifications” updated:
  - Section 14.3 “Test Configuration” added
  - Section 14.4 “Current Consumption – I^2C Interface” added
  - Section 14.5 “Current Consumption – SPI Interface” added
  - Section 14.6.1 “Touch Latency” added
  - Section 14.6.2 “Report Rate” added
  - Section 14.6.4 “Reset Timings” added
- Other minor changes to text for clarity

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PRODUCT IDENTIFICATION SYSTEM

The table below gives details on the product identification system for maXTouch devices. See "Orderable Part Numbers" below for example part numbers for the mXT2113TG-AT/mXT2113TG-AB.

To order or obtain information, for example on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–XXX	[X]	[X]	[XXX]
Device	Package	Temperature Range	Tape and Reel Option	Pattern

Device:	Base device name		
Package:	A	=	QFP (Plastic Quad Flatpack)
	AM	=	VQFN (Plastic Very Thin Quad Flat No Lead)
Temperature Range:	T	=	–40°C to +85°C (Grade 3)
	B	=	–40°C to +105°C (Grade 2)
Tape and Reel Option:	*Blank*	=	Standard Packaging (Tube or Tray)
	R	=	Tape and Reel (1)
Pattern:	Extension, QTP, SQTP, Code or Special Requirements (Blank Otherwise)		

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. See "Orderable Part Numbers" below or check with your Microchip Sales Office for package availability with the Tape and Reel option.

Orderable Part Numbers

Orderable Part Number	Firmware Revision	Description
ATMXT2113TG-ATVAO (Supplied in trays)	1.0.AA	144-lead LQFP 20 × 20 × 1.4 mm, RoHS compliant Operating temperature range –40°C to +85°C (Grade 3)
ATMXT2113TG-ATRVAO (Supplied in tape and reel)		
ATMXT2113TG-ABVAO (Supplied in trays)	1.0.AA	144-lead LQFP 20 × 20 × 1.4 mm, RoHS compliant Operating temperature range –40°C to +105°C (Grade 2)
ATMXT2113TG-ABRVAO (Supplied in tape and reel)		

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- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

THE MAXTOUCH WEB SITE

Information on Microchip's maXTouch product line can be accessed via the microchip web site at www.microchip.com, This information is also available for direct access via a short-cut at www.maxtouch.com. The maXTouch web pages contain the following information:

- **Product Information** – Product specifications, brochures, datasheets, protocol guides
- **Tools and Software** – Evaluation kits, maXTouch Studio, software libraries for individual maXTouch touch controllers
- **Training and Support** – Generic application notes and training material for the maXTouch product range

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