NEC

TFT COLOR LCD MODULE

Type: NL128102AC28-01E
46cm (18.1 Type), SXGA
Analog, Full-color

SPECIFICATIONS

Third edition

PRELIMINARY

This document is preliminary. All information in this document is subject to change without prior notice.

The former specifications (filed number DOD-H-7451, issued October 4, 1999)

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CONTENTS

1. DESCRIPTION

NL128102AC28-01E is a TFT (thin film transistor) active matrix color liquid crystal display (LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight.
NL128102AC28-01E has a built-in backlight with an inverter.

The 46cm(18.1" Type) diagonal display area contains 1280 × 1024 pixels and can display full-color (more than 16 million colors simultaneously). Also, it has wide viewing angle and multi-scan function. Therefore, this module is so called Super Fine TFT.

2. FEATURES

- Ultra wide viewing angle with lateral electric field.
- High luminance and Low reflection
- Analog RGB signals
- Multi-scan function: e.g., SXGA, XGA, SVGA, VGA, VGA-TEXT, PC-9801, MAC, SUN
- Direct type backlight (Eight lamps, Inverter)
- Backlight unit replaceable (Type No. : 181LHS03)
- On Screen Display
  Application with the OSD function might conflict with patents in Europe and/or the U.S.A. If you apply the OSD function appreciate the patents at your side.
- Approved by UL1950 Third Edition and CSA-C22.2 No.950-95

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VESA:	Video Electronics Standards Association
DPMS:	Display Power Management Signaling
DDC1:	Display Data Channel 1
DDC2B:	Display Data Channel 2B

3. APPLICATIONS

- Engineering work stations, Desk-top type of PCs
- Display terminals for control system
- Monitors

4. STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. Sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate creates the TFT panel structure. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.

RGB (red, green, blue) data signals from a source system is modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.

Acting as an Electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

5. OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	359.04(H) × 287.232(V)mm
Drive system	a-Si TFT active matrix
Display colors	full-color
Number of pixels	1280 × 1024
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.2805(H) × 0.2805(V)mm
Module size	424.0(H) × 337.0(V) × 38.5 typ. (D) mm
Weight	2000 g(typ.)
Contrast ratio	300:1(typ.)

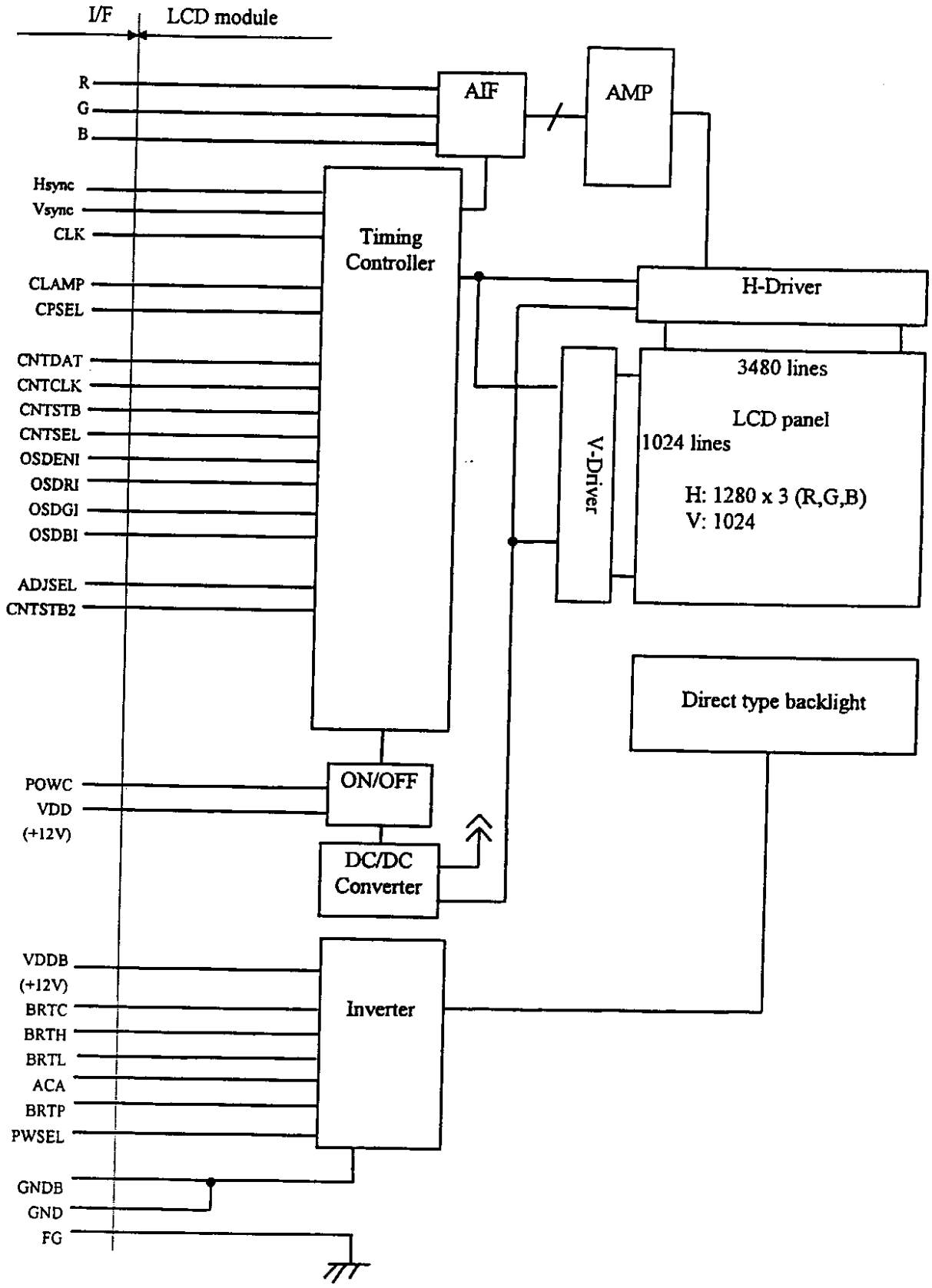
Viewing angle (more than the contrast ratio of 10:1)

- Horizontal: 85 ° (typ. , left side, right side)
- Vertical: 85 ° (typ. , up side, down side)

Optimum grayscale (γ =2.2): perpendicular

Pencil hardness	3 H (min. JIS K5400)
Color gamut	60 % (typ. At center, To NTSC)
Response time	40 ms (typ.), " black " to " white "
Luminance	200 cd/m^2 (typ.)
Signal system	Analog RGB signals, Synchronous signals(Hsync, Vsync), Dot clock(CLK)
Supply voltage	12 V, 12 V (Logic, LCD driving, Backlight)
Backlight	Direct type: Eight cold cathode fluorescent lamps with inverter 〈Replacement parts〉 Inverter Parts No. : 181PW031 Backlight unit Parts No. : 181LHS03
Power consumption	40.8 W (typ.)

6. BLOCK DIAGRAM



Note 1: FG (Frame Ground) is not connected to GND and GNDB.

7. SPECIFICATIONS

7.1 GENERAL SPECIFICATIONS

Items	Contents	Unit
Module size	424.0±1.0 (H) x 337.0±1.0 (V) x 40.0 (max.)(D)	mm
Display area	359.04 (H) x 287.232 (V)	mm
Number of dots	1280 x 3 (H) x 1024 (V)	dots
Pixel pitch	0.2805 (H) x 0.2805 (V)	mm
Dot pitch	0.0935 (H) x 0.2805 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	–
Display colors	full color	Color
Weight	2000 (typ.) 2100 (max.)	g

7.2 ABSOLUTE MAXIMUM RATINGS

Parameters	Symbols	Ratings	Unit	Remarks
Supply voltage	VDD	-0.3 to +14	V	Ta=25℃
	VDDB	-0.3 to +14	V	
Logic input voltage	Vin1	-0.3 to +5.5	V	Ta=25℃ VDD=12V
R,G, B input voltage	Vin2	-6.0 to +6.0	V	
CLK input voltage	Vin3	-7.0 to +7.0	V	
BRTL input voltage	Vin4	-0.3 to +1.5	V	
Storage temp.	Tst	-20 to +60	℃	–
Operating temp.	Top	0 to +55	℃	Module surface Note 1
Relative humidity (RH) Note 2	≦ 95%		%	Ta≦40 ℃
	≦ 85%		%	40<Ta≦50 ℃
	≦ 70%		%	50<Ta≦55 ℃
Absolute humidity Note 2	Absolute humidity (g/m^3) shall not exceed Ta=55℃, RH=70% level.		g/m^3	Ta>55 ℃

Note 1: Measured at the surface of LCD panel
Note 2: No condensation

7.3 ELECTRICAL CHARACTERISTICS

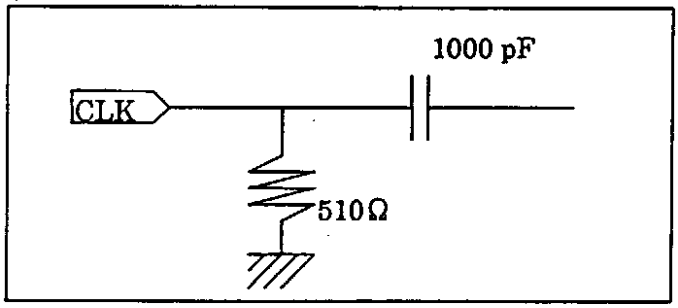
(1) Logic, LCD driving, Backlight

(Ta=25℃)

Items	Symbols	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	VDD	11.4	12.0	12.6	V	for LCD driving
	VDDB	11.4	12.0	12.6	V	for backlight
Logic input " L " voltage	ViL1	0	–	0.8	V	for BRTP
Logic input " H " voltage	ViH1	2.0	–	5.25	V	
Logic input " L " voltage	ViL2	0	–	0.8	V	for except BRTP
Logic input " H " voltage	ViH2	2.0	–	5.25	V	
CLK input voltage	ViCLK	0.6	–	1.0	Vp-p	for CLK
CLK DC input voltage	ViDC CLK	-4.5	–	+4.5	V	
Logic input " L " current 1	IiL1	-10	–	–	μA	for Hsync, Vsync
Logic input " H " current 1	IiH1	–	–	160	μA	
Logic input " L " current 2	IiL2	-10	–	–	μA	for CNTSEL, CPSEL, and POWC
Logic input " H " current 2	IiH2	–	–	10	μA	
Logic input " L " current 3	IiL3	-10	–	–	μA	for CNTDAT, CNTSTB, CNTCLK, CLAMP, OSDENI, OSDRI, OSDGI, OSDBI, ADJDEL, CNTSTB2
Logic input " H " current 3	IiH3	–	–	1400	μA	
Logic input " L " current 4	IiL4	-1580	–	–	μA	for BRTP
Logic input " H " current 4	IiH4	–	–	3500	μA	
Logic input " L " current 5	IiL5	-810	–	–	μA	for BRTC, PWSEL, and ACA
Logic input " H " current 5	IiH5	–	–	440	μA	
Supply current	IDDB	–	2550 note 1	3500	mA	for backlight VDDB=12.0V (Max. luminance)
	IDD	–	850 note 1	1400	mA	for LCD driving VDD=12.0V

Note 1: The display is Dot- checkered pattern.

(2)CLK input equivalent circuit



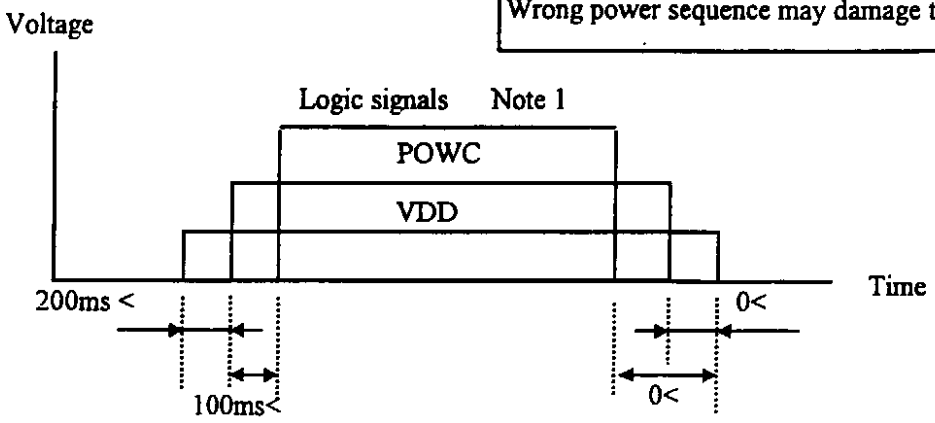
(3) Video signal (R, G, B) input

(Ta=25℃)

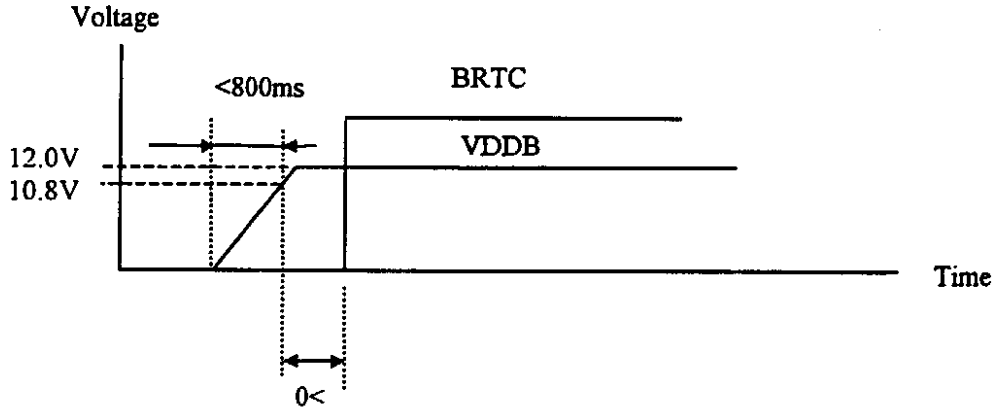
Items	Min.	Typ.	Max.	Unit	Remarks
Maximum amplitude (white – black)	0 (black)	0.7 (white)	0.9	Vp-p	Need to adjust contrast if input is more than 0.7Vp-p
DC input level (black)	-3.5	–	+3.5	V	–

7.4 POWER SUPPLY SEQUENCE

CAUTION
Wrong power sequence may damage the module.



Note 1: Synchronous signals, Control signals, CLK



(1) Logic signals (synchronous signals and control signals) should be "0" voltage (V), when VDD is not input. If input voltage to signal lines is higher than 0.3 V, the internal circuit will be damaged.

(2) LCD module will shut down the power supply of driving voltage to LCD panel internally, when one of CLK, Hsync, and Vsync is not input more than 90 ms typically.
As the display data are unstable in this period, the display maybe disordered. But the backlight works correctly even this period. So the backlight should be controlled by BRTC signal.

(3) The backlight ON/OFF (BRTC signal) should be controlled while logic signals are supplied. The backlight power supply (VDDB) is not related to the power supply sequence. However, unstable data will be displayed when the backlight power is turned ON with no logic signals.

(4) Keep POWC signal "L" more than 200 ms after the power supply (VDD) is input, if POWC signal is controlled.

(5) Analog RGB inputs are independent from this power supply sequence.

(6) 12V for backlight should be started up within 800ms, otherwise, the protection circuit makes the backlight turn off.

(7)The backlight is turned off with safety circuit, when "L" period of BRTP signal is input more than 50 ms.

(8) Do not input "H" ACA and PWSEL, when VDD is 0V or BRTC is "L".

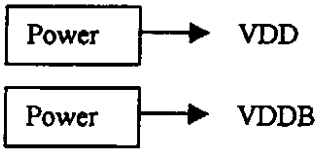
(9) Ripple of supply voltage

Supply voltage	VDD (for logic and LCD driver)	VDDB (for backligth)
Acceptable range	≦ 100 m Vp-p	≦ 200 m Vp-p

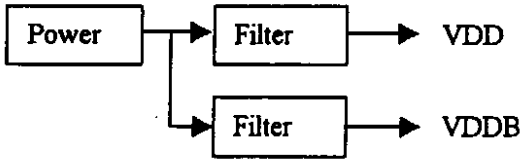
Note 1: The acceptable range of ripple voltage includes spike noise.

Example of the power supply connection

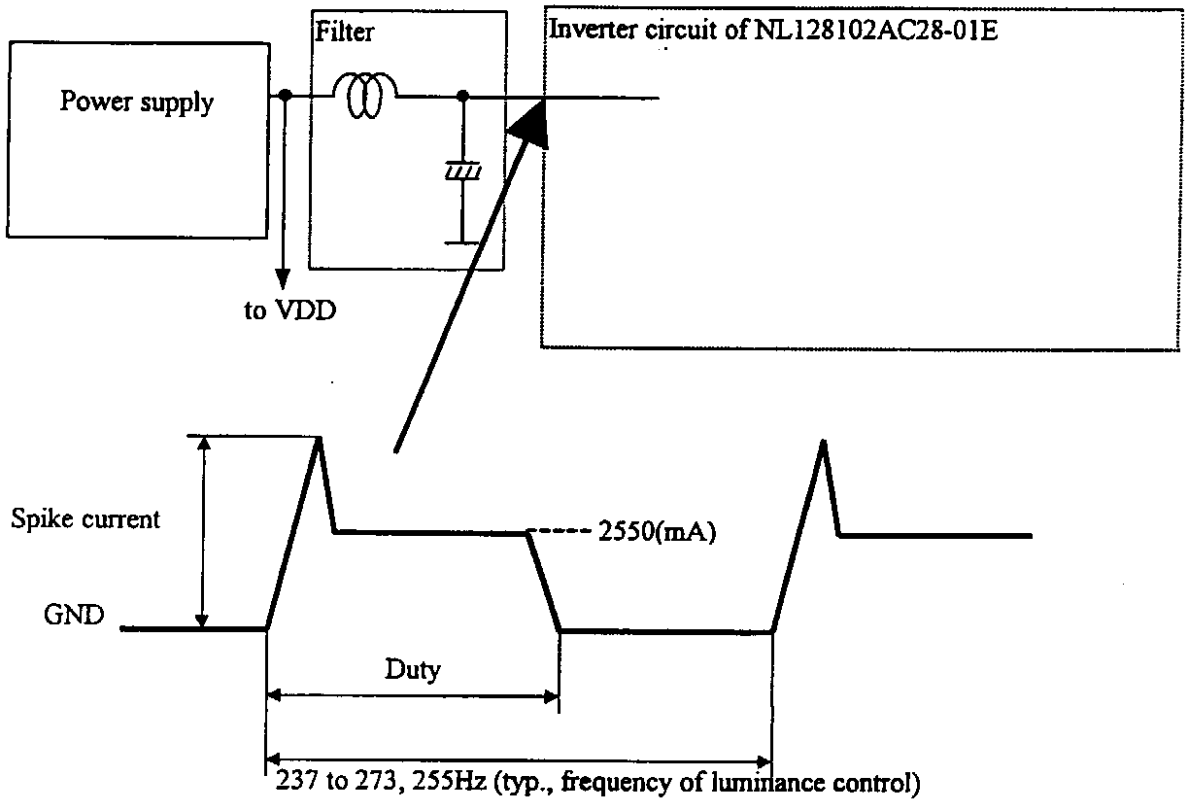
a) Separate the power supplies



b) Put the filters



(10) Inverter current wave



In the maximum luminance, the inverter current is DC. However, in the luminance control by BRTP signal, the above duty varies 100% to 20% and the spike current, which causes the noise on the screen, may be observed. In this case, adjust the value of the capacitance in the above filter to eliminate the noise on the screen.

(11) Fuse

Supply voltage	Part No.	Supplier	Ratings	Remarks
VDD	CCP2E50TE	KOA	2A	-
VDDB	MMCT 5A	SOC	5A	-

Remarks: Before the power is designed, the fuses should be considered. The power capacity should be use more than 2 times of fuse rating.
In case of small power capacity, the module should be evaluated enough.

7.5 INTERFACE PIN CONNECTIONS

(1) CN1

Part No. : MRF03-6R-SMT
Adaptable socket : MRF03-2 × 6P-1.27(For cable type) or MRF03-6PR-SMT(For board to board type)
Supplier : HIROSE ELECTRIC CO., LTD. (coaxial type)

Pin No.	Symbols	Pin No.	Symbols
1	B	4	Vsync
2	G	5	Hsync
3	R	6▼	CLK

Figure from socket view

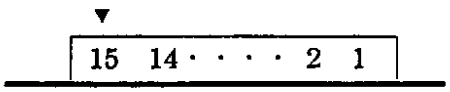
(2) CN2

Part No. : IL-Z-15PL-SMTY
Adaptable socket : IL-Z-15S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbols	Pin No.	Symbols
1	VDD	9	GND
2	VDD	10	CNTCLK
3	GND	11	CPSEL
4	GND	12	CLAMP
5	POWC	13	GND
6	CNTSEL	14	N.C.
7	CNTDAT	15▼	GND
8	CNTSTB	-	

Note 1:N.C. (No connection) must be open.

Figure from socket view

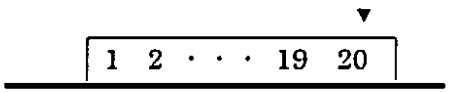


(3) CN3

Part No. : DF14A-20P-1.25H
Adaptable socket : DF14-20S-1.25C
Supplier : HIROSE ELECTRIC CO., LTD. (coaxial type)

Pin No.	Symbols	Pin No.	Symbols
1	GND	11	ADJSEL
2	OSDENI	12	N.C.
3	GND	13	CNTSTB2
4	OSDBI	14	GND
5	GND	15	N.C.
6	OSDGI	16	GND
7	GND	17	N.C.
8	OSDRI	18	N.C.
9	GND	19	N.C.
10	N.C.	20▼	N.C.

Figure from socket view



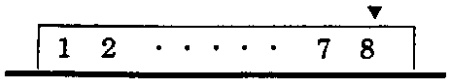
(4) CN201

Part No. : DF3-8P-2H
Adaptable socket: DF3-8S-2C
Supplier: HIROSE ELECTRIC CO., LTD.

Pin No.	Symbols	Pin No.	Symbols
1	GNDB	5	VDDB
2	GNDB	6	VDDB
3	GNDB	7	VDDB
4	GNDB	8 ▼	VDDB

note 1: N.C. (No connection) must be open.

Figure from socket view

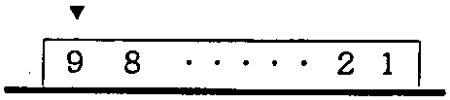


(5) CN202

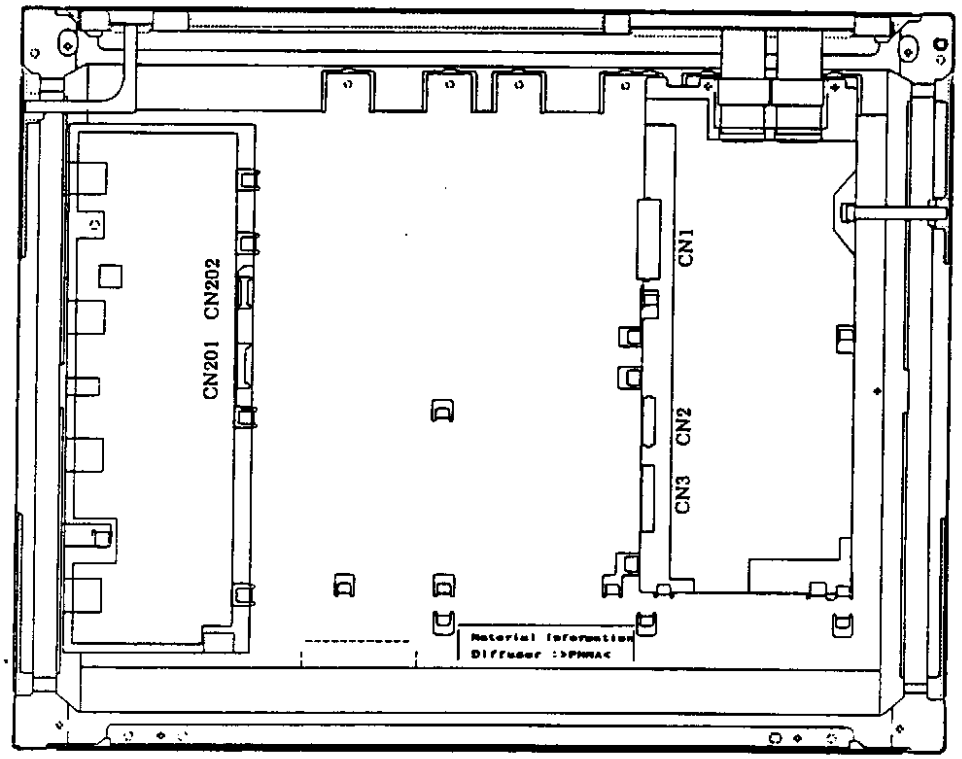
Part No. : IL-Z-9PL1-SMTY
Adaptable socket: IL-Z-9S-S125C3
Supplier: Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbols	Pin No.	Symbols
1	GNDB	6	BRTL
2	GNDB	7	BRTP
3	ACA	8	GNDB
4	BRTC	9 ▼	PWSEL
5	BRTH	-	

Figure from socket view



Rear view



7.6 PIN FUNCTIONS

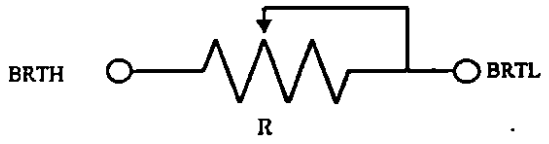
Symbols	I/O	Logic	Description
CLK	Input	Negative	Dot clock input. (ECL level) Timing signal for display data.
Hsync	Input	Negative	Horizontal synchronous signal input (TTL level)
Vsync	Input	Negative	Vertical synchronous signal input (TTL level)
R	Input	—	Red video signal input (0.7Vp-p, input impedance 75Ω)
G	Input	—	Green video signal input (0.7Vp-p, input impedance 75Ω)
B	Input	—	Blue video signal input (0.7Vp-p, input impedance 75Ω)
POWC	Input	Positive	Power control signal (TTL level) "H" or "open" : Logic and LCD powers are on. "L" : Logic and LCD powers are off. (Note 2)
CNTSEL	Input	—	Display control signal in case of serial communications.(TTL level) "H" or "Open" : Default "L" : External control Serial communications are set up by external control.
CNTDAT	Input	Positive	Display control data (TTL level) Detail of CNTDAT is mentioned in 7.7 FUNCTIONS.
CNTCLK	Input	Positive	CLK for display control data (TTL level) Detail of CNTCLK is mentioned in 7.7 FUNCTIONS.
CNTSTB	Input	Positive	Latch pulse for display control data (TTL level) Detail of CNTSTB is mentioned in 7.7 FUNCTIONS.
CPSEL	Input	—	Clamp function select signal (TTL level) "H" or "Open" : Default "L" : CLAMP signal is possible.(External control)
CLAMP	Input	Positive	Clamp timing signal of black level (TTL level) This mode works in CPSEL = "L".
ACA	Input	Positive	Luminance control signal(TTL level) "H" or "Open" : Normal luminance "L" : Low luminance (1/2 of normal luminance)
BRTC	Input	Positive	Backlight ON/OFF control signal(TTL level) "H" or "Open" : Backlight on "L" : Backlight off
BRTH	Input	—	Backlight luminance control-1 Variable resistor control(Note 3) or voltage control (Note 4) These controls work in BRTP = "Open".
BRTL	Input	—	
BRTP	Input	—	Backlight luminance control-2 (TTL level) BRTP signal control (Note 5)
PWSEL	Input	—	Luminance control select signal (TTL level) "H" or "Open" : Variable resistor control or voltage control "L" : BRTP signal control
ADJSEL	Input	Positive	Contrast, brightness select control signal (TTL level) "H" or "Open" : Default "L" : External control Serial communications are set up by external control.

Symbols	I/O	Logic	Description
CNTSTB2	Input	Positive	Latch pulse2 for display control data Detail of CNTSTB2 is mentioned in **7.9 OSD FUNCTIONS.**
OSDRI	Input	–	OSD Red input (TTL level) Detail of OSDRI is mentioned in **7.9 OSD FUNCTIONS.**
OSDGI	Input	–	OSD Green input (TTL level) Detail of OSDGI is mentioned in **7.9 OSD FUNCTIONS.**
OSDBI	Input	–	OSD Blue input (TTL level) Detail of OSDBI is mentioned in **7.9 OSD FUNCTIONS.**
OSDENI	Input	Positive	OSD enable signal (TTL 0level) Detail of OSDENI is mentioned in **7.9 OSD FUNCTIONS.**
VDD	–	–	VDD (+12V±5%) power supply for logic and LCD driving.
VDDB	–	–	VDDB (+12V±5%) power supply for backlight. (Note 1)
GND	–	–	Ground for logic and LCD driving (VDD) GND is connected to the module GND (FG).
GNDB	–	–	Ground for backlight power supply (VDDB) GNDB is not connected to the module GND (FG).

Note 1: When POWC is "L", serial communication data is clear, please set again. When POWC is "L", logic input signal has to be all "0V". If more than "0.3V" is inputted, the LCD module may be broken.

Note 2: The way of luminance control by a variable resistor

This way works in PWSEL = "H" or "Open" and in BRTP = "Open". The variable resistor for luminance control should be 10kΩ type, and zero point of the resistor correspond to minimum luminance.



Mating variable resistor:
10KΩ±5% , B curve

Maximum luminance (100%): R= 10KΩ
Minimum luminance (30%; ACA="H", 60%; ACA="L"): R= 0Ω

Note 4: The way of luminance control by voltage

This way works in PWSEL = "H" or "Open" and in BRTP = "Open". If luminance is controlled with BRTH/BRTL input voltage, at first BRTH is "0V", and BRTL input voltage controls luminance. When BRTL input voltage is "1V", the luminance becomes maximum, and when BRTL input voltage is "0V", the luminance becomes minimum.

Maximum luminance (100%): BRTL="1V"
Minimum luminance (30%; ACA="H", 60%; ACA="L"): BRTL="0V"

Note 5: The way of luminance control with BRTP signal
Detail of **7.10 OUTSIDE CONTROL FOR LUMINANCE**

7.7 FUNCTIONS

This LCD module has following functions by serial data input (table 1)

(1) Expansion mode:	See table 2 and 7.8 EXPANSION FUNCTIONS
(2) Control Display position (VERTICAL):	See table 3
(3) Control Display position (HORIZONTAL):	See table 6
(4) Control CLK delay:	See table 4
(5) Change CLK fall/rise synchronous:	See table 5
(6) Contrast control:	See table 9, 10 and 7.8.4 COLOR CONTROL FUNCTION AND GRAPH IMAGE
(7) Sub-Contrast control:	
(8) Sub-Brightness control:	

Set up the following items to work the above functions

(A) CLK counts of horizontal period:	See table 7
(B) CLK frequency range:	See table 8

7.7.1 HOW TO USE THE ABOVE FUNCTIONS

If CNTSEL is "L", the above functions((1)-(5))are valid. (CNTSEL is "H" or open, default values are valid.) After serial data are transferred, the data is latched by CNTSTB. Once, the data is latched, the above functions((1)-(5)) are effective.

If ADJSEL is "L", the above functions((6)-(8))are valid. (ADJSEL is "H" or open, default values are valid.) After serial data are transferred, the data is latched by CNTSTB2. Once, the data is latched, the above functions((6)-(8)) are effective.

Please keep CNTSTB/2 to be "L" during transferring data. Input data can be changed during power on, but LCD display may be disturbed. When the serial data are changed, we recommend that the backlight power is off using BRTC function.

Table 1. CNTDAT (Serial data) Composition

DATA	DATA name	Function	
D0	VEX3	Expansion mode	See table 2
D1	VEX2	Expansion mode	
D2	VEX1	Expansion mode	
D3	VEX0	Expansion mode	
D4	VD10	Vertical display position (MSB)	See table 3
D5	VD9	Vertical display position	
D6	VD8	Vertical display position	
D7	VD7	Vertical display position	
D8	VD6	Vertical display position	
D9	VD5	Vertical display position	
D10	VD4	Vertical display position	
D11	VD3	Vertical display position	
D12	VD2	Vertical display position	
D13	VD1	Vertical display position	
D14	VD0	Vertical display position (LSB)	
D15	DELAY6	CLK delay (MSB)	See table 4
D16	DELAY5	CLK delay	
D17	DELAY4	CLK delay	
D18	DELAY3	CLK delay	
D19	DELAY2	CLK delay	
D20	DELAY1	CLK delay	
D21	DELAY0	CLK delay (LSB)	
D22	CKS	CLK signal	See table 5
D23	HD8	Horizontal display position (MSB)	See table 6
D24	HD7	Horizontal display position	
D25	HD6	Horizontal display position	
D26	HD5	Horizontal display position	
D27	HD4	Horizontal display position	
D28	HD3	Horizontal display position	
D29	HD2	Horizontal display position	
D30	HD1	Horizontal display position	
D31	HD0	Horizontal display position (LSB)	
D32	HSE10	CLK counts of horizontal period (MSB)	See table 7
D33	HSE9	CLK counts of horizontal period	
D34	HSE8	CLK counts of horizontal period	
D35	HSE7	CLK counts of horizontal period	
D36	HSE6	CLK counts of horizontal period	
D37	HSE5	CLK counts of horizontal period	
D38	HSE4	CLK counts of horizontal period	
D39	HSE3	CLK counts of horizontal period	
D40	HSE2	CLK counts of horizontal period	
D41	HSE1	CLK counts of horizontal period	
D42	HSE0	CLK counts of horizontal period (LSB)	
D43	MOD1	CLK frequency select	See table 8
D44	MOD0	CLK frequency select	

Table 1. CNTDAT Composition (continuation)

DATA	DATA name	Function	
AD11	DAA0	Color adjust select data (LSB)	See table 10
AD10	DAA1	Color adjust select data	
AD9	DAA2	Color adjust select data	
AD8	DAA3	Color adjust select data (MSB)	
AD7	DAD7	Color adjust data (MSB)	See table 9
AD6	DAD6	Color adjust data	
AD5	DAD5	Color adjust data	
AD4	DAD4	Color adjust data	
AD3	DAD3	Color adjust data	
AD2	DAD2	Color adjust data	
AD1	DAD1	Color adjust data	
AD0	DAD0	Color adjust data (LSB)	

Table 2. Expansion mode (VEX3 to VEX0 : 4bit)

VEX3	VEX2	VEX1	VEX0	Vertical magnification	Display mode	Display image
0	0	0	0	1	SXGA	Standard Note 1
0	0	0	1	1.25	XGA	See 7.8.3 DISPLAY IMAGE
0	0	1	0	1.6	SVGA, MAC	
0	0	1	1	2.0	VGA	
0	1	0	0	2.5	PC98,VGA-TEXT	
0	1	0	1	–	Prohibit	
0	1	1	0	–	Prohibit	
0	1	1	1	–	Prohibit	
1	0	0	0	1.1	SUN	
1	0	0	1	–	Prohibit	
1	0	1	0	–	Prohibit	
1	0	1	1	–	Prohibit	
1	1	0	0	–	Prohibit	
1	1	0	1	–	Prohibit	
1	1	1	0	–	Prohibit	
1	1	1	1	–	Prohibit	

Note 1: Display mode is SXGA, when CNTSEL is "H" or open".

Table 3. Vertical display position (VD10 to VD0 : 11bit)

VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0	Vertical position [H] note 1
0	0	0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	0	0	1	Prohibit
0	0	0	0	0	0	0	0	0	1	0	Prohibit
0	0	0	0	0	0	0	0	0	1	1	Prohibit
0	0	0	0	0	0	0	0	1	0	0	4
0	0	0	0	0	0	0	0	1	0	1	5
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047 note 2

Note 1: The number of horizontal line between Vsync-fall and RGB data valid.
Note 2: The maximum number is based on horizontal line count of the display mode.
Note 3: Vertical position is fixed at 41H, when CNTCEL is "H" or "open".

Table 4. CLK delay (DELAY6 to DELAY0 : 7bit)

DELAY[6..0]	Delay (relative)		Unit	DELAY[6..0]	Delay (relative)		Unit	DELAY[6..0]	Delay (relative)		Unit
00H	9.54	(0)	ns	30H	24.58	(15.04)	ns	60H	39.72	(30.18)	ns
01H	9.9	(0.36)	ns	31H	24.89	(15.35)	ns	61H	40.03	(30.49)	ns
02H	10.21	(0.67)	ns	32H	25.2	(15.66)	ns	62H	40.34	(30.8)	ns
03H	10.52	(0.98)	ns	33H	25.5	(15.98)	ns	63H	40.65	(31.11)	ns
04H	10.86	(1.32)	ns	34H	25.85	(16.31)	ns	64H	40.99	(31.45)	ns
05H	11.17	(1.63)	ns	35H	26.15	(16.61)	ns	65H	41.3	(31.76)	ns
06H	11.49	(1.95)	ns	36H	26.47	(16.93)	ns	66H	41.62	(32.08)	ns
07H	11.81	(2.27)	ns	37H	26.79	(17.25)	ns	67H	41.93	(32.39)	ns
08H	12.06	(2.52)	ns	38H	27.06	(17.52)	ns	68H	42.23	(32.69)	ns
09H	12.37	(2.83)	ns	39H	27.37	(17.83)	ns	69H	42.53	(32.99)	ns
0AH	12.68	(3.14)	ns	3AH	27.68	(18.14)	ns	6AH	42.84	(33.3)	ns
0BH	12.99	(3.45)	ns	3BH	27.99	(18.45)	ns	6BH	43.15	(33.61)	ns
0CH	13.33	(3.79)	ns	3CH	28.33	(18.79)	ns	6CH	43.49	(33.95)	ns
0DH	13.64	(4.1)	ns	3DH	38.64	(19.1)	ns	6DH	43.8	(34.26)	ns
0EH	13.96	(4.42)	ns	3EH	28.96	(19.42)	ns	6EH	44.12	(34.58)	ns
0FH	14.27	(4.73)	ns	3FH	29.28	(19.74)	ns	6FH	44.45	(34.91)	ns
10H	14.54	(5)	ns	40H	29.51	(19.97)	ns	70H	44.71	(35.17)	ns
11H	14.85	(5.31)	ns	41H	29.83	(20.29)	ns	71H	45.02	(35.48)	ns
12H	15.16	(5.62)	ns	42H	30.17	(20.63)	ns	72H	45.33	(35.79)	ns
13H	15.47	(5.93)	ns	43H	30.48	(20.94)	ns	73H	45.64	(36.06)	ns
14H	15.81	(6.27)	ns	44H	30.82	(21.28)	ns	74H	45.98	(36.44)	ns
15H	16.12	(6.58)	ns	45H	31.12	(21.58)	ns	75H	46.28	(36.74)	ns
16H	16.44	(6.9)	ns	46H	31.45	(21.91)	ns	76H	46.6	(37.06)	ns
17H	16.76	(7.22)	ns	47H	31.78	(22.24)	ns	77H	46.92	(37.38)	ns
18H	17.04	(7.5)	ns	48H	32.12	(22.58)	ns	78H	47.21	(37.67)	ns
19H	17.35	(7.81)	ns	49H	32.45	(22.91)	ns	79H	47.52	(37.98)	ns
1AH	17.66	(8.12)	ns	4AH	32.79	(23.23)	ns	7AH	47.83	(38.29)	ns
1BH	17.97	(8.43)	ns	4BH	33.09	(23.55)	ns	7BH	48.14	(38.6)	ns
1CH	18.31	(8.77)	ns	4CH	33.44	(23.9)	ns	7CH	48.48	(38.94)	ns
1DH	18.62	(9.08)	ns	4DH	33.74	(24.2)	ns	7DH	48.79	(39.25)	ns
1EH	18.95	(9.41)	ns	4EH	34.06	(24.52)	ns	7EH	49.11	(39.57)	ns
1FH	19.26	(9.72)	ns	4FH	34.41	(24.87)	ns	7FH	49.4	(39.86)	ns
20H	19.57	(10.03)	ns	50H	34.7	(25.16)	ns				
21H	19.89	(10.35)	ns	51H	35.01	(25.47)	ns				
22H	20.21	(10.67)	ns	52H	35.32	(25.78)	ns				
23H	20.53	(10.99)	ns	53H	35.63	(26.09)	ns				
24H	20.86	(11.32)	ns	54H	35.97	(26.43)	ns				
25H	21.17	(11.63)	ns	55H	36.28	(26.74)	ns				
26H	21.49	(11.95)	ns	56H	36.6	(27.06)	ns				
27H	21.82	(12.28)	ns	57H	36.91	(27.27)	ns				
28H	22.07	(12.53)	ns	58H	37.17	(27.63)	ns				
29H	22.38	(12.84)	ns	59H	37.48	(27.94)	ns				
2AH	22.69	(13.15)	ns	5AH	37.79	(28.25)	ns				
2BH	23	(13.46)	ns	5BH	38.1	(28.56)	ns				
2CH	23.34	(13.8)	ns	5CH	38.44	(28.9)	ns				
2DH	26.65	(14.11)	ns	5DH	38.76	(29.22)	ns				
2EH	23.97	(14.43)	ns	5EH	39.09	(29.55)	ns				
2FH	24.28	(14.74)	ns	5FH	39.41	(29.87)	ns				

Note 1: DELAY[6..0] is fixed at 00H, when CNTSEL is "H" or "open".

note 2: This delay value is typical value at Ta=25℃. And the value varies by the ambient temperature and the module itself.

Please set up a preferable display position. See the following references.

① Variation of CLK delay by temperature drift. (only reference) The temperature constant of CLK delay is 0.2%/℃.

Calculated example:

In case of delay time is 20ns at Ta=25℃;

(a) In case Ta rising to 50℃.

Increase of delay time → (50℃−25℃)×0.002×20ns=+1ns

So, the total delay time is 21 ns at Ta=50℃.

(b) In case Ta falling to 0℃.

Decrease of delay time → (0℃−25℃)×0.002×20ns=-1ns

So, the total delay time is 19 ns at Ta=0℃.

② Variation of CLK delay time against each LCD module. (only reference)

−10.5% to +14.4%

Table 5. CLK reverse signal

CKS	FUNCTION
0	DATA is sampled on rising edge of CLK. 
1	DATA is sampled on falling edge of CLK. 

Note 1: CKS is "0", when CNTSEL is "H" or "open".

Table 6. Horizontal display position (HD8 to HD0 : 9bit)

HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	Horizontal position [CLK] Note 1
0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	1	Prohibit
·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·
0	0	1	1	1	1	1	1	1	Prohibit
0	1	0	0	0	0	0	0	0	64
0	1	0	0	0	0	0	0	1	65
·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·
1	1	1	1	1	1	1	0	1	509
1	1	1	1	1	1	1	1	0	510
1	1	1	1	1	1	1	1	1	511

Note 1: The number of CLK between Hsync-fall and RGB data valid.

Note 2: Horizontal position is set at 360 CLK, when CNTSET is "H" or "open".

Table 7. CLK counts of horizontal period (HSE10 to HSE0 : 11bit)

HSE10	HSE9	HSE8	HSE7	HSE6	HSE5	HSE4	HSE3	HSE2	HSE1	HSE0	CLK countNote 1
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047

Note 1: The number of CLK between Hsync signals.
Note 2: CLK number is set 1688 CLK, when CNTSEL is "H" or "open".
Note 3: If setting value is different from actual input signal, it may cause to malfunction.

Table 8. CLK frequency select (MOD1 to MOD0 : 2bit)

MOD1	MOD0	CLK frequency [MHz]
0	0	90 to 135
0	1	65 to 90
1	0	50 to 65
1	1	20 to 50

Note 1: Set complying with input CLK frequency.
Note 2: CLK frequency is set 90 to 135 MHz, when CNTSEL is "H" or "open".

Table 9. Color control data (DAD7 to DAD0 : 8bit)

DAD7	DAD6	DAD5	DAD4	DAD3	DAD2	DAD1	DAD0	Adjusting value
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
0	1	1	1	1	1	1	1	127
1	0	0	0	0	0	0	0	128
1	0	0	0	0	0	0	1	129
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

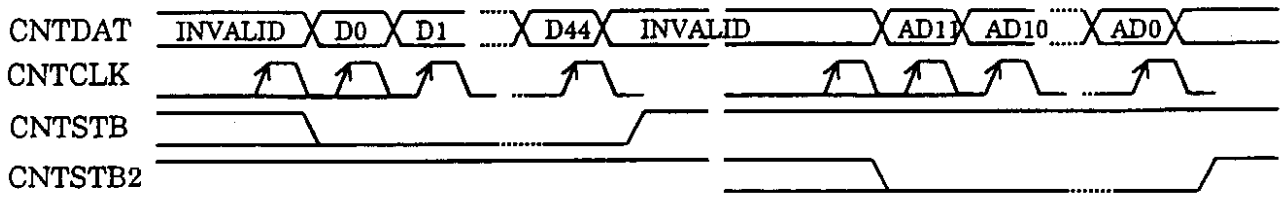
Note 1: Adjust value for selecting function above table.10.
Note 2: Different D/A-range depends on function selected.
Note 3: See more detail 7.8.4. COLOR CONTROL FUNCTIONS AND GRAPH IMAGES.

Table 10. Color adjust select data (DAA3 to DAA0 : 4bit)

DAA3	DAA2	DAA1	DAD0	Function
0	0	0	0	Prohibit
0	0	0	1	Main contrast
0	0	1	0	Prohibit
0	0	1	1	Prohibit
0	1	0	0	Sub-contrast R
0	1	0	1	Sub-contrast G
0	1	1	0	Sub-contrast B
0	1	1	1	Sub-brightness R
1	0	0	0	Sub-brightness G
1	0	0	1	Sub-brightness B
1	0	1	0	Prohibit
1	0	1	1	Prohibit
1	1	0	0	Prohibit
1	1	0	1	Prohibit
1	1	1	0	Prohibit
1	1	1	1	Prohibit

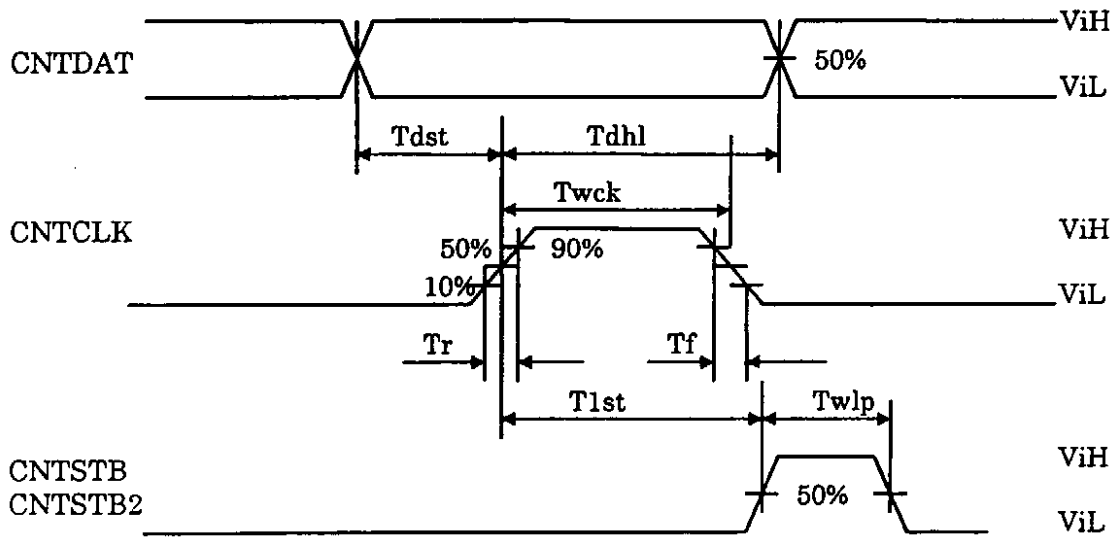
Note 1: See more detail 7.8.4. COLOR CONTROL FUNCTIONS AND GRAPH IMAGES.

7.7.2 SERIAL COMMUNICATION TIMINGS



Parameters	Symbols	Min.	Max.	Unit	Remarks
CLK pulse-width	Twck	50	—	ns	CNTCLK
CLK frequency	Fclk	—	5	MHz	
DATA set-up-time	Tdst	50	—	ns	CNTDAT
DATA hold-time	Tdhl	50	—	ns	
Latch pulse-width	Twlp	50	—	ns	CNTSTB, CNTSTB2
Latch set-up-time	T1st	50	—	ns	
Rise / fall time	Tr , Tf	—	50	ns	CNT xxx

SERIAL COMMUNICATION WAVEFORM



7.8 EXPANSION FUNCTIONS

7.8.1 HOW TO USE EXPANSION MODES

Expansion mode is a function to expand screen. For example, VGA signal has 640 × 480 pixels. But, if the display data can expanded to 2.0 times vertically and horizontally, VGA screen image can be displayed fully on the screen of SXGA resolution.

This LCD module has the function that expands vertical direction as shown in Table 1. And expanding horizontal direction is possible by setting input CLK frequency equivalent to the magnification. It is necessary to make this CLK outside of this LCD module.

Please adopt this mode after evaluating display quality, because the appearance in expansion mode is happened to be relatively bad in some cases.

The followings show display magnifications for each mode.

Input display	Number of pixels	Magnification	
		Vertical	Horizontal note 1
SXGA	1280 x 1024	1	1
XGA	1024 x 768	1.25	1.25
SVGA	800 x 600	1.6	1.6
VGA	640 x 480	2.0	2.0
VGA text	720 x 400	2.5	1.7
PC9801	640 x 400	2.5	2.0
MAC	832 x 624	1.6	1.5
SUN	1152 x 900	1.1	1.1

note 1: The horizontal magnification multiples the input clock(CLK).

Input CLK = system CLK × horizontal magnification

Example: In case of SXGA and VGA, CLK frequency can be decided as follows.

SXGA: System CLK(108.0MHz) × 1.0=108.0MHz

VGA : System CLK(25.175MHz) × 2.0= 50.25MHz

7.8.2 SETTING SERIAL DATA FOR EXPANSION

Input signal								Module serial-data setting		
Mode	System CLK [MHz]	Hsync [kHz]	Vsync [Hz]	Horizontal		Vertical		HSE	HD	VD
				Count Number [CLK]	DSP [CLK]	Count Number [H]	DSP [H]	Calculation formula		
				(A)	(B)	–	(C)	(A)x Ver.magni	(B)x Hor.magni	=(C)
SXGA (1280 x1024)	108.0	63.981	60.02	1688	360	1066	41	(A) x 1	(B) x 1	=(C)
	117.0	71.691	67.189	1632	336	1067	41			
	125.0	75.120	71.204	1664	352	1055	28			
	130.076	76.968	72.000	1690	378	1069	42			
	135.0	78.125	72.005	1728	384	1085	58			
	135.0	79.976	75.025	1688	392	1066	41			
XGA (1024 x 768)	65	48.363	60.004	1344	296	806	35	(A) x 1.25	(B) x 1.25	
	75	56.476	70.069	1328	280	806	35			
	78.75	60.023	75.029	1312	272	800	31			
MAC (832x624)	57.283*	49.725	74.5	1152	288	667	42	(A)x1.5	(B)x1.5	
SVGA (800 x 600)	36*	35.156	56.25	1024	200	625	24	(A) x 1.6	(B) x 1.6	
	40*	37.879	60.317	1056	216	628	27			
	50*	48.077	72.188	1040	184	666	29			
	49.5*	46.875	75	1056	240	666	24			
VGA (640 x 480)	25.175*	31.469	59.94	800	144	525	35	(A) x 2.0	(B) x 2.0	
	31.5*	37.861	72.809	832	168	520	31			
	31.5*	37.5	75	840	184	500	19			
	30.24*	35.0	66.667	864	160	525	42			
VGA text (720 x 400)	28.322*	31.469	70.087	900	153	449	37	(A) x 1.7	(B) x 1.7	
PC9801 (640 x 400)	21.053*	24.827	56.432	848	144	440	33	(A) x 2.0	(B) x 2.0	
SUN (1152 x 900)	94.500*	61.845	66.003	1528	336	937	35	(A) x 1.1	(B) x 1.1	

*: Standard timings (Please set them up properly for correct expansion.

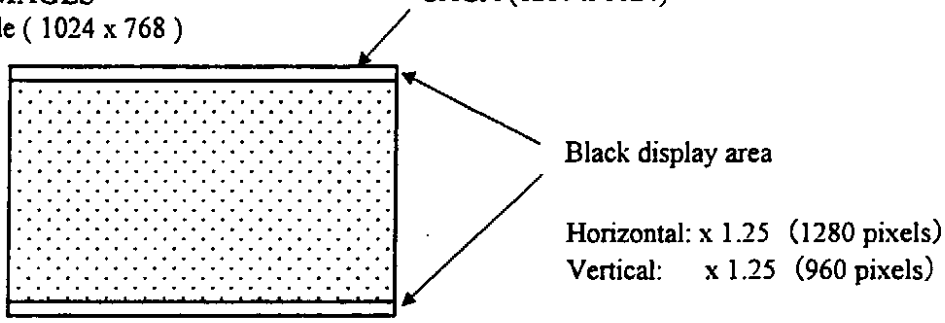
Note 1: DSP = Display Start Period. DSP is total of "pulse-width" and "back-porch".

Note 2: HD and VD are approximate value. Set HD and VD in case of adjusting display to the screen center.

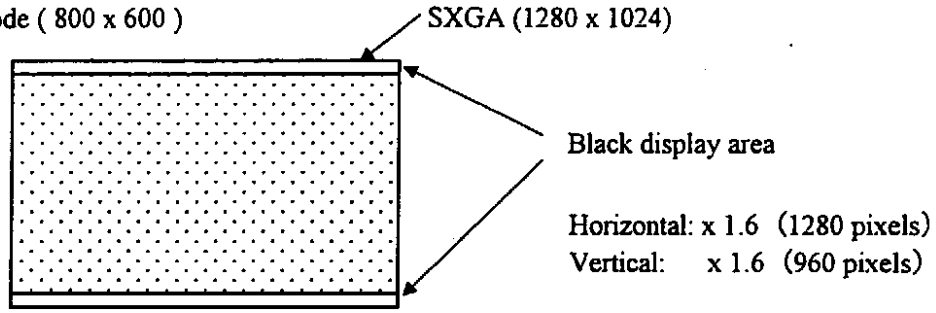
Note 3: The pulse-width of Hsync, Vsync and Back-porch are the same as SXGA-mode (Standard-mode).

7.8.3 DISPLAY IMAGES

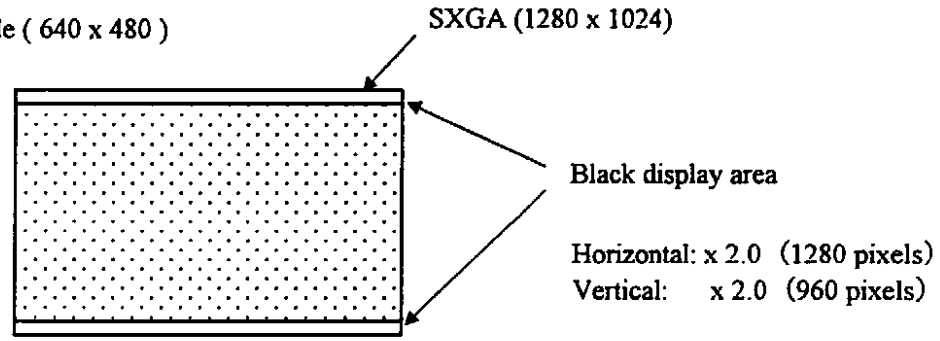
1) XGA mode (1024 x 768)



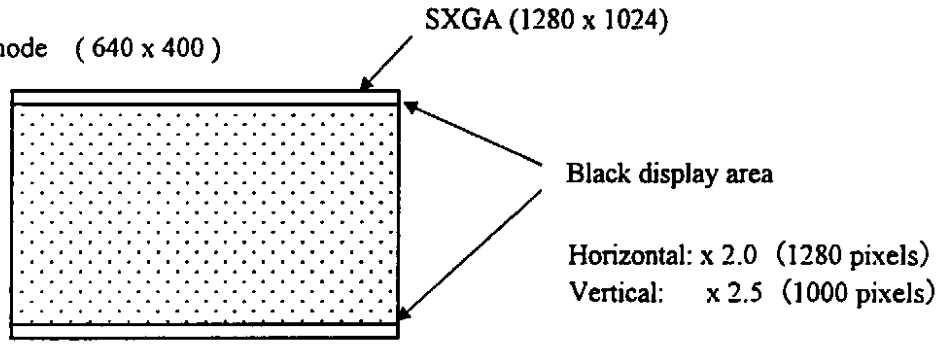
2) SVGA mode (800 x 600)



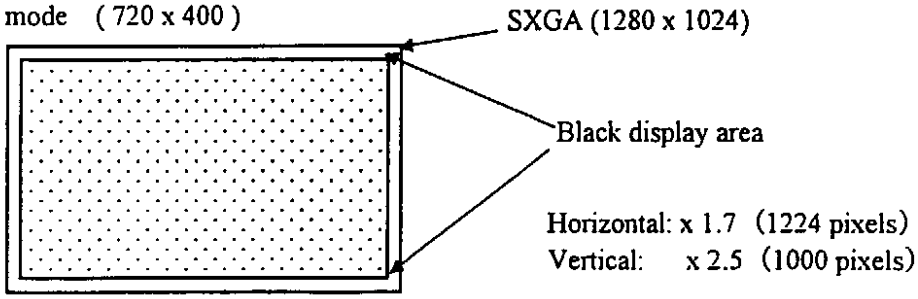
3) VGA mode (640 x 480)



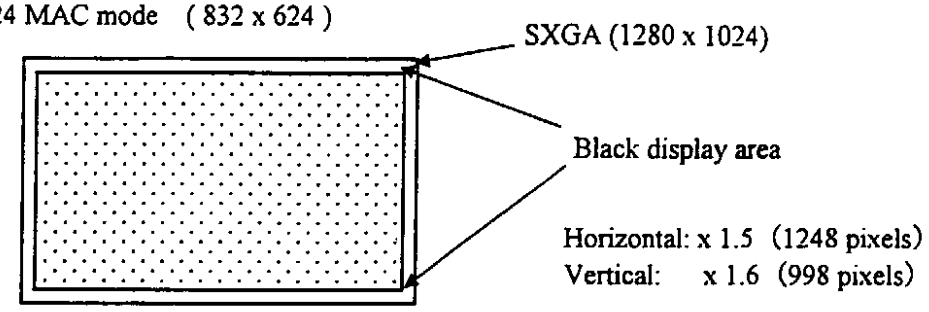
4) PC9801 mode (640 x 400)



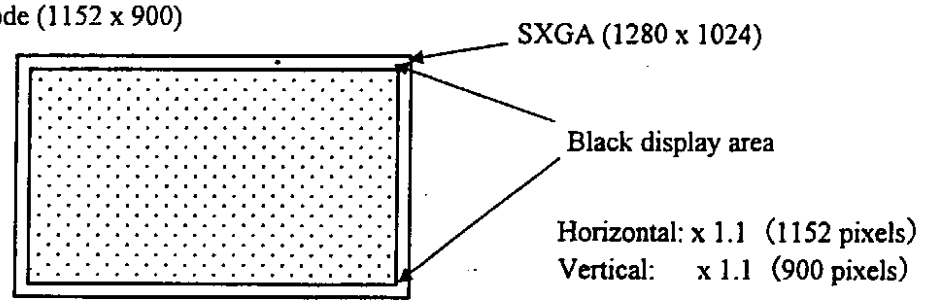
5) VGA text mode (720 x 400)



6) 832 x 624 MAC mode (832 x 624)



7) SUN mode (1152 x 900)



7.8.4 COLOR CONTROL FUNCTIONS AND GRAPHIC IMAGE

This LCD module can adjust the following functions by serial data input (table.1)

(1) Main contrast:
(2) Sub-contrast each R,G,B:
(3) Sub-brightness each R,G,B:

} See table 9, 10 and **7.8.4 COLOR CONTROL FUNCTION AND GRAPH IMAGE**

(1) Main contrast

Main contrast is adjusted R/G/B contrast at the same time with controlling the amplitude of input video signal.

Default value: 128, Valid range: 78 to 198
Contrast minimum: 198
Contrast maximum: 78
ADJSEL="H" or "Open" : Default value=128

(2) Sub-contrast R,G,B

Sub-contrast can adjust each R/G/B with controlling the amplitude of input video signal.

Default value: 128, Valid range: 78 to 198
Contrast minimum: 78
Contrast maximum: 198
ADJSEL="H" or "Open" : Default value=128

(3) Sub-brightness R,G,B

Sub-brightness can adjust each R/G/B with adjusting the black level of input video signal.

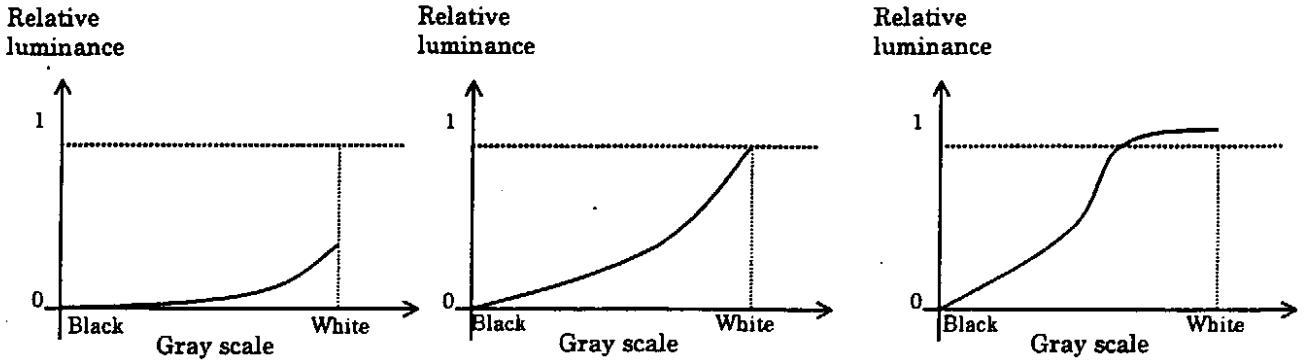
Default value: 128, Valid range: 55 to 163
Brightness minimum: 163
Brightness maximum: 55
ADJSEL="H" or "Open" : Default value=128

Note1: If the values is go over above valid range, LCD module will not be destroy. However LCD will be inferiority. Please keep values within the valid range.

Note2: Although set up the same values are set up for each LCDs, each LCD color might be slightly ill be different. And also, will be afraid to deviate values from optical characteristics. Please adopt this functions evaluating display quality.

《GRAPH IMAGE》

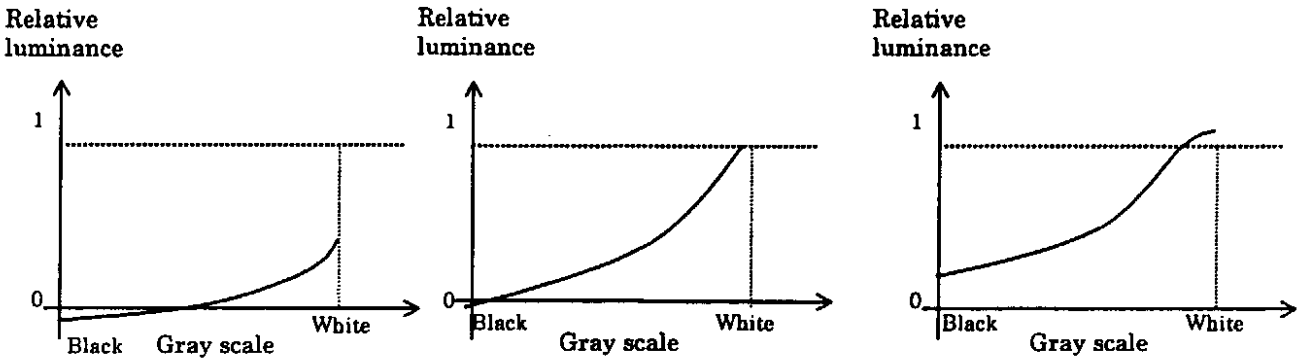
・Main contrast & Sub contrast



Main contrast
Max value ◄——— DEFAULT ———► Min value

Sub contrast
Min value ◄——— DEFAULT ———► Max value

・Sub brightness



Sub brightness
Min value ◄——— DEFAULT ———► Max value

Note 1: In case that the value of the relative luminance is over 1, the display becomes un-uniformity like Gost.

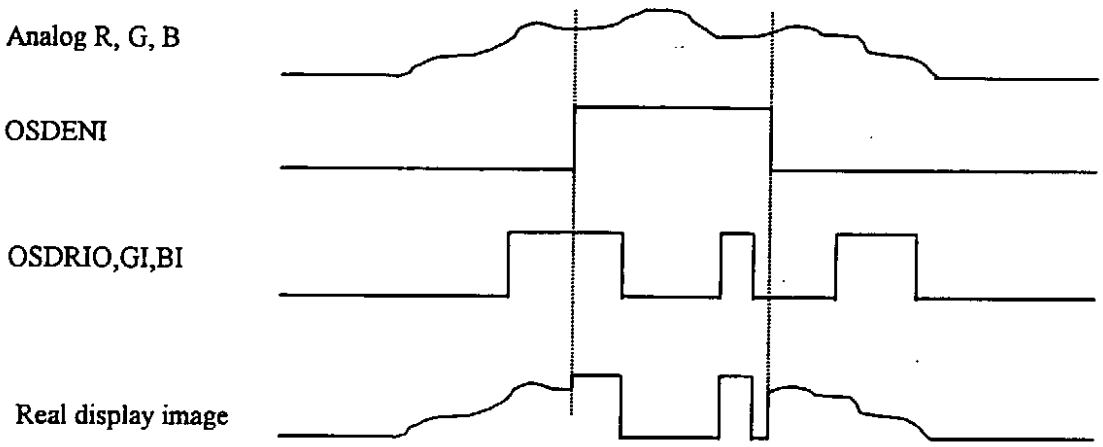
7.9 OSD FUNCTIONS

OSD (On Screen Display) is the function to display the other digital data on the input analog valid data. Possible to display 1 bit data for each R/G/B color (8 colors). OSD function is valid for the period of OSDENI

OSDRI, OSDGI, and OSDBI: digital data for OSD
OSDENI="H": OSD signal is valid
OSDENI="L": OSD signal is not valid

OSD is the sub-display for function-control and the display quality will not be guaranteed. Please adopt the OSD image evaluating display quality.

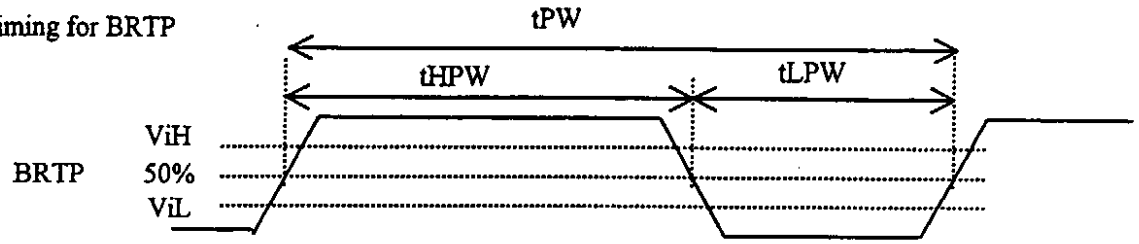
《OSD image》



7.10 OUTSIDE CONTROL FOR LUMINANCE

Outside control is valid, when PWSEL="L" and input signal for BRTP. Luminance can be controlled by the duty value of input signal for BRTP.
Duty=100%: luminance is maximum. (100%)
Duty=20%: luminance is minimum. (30%)

Timing for BRTP



Parameters	Symbols	Min.	Typ.	Max.	Unit	Remarks
Frequency	1/tPW	185	–	325	Hz	–
"L" period	tLPW	–	–	50	ms	
Pulse-width	tHPW/tPW	20	–	100	%	at max. luminance (100%)
Input voltage	ViL	0	-	0.8	V	–
	ViH	2.0	–	5.25	V	–

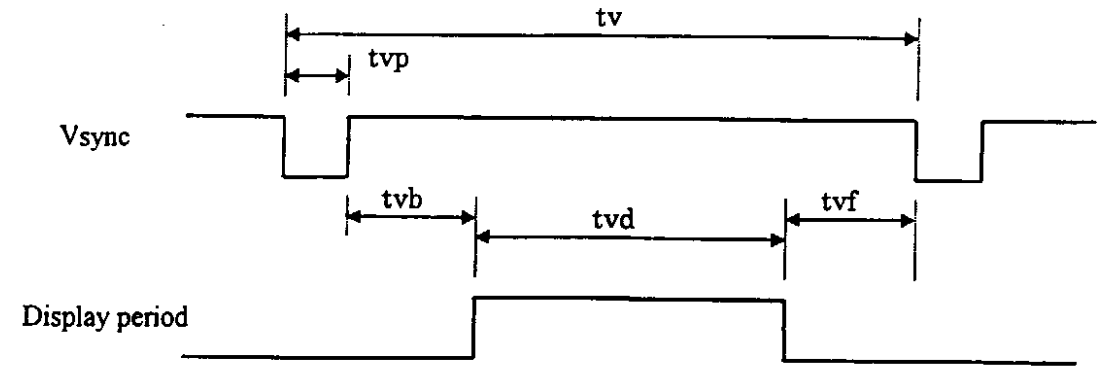
Regarding set up for frequency, refer to the below method.
Set up frequency = Vsync frequency × (n+0.25) or (n+0.75)
Adopt the frequency evaluating the display quality, because the display will be disturbed depend on frequency.

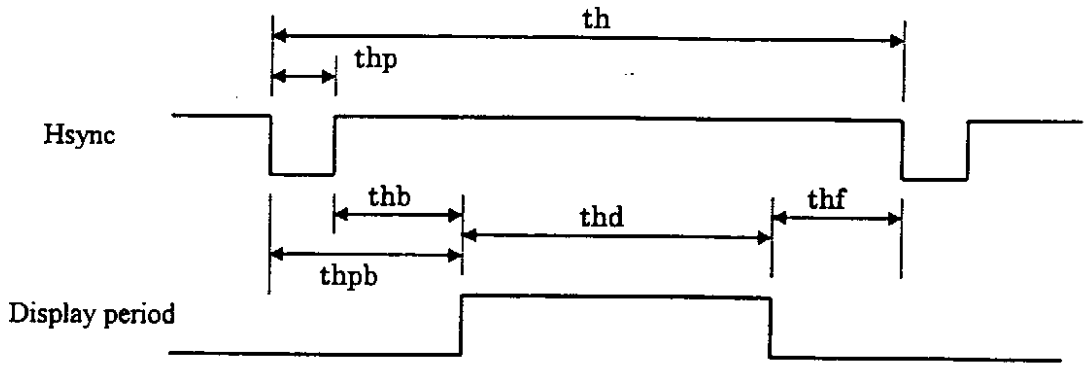
7.11 INPUT SIGNAL TIMINGS

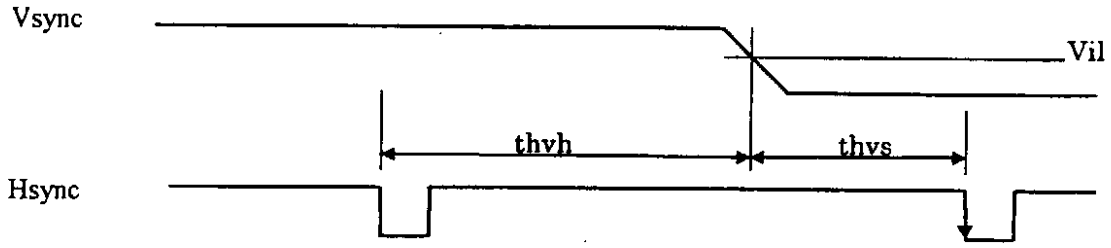
7.11.1 SXGA MODE (STANDARD)

Name		Symbols	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency	1/tc	95.0 –	108.0 9.3	135.0 –	Mhz ns	SXGA standard
	Rise / Fall	tcrf	–	–	10	ns	–
	Pulse-width	tc / tcl	0.4	0.5	0.6	–	–
Hsync	Period	th	12.3 –	15.630 1688	17.0 –	μs CLK	63.981kHz (typ.)
	Display	thd	– –	11.852 1280	– –	μs CLK	–
	Front-porch	thf	– 10	0.444 48	– –	μs CLK	–
	Pulse-width	thp	– 16	1.037 112	– –	μs CLK	–
	Back-porch	thb	1.0 94	2.296 248	– –	μs CLK	Note 1
	Pulse-width +Back-porch	thbp	1.8	–	–	μs	–
	V-Hsync timing hold/setup time	thvh	3	–	–	ns	–
		thvs	1	–	–	CLK	–
	Rise / Fall	thrf	–	–	10	ns	–
Vsync	Period	tv	13.3 –	16.661 1066	18.5 –	ms H	60.020Hz (typ.)
	Display	tvd	– –	16.005 1024	– –	ms H	–
	Front-porch	tvf	– 1	0.016 1	– –	ms H	–
	Pulse-width	tvp	– 2	0.047 3	– –	ms H	–
	Back-porch	tvb	– 5	0.594 38	– –	ms H	–

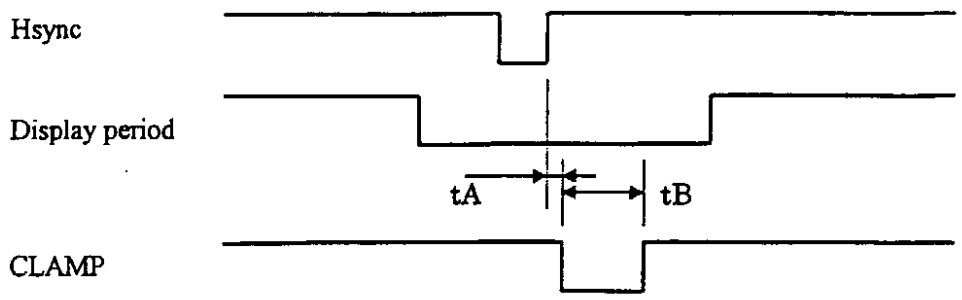
Note 1: Minimum value of Back-porch (thb) must be satisfied with both 1.0 μs and 94 CLK.


tv
tvp
Vsync
tvb
tvd
tvf
Display period


th
thp
Hsync
thb
thd
thf
thpb
Display period


Vsync
Vil
thvh
thvs
Hsync

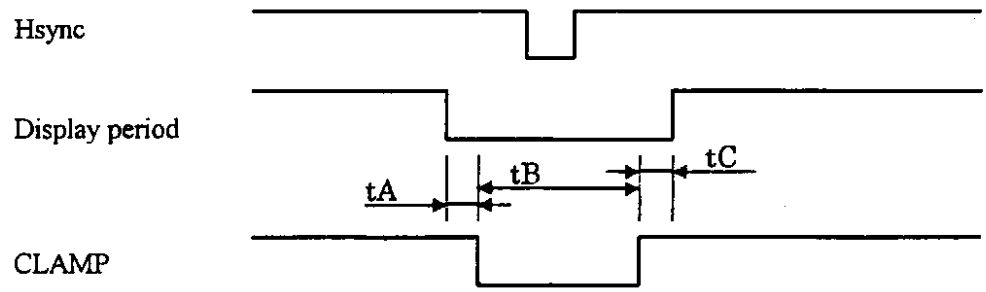
7.11.2 TIMING FOR GENERATING CLAMP SIGNAL INTERNALLY



MOD1	MOD2	tA [CLK]	tB[CLK]
0	0	2	41
0	1		27
1	0		20
1	1		15

note 1: Exclude noises on analog R, G, B signals, because analog R, G, B signals are the black level reference during CLAMP="L". If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

7.11.3 TIMING FOR INPUTTING CLAMP SIGNAL FROM OUTSIDE

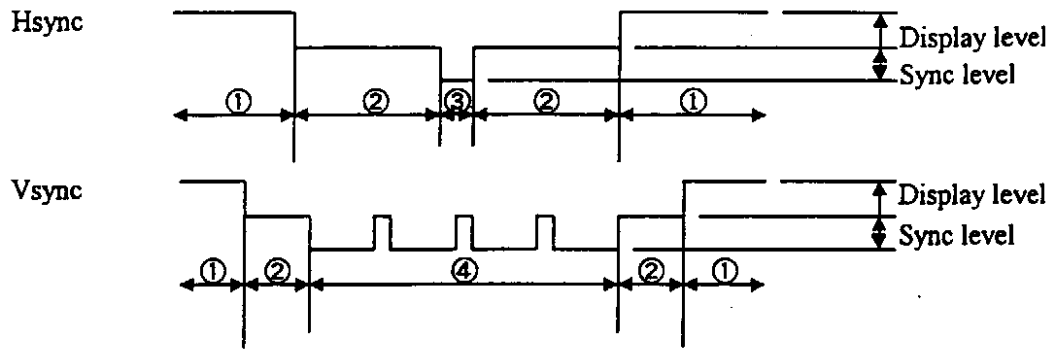


Items	Min.	Typ.	Max.	Unit	Remarks
tA	0.1	—	—	μs	—
tB	0.3	—	—	μs	—
tC	0.2	—	—	μs	—

note 1: Exclude noises on analog R, G, B signals, because analog R, G, B signals are the black level reference during CLAMP="L". If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

note 2 : Attention for using Sync On Green signal
Clamp signals must be input during black level period as next page.
If Clamp signals are input during other period, the display becomes un-uniformity.

Sync on Green Input signal timings



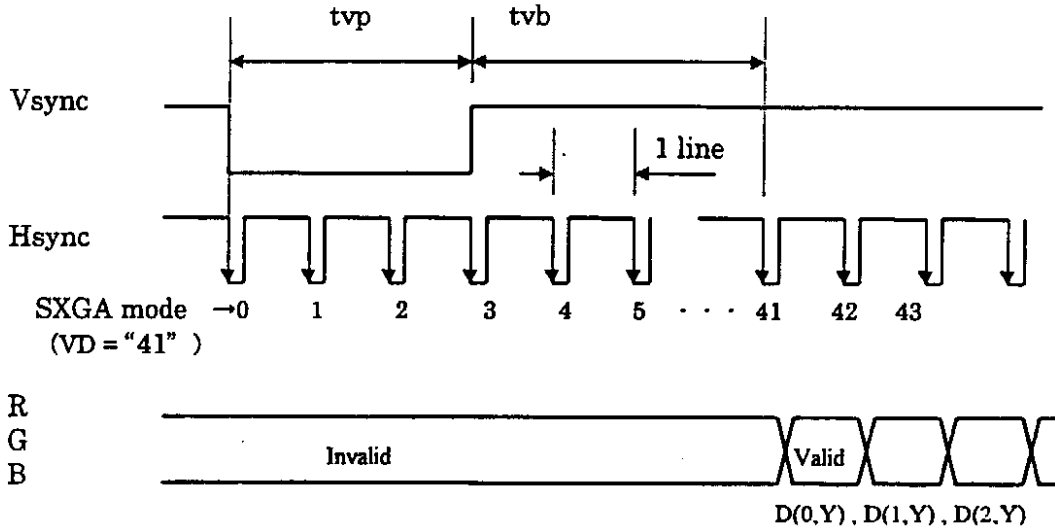
①:Display period ②:Black level period ③:Hsync period ④:Vsync period

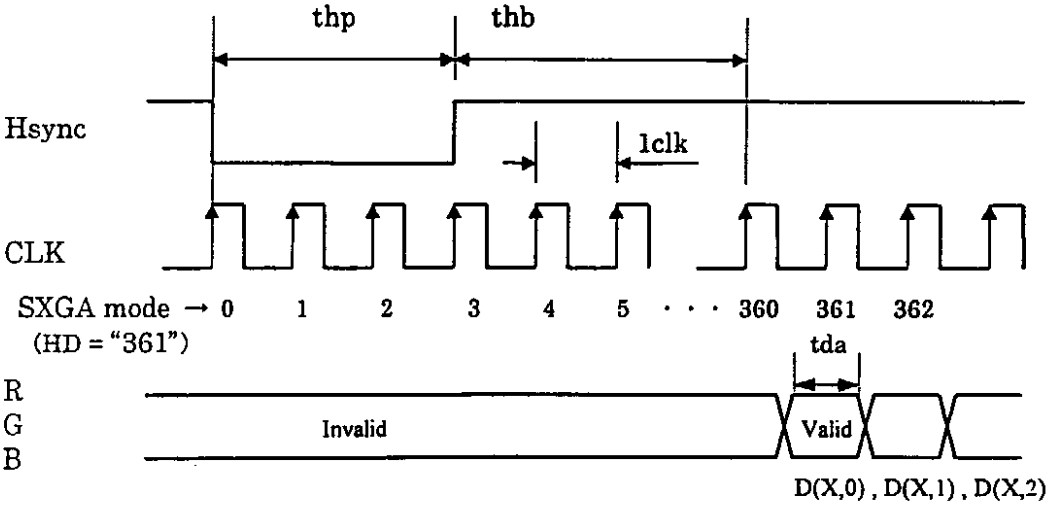
7.12 INPUT SIGNAL AND DISPLAY POSITIONS

7.12.1 SXGA STANDARD TIMINGS

Pixels

D(0,0)	D(1,0)	D(2,0)	· · · · · ·	D(1279,0)
D(0,1)	D(1,1)	D(2,1)	· · · · · ·	D(1279,1)
D(0,2)	D(1,2)	D(2,2)	· · · · · ·	D(1279,2)
·	·	·		·
·	·	·	· · ·	·
·	·	·		·
·	·	·		·
D(0,1023)	D(1,1023)	D(2,1023)	· · · · · ·	D(1279,1023)





note 1: The tda should be more than 4ns

7.13 OPTICAL CHARACTERISTICS

(Ta = 25℃, VDD = 12V, VDDB = 12V)

Items	Symbols	Condition	Min.	Typ.	Max.	Unit	Remarks
Contrast ratio	CR	γ=2.2 viewing angle θR=0°, θL=0°, θD=0°, White/Black, at center	200	300	-	-	note 1
Luminance	Lvmax	White, at center	150	200	-	cd/m^2	note 2
Luminance uniformity	—	White	-	1.10	1.30	-	note 3

Reference data

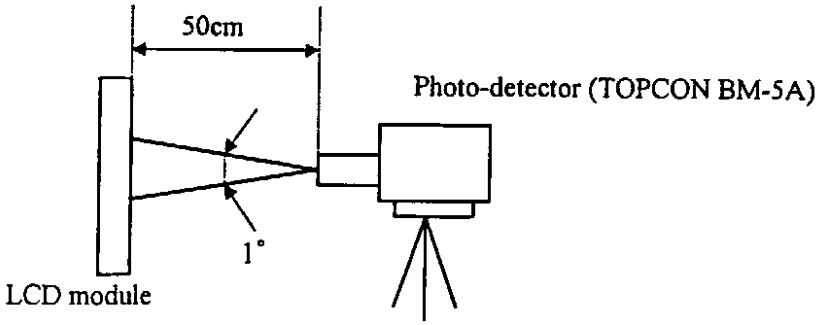
(Ta = 25℃, VDD = 12V, VDDB = 12V)

Items	Symbols	Condition	Min.	Typ.	Max.	Unit	Remarks
Chromaticity Coordinates	C	θR=0°, θL=0°, θU=0°, θD=0°, at center, to NTSC	50	60	-	%	-
	W	White (x, y)	-	0.302, 0.312	-	-	-
	R	Red (x, y)	-	0.618, 0.339	-	-	-
	G	Green (x, y)	-	0.311, 0.584	-	-	-
	B	Blue (x, y)	-	0.143, 0.095	-	-	-
Viewing angle range (CR>10)	θR	CR > 10, θU=0°, θD=0°	70	85	-	deg.	note 4
	θL		70	85	-	deg.	
	θU	CR > 10, θR=0°, θL=0°	70	85	-	deg.	
	θD		70	85	-	deg.	
Viewing angle range (CR>5)	θR	CR > 5, θU=0°, θD=0°	-	85	-	deg.	
	θL		-	85	-	deg.	
	θU	CR > 5, θR=0°, θL=0°	-	85	-	deg.	
	θD		-	85	-	deg.	
Response time (Panel surface temperature =29℃)	Ton	Black to White	-	40	70	ms	note 5
	Toff	White to Black	-	35	60		
Luminance control range	—	Maximum luminance(100%)	-	30 to 100	—	%	-

note 1: The contrast ratio is calculated by using the following formula.

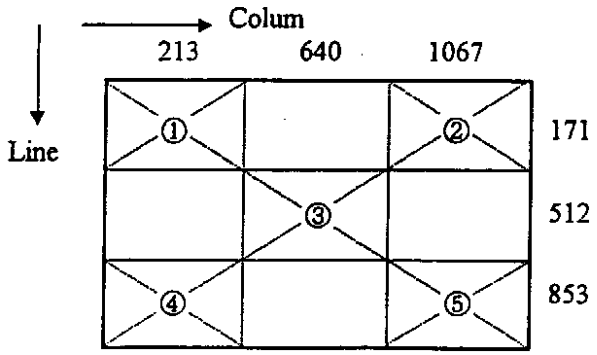
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in "white"}}{\text{Luminance with all pixels in "black"}}$$

note 2: The luminance is measured after 20 minutes from the module works, with all pixels in "white". The typical value is measured after luminance saturation.

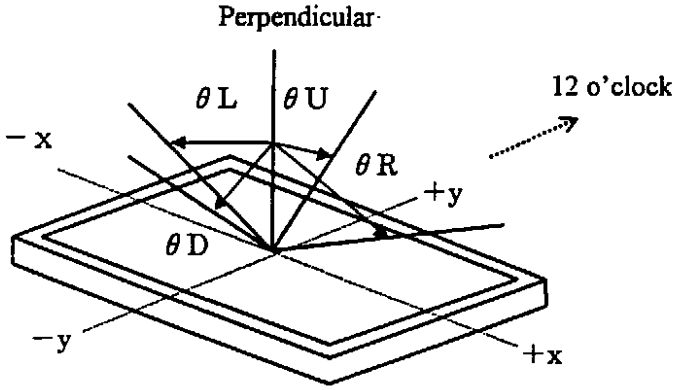


$$\text{Luminance uniformity} = \frac{\text{Maximum luminance}}{\text{Minimum luminance}}$$

The luminance is measured at near the five points shown below.

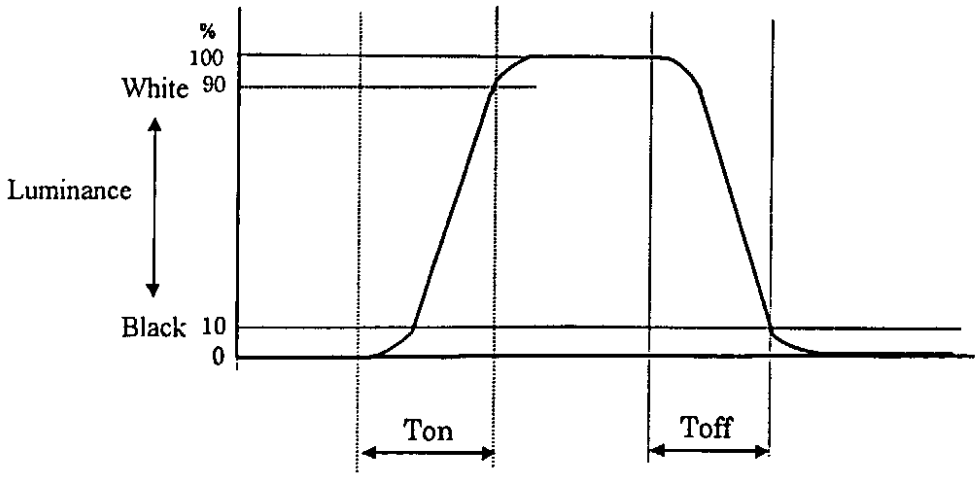


note 4: Definitions of viewing angle are as follows.



note 5: Definitions of response time is as follows.

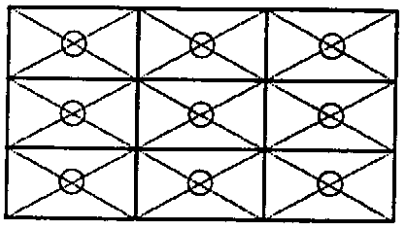
Photo-detector out put signal is measured when the luminance changes "black" to "white". Response time is the time between 0% and 90% of the photo-detector output amplitude.



7.14 RELIABILITY TEST

Test items	Test condition	Judgment
High temperature/humidity operation	60±2℃, RH=60% 240 hours, Display data is black.	*1
Heat cycle (operation)	① 0℃±3℃···1 hour 55℃±3℃···1 hour ② 50 cycles , 4 hours/cycle ③ Display data is black.	*1
Thermal shock (non-operation)	① -20℃±3℃···30 minutes 60℃±3℃···30 minutes ② 100 cycles ③ Temperature transition time is within 5 minutes.	*1
Vibration (non-operation)	① 5-100Hz, 11.76m/s^2(1.2G) 1 minute/cycle, X,Y,Z direction ② 10 times each direction	*1, *2
Mechanical shock (non-operation)	① 294m/s^2(30G), 11ms X,Y,Z direction ② 3 times each direction	*1, *2
ESD (operation)	150pF, 150Ω, ±10kV 9 places on a panel *3 10 times each place at one-second intervals	*1
Dust (operation)	15 kinds of dust (JIS-Z 8901) Hourly 15 seconds stir, 8 times repeat	*1

*1: Display function is checked by the same condition as LCD module out-going inspection.
*2: Physical damage
*3: Discharge points are shown in the figure.



7.15 EXPECTED LIFE-TIME OF THE LAMP

	Lamp
Condition	Luminance Maximum Room temp. (25±2℃) , Continuous operation
Expected value (MTTF)	45,000 h
Criteria	Half value luminance (compared with initial value.)

Note 1: The life-time is expected value (reference).
Note 2: This expected value is based on the test results with a bare lamp operation.
The MTTF for the module might be different from these values, because of the influence of ambient and clamshell conditions.
Note 3: The life-time becomes short if the module is operated under the low temperature environment.

8. GENERAL CAUTIONS

Because next figures and sentences are very important, please understand these contents as follows.

⚠CAUTION	This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.

	This figure is a mark that you will get electric shock when you make a mistake to operate.
	This figure is a mark that you will get hurt when you make a mistake to operate.

 **CAUTIONS**

Do not touch an inverter --on which a caution label is stucked-- while the LCD module is working, because of dangerous high voltage.

(1) Caution when taking out the module

① Pick the pouch only, when in taking out the module from the carrier box.

(2) Cautions for handling the module

① As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges.

②

 As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.

③ As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.

④ Do not pull the interface connectors in or out while the LCD module is operating.

⑤ Put the module display side down on a flat horizontal plane.

⑥ Handle connectors and cables with care.

⑦ When the module is operating, do not lose CLK, Hsync, or Vsync signal. If any one or more of these signals is lost, the LCD panel would be damaged.

⑧ Do not put front side (display surface side) of the module on a desk or a table for a long time, because the display may become un-uniformity.

⑨ Don't push or rub the surface of LCD module.
If you do the scratches or the rubbing marks may left on the surface of the module.

⑩ The torque for mounting screw should never exceed 0.451 N·m (4.6kgf·cm)

(3) Cautions for the atmosphere

①Dew drop atmosphere must be avoided.

②Do not store and/or operate the LCD module in high temperature and/or high humidity atmosphere. Storage in an Electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

③This module uses cold cathode fluorescent lamps. Therefore, the life-time of lamps becomes short conspicuously at low temperature.

④Do not operate the LCD module in high magnetic field.

(4) Cautions for the module characteristics

① Do not apply any fixed patterns data signal for a long time to the LCD module. It may cause image sticking. Use screen savers if the display pattern is fixed more than 30 minutes.

② The noise from the inverter circuit may be observed in the luminance control mode. This is neither defects nor malfunctions.

(5) Other cautions

① Do not disassemble and/or reassemble LCD module.

② Do not readjust variable resistors nor switches etc.

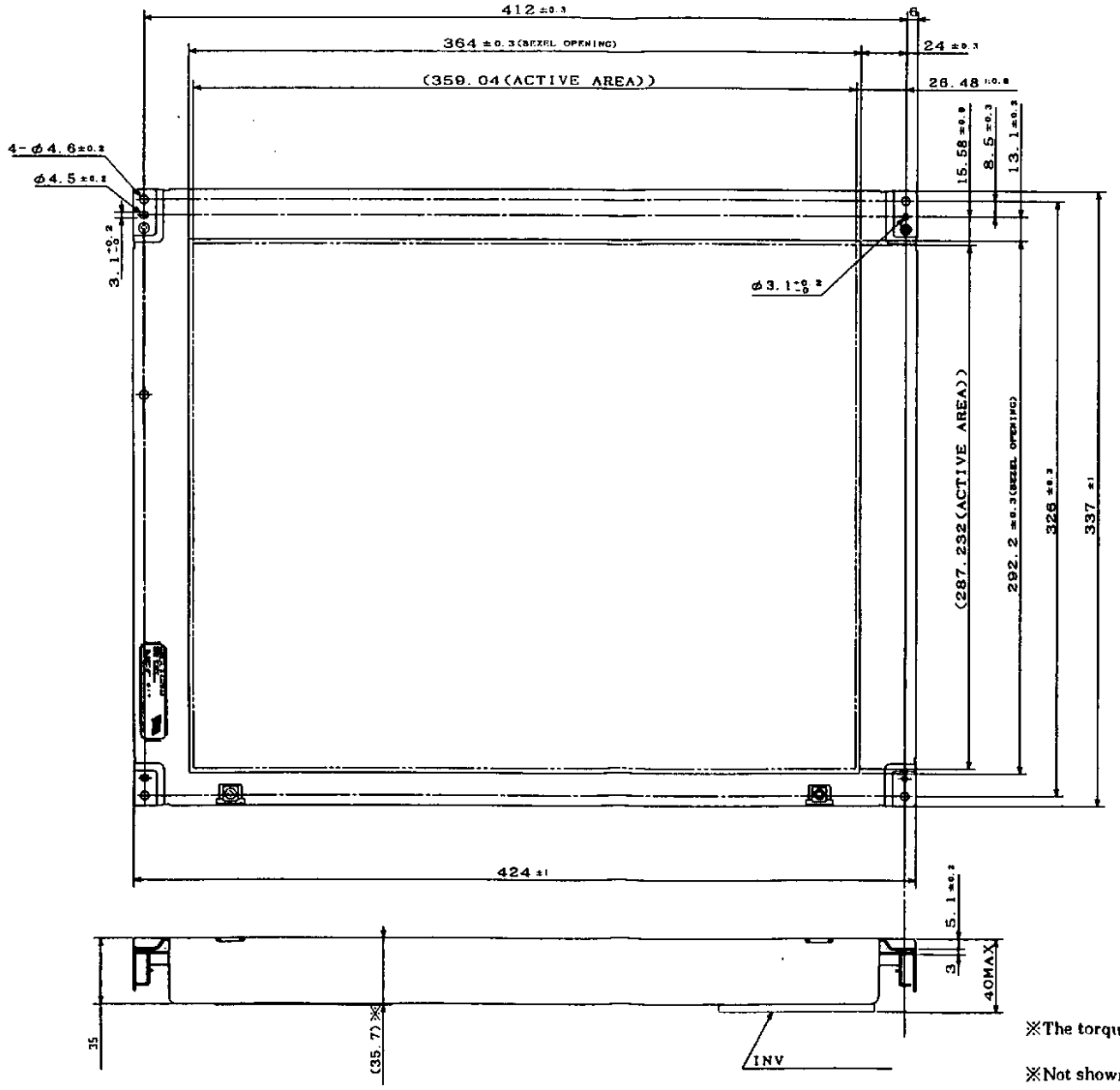
③ When returning the module for repair or etc., pack the module not to be broken. We recommend the original shipping packages.

Liquid Crystal Display has the following specific characteristics. There are not defects nor malfunctions.

The ambient temperature may affect the display condition of LCD module.
The LCD module uses cold cathode tube for backlight. Optical characteristics, like luminance or uniformity, will change during time.

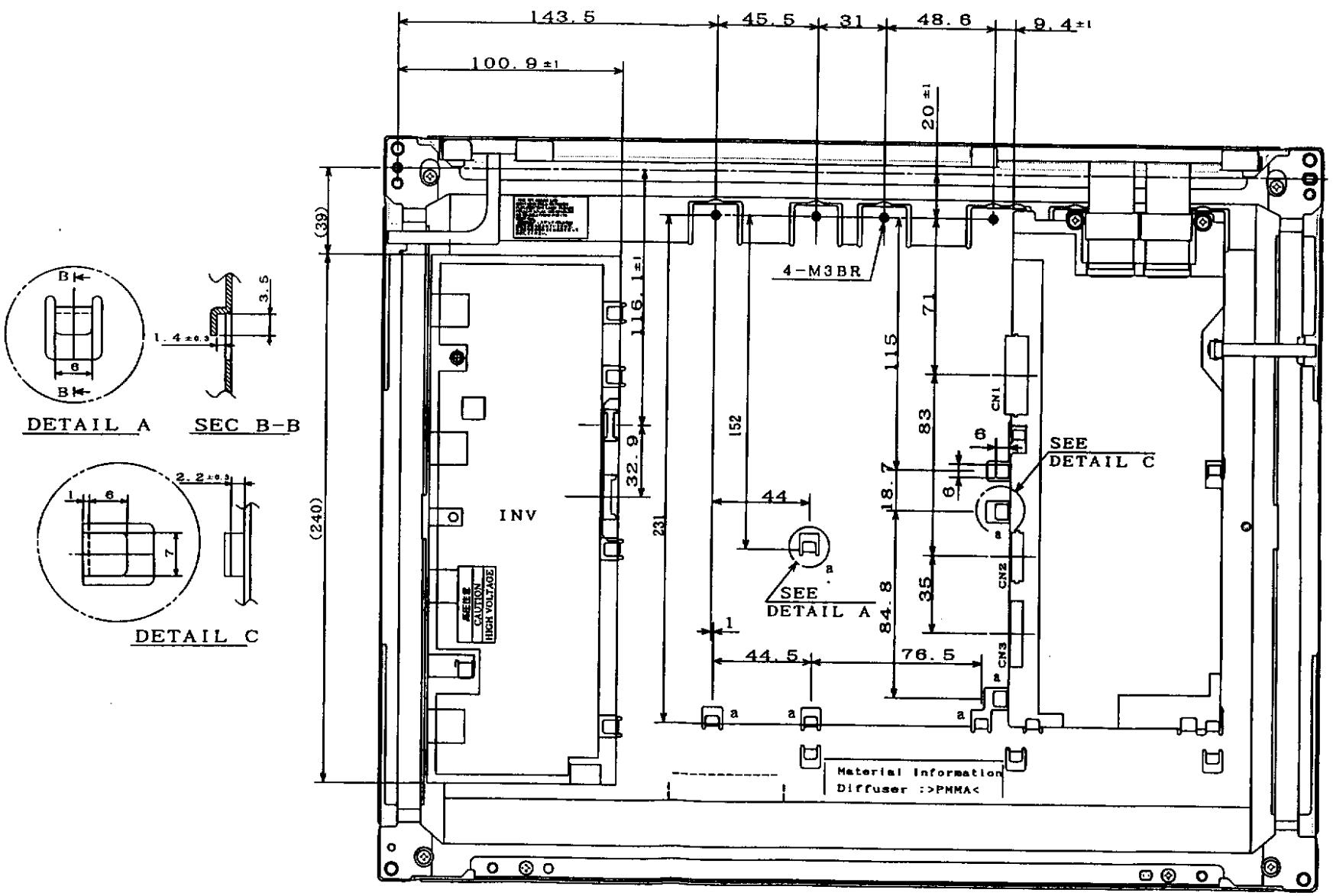
Uneven brightness and/or small spots may be noticed depending on different display patterns.

9.OUTLINE DRAWINGS
9.1 FRONT VIEW



※The torque for mounting screws should never exceed 0.451 N·m (4.6kgf·cm).
※Not shown tolerance of the dimensions are ±0.5 mm.

9.2 REAR VIEW


143.5
45.5
31
48.6
9.4±1
100.9±1
20±1
(39)
(240)
4-M3BR
116.1±1
32.9
152
115
71
83
231
CN1
CN2
CN3
6
18.7
8
44
35
84.8
1
44.5
76.5
SEE
DETAIL C
SEE
DETAIL A
INV
CAUTION
HIGH VOLTAGE
Material Information
Diffuser :>PMMA<
B
B
6
1.4±0.3
3.5
DETAIL A
SEC B-B
1
6
2.2±0.3
7
DETAIL C

Revision History

Rev.	Prepared Date	Revision contents	Approved	Checked	Prepared	Issued date
1	July 8, 1999	DOD-H-7269(abstract)	H. Tachimoto	T. Kusanagi	Y. Okuda	-
2	Oct. 4, 1999	DOD-H-7451 P5,7 Weight 2150g →2200g (typ.) P7 Operating temp 50 → 55℃ Humidity 85% → 66.6% P19 CLK delay P29 Note 1 is added. P39 High temperature/humidity operation 50℃, RH=85%→ 60℃, RH=55%	H. Tachimoto	T. Kusanagi	Y. Okuda	-
3	March 30, 2000	DOD-H-7818 P4,5 Backlight unit: 181LHS02 → 181LHS03 P5 ·Module size: 39.3 (D) → 38.5 (D) ·Weight: 2200 → 2000 ·Contrast ratio: 150 → 300 ·Inverter: 181PW021 → 181PW031 ·Power consumption: 50.4 → 40.8 P5,37 Response time: 45 → 40 P6 ·Note1:GND=FG → GNDF≠FG GNDB≠FG P7 ·Weight: 2250 → 2100 ·Humidity: 66.6%(40<Ta≦55) → 85%(40<Ta≦50) 70%(50<Ta≦55) P8 Supply current IDDB: (3200) → 2550 IDD : (1000) → 850 P9 Power supply sequence: "0<" is deleted. P10 (11) Fuse is added. P36 Pixels are corrected. D(0,1), D(0,2) …→ D(1,0), D(2,0)… D(0,X), D(1,X)…→ D(0,Y), D(1,Y)… P37 Contrast ratio: 100, 150 → 200, 300 Chromaticity Coordinates W: (0.305, 0.311) → (0.302,0.312) R: (0.609, 0.339) → (0.618,0.339) G: (0.319, 0.598) → (0.311,0.584) B: (0.146, 0.094) → (0.143,0.095) LCD surface tmp. is added. P39 ·RH:55→ 60% ·Vibration is corrected. : 19.6 → 11.76m/s^2 ·Expected value: 50000h → 45000h ·Notes are added.	H. Tachimoto	T. Kusanagi	Y. Okuda	