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S1D13504 Color Graphics LCD/CRT Controller

Hardware Functional Specification

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1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13504 Series Color Graphics LCD/CRT Controller Chip. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

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1.2 Overview Description

The S1D13504 is a low cost, low power color/monochrome LCD/CRT controller interfacing to a wide range of CPUs and LCDs. The S1D13504 architecture is designed to meet the requirements of embedded markets such as Office Automation equipment, Mobile Communications devices and Hand-Held PCs where Windows CE may serve as a primary operating system.

The S1D13504 supports LCD interfaces with data widths up to 16 bits. Using Frame Rate Modulation (FRM), it can display 16 shades of gray on monochrome LCD panels, up to 4096 colors on passive color LCDs, and 64K colors on active matrix TFT LCD panels. CRT support is handled through the use of an external RAMDAC interface allowing simultaneous display of both the CRT and LCD panel. A 16-bit memory interface supports up to 2M bytes of FPM-DRAM or EDO-DRAM. Flexible operating voltages from 2.7V to 5.5V provide for very low power consumption.

2 Features

2.1 Memory Interface

- 16-bit DRAM interface:
  - EDO-DRAM up to 40MHz data rate (80M bytes per second).
  - FPM-DRAM up to 25MHz data rate (50M bytes per second).
- Memory size options:
  - 512K bytes using one 256K×16 device.
  - 2M bytes using one 1M×16 device.
- A configuration register can be programmed to enhance performance by tailoring the memory control output timing to the DRAM device.

2.2 CPU Interface

- Supports the following interfaces:
  - 8/16-bit Hitachi SH-3 bus interface.
  - 16-bit interface to 16/32-bit Motorola MC68K microprocessors/microcontrollers.
  - Philips MIPS PR31500 / PR31700.
  - NEC MIPS VR4102.
  - 8/16-bit generic interface bus.
- One-Stage write buffer for minimum wait-state CPU writes.
- Registers are memory-mapped; M/R# pin selects between memory and register address space.
- The complete 2M byte display buffer address space is directly and contiguously available through the 21-bit address bus.

2.3 Display Support

- 4/8-bit monochrome or 4/8/16-bit color passive LCD interface for single-panel, single-drive displays.
- 8-bit monochrome or 8/16-bit color passive LCD interface for dual-panel, dual-drive displays.
- Direct support for 9/12-bit TFT, 18/24-bit TFT are supported up to 64K color depth (16-bit data).
- External RAMDAC support using the upper byte of the LCD data bus for the RAMDAC pixel data bus.
- Simultaneous display of CRT and 4/8-bit passive panel or 9-bit TFT panel:
  - Normal mode for cases where LCD and CRT image sizes are identical.
  - Line-Doubling mode for simultaneous display of 240-line images on 240-line LCD and 480-line CRT.
  - Even-Scan and interlace modes for simultaneous display of 480-line images on 240-line LCD and 480-line CRT.

2.4 Display Modes

- 1/2/4/8/16 bit-per-pixel modes supported on LCD.
- 1/2/4/8 bit-per-pixel modes supported on CRT.
- Up to 16 shades of gray by FRM on monochrome passive LCD panels; a 16x4 Look-Up Table is used to map 1/2/4 bit-per-pixel modes into these shades.
- Up to 4096 colors on color passive LCD panels; three 16x4 Look-Up Tables are used to map 1/2/4/8 bit-per-pixel modes into these colors, 16 bit-per-pixel mode is mapped directly using the 4 most significant bits of the red, green and blue colors.
- Up to 64K colors in 16 bit-per-pixel mode on TFT panels.
- Split screen mode – allows two different images to be simultaneously displayed.
- Virtual display mode – displays images larger than the panel size through the use of panning and scrolling.
- Double buffering / multi-pages – for smooth animation and instantaneous screen update.
- Fast-Update feature – accelerates screen update by allocating full display buffer bandwidth to CPU (see REG[23h] bit 7).

2.5 Clock Source

- Single clock input for both pixel and memory clocks.
- Memory clock can be input clock or (input clock)/2 – this provides flexibility to use CPU bus clock as input clock.
- Pixel clock can be memory clock, (memory clock)/2, (memory clock)/3 or (memory clock)/4.

2.6 Miscellaneous

- The memory data bus MD[15:0], is used to configure the chip at power-on.
- Up to 12 General Purpose Input/Output pins are available:
  - GPIO0 is always available.
  - GPIO[3:1] are available if upper Memory Address pins are not required for DRAM support.
  - GPIO[11:4] are available if there is no external RAMDAC.
- Suspend power save mode is initiated by hardware or software.
- The SUSPEND# pin is used either as an input to initiate Suspend mode, or as a General Purpose Output that can be used to control the LCD backlight – its power-on polarity is selected by an MD configuration pin.

2.7 Package and Pin

Table 2-1: S1D13504 Series Package list

Name	Package	Pin
S1D13504F00A	QFP15	128
S1D13504F01A	TQFP15	128
S1D13504F02A	QFP20	144

3 Typical System Implementation Diagrams

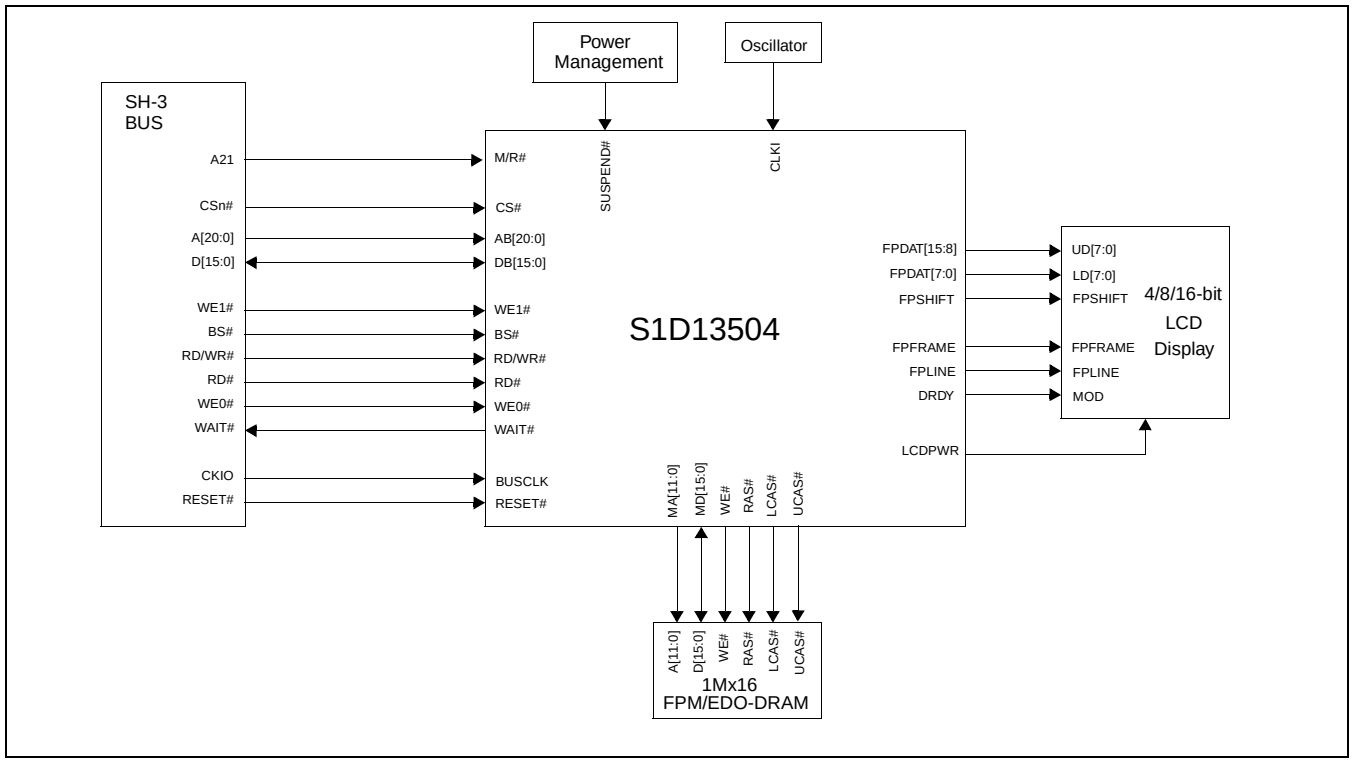


Figure 3-1: Typical System Diagram – SH-3 Bus, 1Mx16 FPM/EDO-DRAM

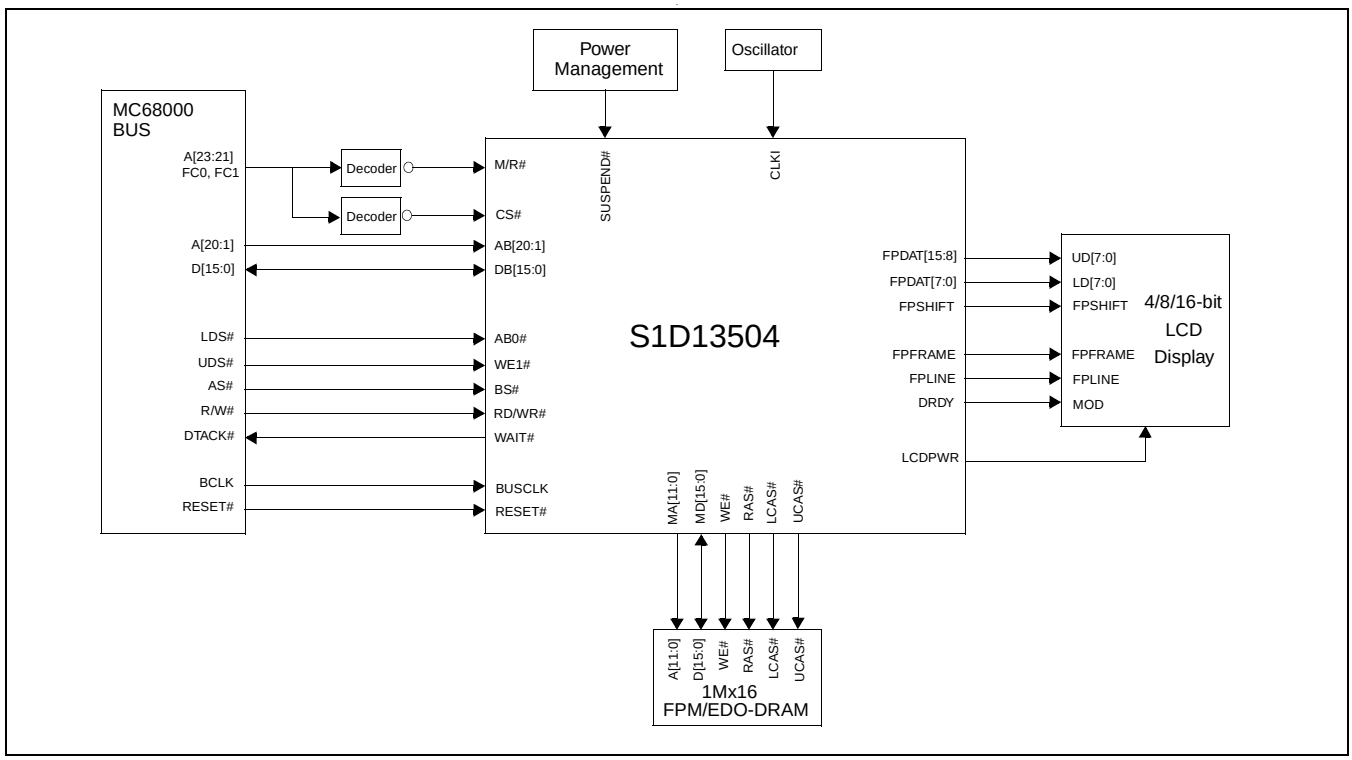


Figure 3-2: Typical System Diagram – MC68K Bus 1, 1Mx16 FPM/EDO-DRAM (16-Bit MC68000)

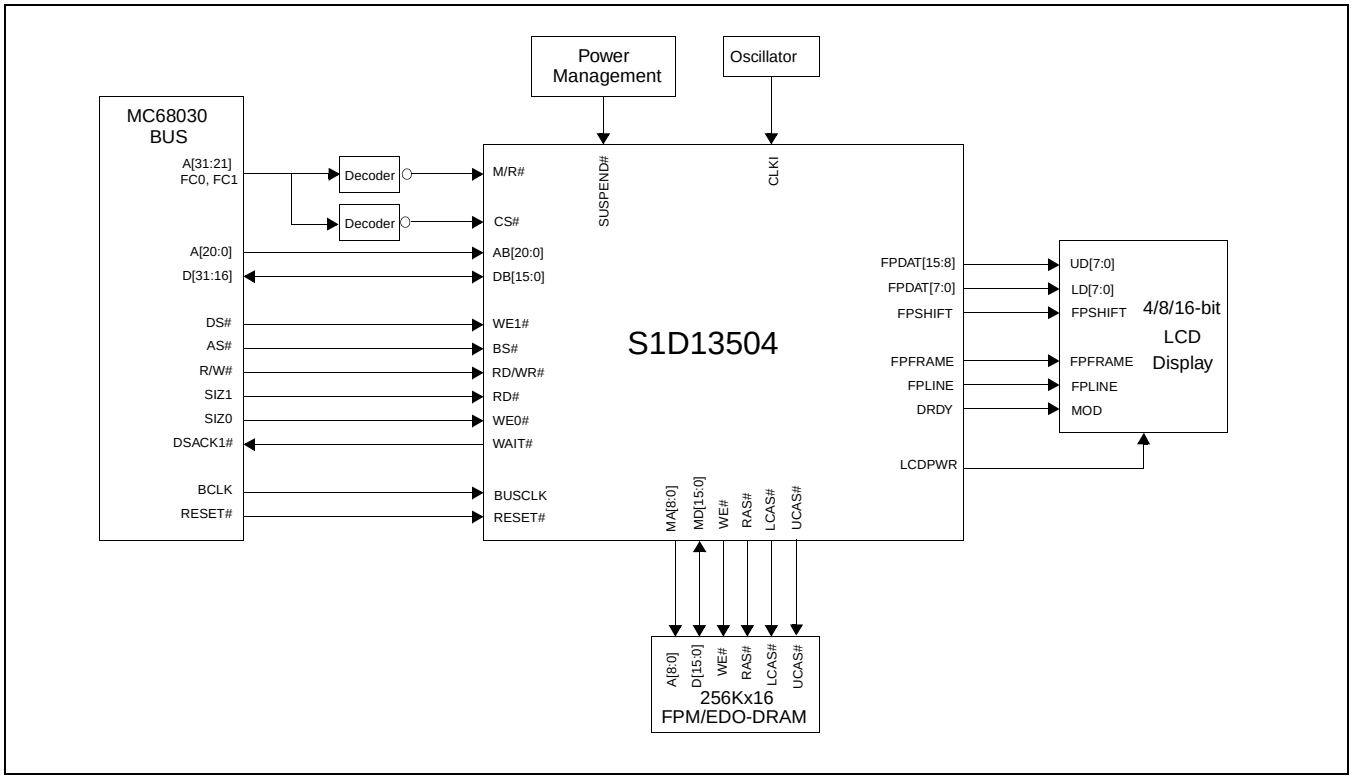


Figure 3-3: Typical System Diagram – MC68K Bus 2, 256Kx16 FPM/EDO-DRAM (32-Bit MC68030)

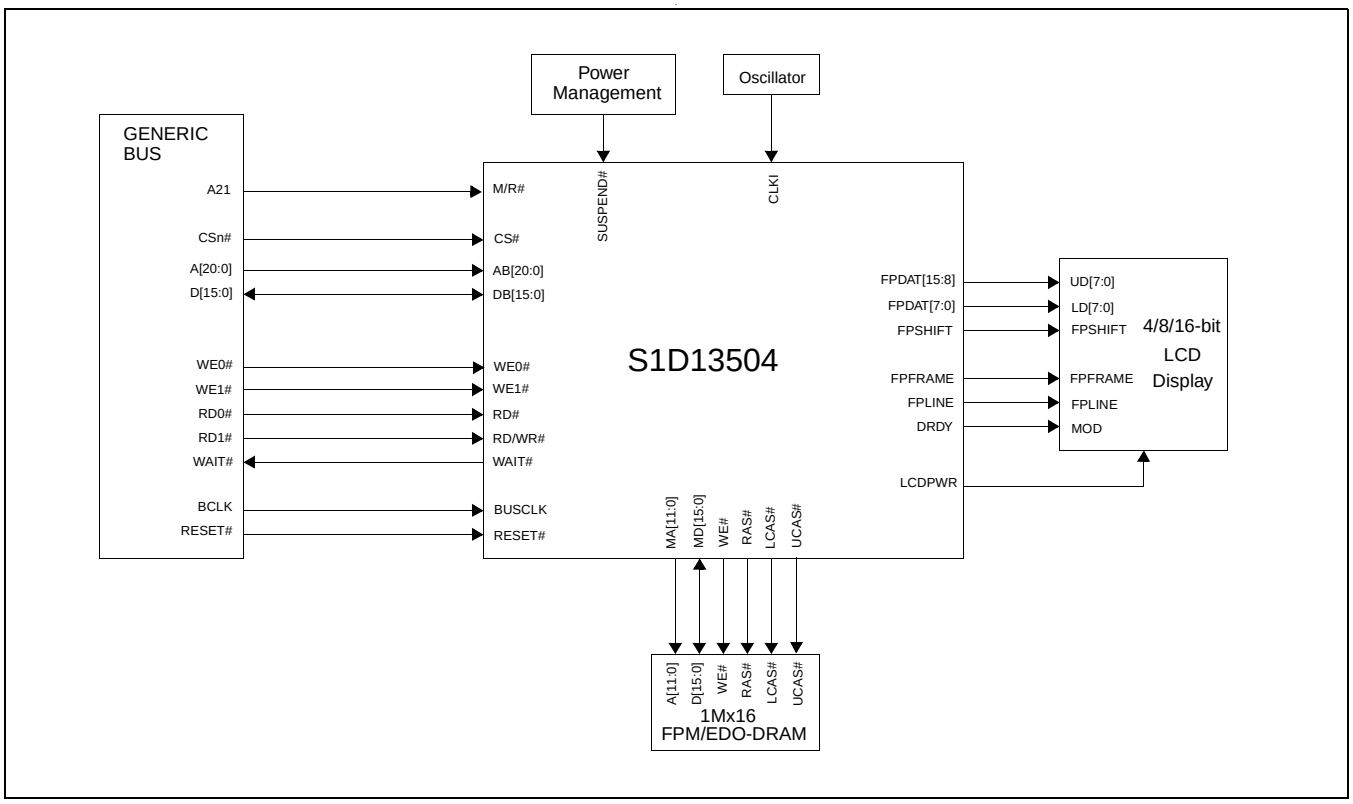


Figure 3-4: Typical System Diagram – Generic Bus, 1Mx16 FPM/EDO-DRAM

4 Block Description

4.1 Functional Block Diagram

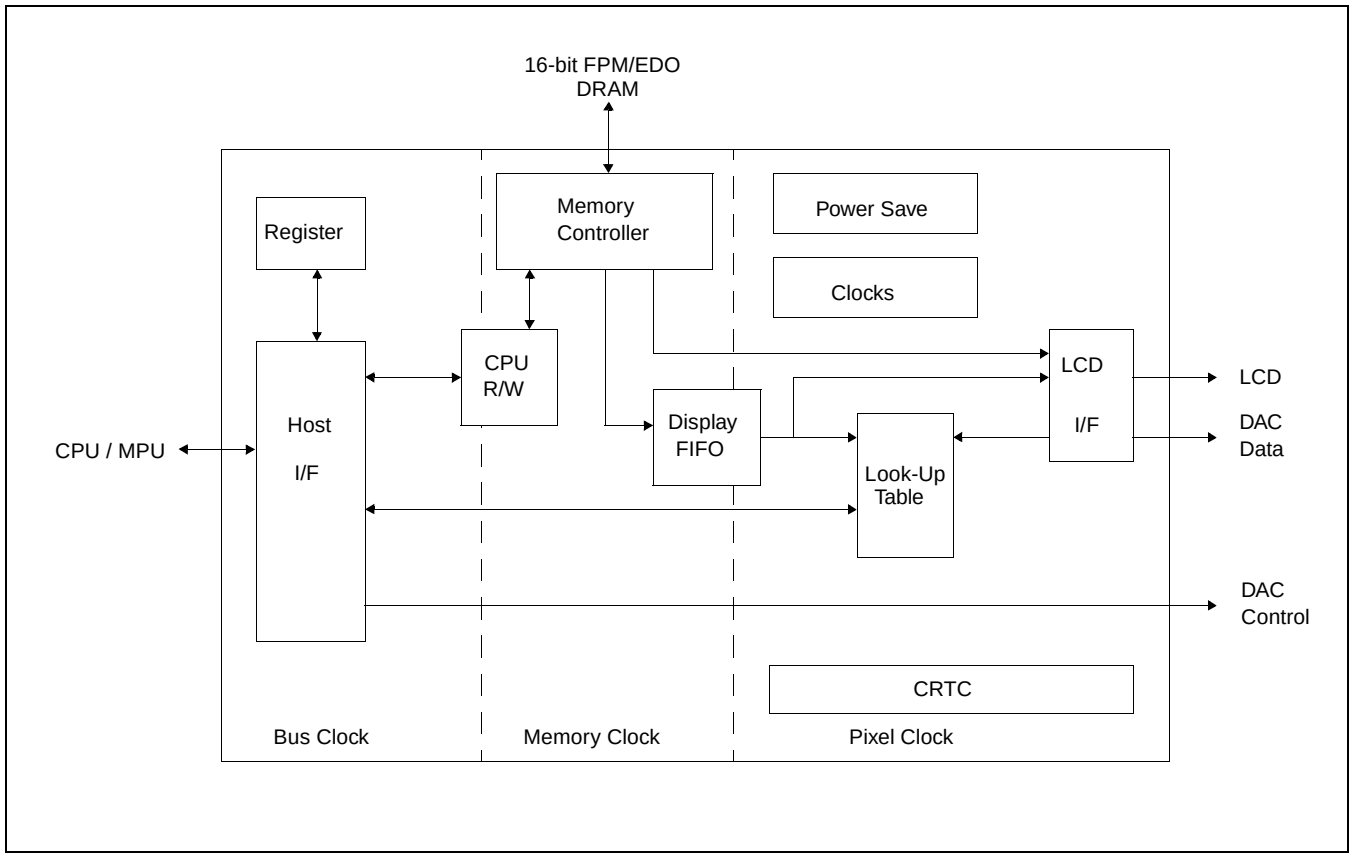


Figure 4-1: System Block Diagram Showing Datapaths

4.2 Functional Block Descriptions

4.2.1 Host Interface

The Host Interface block provides the means for the CPU/MPU to communicate with the display buffer and internal registers, via one of the supported bus interfaces.

4.2.2 Memory Controller

The Memory Controller block arbitrates between CPU accesses and display refresh accesses as well as generates the necessary signals to interface to one of the supported 16-bit memory devices (FPM-DRAM or EDO-DRAM).

4.2.3 Display FIFO

The Display FIFO block fetches display data from the Memory Controller for display refresh.

4.2.4 Look-Up Table

The Look-Up Table block contains three 16x4 Look-Up Tables, one for each primary color. In monochrome mode only one of these Look-Up Tables is selected and used.

4.2.5 LCD Interface

The LCD Interface block performs frame rate modulation for passive LCD panels. It also generates the correct data format and timing control signals for various LCD and TFT panels.

4.2.6 Power Save

The Power Save block contains the power save mode circuitry.

5 Pin Out

5.1 Pinout Diagram for S1D13504F00A

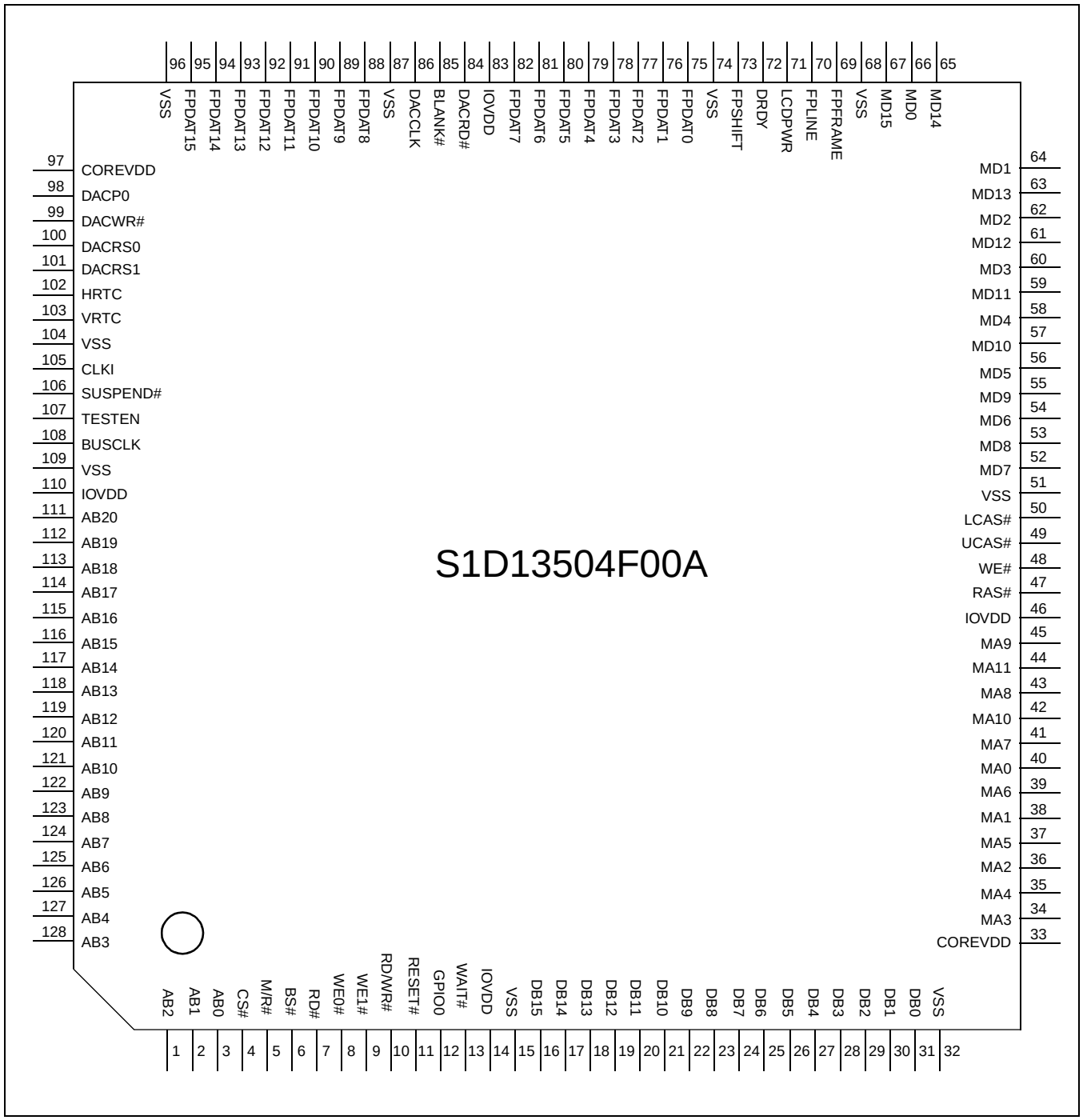


Figure 5-1: Pinout Diagram of F00A

Package type: 128 pin surface mount QFP15

5.2 Pinout Diagram for S1D13504F01A

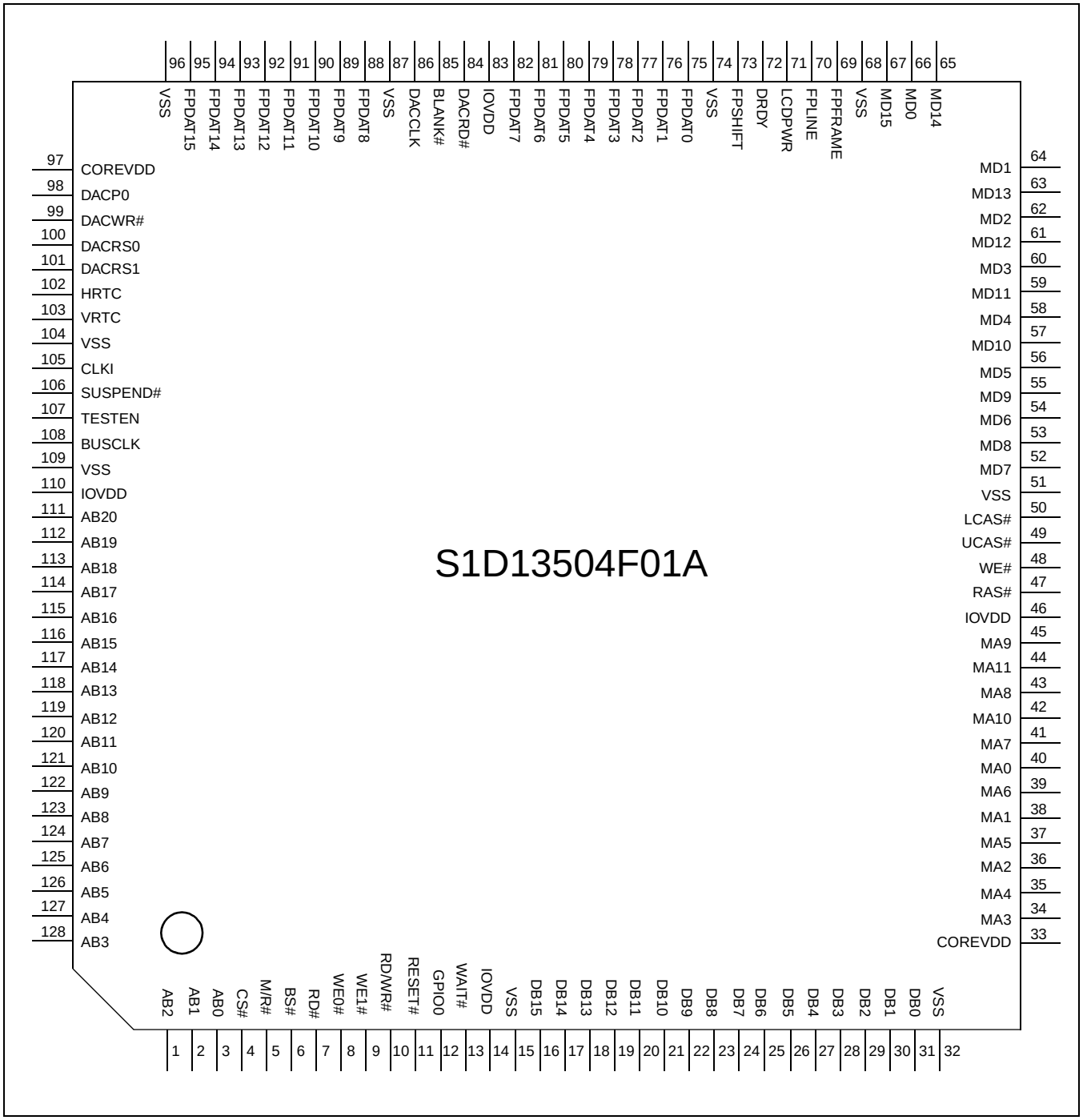


Figure 5-2: Pinout Diagram of F01A

Package type: 128 pin surface mount TQFP15

5.3 Pinout Diagram for S1D13504F02A

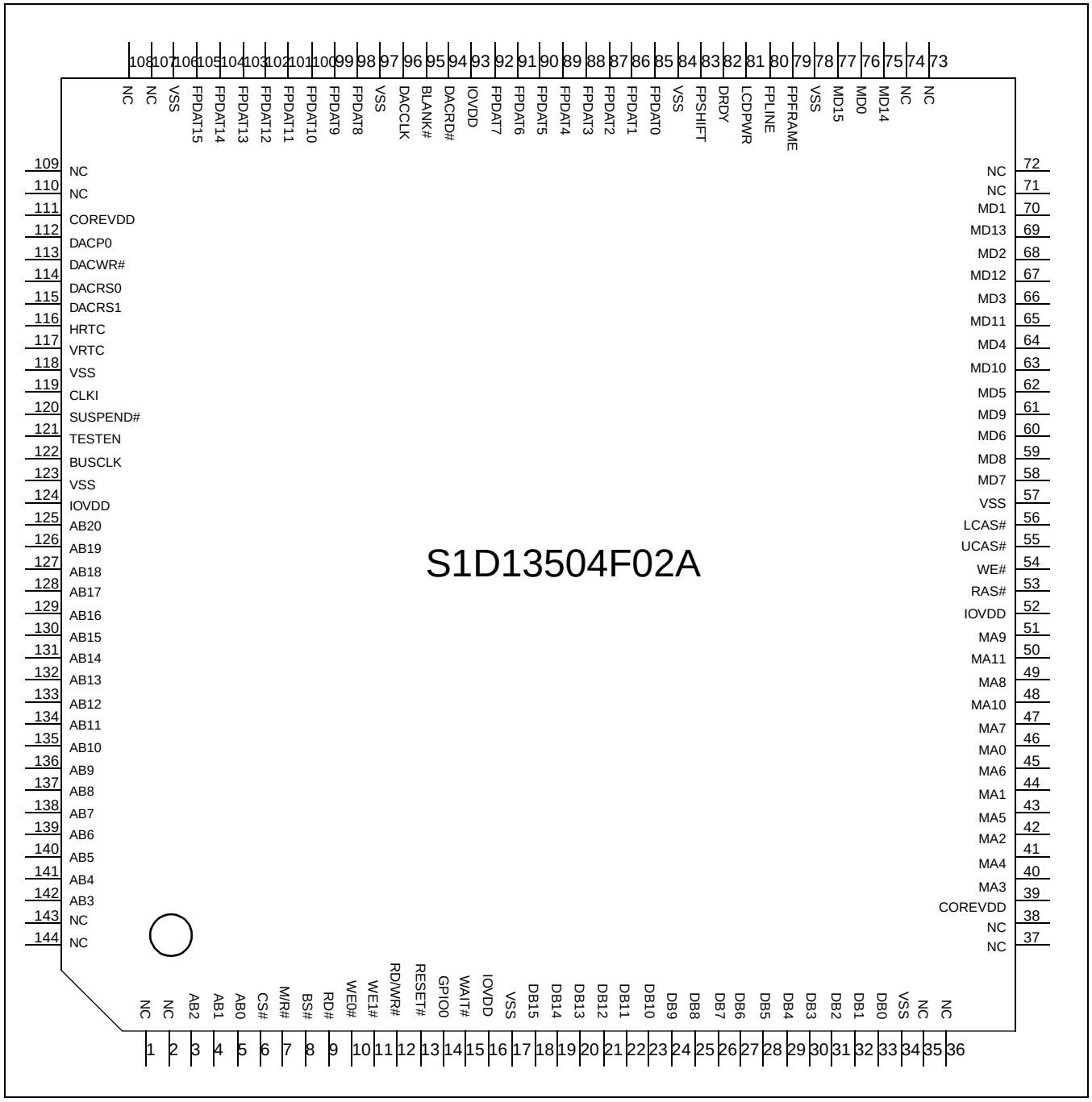


Figure 5-3: Pinout Diagram of F02A

Package type: 144 pin surface mount QFP20

5.4 Pin Description

Key:

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin
C	=	CMOS level input
CD	=	CMOS level input with pull-down resistor (typical values of 100KΩ/180KΩ at 5V/3.3V respectively)
CS	=	CMOS level Schmitt input
COx	=	CMOS output driver, x denotes driver type (1=3/-1.5mA, 2=6/-3mA, 3=12/-6mA)
TSx	=	Tri-state CMOS output driver, x denotes driver type (1=3/-1.5mA, 2=6/-3mA, 3=12/-6mA)
TSxD	=	Tri-state CMOS output driver with pull-down resistor (typical values of 100KΩ/180KΩ at 5V/3.3V respectively), x denotes driver type (1=3/-1.5mA, 2=6/-3mA, 3=12/-6mA)
CNx	=	CMOS low-noise output driver, x denotes driver type (1=3/-1.5mA, 2=6/-3mA, 3=12/-6mA)

5.4.1 Host Interface

Table 5-1: Host Interface Pin Descriptions

Pin Name	Type	Pin #		Driver	Reset = 0 Value	Description
		F00A F01A	F02A			
AB0	I	3	5	CS	Hi-Z	This pin has multiple functions. • For SH-3 mode, this pin inputs system address bit 0 (A0). • For MC68K Bus 1, this pin inputs the lower data strobe (LDS#). • For MC68K Bus 2, this pin inputs system address bit 0 (A0). • For Generic Bus, this pin inputs system address bit 0 (A0). See Table 5-9: “Host Bus Interface Pin Mapping,” on page 31 for summary.
AB[20:1]	I	111-128 1, 2	125-142 3,4	C	Hi-Z	System address bus bits [20:1].
DB[15:0]	IO	16-31	18-33	C/TS2	Hi-Z	System data bus. Unused data pins should be connected to IO V_{DD}. • For SH-3 mode, these pins are connected to D[15:0]. • For MC68K Bus 1, these pins are connected to D[15:0]. • For MC68K Bus 2, these pins are connected to D[31:16] for 32-bit devices (e.g. MC68030) or D[15:0] for 16-bit devices (e.g. MC68340). • For Generic Bus, these pins are connected to D[15:0]. See Table 5-9: “Host Bus Interface Pin Mapping,” on page 31 for summary.

Table 5-1: Host Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #		Driver	Reset = 0 Value	Description
		F00A F01A	F02A			
WE1#	I	9	11	CS	Hi-Z	This pin has multiple functions. • For SH-3 mode, this pin inputs the write enable signal for the upper data byte (WE1#). • For MC68K Bus 1, this pin inputs the upper data strobe (UDS#). • For MC68K Bus 2, this pin inputs the data strobe (DS#). • For Generic Bus, this pin inputs the write enable signal for the upper data byte (WE1#). See Table 5-9: "Host Bus Interface Pin Mapping," on page 31.
M/R#	I	5	7	C	Hi-Z	This input pin is used to select between the memory and register address spaces of the S1D13504. M/R# is set high to access the memory and low to access the registers. See Section 8.1, *"Register Mapping"* on page 89. See Table 5-9: "Host Bus Interface Pin Mapping," on page 31.
CS#	I	4	6	C	Hi-Z	Chip select input. See Table 5-9: "Host Bus Interface Pin Mapping," on page 31.
BUSCLK	I	108	122	C	Hi-Z	System bus clock. See Table 5-9: "Host Bus Interface Pin Mapping," on page 31.
BS#	I	6	8	CS	Hi-Z	This pin has multiple functions. • For SH-3 mode, this pin inputs the bus start signal (BS#). • For MC68K Bus 1, this pin inputs the address strobe (AS#). • For MC68K Bus 2, this pin inputs the address strobe (AS#). • For Generic Bus, this pin must be tied to IO V_{DD}. See Table 5-9: "Host Bus Interface Pin Mapping," on page 31.
RD/WR#	I	10	12	CS	Hi-Z	This pin has multiple functions. • For SH-3 mode, this pin inputs the RD/WR# signal. The S1D13504 needs this signal for early decode of the bus cycle. • For MC68K Bus 1, this pin inputs the R/W# signal. • For MC68K Bus 2, this pin inputs the R/W# signal. • For Generic Bus, this pin inputs the read command for the upper data byte (RD1#). See Table 5-9: "Host Bus Interface Pin Mapping," on page 31.
RD#	I	7	9	CS	Hi-Z	This pin has multiple functions. • For SH-3 mode, this pin inputs the read signal (RD#). • For MC68K Bus 1, this pin must be tied to IO V_{DD}. • For MC68K Bus 2, this pin inputs the bus size bit 1 (SIZ1). • For Generic Bus, this pin inputs the read command for the lower data byte (RD0#). See Table 5-9: "Host Bus Interface Pin Mapping," on page 31.

Table 5-1: Host Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #		Driver	Reset = 0 Value	Description
		F00A F01A	F02A			
WE0#	I	8	10	CS	Hi-Z	This pin has multiple functions. • For SH-3 mode, this pin inputs the write enable signal for the lower data byte (WE0#). • For MC68K Bus 1, this pin must be tied to IO V_{DD}. • For MC68K Bus 2, this pin inputs the bus size bit 0 (SIZ0). • For Generic Bus, this pin inputs the write enable signal for the lower data byte (WE0#). See Table 5-9: "Host Bus Interface Pin Mapping," on page 31.
WAIT#	O	13	15	TS2	Hi-Z	The active polarity of the WAIT# output is configurable on the rising edge of RESET# - see Section 5.5, *"Summary of Configuration Options"* on page 30. This pin has multiple functions. • For SH-3 mode, this pin outputs the wait request signal (WAIT#); MD5 must be pulled low during reset by the internal pull-down resistor. • For MC68K Bus 1, this pin outputs the data transfer acknowledge signal (DTACK#); MD5 must be pulled high during reset by an external pull-up resistor. • For MC68K Bus 2, this pin outputs the data transfer and size acknowledge bit 1 (DSACK1#); MD5 must be pulled high during reset by an external pull-up resistor. • For Generic Bus, this pin outputs the wait signal (WAIT#); MD5 must be pulled low during reset by the internal pull-down resistor. See Table 5-9: "Host Bus Interface Pin Mapping," on page 31.
RESET#	I	11	13	CS	Input 0	Active low input to clear all internal registers and to force all signals to their inactive states.

5.4.2 Memory Interface

Table 5-2: Memory Interface Pin Descriptions

Pin Name	Type	Pin #		Driver	Reset = 0 Value	Description
		F00A F01A	F02A			
LCAS#	O	50	56	CO1	Output 1	This pin has multiple functions. • For dual CAS# DRAM, this is the column address strobe for the lower byte (LCAS#). • For single CAS# DRAM, this is the column address strobe (CAS#). See Table 5-10: “Memory Interface Pin Mapping,” on page 32 for summary.
UCAS#	O	49	55	CO1	Output 1	This pin has multiple functions. • For dual CAS# DRAM, this is the column address strobe for the upper byte (UCAS#). • For single CAS# DRAM, this is the write enable signal for the upper byte (UWE#). See Table 5-10: “Memory Interface Pin Mapping,” on page 32 for summary.
WE#	O	48	54	CO1	Output 1	This pin has multiple functions. • For dual CAS# DRAM, this is the write enable signal (WE#). • For single CAS# DRAM, this is the write enable signal for the lower byte (LWE#). See Table 5-10: “Memory Interface Pin Mapping,” on page 32 for summary.
RAS#	O	47	53	CO1	Output 1	Row address strobe.
MD[15:0]	IO	67, 65, 63, 61, 59, 57, 55, 53, 52, 54, 56, 58, 60, 62, 64, 66	76, 70, 68, 66, 64, 62, 60, 58, 59, 61, 63, 65, 67, 69, 75, 77	CD2/TS1	Hi-Z (pulled 0)	These pins have multiple functions. • Bi-directional memory data bus. • During reset, these pins are inputs and their states at the rising edge of RESET# are used to configure the chip. Internal pull-down resistors (typical values of 100KΩ/100KΩ/120KΩ at 5.0V/3.3V/3.0V respectively) pull the reset states to 0. External pull-up resistors can be used to pull the reset states to 1. See Section 5.5, *“Summary of Configuration Options”* on page 30.

Table 5-2: Memory Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #		Driver	Reset = 0 Value	Description
		F00A F01A	F02A			
MA[8:0]	O	43, 41, 39, 37, 35, 34, 36, 38, 40	46, 44, 42, 40, 41, 43, 45, 47, 49	CO1	Output 0	Multiplexed memory address.
MA9	IO	45	51	C/TS1	Hi-Z / Output 0[1]	This pin has multiple functions. • For 2M byte DRAM, this is memory address bit 9 (MA9). • For asymmetrical 512K byte DRAM, this is memory address bit 9 (MA9). • For symmetrical 512K byte DRAM, this pin can be used as general purpose IO (GPIO3). See Table 5-10: “Memory Interface Pin Mapping,” on page 32 for summary.
MA10	IO	42	48	C/TS1	Hi-Z / Output 0[1]	This pin has multiple functions. • For asymmetrical 2M byte DRAM, this is memory address bit 10 (MA10). • For symmetrical 2M byte DRAM and all 512K byte DRAM, this pin can be used as general purpose IO (GPIO1). See Table 5-10: “Memory Interface Pin Mapping,” on page 32 for summary.
MA11	IO	44	50	C/TS1	Hi-Z / Output 0[1]	This pin has multiple functions. • For asymmetrical 2M byte DRAM, this is memory address bit 11 (MA11). • For symmetrical 2M byte DRAM and all 512K byte DRAM, this pin can be used as general purpose IO (GPIO2). See Table 5-10: “Memory Interface Pin Mapping,” on page 32 for summary.

1 When configured as IO pins.

5.4.3 LCD Interface

Table 5-3: LCD Interface Pin Descriptions

Pin Name	Type	Pin #		Driver	Reset = 0 Value	Description
		F00A F!A	F02A			
FPDAT[8:0]	O	88, 82-75	98, 92-85	CN3	Output 0	Panel Data
FPDAT[15:9]	O	95-89	105-99	CN3	Output 0	These pins have multiple functions. • Panel Data for 16-bit panels. • Pixel Data for external RAMDAC support. See Table 5-11: “LCD, CRT, RAMDAC Interface Pin Mapping,” on page 33.
FPFRAME	O	69	79	CN3	Output 0	Frame Pulse
FPLINE	O	70	80	CN3	Output 0	Line Pulse
FPSHIFT	O	73	83	CN3	Output 0	Shift Clock Pulse
LCDPWR	O	71	81	CO1	Output[1]	LCD power control output. The active polarity of this output is selected by the state of MD10 at the rising edge of RESET# - see Section 5.5, *“Summary of Configuration Options”* on page 30. This output is controlled by the power save mode circuitry - see Section 13, *“Power Save Modes”* on page 127 for details.
DRDY	O	72	82	CN3	Output 0	This pin has multiple functions which are automatically selected depending on panel type used. • For TFT panels, this is the display enable output (DRDY). • For passive LCDs with Format 1 interfaces, this is the 2nd Shift Clock (FPSHIFT2). • For all other LCD panels, this is the LCD backplane bias signal (MOD). See Table 5-11: “LCD, CRT, RAMDAC Interface Pin Mapping,” on page 33 and REG[02h] for details.

1 Output may be 1 or 0.

5.4.4 Clock Input

Table 5-4: Clock Input Pin Description

Pin Name	Type	Pin #		Driver	Reset = 0 Value	Description
		F00A F01A	F02A			
CLKI	I	105	119	C	Hi-Z	Input clock for the internal pixel clock (PCLK) and memory clock (MCLK). PCLK and MCLK are derived from CLKI – see REG[19h] for details.

5.4.5 CRT and External RAMDAC Interface

Table 5-5: CRT and RAMDAC Interface Pin Descriptions

Pin Name	Type	Pin #		Driver	Reset = 0 Value	Description
		F00A F01A	F02A			
DACRD#	IO	84	94	C/TS1	Hi-Z / Output 1[1]	This pin has multiple functions. • Read signal for external RAMDAC support. • General Purpose IO (GPIO4). See Table 5-11: "LCD, CRT, RAMDAC Interface Pin Mapping," on page 33.
DACWR#	IO	99	113	C/TS1	Hi-Z / Output 1[1]	This pin has multiple functions. • Write signal for external RAMDAC support. • General Purpose IO (GPIO7). See Table 5-11: "LCD, CRT, RAMDAC Interface Pin Mapping," on page 33.
DACRS1	IO	101	115	C/TS1	Hi-Z / Output 0[1]	This pin has multiple functions. • Register Select bit 1 for external RAMDAC support. • General Purpose IO (GPIO9). See Table 5-11: "LCD, CRT, RAMDAC Interface Pin Mapping," on page 33.
DACRS0	IO	100	114	C/TS1	Hi-Z / Output 0[1]	This pin has multiple functions. • Register Select bit 0 for external RAMDAC support. • General Purpose IO (GPIO8). See Table 5-11: "LCD, CRT, RAMDAC Interface Pin Mapping," on page 33.
DACP0	IO	98	112	C/CN3	Hi-Z / Output 0[1]	This pin has multiple functions. • Pixel Data bit 0 for external RAMDAC support. • General Purpose IO (GPIO6). See Table 5-11: "LCD, CRT, RAMDAC Interface Pin Mapping," on page 33.

Table 5-5: CRT and RAMDAC Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #		Driver	Reset = 0 Value	Description
		F00A F01A	F02A			
HRTC	IO	102	116	C/CN3	Hi-Z / Output 0[1]	This pin has multiple functions. • Horizontal Retrace signal for CRT. • General Purpose IO (GPIO10). See Table 5-11: “LCD, CRT, RAMDAC Interface Pin Mapping,” on page 33.
VRTC	IO	103	117	C/CN3	Hi-Z / Output 0[1]	This pin has multiple functions. • Vertical Retrace signal for CRT. • General Purpose IO (GPIO11). See Table 5-11: “LCD, CRT, RAMDAC Interface Pin Mapping,” on page 33.
BLANK#	IO	85	95	C/CN3	Hi-Z / Output 0[1]	This pin has multiple functions. • Blanking signal for DAC. • General Purpose IO (GPIO5). See Table 5-11: “LCD, CRT, RAMDAC Interface Pin Mapping,” on page 33.
DACCLK	O	86	96	C/CN3	Output 0	Pixel Clock for RAMDAC.

1 When configured as IO pins

5.4.6 Miscellaneous

Table 5-6: Miscellaneous Pin Descriptions

Pin Name	Type	Pin #		Driver	Reset = 0 Value	Description
		F00A F01A	F02A			
SUSPEND#	IO	106	120	CS/TS1	Hi-Z / Output[1]	This pin has multiple functions. • When MD9 = 0 at rising edge of RESET#, this pin is an active-low input used to place the S1D13504 into suspend mode; see Section 13, *"Power Save Modes"* on page 127 for details. • When MD[10:9] = 01 at rising edge of RESET#, this pin is an output with a reset state of 0. Its state is controlled by REG[21h] bit 7. • When MD[10:9] = 11 at rising edge of RESET#, this pin is an output with a reset state of 1. Its state is controlled by REG[21h] bit 7.
GPIO0	IO	12	14	C/TS1	Hi-Z	General Purpose IO pin 0.
TSTEN	I	107	121	CD	Hi-Z (pulled 0)	Test Enable. This in should be connected to V_{SS} for normal operation.
NC	-	-	1, 2, 35-38, 71-74, 107-110, 143, 144	-	-	No connect

1 When configured as IO pin. Output may be 1 or 0.

5.4.7 Power Supply

Table 5-7: Power Supply Pin Descriptions

Pin Name	Type	Pin #		Driver	Description
		F00A F01A	F02A		
COREVDD	P	33, 97	39, 111	P	Core V_{DD}
IOVDD	P	14, 46, 83, 110	16, 52, 93, 124	P	IO V_{DD}
VSS	P	15, 32, 51, 68, 74, 87, 96, 104, 109	17, 34, 57, 78, 84, 97, 106, 118, 123,	P	Common V_{SS}

5.5 Summary of Configuration Options

Table 5-8: Summary of Power On / Reset Options

Pin Name	value on this pin at rising edge of RESET# is used to configure: (1/0)	
	1	**0**
MD0	8-bit host bus interface	16-bit host bus interface
MD[3:1]	Select host bus interface: 000 = SH-3 bus interface 001 = MC68K bus 1 (e.g. MC68000) 010 = MC68K bus 2 (e.g. MC68030) 011 = Generic bus interface (e.g. Philips MIPS PR31500/PR31700; NEC MIPS VR4102) 1XX = reserved	
MD4	Little Endian	Big Endian
MD5	WAIT# is active high (1 = insert wait state)	WAIT# is active low (0 = insert wait state)
MD[7:6]	Memory Address/GPIO configuration: 00 = symmetrical 256K×16 DRAM. MA[8:0] = DRAM address. MA[11:9] = GPIO[2:1] and GPIO3. 01 = symmetrical 1M×16 DRAM. MA[9:0] = DRAM address. MA[11:10] = GPIO[2:1]. 10 = asymmetrical 256K×16 DRAM. MA[9:0] = DRAM address. MA[11:10] = GPIO[2:1]. 11 = asymmetrical 1M×16 DRAM. MA[11:0] = DRAM address.	
MD8	Configure DACRD#, BLANK#, DACP0, DACWR#, DACRS0, DACRS1, HRTC, VRTC as General Purpose IO (GPIO[11:4]).	Configure DACRD#, BLANK#, DACP0, DACWR#, DACRS0, DACRS1, HRTC, VRTC as DAC and CRT outputs.
MD9	SUSPEND# pin configured as GPO output.	SUSPEND# pin configured as SUSPEND# input.
MD10	Active low LCDPWR or GPO polarities.	Active high LCDPWR or GPO polarities.
MD[15:11]	Not used.	

5.6 Multiple Function Pin Mapping

Table 5-9: Host Bus Interface Pin Mapping

S1D13504 Pin Names	SH-3	MC68K Bus 1	MC68K Bus 2	Generic MPU
AB[20:1]	A[20:1]	A[20:1]	A[20:1]	A[20:1]
AB0	A0	LDS#	A0	A0
DB[15:0]	D[15:0]	D[15:0]	D[31:16]	D[15:0]
WE1#	WE1#	UDS#	DS#	WE1#
M/R#	External Decode	External Decode	External Decode	External Decode
CS#	CSn#	External Decode	External Decode	External Decode
BUSCLK	CKIO	CLK	CLK	BCLK
BS#	BS#	AS#	AS#	Connect to IO V_{DD}
RD/WR#	RD/WR#	R/W#	R/W#	RD1#
RD#	RD#	Connect to IO V_{DD}	SIZ1	RD0#
WE0#	WE0#	Connect to IO V_{DD}	SIZ0	WE0#
WAIT#	WAIT#	DTACK#	DSACK1#	WAIT#
RESET#	RESET#	RESET#	RESET#	RESET#

Table 5-10: Memory Interface Pin Mapping

S1D13504 Pin Names	FPM/EDO-DRAM							
	Sym 256Kx16		Asym 256Kx16		Sym 1Mx16		Asym 1Mx16	
	2-CAS#	2-WE#	2-CAS#	2-WE#	2-CAS#	2-WE#	2-CAS#	2-WE#
MD[15:0]	DQ[15:0]							
MA[8:0]	A[8:0]							
MA9	GPIO3[1]		A9					
MA10	GPIO1[1]						A10	
MA11	GPIO2[1]						A11	
UCAS#	UCAS#	UWE#	UCAS#	UWE#	UCAS#	UWE#	UCAS#	UWE#
LCAS#	LCAS#	CAS#	LCAS#	CAS#	LCAS#	CAS#	LCAS#	CAS#
WE#	WE#	LWE#	WE#	LWE#	WE#	LWE#	WE#	LWE#
RAS#	RAS#							

Note

1. All GPIO pins default to input on reset, and unless programmed otherwise should be connected to either V_{SS} or IO V_{DD} if not used.

Table 5-11: LCD, CRT, RAMDAC Interface Pin Mapping

S1D13504 Pin Names	Monochrome Passive Panel			Color Passive Panel					Color TFT Panel			CRT
	Single		Dual	Single	Single Format 1	Single Format 2	Dual					
	4-bit	8-bit	8-bit	4-bit	8-bit	8-bit	8-bit	16-bit	9-bit	12-bit	18-bit[1]	
FPFRAME	FPFRAME											Note[2]
FPLINE	FPLINE											Note[2]
FPSHIFT	FPSHIFT											Note[2]
DRDY	MOD				FPSHIFT2	MOD			DRDY			Note[2]
FPDAT0	driven 0	D0	LD0	driven 0	D0	D0	LD0	LD0	R2	R3	R5	Note[2]
FPDAT1	driven 0	D1	LD1	driven 0	D1	D1	LD1	LD1	R1	R2	R4	Note[2]
FPDAT2	driven 0	D2	LD2	driven 0	D2	D2	LD2	LD2	R0	R1	R3	Note[2]
FPDAT3	driven 0	D3	LD3	driven 0	D3	D3	LD3	LD3	G2	G3	G5	Note[2]
FPDAT4	D0	D4	UD0	D0	D4	D4	UD0	UD0	G1	G2	G4	Note[2]
FPDAT5	D1	D5	UD1	D1	D5	D5	UD1	UD1	G0	G1	G3	Note[2]
FPDAT6	D2	D6	UD2	D2	D6	D6	UD2	UD2	B2	B3	B5	Note[2]
FPDAT7	D3	D7	UD3	D3	D7	D7	UD3	UD3	B1	B2	B4	Note[2]
FPDAT8	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	LD4	B0	B1	B3	Note[2]
FPDAT9	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	LD5	driven 0	R0	R2	DACP7
FPDAT10	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	LD6	driven 0	driven 0	R1	DACP6
FPDAT11	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	LD7	driven 0	G0	G2	DACP5
FPDAT12	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	UD4	driven 0	driven 0	G1	DACP4
FPDAT13	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	UD5	driven 0	driven 0	G0	DACP3
FPDAT14	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	UD6	driven 0	B0	B2	DACP2
FPDAT15	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	UD7	driven 0	driven 0	B1	DACP1
DACRD#	GPIO4[3]											DACRD#
BLANK#	GPIO5[3]											BLANK#
DACP0	GPIO6[3]											DACP0
DACWR#	GPIO7[3]											DACWR#
DACRS0	GPIO8[3]											DACRS0
DACRS1	GPIO9[3]											DACRS1
HRTC	GPIO10[3]											HRTC
VRTC	GPIO11[3]											VRTC
DACCLK	driven 0											DACCLK

Note

1. Although 18-bit TFT panels are supported only 16 data bits (64K colors) are available - R0 and B0 are not used.
2. If no LCD is active these pins are driven low.
3. All GPIO pins default to input on reset, and unless programmed otherwise should be connected to either V_{SS} or IO V_{DD} if not used.

6 D.C. Characteristics

Table 6-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
Core V_{DD}	Supply Voltage	V_{SS} - 0.3 to 4.6	V
IO V_{DD}	Supply Voltage	V_{SS} - 0.3 to 6.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3 to IO V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 to IO V_{DD} + 0.5	V
T_{STG}	Storage Temperature	-65 to 150	° C
T_{SOL}	Solder Temperature/Time	260 for 10 sec. max at lead	° C

Table 6-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Core V_{DD}	Supply Voltage	V_{SS} = 0 V	2.7	3.0/3.3	3.6	V
IO V_{DD}	Supply Voltage	V_{SS} = 0 V	2.7	3.0/3.3/5.0	5.5	V
V_{IN}	Input Voltage		V_{SS}		IO V_{DD}	V
T_{OPR}	Operating Temperature		-40	25	85	° C

Table 6-3: Input Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage CMOS inputs	IO V_{DD} = 3.0 3.3 5.0			0.8 0.8 1.0	V V V
V_{IH}	High Level Input Voltage CMOS inputs	IO V_{DD} = 3.0 3.3 5.0	1.9 2.0 3.5			V V V
V_{T+}	Positive-Going Threshold CMOS Schmitt inputs	IO V_{DD} = 3.0 3.3 5.0	1.0 1.1 2.0		2.3 2.4 4.0	V V V
V_{T-}	Negative-Going Threshold CMOS Schmitt inputs	IO V_{DD} = 3.0 3.3 5.0	0.5 0.6 0.8		1.7 1.8 3.1	V V V
I_{IZ}	Input Leakage Current	V_{DD} = Max V_{IH} = IO V_{DD} V_{IL} = V_{SS}	-1		1	µA
C_{IN}	Input Pin Capacitance				10	pF
HR_{PD}	Pull-down Resistance	V_{IN} = V_{DD} = 3.0 = 3.3 = 5.0	60 50 50	120 100 100	300 300 300	kΩ kΩ kΩ

Table 6-4: Output Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Low Level Output Voltage Type 1 - TS1, CO1, TS1D Type 2 - TS2, CO2 Type 3 - TS3, CO3	 I_{OL} = 3mA I_{OL} = 6mA I_{OL} = 12mA			0.4	V
V_{OH}	High Level Output Voltage Type 1 - TS1, CO1, TS1D Type 2 - TS2, CO2 Type 3 - TS3, CO3	 I_{OL} = -1.5 mA I_{OL} = -3 mA I_{OL} = -6 mA	IO V_{DD} - 0.4			V
I_{OZ}	Output Leakage Current	IO V_{DD} = Max $V_{OH} = V_{DD}$ $V_{OL} = V_{SS}$	-1		1	µA
C_{OUT}	Output Pin Capacitance				10	pF
C_{BID}	Bidirectional Pin Capacitance				10	pF

7 A.C. Characteristics

Conditions: IO V_{DD} = 2.7V to 5.5V unless otherwise specified
T_A = -40° C to 85° C
T_{rise} and T_{fall} for all inputs must be ≤ 5 nsec (10% ~ 90%)
C_L = 50pF (Bus / MPU Interface)
C_L = 100pF (LCD Panel Interface)
C_L = 10pF (Display Buffer Interface)
C_L = 10pF (CRT / DAC Interface)

7.1 CPU Interface Timing

7.1.1 SH-3 Interface Timing

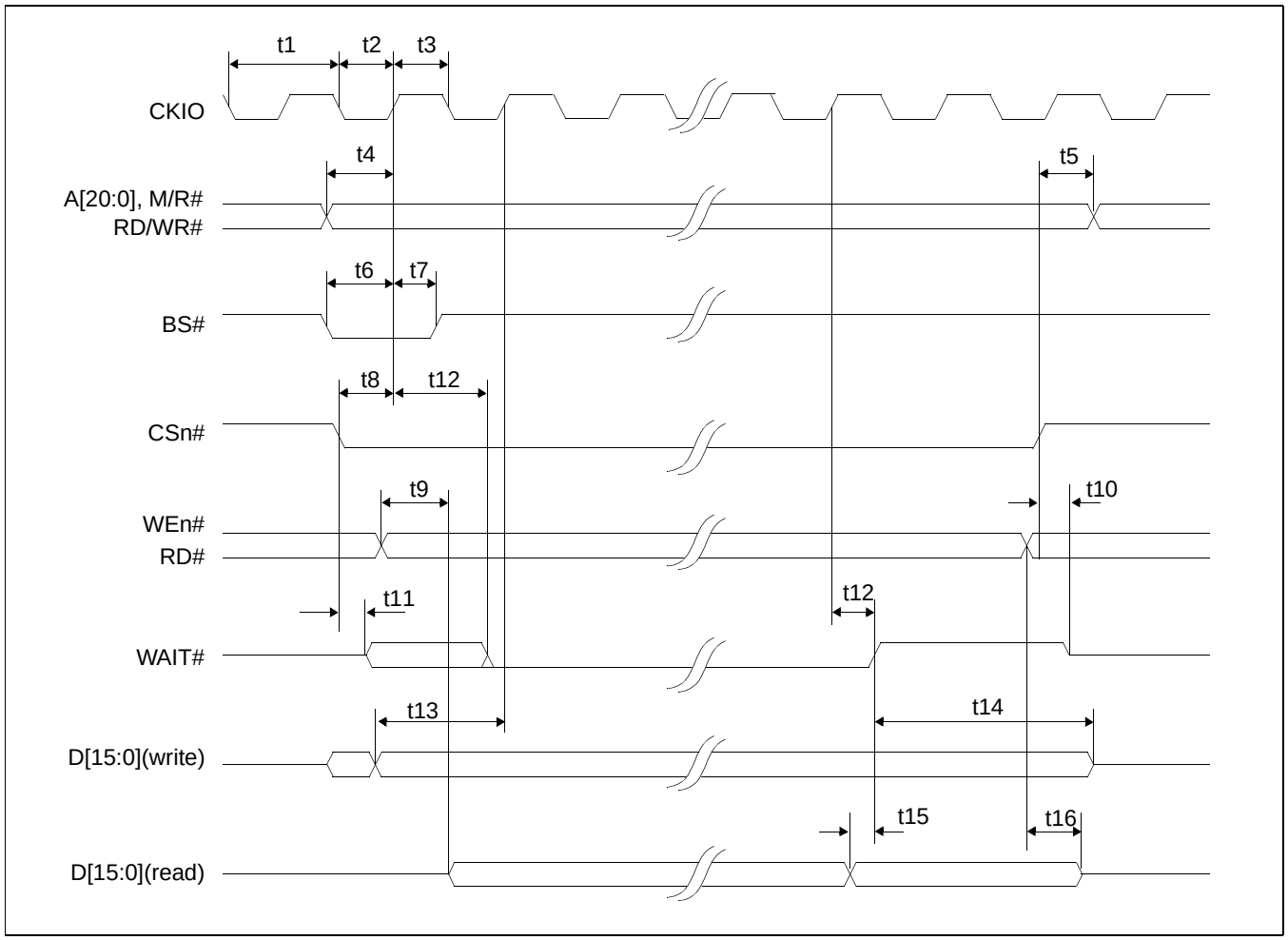


Figure 7-1: SH-3 Interface Timing

Note

The SH-3 Wait State Control Register for the area in which the S1D13504 resides must be set to a non-zero value.

Table 7-1: SH-3 Interface Timing

Symbol	Parameter	Min	Max	Units
t1	Clock period	25		ns
t2	Clock pulse width high	5		ns
t3	Clock pulse width low	5		ns
t4	A[20:0], M/R#, RD/WR# setup to CKIO	4		ns
t5	A[20:0], M/R#, RD/WR# hold from CS#	0		ns
t6	BS# setup	3		ns
t7	BS# hold	0		ns
t8	CSn# setup	0		ns
t9[2]	Falling edge RD# to D[15:0] driven	3		ns
t10	Rising edge CSn# to WAIT# tri-state	0	4	ns
t11[1]	Falling edge CSn# to WAIT# driven	1	11	ns
t12	CKIO to WAIT# delay	3	15	ns
t13	D[15:0] setup to first CKIO after BS# (write cycle)	0		ns
t14	D[15:0] hold (write cycle)	0		ns
t15	D[15:0] valid to WAIT# rising edge (read cycle)	0		ns
t16	Rising edge RD# to D[15:0] tri-state (read cycle)	2	9	ns

1. If the S1D13504 host interface is disabled, the timing for WAIT# driven is relative to the falling edge of CSn# or the first positive edge of CKIO after A[20:0] and M/R# become valid, whichever occurs later.

2. If the S1D13504 host interface is disabled, the timing for D[15:0] driven is relative to the falling edge of RD# or the first positive edge of CKIO after A[20:0] and M/R# become valid, whichever occurs later.

7.1.2 MC68K Bus 1 Interface Timing (e.g. MC68000)

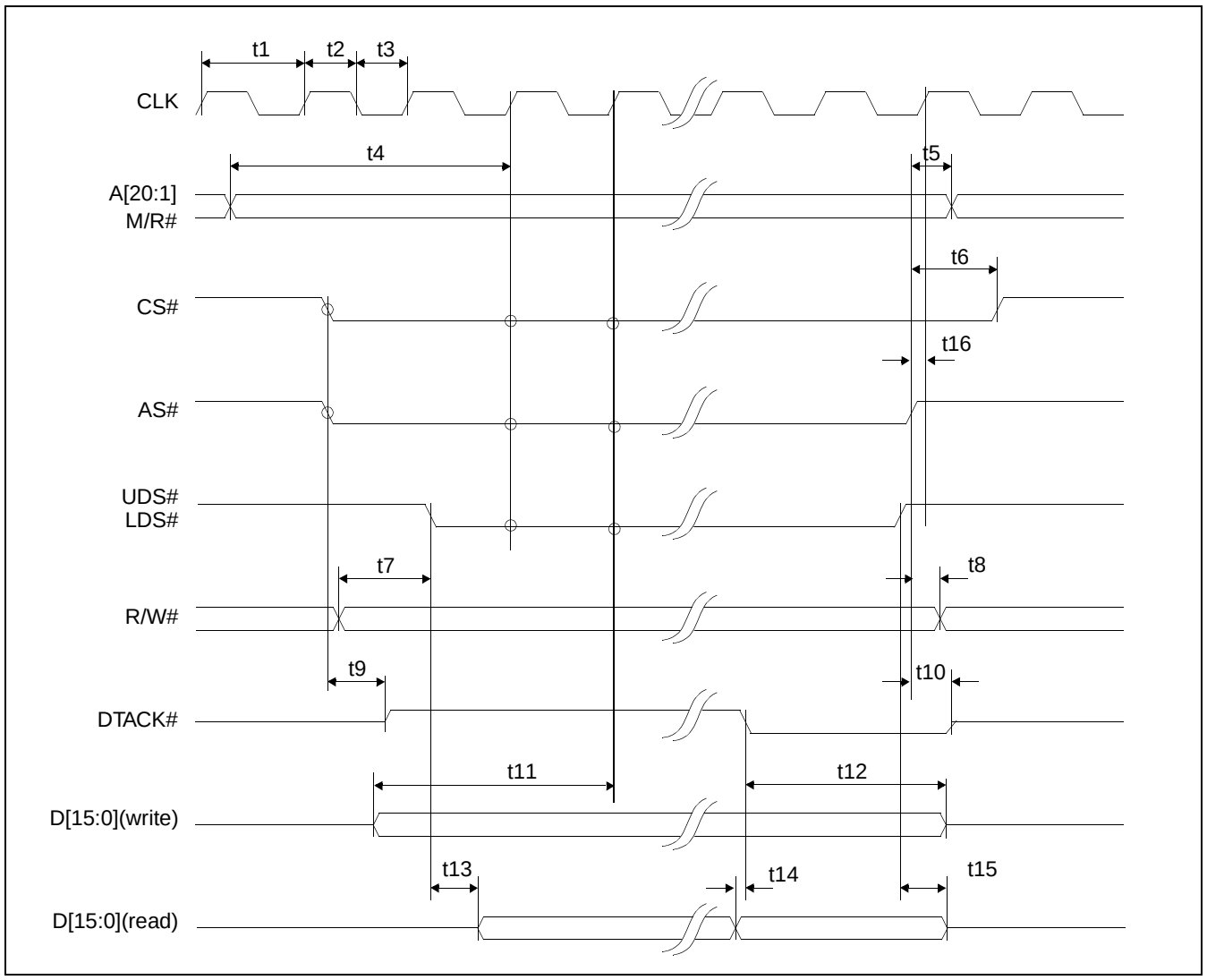


Figure 7-2: MC68K Bus 1 Interface Timing

Table 7-2: MC68K Bus 1 Interface Timing

Symbol	Parameter	Min	Max	Units
t1	Clock period	30		ns
t2	Clock pulse width high	5		ns
t3	Clock pulse width low	5		ns
t4	A[20:1], M/R# setup to first CLK where CS# = 0 AS# = 0, and either UDS#=0 or LDS# = 0	4		ns
t5	A[20:1], M/R# hold from AS#	0		ns
t6	CS# hold from AS#	0		ns
t7	R/W# setup to before to either UDS#=0 or LDS# = 0	5		ns
t8	R/W# hold from AS#	0		ns
t9[1]	AS# = 0 and CS# = 0 to DTACK# driven high	1		ns
t10	AS# high to DTACK# high impedance	1	5	ns
t11	D[15:0] valid to second CLK where CS# = 0 AS# = 0, and either UDS#=0 or LDS# = 0 (write cycle)	0		ns
t12	D[15:0] hold from falling edge of DTACK# (write cycle)	0		ns
t13[2]	Falling edge of UDS#=0 or LDS# = 0 to D[15:0] driven (read cycle)	3		ns
t14	D[15:0] valid to DTACK# falling edge (read cycle)	0		ns
t15	UDS# and LDS# high to D[15:0] invalid/high impedance (read cycle)	2	11	ns
t16	AS# high setup to CLK	3		ns

1. If the S1D13504 host interface is disabled, the timing for DTACK# driven high is relative to the falling edge of AS# or the first positive edge of CLK after A[20:1] and M/R# become valid,
   whichever occurs later.

2. If the S1D13504 host interface is disabled, the timing for D[15:0] driven is relative to the falling edge of UDS#/LDS# or the first positive edge of CLK after A[20:1] and M/R# become valid, whichever occurs later.

7.1.3 MC68K Bus 2 Interface Timing (e.g. MC68030)

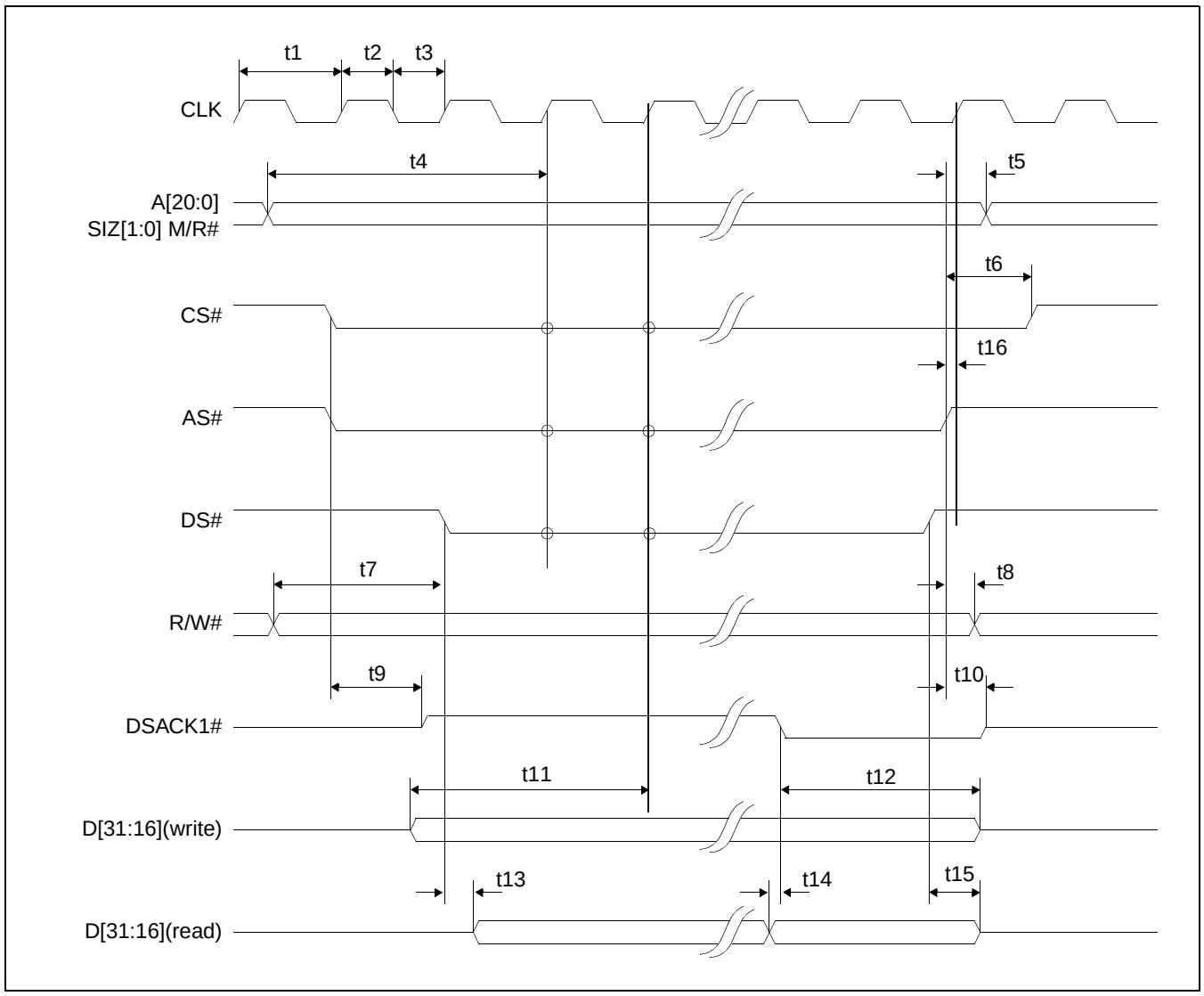


Figure 7-3: MC68K Bus 2 Interface Timing

Table 7-3: MC68K Bus 2 Interface Timing

Symbol	Parameter	Min	Max	Units
t1	Clock period	30		ns
t2	Clock pulse width high	5		ns
t3	Clock pulse width low	5		ns
t4	A[20:0], SIZ[1:0], M/R# setup to first CLK where CS# = 0 AS# = 0, and either UDS#=0 or LDS# = 0	4		ns
t5	A[20:0], SIZ[1:0], M/R# hold from AS#	0		ns
t6	CS# hold from AS#	0		ns
t7	R/W# setup to DS#	5		ns
t8	R/W# hold from AS#	0		ns
t9[1]	AS# = 0 and CS# = 0 to DSACK1# driven high	1		ns
t10	AS# high to DSACK1# high impedance	1	5	ns
t11	D[31:16] valid to second CLK where CS# = 0 AS# = 0, and either UDS#=0 or LDS# = 0 (write cycle)	0		ns
t12	D[31:16] hold from falling edge of DSACK1# (write cycle)	0		ns
t13[2]	Falling edge of UDS# = 0 or LDS# = 0 to D[31:16] driven (read cycle)	3		ns
t14	D[31:16] valid to DSACK1# falling edge (read cycle)	0		ns
t15	UDS# and LDS# high to D[31:16] invalid/high impedance (read cycle)	2	11	ns
t16	AS# high setup to CLK	3		ns

1. If the S1D13504 host interface is disabled, the timing for DSACK1# driven high is relative to the falling edge of AS# or the first positive edge of CLK after A[20:0] and M/R# become valid, whichever occurs later.

2. If the S1D13504 host interface is disabled, the timing for D[15:0] driven is relative to the falling edge of UDS#/LDS# or the first positive edge of CLK after A[20:1] and M/R# becomes valid, whichever occurs later.

7.1.4 Generic MPU Interface Synchronous Timing

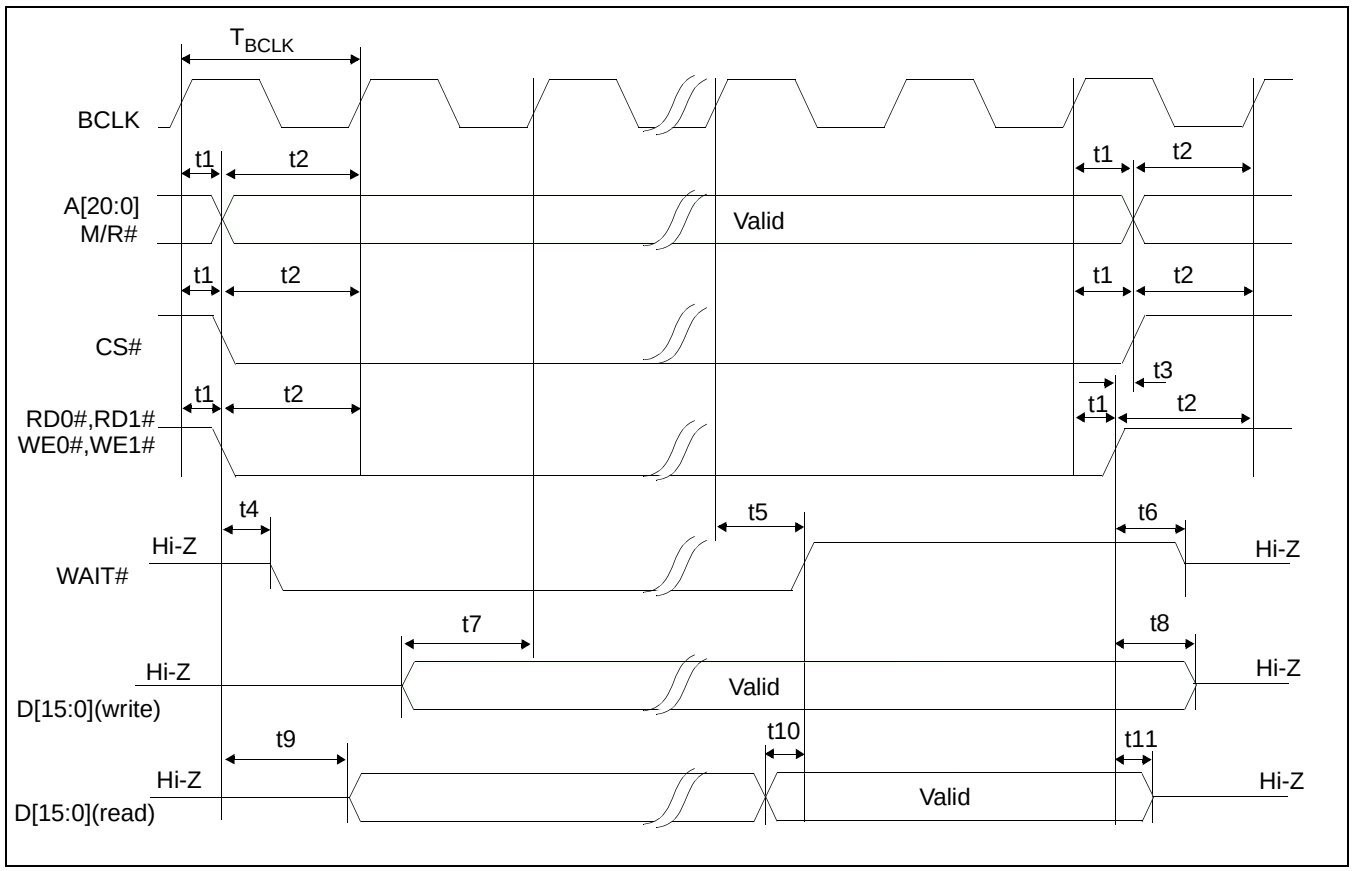


Figure 7-4: Generic MPU Interface Synchronous Timing

Table 7-4: Generic MPU Interface Synchronous Timing

Symbol	Parameter	Min	Max	Units
T_{BCLK}	Bus clock period	25		ns
t1	A[20:0], M/R#, CS#, RD0#,RD1#,WE0#,WE1# hold time	1		ns
t2	A[20:0], M/R#, CS#, RD0#,RD1#,WE0#,WE1# setup time	5		ns
t3	RD0#,RD1#,WE0#,WE1# high to A[20:0], M/R# invalid and CS# high	0		ns
t4[1]	RD0#,RD1#,WE0#,WE1# low and CS# low to WAIT# driven low	1	7	ns
t5	BCLK to WAIT# high	0	15	ns
t6	RD0#,RD1#,WE0#,WE1# high to WAIT# high impedance	1	6	ns
t7	D[15:0] valid to second BCLK where RD0#,RD1#,WE0#,WE1# low and CS# low (write cycle)	5		ns
t8	D[15:0] hold from WE0#, WE1# high (write cycle)	0		ns
t9[2]	RD0#,RD1# low to D[15:0] driven (read cycle)	3	15	ns
t10	D[15:0] valid to WAIT# high (read cycle)	0		
t11	RD0#, RD1# high to D[15:0] high impedance (read cycle)	2	10	

1. If the S1D13504 host interface is disabled, the timing for WAIT# driven low is relative to the falling edge of CS# and RD0#, RD1#, WE0#, WE1# or the first positive edge of BCLK after A[20:0] and M/R# become valid, whichever occurs later.

2. If the S1D13504 host interface is disabled, the timing for D[15:0] driven is relative to the falling edge of RD0#, RD1# or the first positive edge of BCLK after A[20:0] and M/R# become valid, whichever occurs later.

7.1.5 Generic MPU Interface Asynchronous Timing

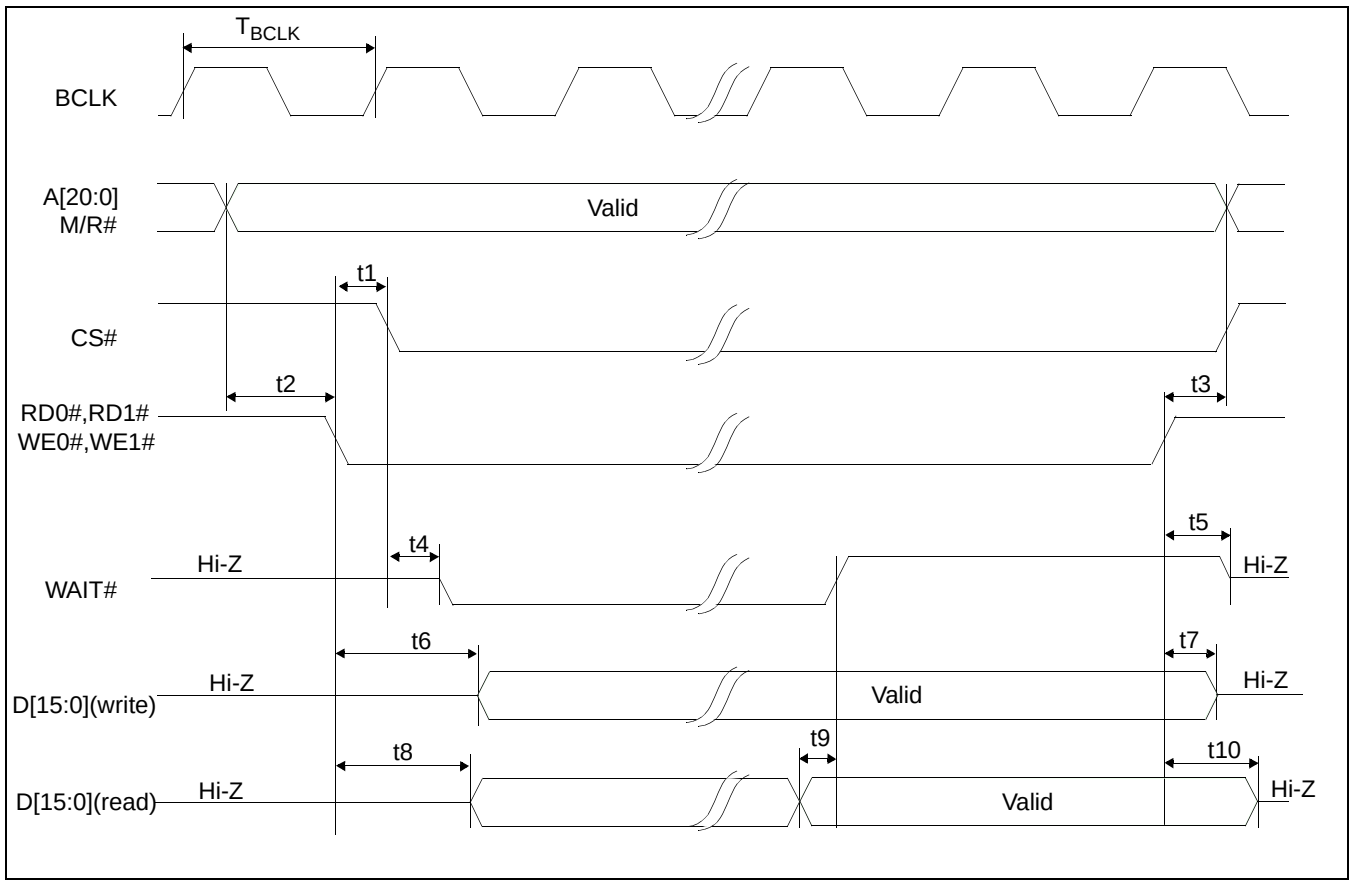


Figure 7-5: Generic MPU Interface Asynchronous Timing

Table 7-5: Generic MPU Interface Asynchronous Timing

Symbol	Parameter	Min	Max	Units
T_{BCLK}	Bus clock period	25		ns
t1	RD0#, RD1#, WE0#, WE1# low to CS# low	4		ns
t2	A[20:0], M/R# valid to RD0#, RD1#, WE0#, WE1# low	0		ns
t3	RD0#, RD1#, WE0#, WE1# high to A[20:0], CS#, M/R# invalid and CS# high	0		ns
t4[1]	CS# low to WAIT# driven low	1	7	ns
t5	RD0#, RD1#, WE0#, WE1# high to WAIT# high impedance	1	6	ns
t6	WE0#, WE1# low to D[15:0] valid (write cycle)		20	ns
t7	D[15:0] hold from WE0#, WE1# high (write cycle)	0		ns
t8[2]	RD0#, RD1# low to D[15:0] driven (read cycle)	3	15	ns
t9	D[15:0] valid to WAIT# high (read cycle)	0		
t10	RD0#, RD1# high to D[15:0] high impedance (read cycle)	2	10	

1. If the S1D13504 host interface is disabled, the timing for WAIT# driven low is relative to the falling edge of CS# or the first positive edge of BCLK after A[20:0] and M/R# become valid, whichever occurs later.

2. If the S1D13504 host interface is disabled, the timing for D[15:0] driven is relative to the falling edge of RD0#, RD1# or the first positive edge of BCLK after A[20:0] and M/R# become valid,
whichever occurs later.

7.2 Clock Input Requirements

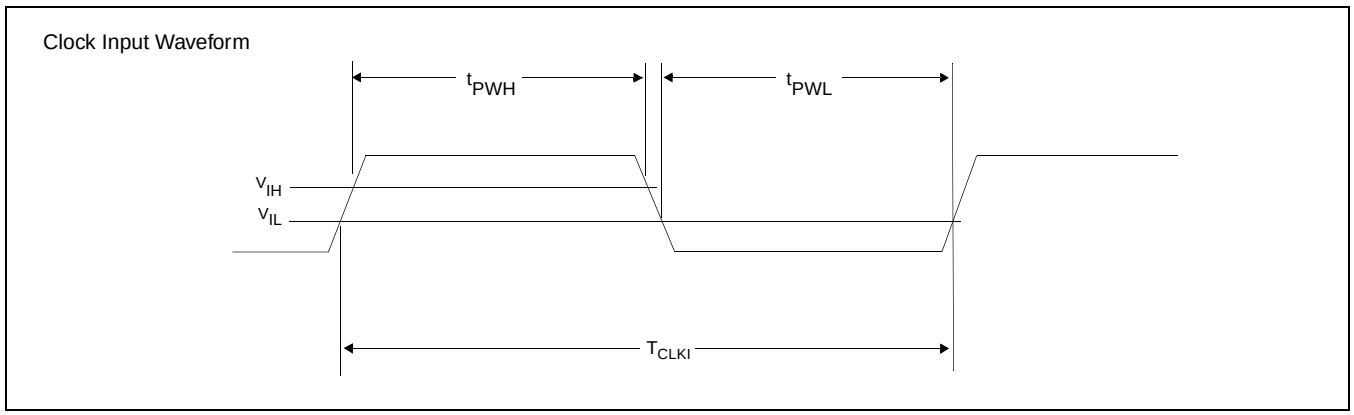


Figure 7-6: Clock Input Requirements

Table 7-6: Clock Input Requirements

Symbol	Parameter	Min	Typ	Max	Units
T_{CLKI}	Input Clock Period (CLKI)	12.5			ns
T_{PCLK}	Pixel Clock Period (PCLK) not shown	25			ns
T_{MCLK}	Memory Clock Period (MCLK) not shown	25			ns
t_{PWH}	Input Clock Pulse Width High (CLKI)	45%		55%	T_{CLKI}
t_{PWL}	Input Clock Pulse Width Low (CLKI)	45%		55%	T_{CLKI}

Note

When CLKI is more than 40MHz, REG[19h] bit 2 must be set to 1 (MCLK = CLKI/2). There is no minimum frequency for CLKI.

7.3 Memory Interface Timing

7.3.1 EDO-DRAM Read Timing

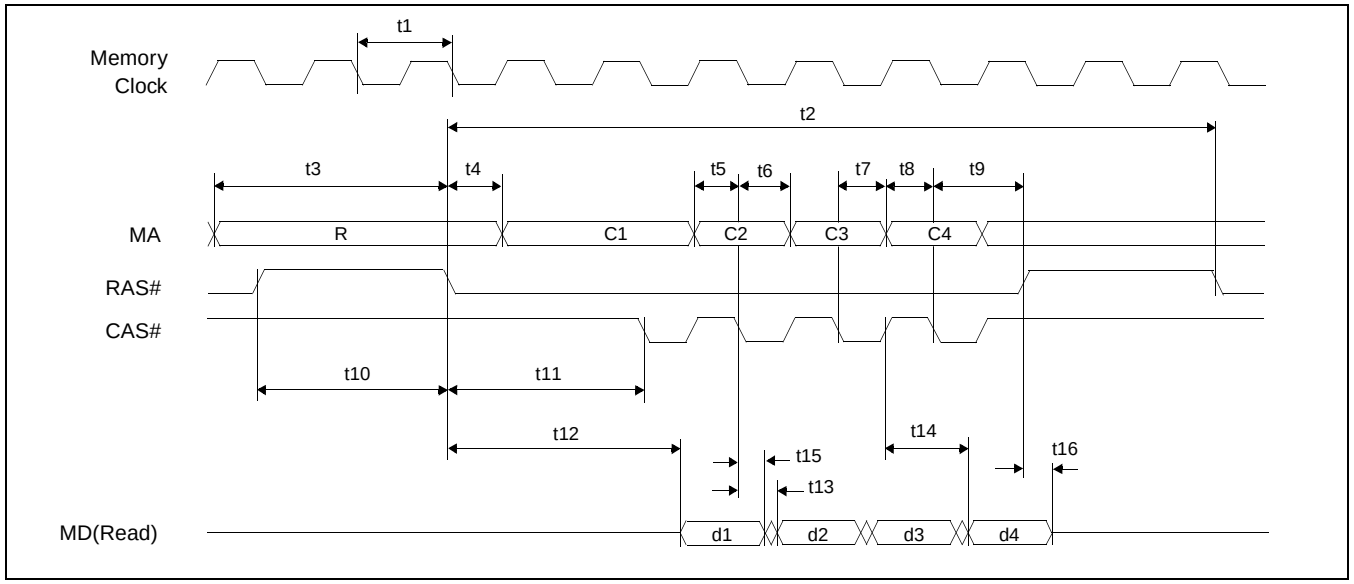


Figure 7-7: EDO-DRAM Read Timing

Table 7-7: EDO DRAM Read Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Memory clock period	25			ns
t2	Random read or write cycle time (REG[22h] bits [6:5] = 00)	5 t1			ns
	Random read or write cycle time (REG[22h] bits [6:5] = 01)	4 t1			ns
	Random read or write cycle time (REG[22h] bits [6:5] = 10)	3 t1			ns
t3	Row address setup time (REG[22h] bits [3:2] = 00)	2.45 t1			ns
	Row address setup time (REG[22h] bits [3:2] = 01)	2 t1			ns
	Row address setup time (REG[22h] bits [3:2] = 10)	1.45 t1			ns
t4	Row address hold time (REG[22h] bits [3:2] = 00 or 10)	0.45 t1 - 1			ns
	Row address hold time (REG[22h] bits [3:2] = 01)	t1 - 1			ns
t5	Column address setup time	0.45 t1 - 1			ns
t6	Column address hold time	0.45 t1 - 1			ns
t7	CAS# pulse width	0.45 t1		0.55 t1 + 1	ns
t8	CAS# precharge time	0.45 t1 - 1		0.55 t1	ns
t9	RAS# hold time	1 t1			ns
t10	RAS# precharge time (REG[22h] bits [3:2] = 00)	2 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 01)	1.45 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 10)	1 t1 - 1			ns
t11	RAS# to CAS# delay time (REG[22h] bit 4 = 0 and bits [3:2] = 00 or 10)	2 t1 - 2		2 t1	ns
	RAS# to CAS# delay time (REG[22h] bit 4 = 1 and bits [3:2] = 00 or 10)	1 t1 - 2		1 t1	ns
	RAS# to CAS# delay time (REG[22h] bits [3:2] = 01)	1.45 t1 - 2		1.55 t1	ns
t12	Access time from RAS# (REG[22h] bit 4 = 0 and bits [3:2] = 00 or 10)			3 t1 - 11	ns
	Access time from RAS# (REG[22h] bit 4 = 1 and bits [3:2] = 00 or 10)			2 t1 - 11	ns
	Access time from RAS# (REG[22h] bits [3:2] = 01)			2.45 t1 - 12	ns
t13	Access time from CAS#			t1 - 10	ns
t14	Access time from CAS# precharge, column address			1.45 t1 - 6	ns
t15	Read Data hold after CAS# low	2			ns
t16	Read Data turn-off delay from RAS#	2			ns

7.3.2 EDO-DRAM Write Timing

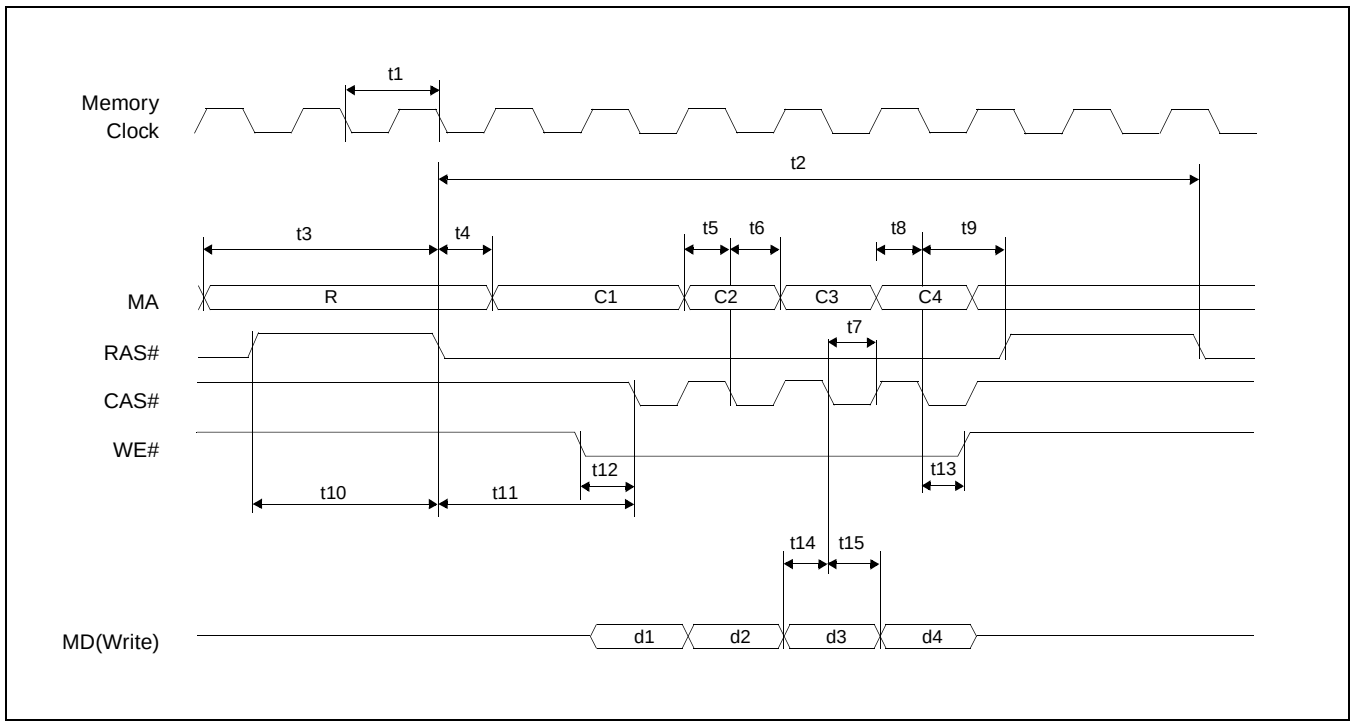


Figure 7-8: EDO-DRAM Write Timing

Table 7-8: EDO DRAM Write Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Memory clock period	25			ns
t2	Random read or write cycle time (REG[22h] bits [6:5] = 00)	5 t1			ns
	Random read or write cycle time (REG[22h] bits [6:5] = 01)	4 t1			ns
	Random read or write cycle time (REG[22h] bits [6:5] = 10)	3 t1			ns
t3	Row address setup time (REG[22h] bits [3:2] = 00)	2.45 t1			ns
	Row address setup time (REG[22h] bits [3:2] = 01)	2 t1			ns
	Row address setup time (REG[22h] bits [3:2] = 10)	1.45 t1			ns
t4	Row address hold time (REG[22h] bits [3:2] = 00 or 10)	0.45 t1 - 1			ns
	Row address hold time (REG[22h] bits [3:2] = 01)	t1 - 1			ns
t5	Column address setup time	0.45 t1 - 1			ns
t6	Column address hold time	0.45 t1 - 1			ns
t7	CAS# pulse width	0.45 t1		0.55 t1 + 1	ns
t8	CAS# precharge time	0.45 t1 - 1		0.55 t1	ns
t9	RAS# hold time	1 t1			ns
t10	RAS# precharge time (REG[22h] bits [3:2] = 00)	2 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 01)	1.45 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 10)	1 t1 - 1			ns
t11	RAS# to CAS# delay time (REG[22h] bit 4 = 0 and bits [3:2] = 00 or 10)	2 t1 - 2		2 t1	ns
	RAS# to CAS# delay time (REG[22h] bit 4 = 1 and bits [3:2] = 00 or 10)	1 t1 - 2		1 t1	ns
	RAS# to CAS# delay time (REG[22h] bits [3:2] = 01)	1.45 t1 - 2		1.55 t1	ns
t12	Write command setup time	0.45 t1 - 1			ns
t13	Write command hold time	0.45 t1			ns
t14	Write Data setup time	0.45 t1 - 3			ns
t15	Write Data hold time	0.45 t1 - 2			ns

7.3.3 EDO-DRAM Read-Write Timing

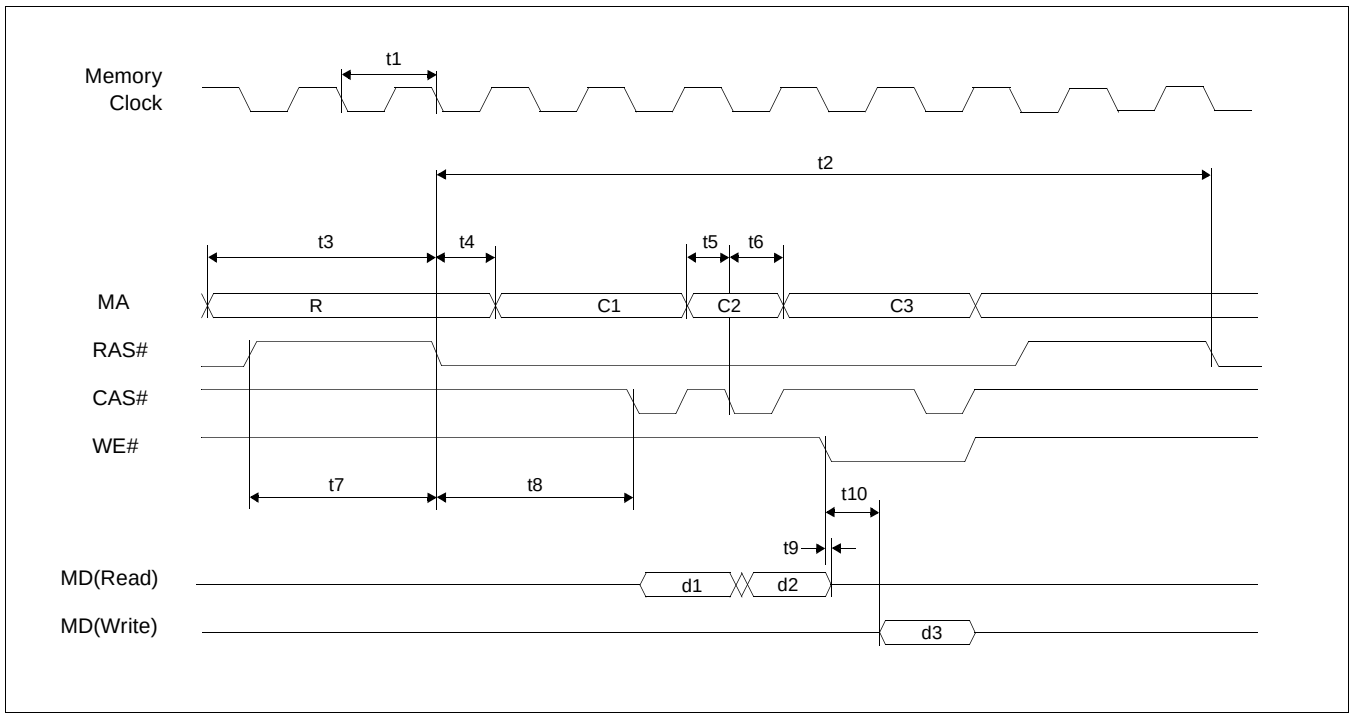


Figure 7-9: EDO-DRAM Read-Write Timing

Table 7-9: EDO DRAM Read-Write Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Memory clock period	25			ns
t2	Random read or write cycle time (REG[22h] bits [6:5] = 00)	5 t1			ns
	Random read or write cycle time (REG[22h] bits [6:5] = 01)	4 t1			ns
	Random read or write cycle time (REG[22h] bits [6:5] = 10)	3 t1			ns
t3	Row address setup time (REG[22h] bits [3:2] = 00)	2.45 t1			ns
	Row address setup time (REG[22h] bits [3:2] = 01)	2 t1			ns
	Row address setup time (REG[22h] bits [3:2] = 10)	1.45 t1			ns
t4	Row address hold time (REG[22h] bits [3:2] = 00 or 10)	0.45 t1 - 1			ns
	Row address hold time (REG[22h] bits [3:2] = 01)	t1 - 1			ns
t5	Column address setup time	0.45 t1 - 1			ns
t6	Column address hold time	0.45 t1 - 1			ns
t7	RAS# precharge time (REG[22h] bits [3:2] = 00)	2 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 01)	1.45 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 10)	1 t1 - 1			ns
t8	RAS# to CAS# delay time (REG[22h] bit 4 = 0 and bits [3:2] = 00 or 10)	2 t1 - 2		2 t1	ns
	RAS# to CAS# delay time (REG[22h] bit 4 = 1 and bits [3:2] = 00 or 10)	1 t1 - 2		1 t1	ns
	RAS# to CAS# delay time (REG[22h] bits [3:2] = 01)	1.45 t1 - 2		1.55 t1	ns
t9	Read Data turn-off delay from WE#	0			ns
t10	Write Data delay from WE# (REG[22h] bit 7 = 0)	1.45 t1			ns
	Write Data delay from WE# (REG[22h] bit 7 = 1)	0.45 t1			ns

7.3.4 EDO-DRAM CAS Before RAS Refresh Timing

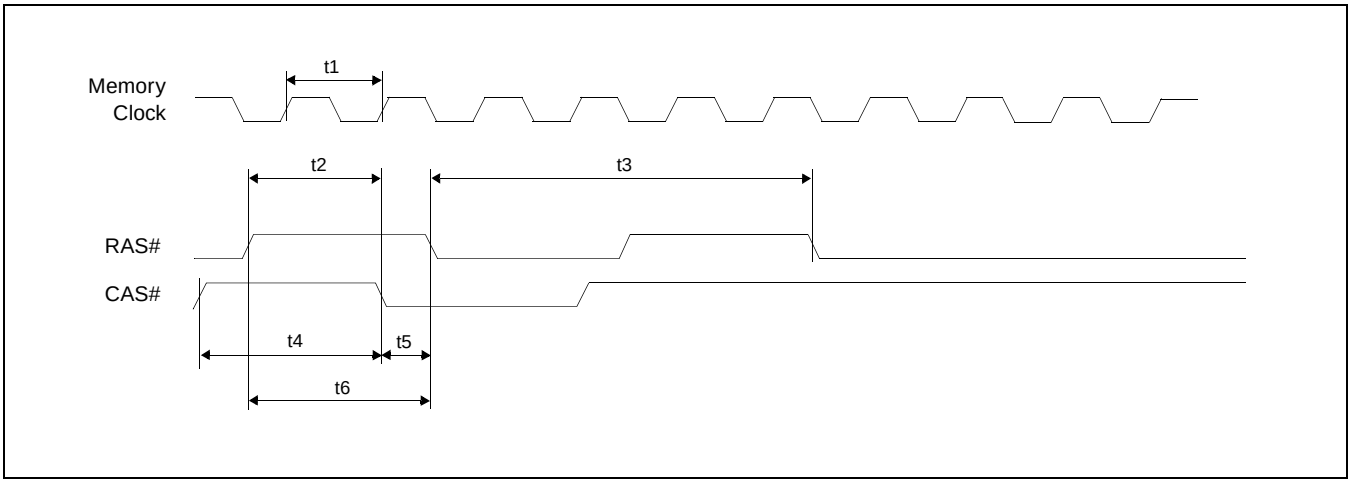


Figure 7-10: EDO-DRAM CAS Before RAS Refresh Timing

Table 7-10: EDO-DRAM CAS Before RAS Refresh Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Memory clock period	25			ns
t2	RAS# to CAS# precharge time (REG[22h] bits [3:2] = 00)	1.45 t1			ns
	RAS# to CAS# precharge time (REG[22h] bits [3:2] = 01 or 10)	0.45 t1			ns
t3	Random read or write cycle time (REG[22h] bits [6:5] = 00)	5 t1			ns
	Random read or write cycle time (REG[22h] bits [6:5] = 01)	4 t1			ns
	Random read or write cycle time (REG[22h] bits [6:5] = 10)	3 t1			ns
t4	CAS# precharge time (REG[22h] bits [3:2] = 00)	2 t1			ns
	CAS# precharge time (REG[22h] bits [3:2] = 01 or 10)	1 t1			ns
t5	CAS# setup time (REG[22h] bits [3:2] = 00 or 10)	0.45 t1 - 2			ns
	CAS# setup time (REG[22h] bits [3:2] = 01)	1 t1 - 2			ns
t6	RAS# precharge time (REG[22h] bits [3:2] = 00)	2 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 01)	1.45 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 10)	1 t1 - 1			ns

7.3.5 EDO-DRAM Self-Refresh Timing

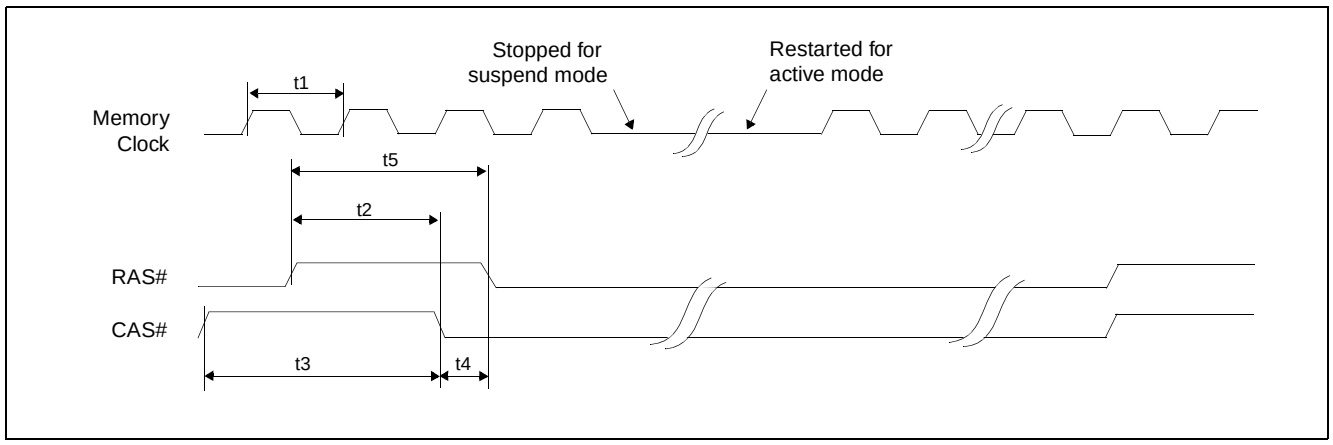


Figure 7-11: EDO-DRAM Self-Refresh Timing

Table 7-11: EDO-DRAM Self-Refresh Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Memory clock period	25			ns
t2	RAS# to CAS# precharge time (REG[22h] bits [3:2] = 00)	1.45 t1			ns
	RAS# to CAS# precharge time (REG[22h] bits [3:2] = 01 or 10)	0.45 t1			ns
t3	CAS# precharge time (REG[22h] bits [3:2] = 00)	2 t1			ns
	CAS# precharge time (REG[22h] bits [3:2] = 01 or 10)	1 t1			ns
t4	CAS# setup time (REG[22h] bits [3:2] = 00 or 10)	0.45 t1 - 2			ns
	CAS# setup time (REG[22h] bits [3:2] = 01)	1 t1 - 2			ns
t5	RAS# precharge time (REG[22h] bits [3:2] = 00)	2 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 01)	1.45 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 10)	1 t1 - 1			ns

7.3.6 FPM-DRAM Read Timing

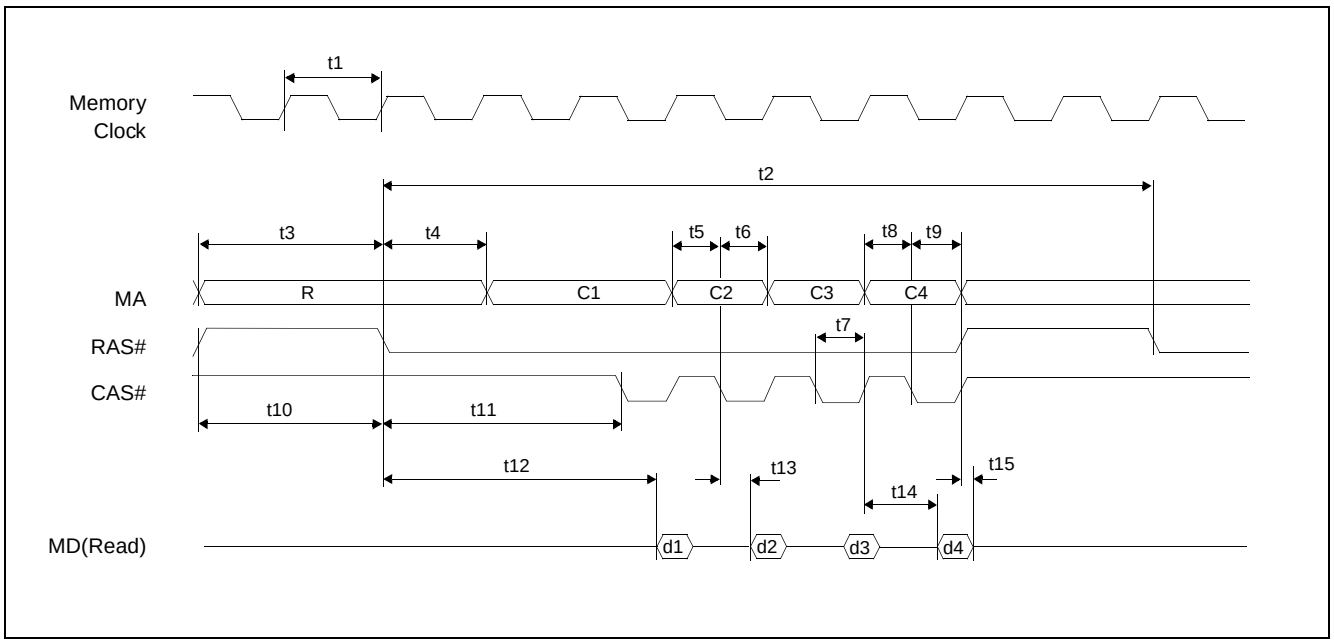


Figure 7-12: FPM-DRAM Read Timing

Table 7-12: FPM DRAM Read Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Memory clock	40			ns
t2	Random read or write cycle time (REG[22h] bits [6:5] = 00)	5 t1			ns
	Random read or write cycle time (REG[22h] bits [6:5] = 01)	4 t1			ns
	Random read or write cycle time (REG[22h] bits [6:5] = 10)	3 t1			ns
t3	Row address setup time (REG[22h] bits [3:2] = 00)	2 t1			ns
	Row address setup time (REG[22h] bits [3:2] = 01)	1.45 t1			ns
	Row address setup time (REG[22h] bits [3:2] = 10)	1 t1			ns
t4	Row address hold time (REG[22h] bits [3:2] = 00 or 10)	t1 - 1			ns
	Row address hold time (REG[22h] bits [3:2] = 01)	0.45 t1 - 1			ns
t5	Column address set-up time	0.45 t1 - 1			ns
t6	Column address hold time	0.45 t1 - 1			ns
t7	CAS# pulse width	0.45 t1		0.55 t1 + 1	ns
t8	CAS# precharge time	0.45 t1 - 1		0.55 t1	ns
t9	RAS# hold time	0.45 t1			ns
t10	RAS# precharge time (REG[22h] bits [3:2] = 00)	2 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 01)	1.45 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 10)	1 t1 - 1			ns
t11	RAS# to CAS# delay time (REG[22h] bit 4 = 1 and bits [3:2] = 00 or 10)	1.45 t1 - 2		1.55 t1	ns
	RAS# to CAS# delay time (REG[22h] bit 4 = 0 and bits [3:2] = 00 or 10)	2.45 t1 - 2		2.55 t1	ns
	RAS# to CAS# delay time (REG[22h] bit 4 = 1 and bits [3:2] = 01)	1 t1 - 2		1 t1	ns
	RAS# to CAS# delay time (REG[22h] bit 4 = 0 and bits [3:2] = 01)	2 t1 - 2		2 t1	ns
t12	Access time from RAS# (REG[22h] bit 4 = 1 and bits [3:2] = 00 or 10)			2 t1 - 2	ns
	Access time from RAS# (REG[22h] bit 4 = 0 and bits [3:2] = 00 or 10)			3 t1 - 2	ns
	Access time from RAS# (REG[22h] bit 4 = 1 and bits [3:2] = 01)			1.45 t1 - 2	ns
	Access time from RAS# (REG[22h] bit 4 = 0 and bits [3:2] = 01)			2.45 t1 - 2	ns
t13	Access time from CAS#			0.45 t1 - 1	ns
t14	Access time from CAS# precharge			1 t1 - 2	ns
t15	Read Data hold from CAS# or RAS#	2			ns

7.3.7 FPM-DRAM Write Timing

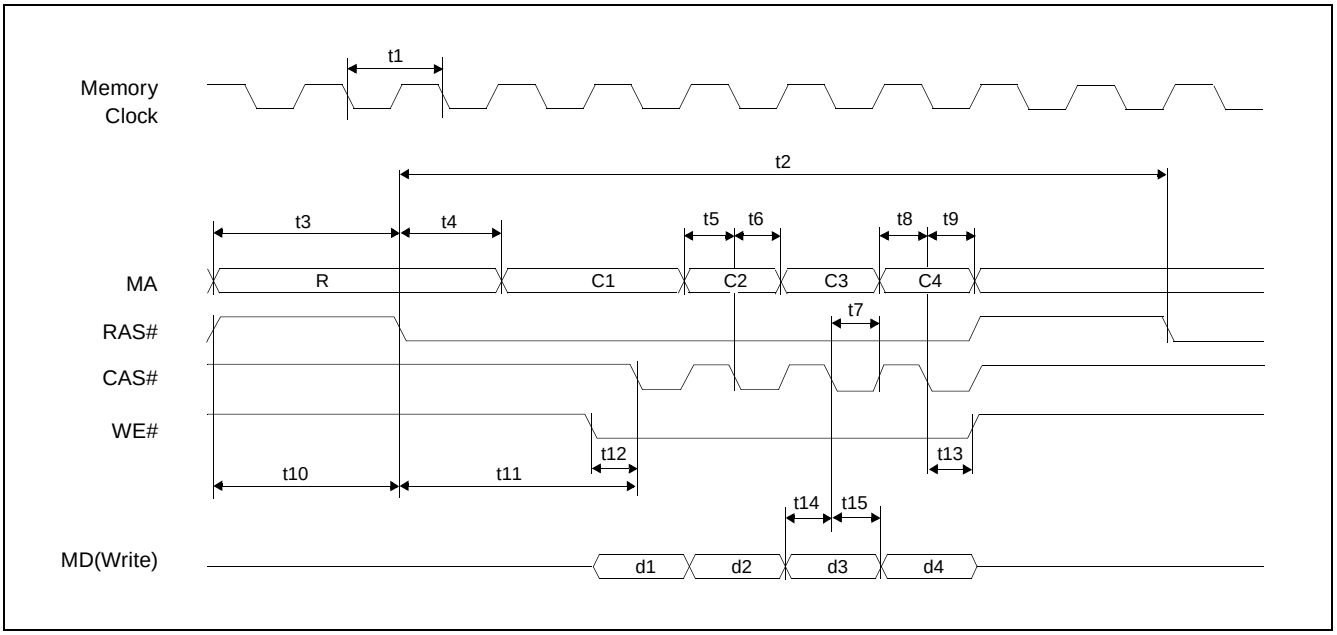


Figure 7-13: FPM-DRAM Write Timing

Table 7-13: FPM-DRAM Write Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Memory clock	40			ns
t2	Random read or write cycle time (REG[22h] bits [6:5] = 00)	5 t1			ns
	Random read or write cycle time (REG[22h] bits [6:5] = 01)	4 t1			ns
	Random read or write cycle time (REG[22h] bits [6:5] = 10)	3 t1			ns
t3	Row address setup time (REG[22h] bits [3:2] = 00)	2 t1			ns
	Row address setup time (REG[22h] bits [3:2] = 01)	1.45 t1			ns
	Row address setup time (REG[22h] bits [3:2] = 10)	1 t1			ns
t4	Row address hold time (REG[22h] bits [3:2] = 00 or 10)	t1 - 1			ns
	Row address hold time (REG[22h] bits [3:2] = 01)	0.45 t1 - 1			ns
t5	Column address set-up time	0.45 t1 - 1			ns
t6	Column address hold time	0.45 t1 - 1			ns
t7	CAS# pulse width	0.45 t1		0.55 t1 + 1	ns
t8	CAS# precharge time	0.45 t1 - 1		0.55 t1	ns
t9	RAS# hold time	0.45 t1			ns
t10	RAS# precharge time (REG[22h] bits [3:2] = 00)	2 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 01)	1.45 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 10)	1 t1 - 1			ns
t11	RAS# to CAS# delay time (REG[22h] bit 4 = 1 and bits [3:2] = 00 or 10)	1.45 t1 - 2		1.55 t1	ns
	RAS# to CAS# delay time (REG[22h] bit 4 = 0 and bits [3:2] = 00 or 10)	2.45 t1 - 2		2.55 t1	ns
	RAS# to CAS# delay time (REG[22h] bit 4 = 1 and bits [3:2] = 01)	1 t1 - 2		1 t1	ns
	RAS# to CAS# delay time (REG[22h] bit 4 = 0 and bits [3:2] = 01)	2 t1 - 2		2 t1	ns
t12	Write command setup time	0.45 t1 - 1			ns
t13	Write command hold time	0.45 t1			ns
t14	Write Data setup time	0.45 t1 - 3			ns
t15	Write Data hold time	0.45 t1 - 2			ns

7.3.8 FPM-DRAM Read-Write Timing

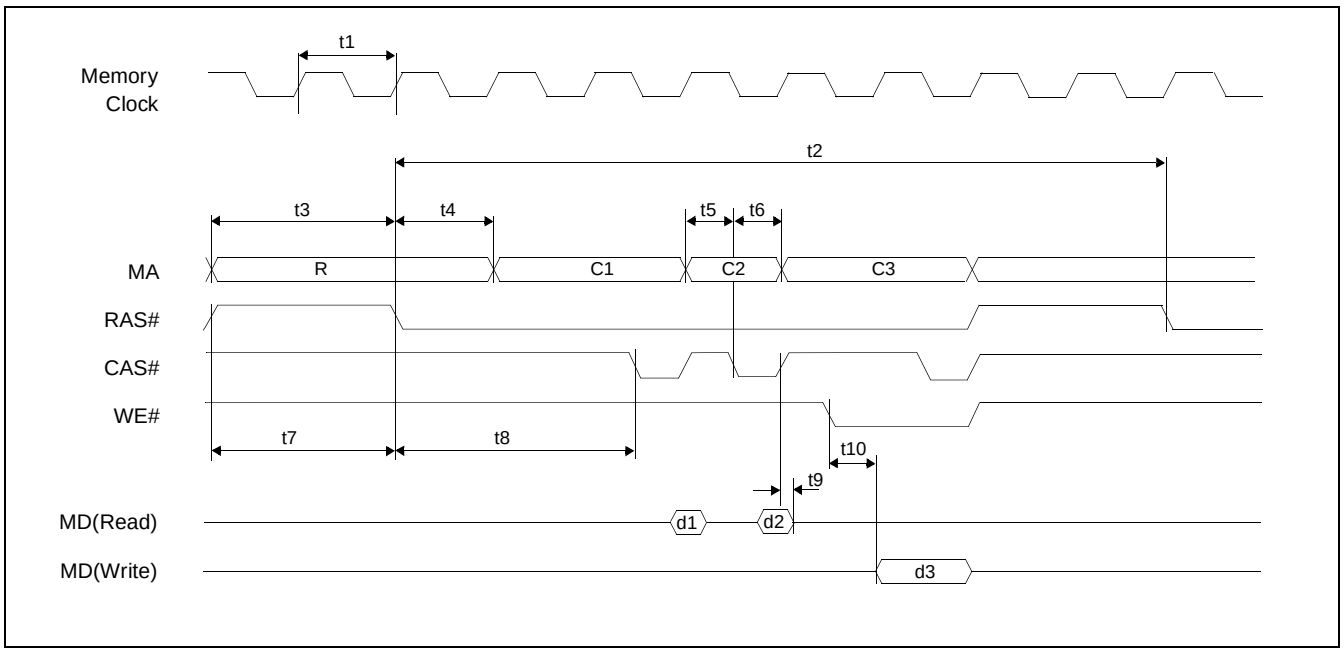


Figure 7-14: FPM-DRAM Read-Write Timing

Table 7-14: FPM-DRAM Read-Write Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Memory clock	40			ns
t2	Random read or write cycle time (REG[22h] bits [6:5] = 00)	5 t1			ns
	Random read or write cycle time (REG[22h] bits [6:5] = 01)	4 t1			ns
	Random read or write cycle time (REG[22h] bits [6:5] = 10)	3 t1			ns
t3	Row address setup time (REG[22h] bits [3:2] = 00)	2 t1			ns
	Row address setup time (REG[22h] bits [3:2] = 01)	1.45 t1			ns
	Row address setup time (REG[22h] bits [3:2] = 10)	1 t1			ns
t4	Row address hold time (REG[22h] bits [3:2] = 00 or 10)	t1 - 1			ns
	Row address hold time (REG[22h] bits [3:2] = 01)	0.45 t1 - 1			ns
t5	Column address set-up time	0.45 t1 - 1			ns
t6	Column address hold time	0.45 t1 - 1			ns
t7	RAS# precharge time (REG[22h] bits [3:2] = 0)	2 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 01)	1.45 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 10)	1 t1 - 1			ns
t8	RAS# to CAS# delay time (REG[22h] bit 4 = 1 and bits [3:2] = 00 or 10)	1.45 t1 - 2		1.55 t1	ns
	RAS# to CAS# delay time (REG[22h] bit 4 = 0 and bits [3:2] = 00 or 10)	2.45 t1 - 2		2.55 t1	ns
	RAS# to CAS# delay time (REG[22h] bit 4 = 1 and bits [3:2] = 01)	1 t1 - 2		1 t1	ns
	RAS# to CAS# delay time (REG[22h] bit 4 = 0 and bits [3:2] = 01)	2 t1 - 2		2 t1	ns
t9	Read Data turn-off delay from CAS#	2			ns
t10	Write Data enable delay from WE#	0.45 t1			ns

7.3.9 FPM-DRAM CAS# Before RAS# Refresh Timing

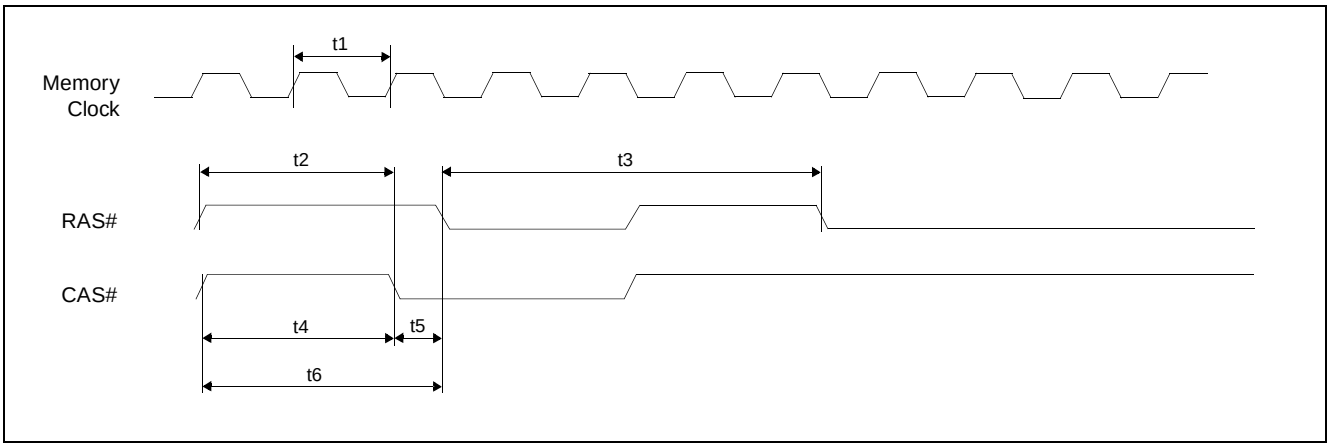


Figure 7-15: FPM-DRAM CAS# Before RAS# Refresh Timing

Table 7-15: FPM-DRAM CAS# Before RAS# Refresh Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Memory clock	40			ns
t2	RAS# to CAS# precharge time (REG[22h] bits [3:2] = 00)	2 t1			ns
	RAS# to CAS# precharge time (REG[22h] bits [3:2] = 01 or 10)	1 t1			ns
t3	Random read or write cycle time (REG[22h] bits [6:5] = 00)	5 t1			ns
	Random read or write cycle time (REG[22h] bits [6:5] = 01)	4 t1			ns
	Random read or write cycle time (REG[22h] bits [6:5] = 10)	3 t1			ns
t4	CAS# precharge time (REG[22h] bits [3:2] = 00)	2 t1			ns
	CAS# precharge time (REG[22h] bits [3:2] = 01 or 10)	1 t1			ns
t5	CAS# setup time (CAS# before RAS# refresh)	0.45 t1 - 2			ns
t6	RAS# precharge time (REG[22h] bits [3:2] = 00)	2.45 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 01 or 10)	1.45 t1 - 1			ns

7.3.10 FPM-DRAM Self-Refresh Timing

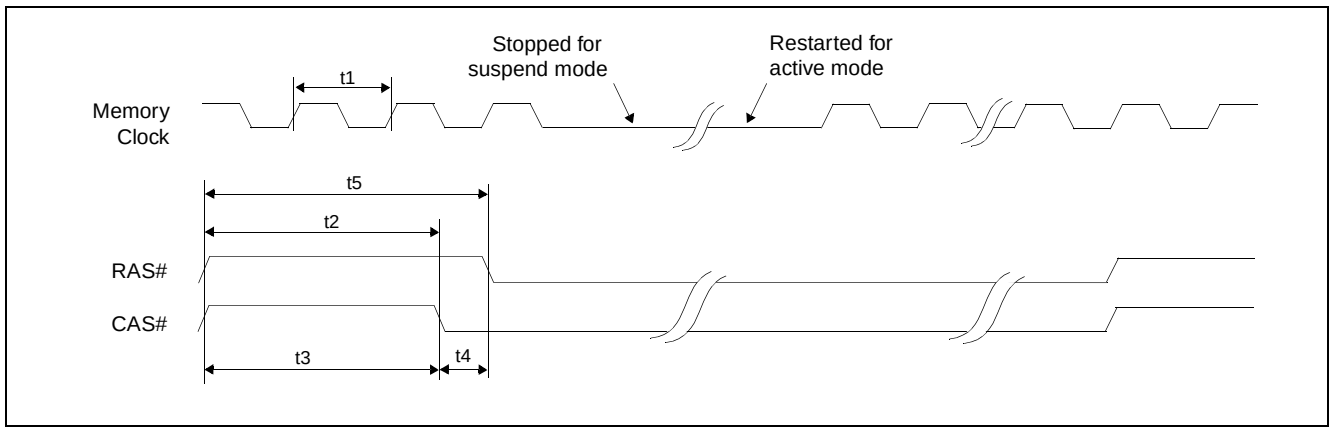


Figure 7-16: FPM-DRAM CBR Self-Refresh Timing

Table 7-16: FPM-DRAM CBR Self-Refresh Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Memory clock	40			ns
t2	RAS# to CAS# precharge time (REG[22h] bits [3:2] = 00)	2 t1			ns
	RAS# to CAS# precharge time (REG[22h] bits [3:2] = 01 or 10)	1 t1			ns
t3	CAS# precharge time (REG[22h] bits [3:2] = 00)	2 t1			ns
	CAS# precharge time (REG[22h] bits [3:2] = 01 or 10)	1 t1			ns
t4	CAS# setup time (CAS# before RAS# refresh)	0.45 t1 - 2			ns
t5	RAS# precharge time (REG[22h] bits [3:2] = 00)	2.45 t1 - 1			ns
	RAS# precharge time (REG[22h] bits [3:2] = 01 or 10)	1.45 t1 - 1			ns

7.4 Display Interface

7.4.1 Power-On/Reset Timing

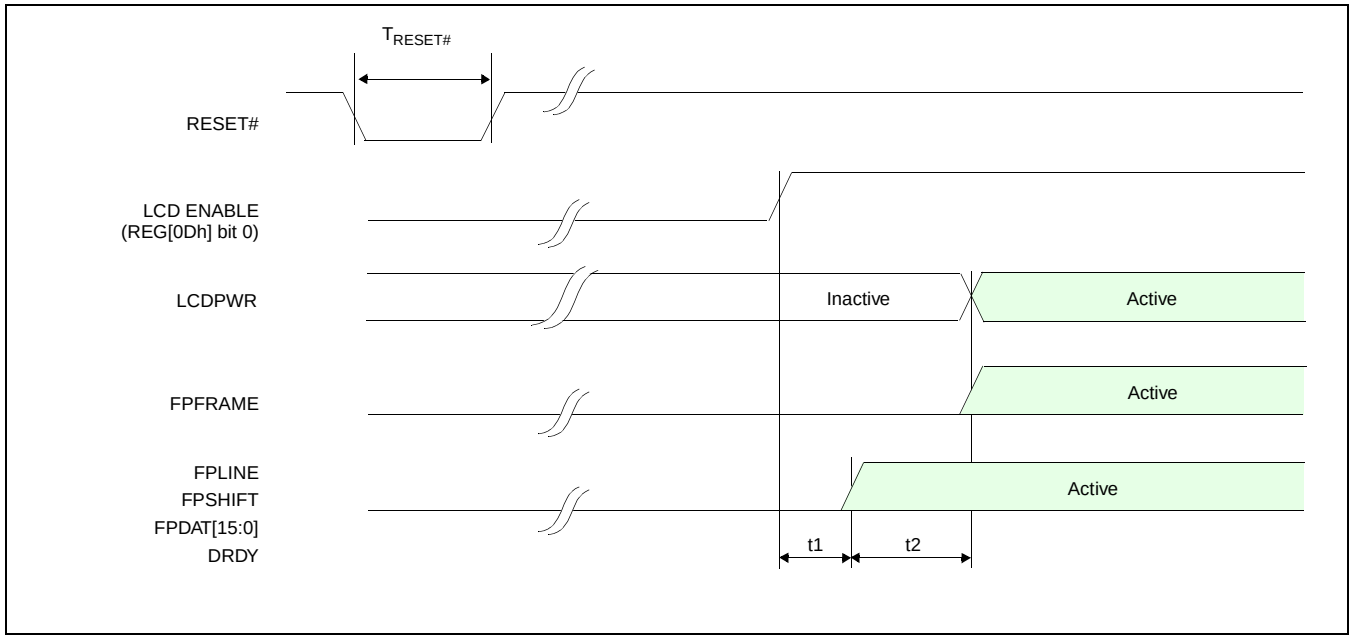


Figure 7-17: LCD Panel Power-On/Reset Timing

Table 7-17: LCD Panel Power-On/Reset Timing

Symbol	Parameter	Min	Typ	Max	Units
$T_{RESET\#}$	RESET# pulse time	100			us
t1	LCD Enable bit high to FPLINE, FPSHIFT, FPDAT[15:0], DRDY active			$T_{FPFRAME} + 6T_{PCLK}$	ns
t2	FPLINE, FPSHIFT, FPDAT[15:0], DRDY active to LCDPWR, on and FPFRAME active		128		Frames

Note

Where $T_{FPFRAME}$ is the period of FPFRAME and T_{PCLK} is the period of the pixel clock.

7.4.2 Suspend Timing

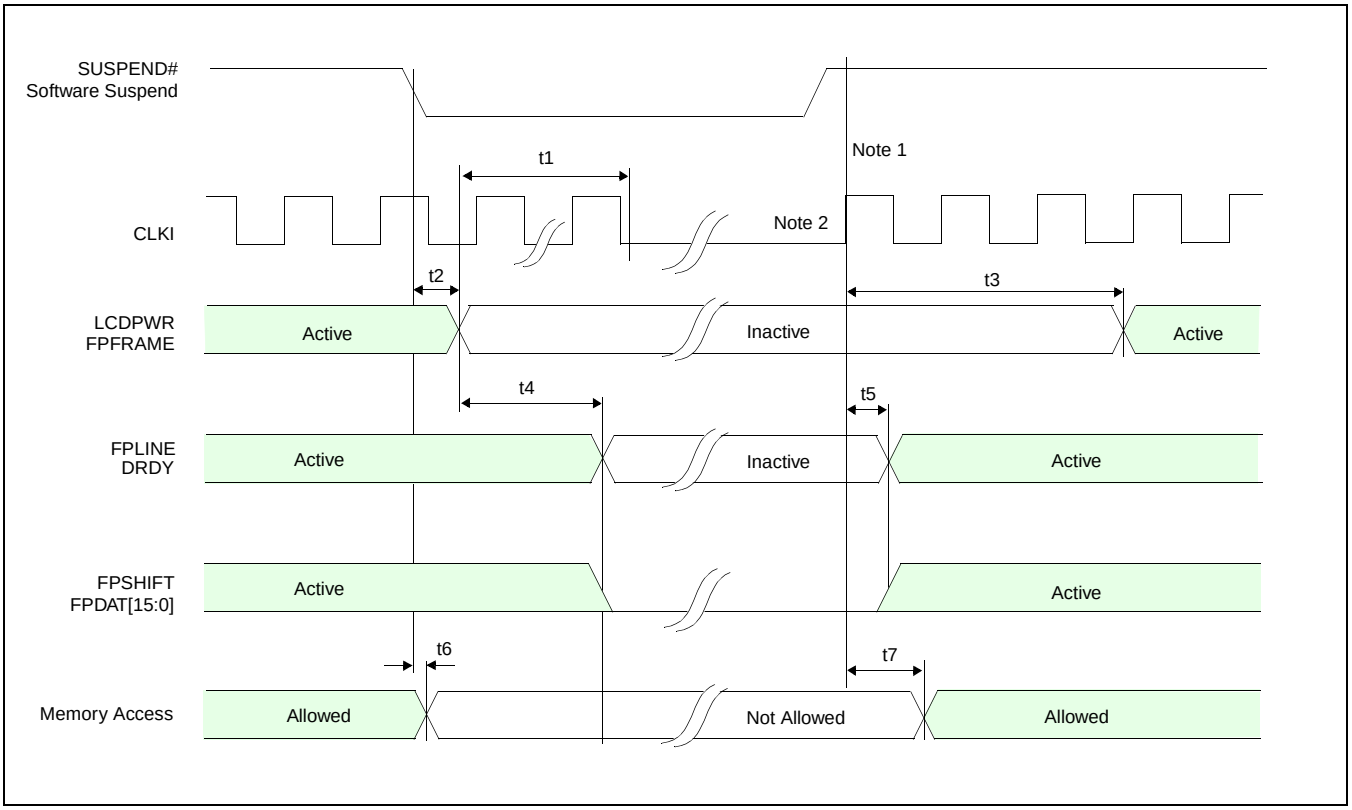


Figure 7-18: LCD Panel Suspend Timing

Table 7-18: LCD Panel Suspend Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	LCDPWR inactive to CLKI inactive	128			Frames
t2	SUSPEND# active to FPFRAME, LCDPWR inactive	0		1	Frames
t3	First CLKI after SUSPEND# inactive to FPFRAME, LCDPWR active			1	Frames
t4	LCDPWR inactive to FPLINE, FPSHIFT, FPDAT[15:0], DRDY active			128	Frames
t5	First CLKI after SUSPEND# inactive to FPLINE, FPSHIFT, FPDAT[15:0], DRDY active	0			Frames
t6	LCDPWR inactive to Memory Access not allowed			8	MCLK
t7	First CLKI after SUSPEND# inactive to Memory Access allowed	0			MCLK

Note

1. t3, t5, and t7 are measured from the first CLKI after SUSPEND# inactive.
2. CLKI may be active throughout SUSPEND# active.
3. Where MCLK is the period of the memory clock.

7.4.3 Single Monochrome 4-Bit Panel Timing

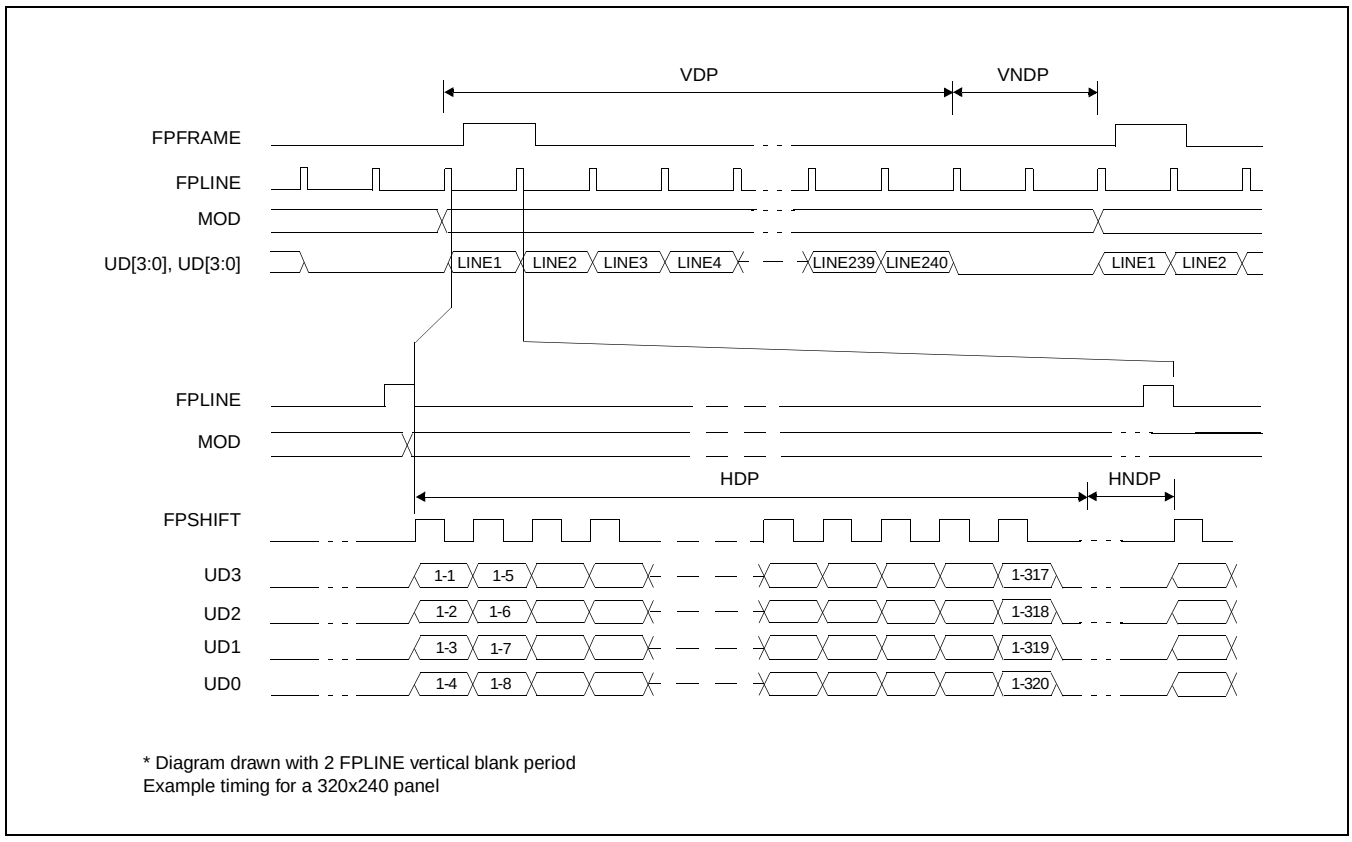


Figure 7-19: Single Monochrome 4-Bit Panel Timing

VDP =	Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP =	Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP =	Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP =	Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1)*8Ts

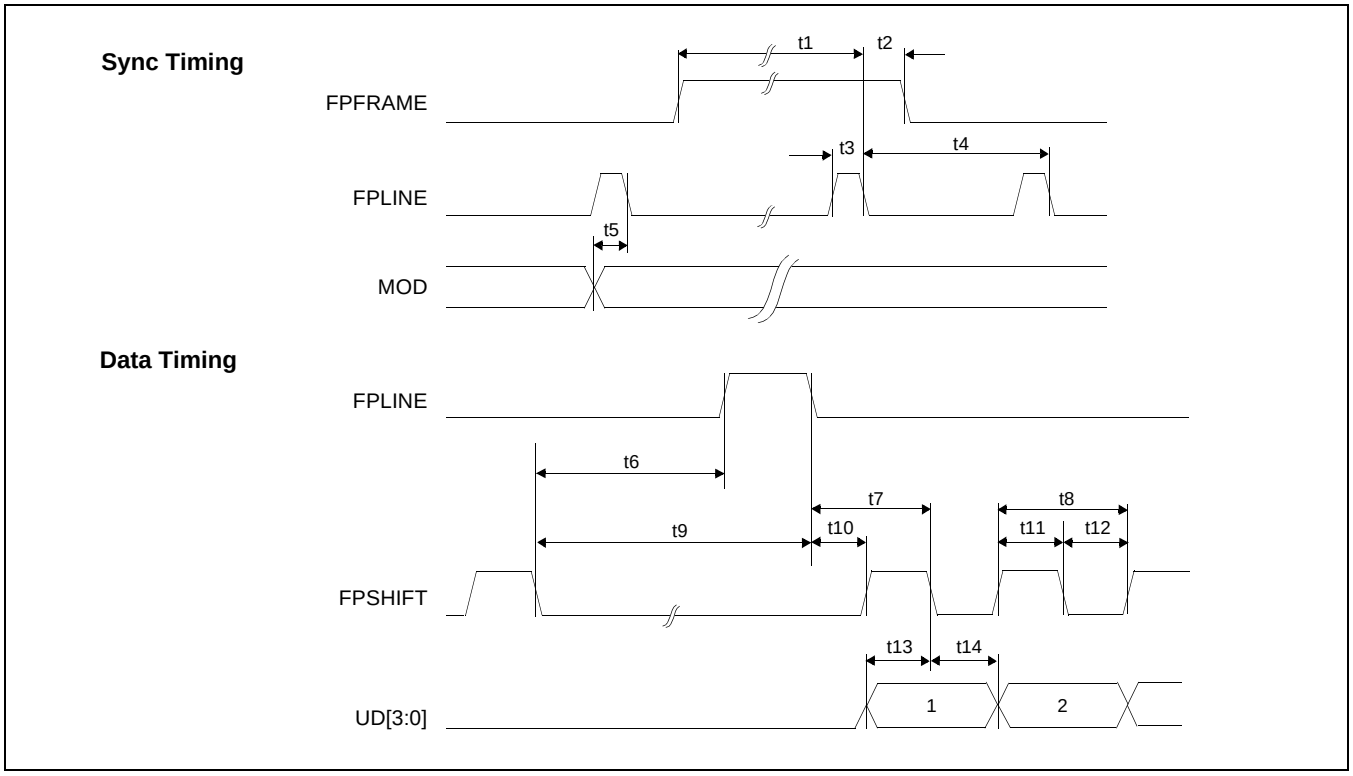


Figure 7-20: Single Monochrome 4-Bit Panel A.C. Timing

Table 7-19: Single Monochrome 4-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			
t2	FPFRAME hold from FPLINE falling edge	9			Ts (note 1)
t3	FPLINE pulse width	9			Ts
t4	FPLINE period	note 3			
t5	MOD transition to FPLINE falling edge	33		note 4	Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 5			
t7	FPLINE falling edge to FPSHIFT falling edge	t14 + 2			Ts
t8	FPSHIFT period	4			Ts
t9	FPSHIFT falling edge to FPLINE falling edge	note 6			
t10	FPLINE falling edge to FPSHIFT rising edge	18			Ts
t11	FPSHIFT pulse width high	2			Ts
t12	FPSHIFT pulse width low	2			Ts
t13	UD[3:0] setup to FPSHIFT falling edge	2			Ts
t14	UD[3:0] hold to FPSHIFT falling edge	2			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t4_{min}$ - 9Ts
3. $t4_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] + 33 Ts
4. $t5_{min}$ = [((REG[04h] bits [6:0]) + 1)*8 - 1] Ts
5. $t6_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 25] Ts
6. $t9_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 16] Ts

7.4.4 Single Monochrome 8-Bit Panel Timing

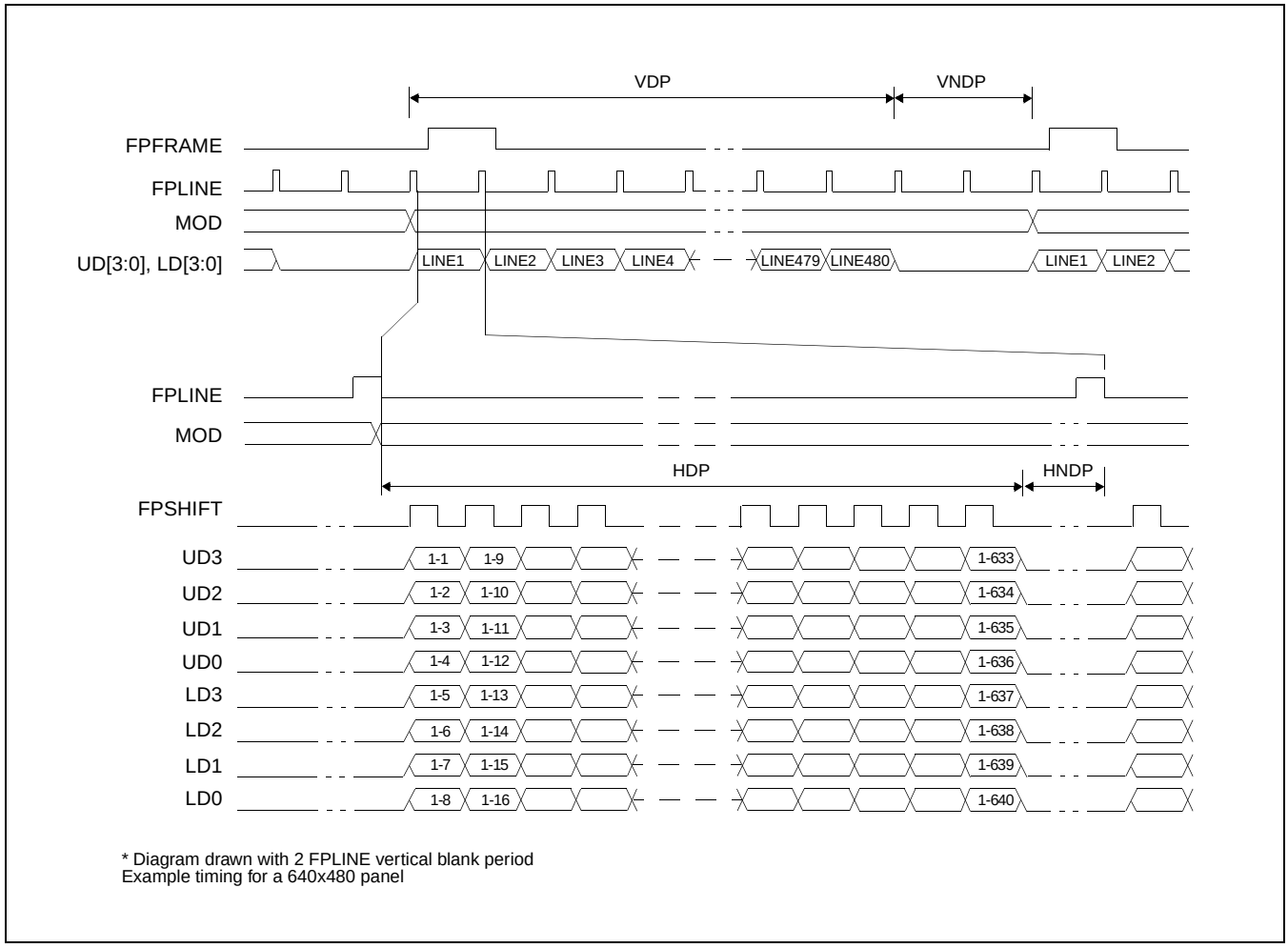


Figure 7-21: Single Monochrome 8-Bit Panel Timing

VDP = Vertical Display Period = (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP = Vertical Non-Display Period = (REG[0Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP = Horizontal Non-Display Period = ((REG[05h] bits [4:0]) + 1)*8Ts

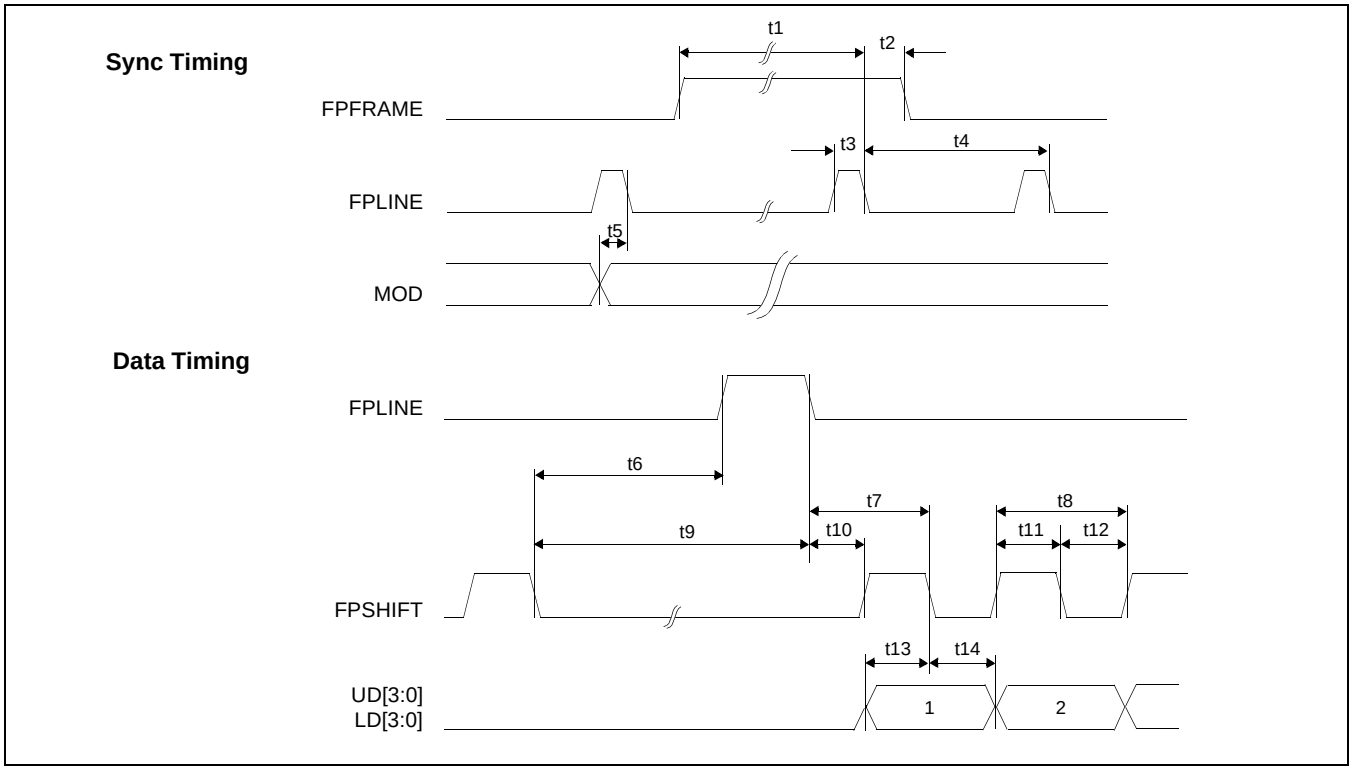


Figure 7-22: Single Monochrome 8-Bit Panel A.C. Timing

Table 7-20: Single Monochrome 8-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			
t2	FPFRAME hold from FPLINE falling edge	9			Ts (note 1)
t3	FPLINE pulse width	9			Ts
t4	FPLINE period	note 3			
t5	MOD transition to FPLINE falling edge	33		note 4	Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 5			
t7	FPLINE falling edge to FPSHIFT falling edge	t14 + 4			Ts
t8	FPSHIFT period	8			Ts
t9	FPSHIFT falling edge to FPLINE falling edge	note 6			
t10	FPLINE falling edge to FPSHIFT rising edge	18			Ts
t11	FPSHIFT pulse width high	4			Ts
t12	FPSHIFT pulse width low	4			Ts
t13	UD[3:0], LD[3:0] setup to FPSHIFT falling edge	4			Ts
t14	UD[3:0], LD[3:0] hold to FPSHIFT falling edge	4			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t4_{min}$ - 9Ts
3. $t4_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] + 33 Ts
4. $t5_{min}$ = [((REG[04h] bits [6:0]) + 1)*8 - 1] Ts
5. $t6_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 23] Ts
6. $t9_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 14] Ts

7.4.5 Single Color 4-Bit Panel Timing

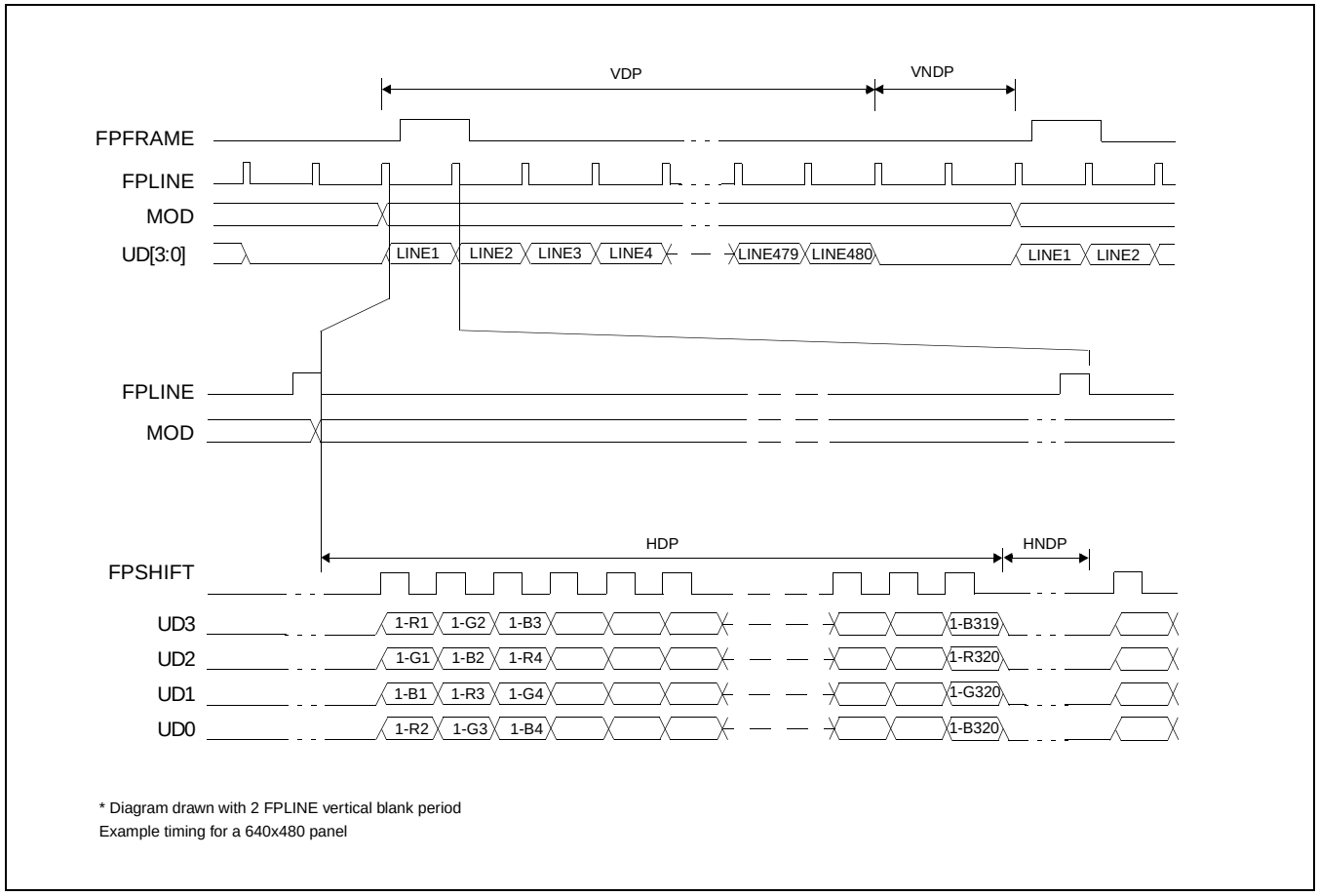


Figure 7-23: Single Color 4-Bit Panel Timing

VDP = Vertical Display Period = (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP = Vertical Non-Display Period = (REG[0Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP = Horizontal Non-Display Period = ((REG[05h] bits [4:0]) + 1)*8Ts

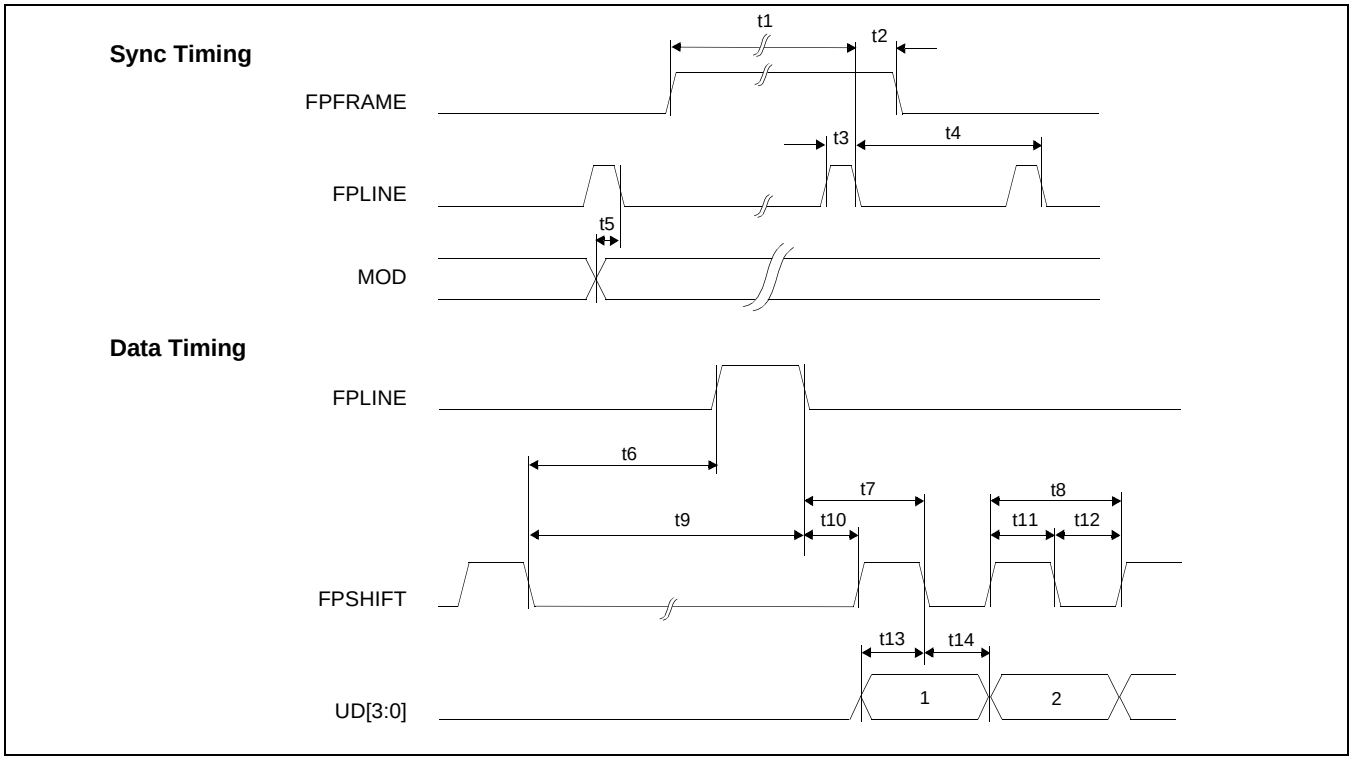


Figure 7-24: Single Color 4-Bit Panel A.C. Timing

Table 7-21: Single Color 4-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			
t2	FPFRAME hold from FPLINE falling edge	9			Ts (note 1)
t3	FPLINE pulse width	9			Ts
t4	FPLINE period	note 3			
t5	MOD transition to FPLINE falling edge	33		note 4	Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 5			
t7	FPLINE falling edge to FPSHIFT falling edge	t14 + 0.5			Ts
t8	FPSHIFT period	1			Ts
t9	FPSHIFT falling edge to FPLINE falling edge	note 6			
t10	FPLINE falling edge to FPSHIFT rising edge	19			Ts
t11	FPSHIFT pulse width high	0.45			Ts
t12	FPSHIFT pulse width low	0.45			Ts
t13	UD[3:0], setup to FPSHIFT falling edge	0.45			Ts
t14	UD[3:0], hold from FPSHIFT falling edge	0.45			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t4_{min}$ - 9Ts
3. $t4_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] + 33 Ts
4. $t5_{min}$ = [((REG[04h] bits [6:0])+1)*8 - 1] Ts
5. $t6_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 26] Ts
6. $t9_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 17] Ts

7.4.6 Single Color 8-Bit Panel Timing (Format 1)

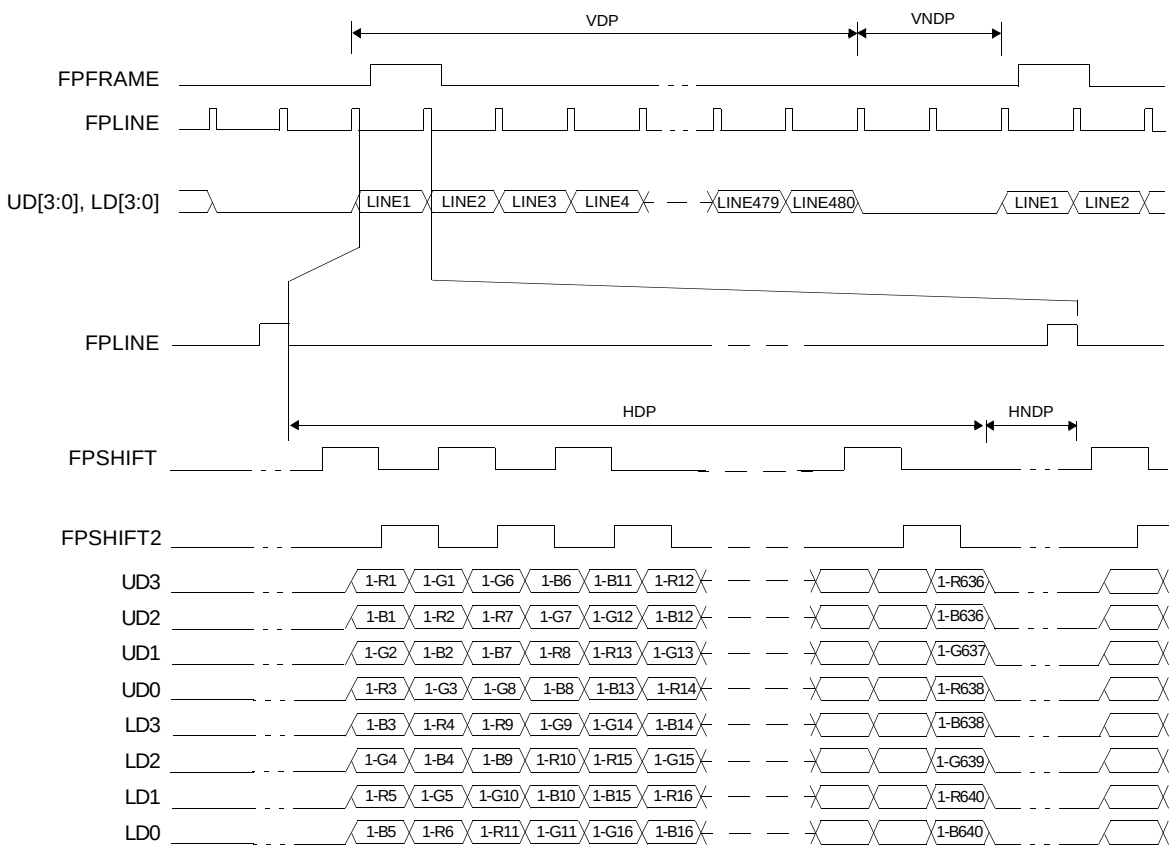


Figure 7-25: Single Color 8-Bit Panel Timing (Format 1)

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1)*8Ts

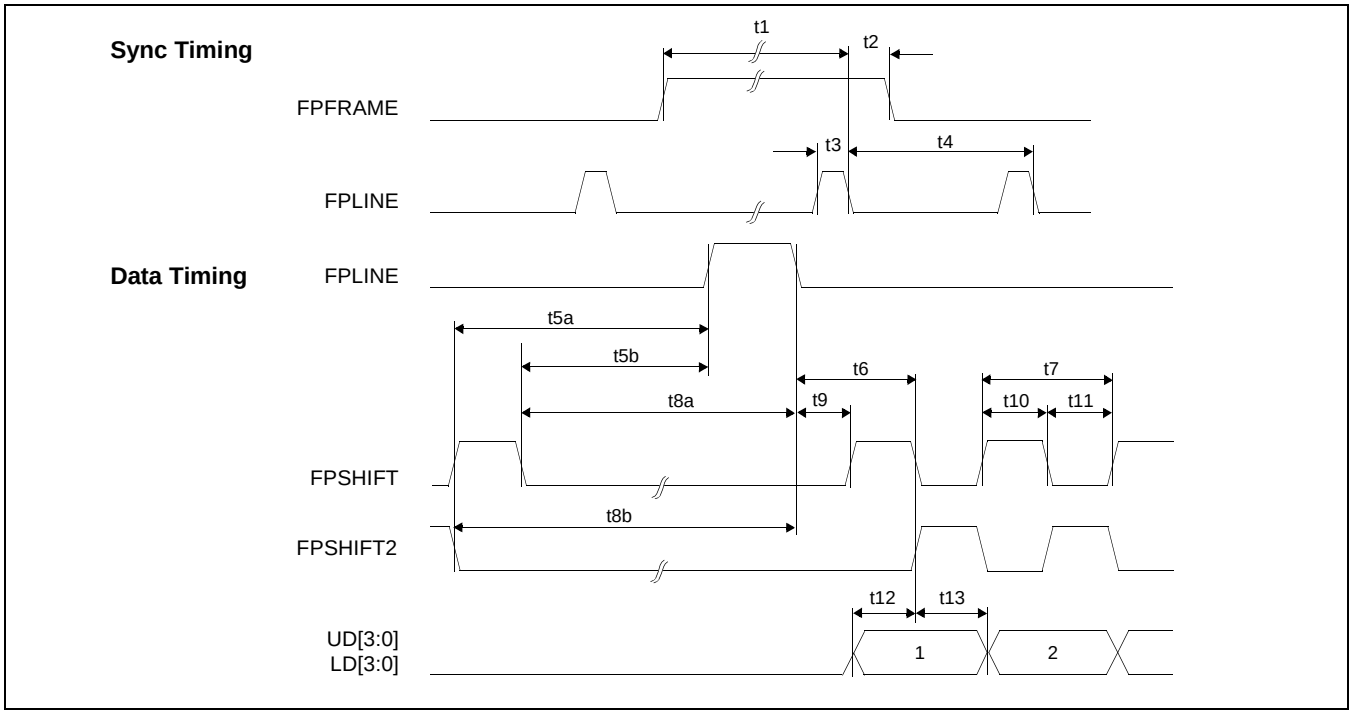


Figure 7-26: Single Color 8-Bit Panel A.C. Timing (Format 1)

Table 7-22: Single Color 8-Bit Panel A.C. Timing (Format 1)

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			
t2	FPFRAME hold from FPLINE falling edge	9			Ts (note 1)
t3	FPLINE pulse width	9			Ts
t4	FPLINE period	note 3			
t5a	FPSHIFT2 falling edge to FPLINE rising edge	note 4			
t5b	FPSHIFT falling edge to FPLINE rising edge	note 5			
t6	FPLINE falling edge to FPSHIFT2 rising, FPSHIFT falling edge	t14 + 2			Ts
t7	FPSHIFT2, FPSHIFT period	4			Ts
t8a	FPSHIFT falling edge to FPLINE falling edge	note 6			
t8b	FPSHIFT2 falling edge to FPLINE falling edge	note 7			
t9	FPLINE falling edge to FPSHIFT rising edge	18			Ts
t10	FPSHIFT2, FPSHIFT pulse width high	2			Ts
t11	FPSHIFT2, FPSHIFT pulse width low	2			Ts
t12	UD[3:0], LD[3:0] setup to FPSHIFT2 rising, FPSHIFT falling edge	1			Ts
t13	UD[3:0], LD[3:0] hold from FPSHIFT2 rising, FPSHIFT falling edge	1			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t4_{min}$ - 9Ts
3. $t4_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] Ts
4. $t5_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 27]+T11 Ts
5. $t5_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 27] Ts
6. $t8_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 18] Ts
7. $t8_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 18]+T11 Ts

7.4.7 Single Color 8-Bit Panel Timing (Format 2)

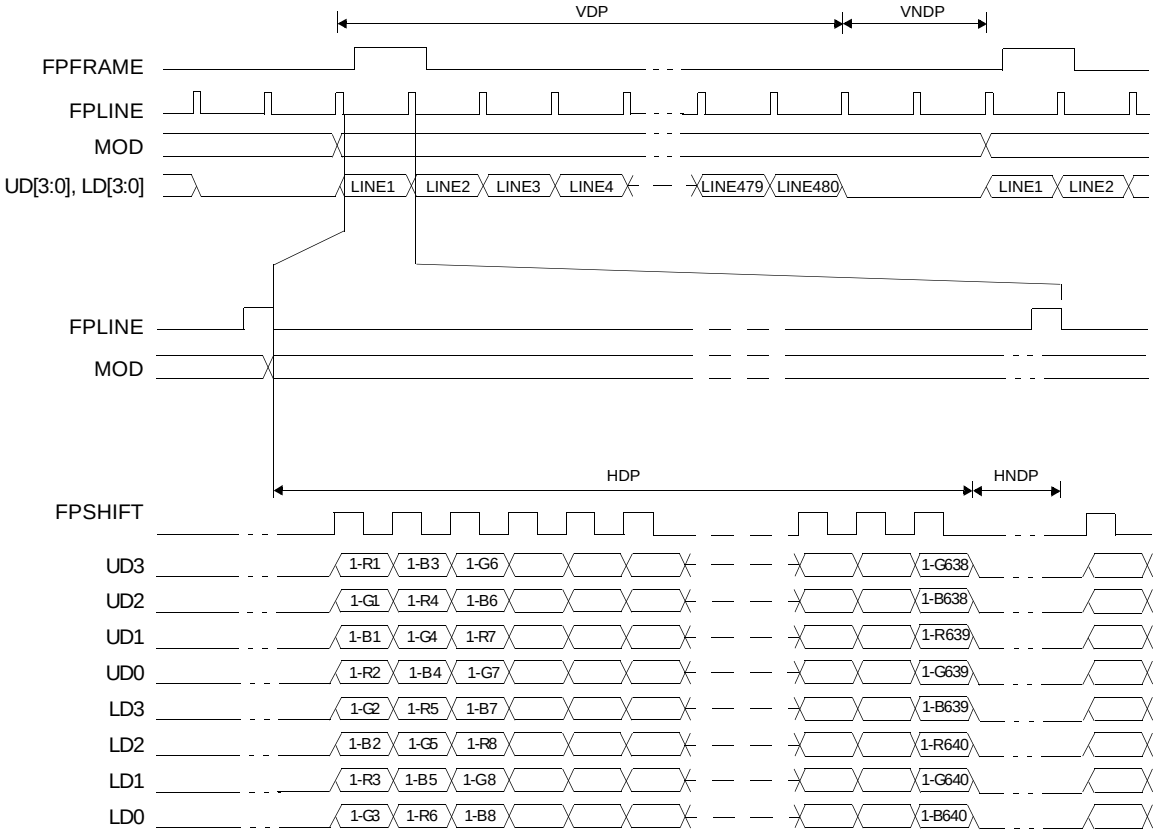


Figure 7-27: Single Color 8-Bit Panel Timing (Format 2)

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1)*8Ts

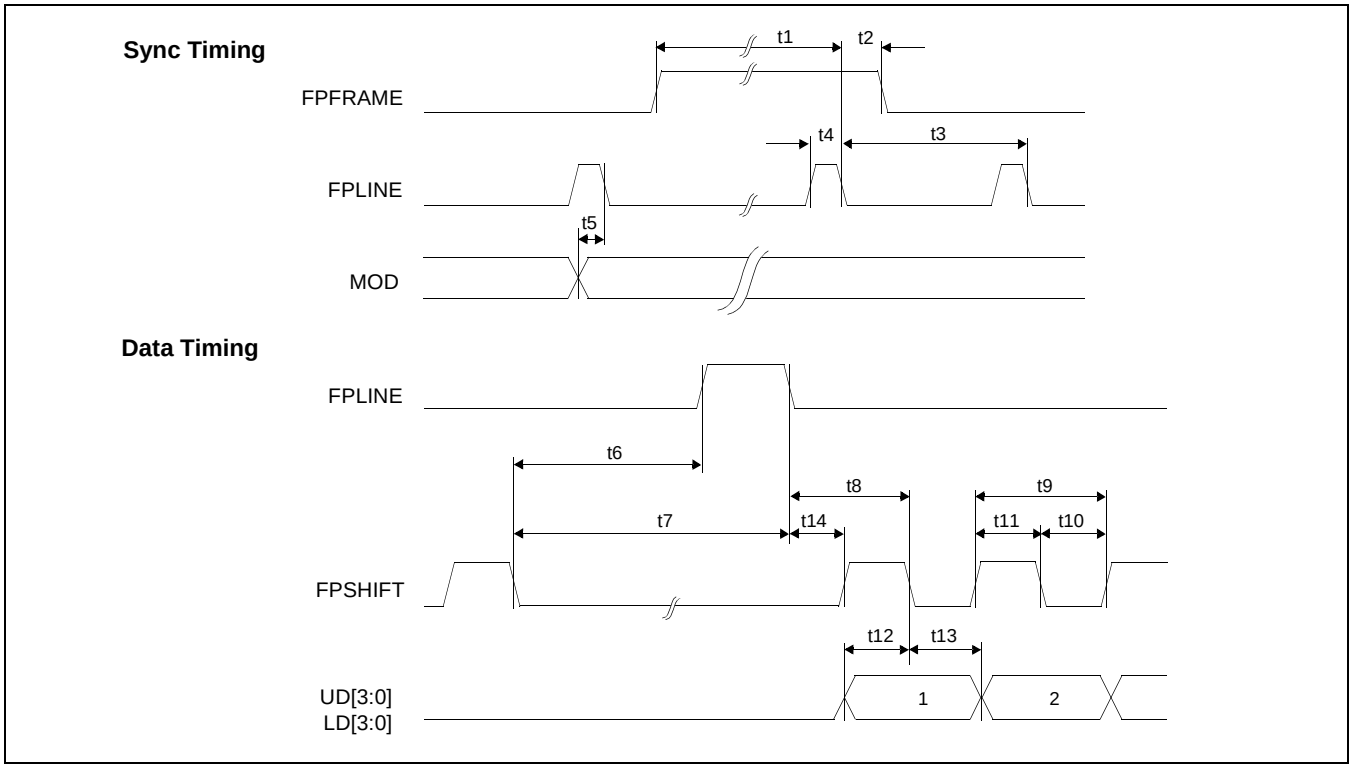


Figure 7-28: Single Color 8-Bit Panel A.C. Timing (Format 2)

Table 7-23: Single Color 8-Bit Panel A.C. Timing (Format 2)

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			
t2	FPFRAME hold from FPLINE falling edge	9			Ts (note 1)
t3	FPLINE period	note 3			
t4	FPLINE pulse width	9			Ts
t5	MOD transition to FPLINE falling edge	33		note 4	Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 5			
t7	FPSHIFT falling edge to FPLINE falling edge	note 6			
t8	FPLINE falling edge to FPSHIFT falling edge	t14 + 2			
t9	FPSHIFT period	2			Ts
t10	FPSHIFT pulse width low	1			Ts
t11	FPSHIFT pulse width high	1			Ts
t12	UD[3:0], LD[3:0] setup to FPSHIFT falling edge	1			Ts
t13	UD[3:0], LD[3:0] hold to FPSHIFT falling edge	1			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	18			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t3_{min}$ - 9Ts
3. $t3_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] + 33 Ts
4. $t5_{min}$ = [((REG[04h] bits [6:0])+1)*8 - 1] Ts
5. $t6_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 26] Ts
6. $t7_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 17] Ts

7.4.8 Single Color 16-Bit Panel Timing

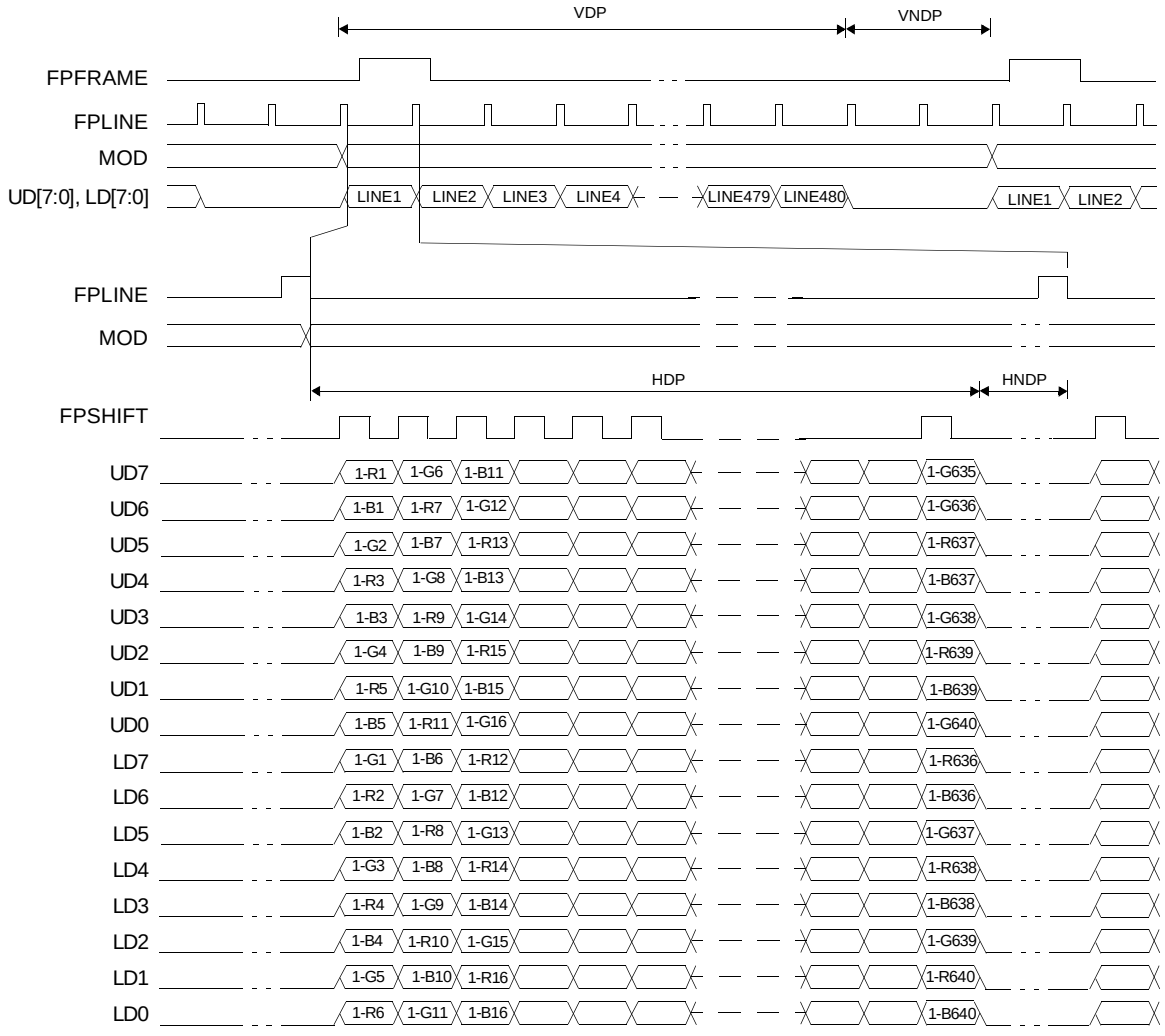


Figure 7-29: Single Color 16-Bit Panel Timing

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1)*8Ts

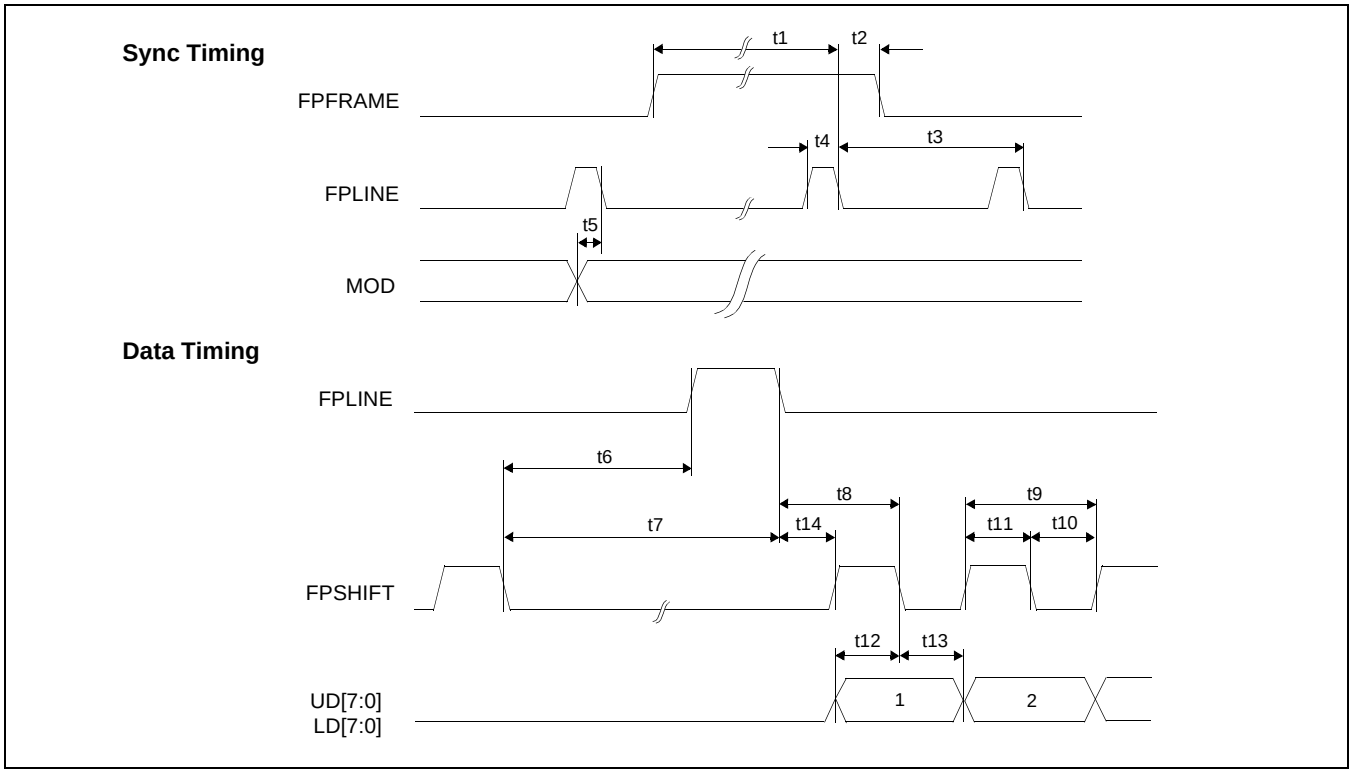


Figure 7-30: Single Color 16-Bit Panel A.C. Timing

Table 7-24: Single Color 16-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			
t2	FPFRAME hold from FPLINE falling edge	9			Ts (note 1)
t3	FPLINE period	note 3			
t4	FPLINE pulse width	9			Ts
t5	MOD transition to FPLINE falling edge	33		note 4	Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 5			
t7	FPSHIFT falling edge to FPLINE falling edge	note 6			
t8	FPLINE falling edge to FPSHIFT falling edge	t14 + 3			Ts
t9	FPSHIFT period	5			Ts
t10	FPSHIFT pulse width low	2			Ts
t11	FPSHIFT pulse width high	2			Ts
t12	UD[7:0], LD[7:0] setup to FPSHIFT falling edge	2			Ts
t13	UD[7:0], LD[7:0] hold to FPSHIFT falling edge	2			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	18			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t3_{min}$ - 9Ts
3. $t3_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] + 33 Ts
4. $t5_{min}$ = [((REG[04h] bits [6:0])+1)*8 - 1] Ts
5. $t6_{min}$ = [(REG[05h] bits [4:0]) + 1)*8 - 25] Ts
6. $t7_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 16] Ts

7.4.9 Dual Monochrome 8-Bit Panel Timing

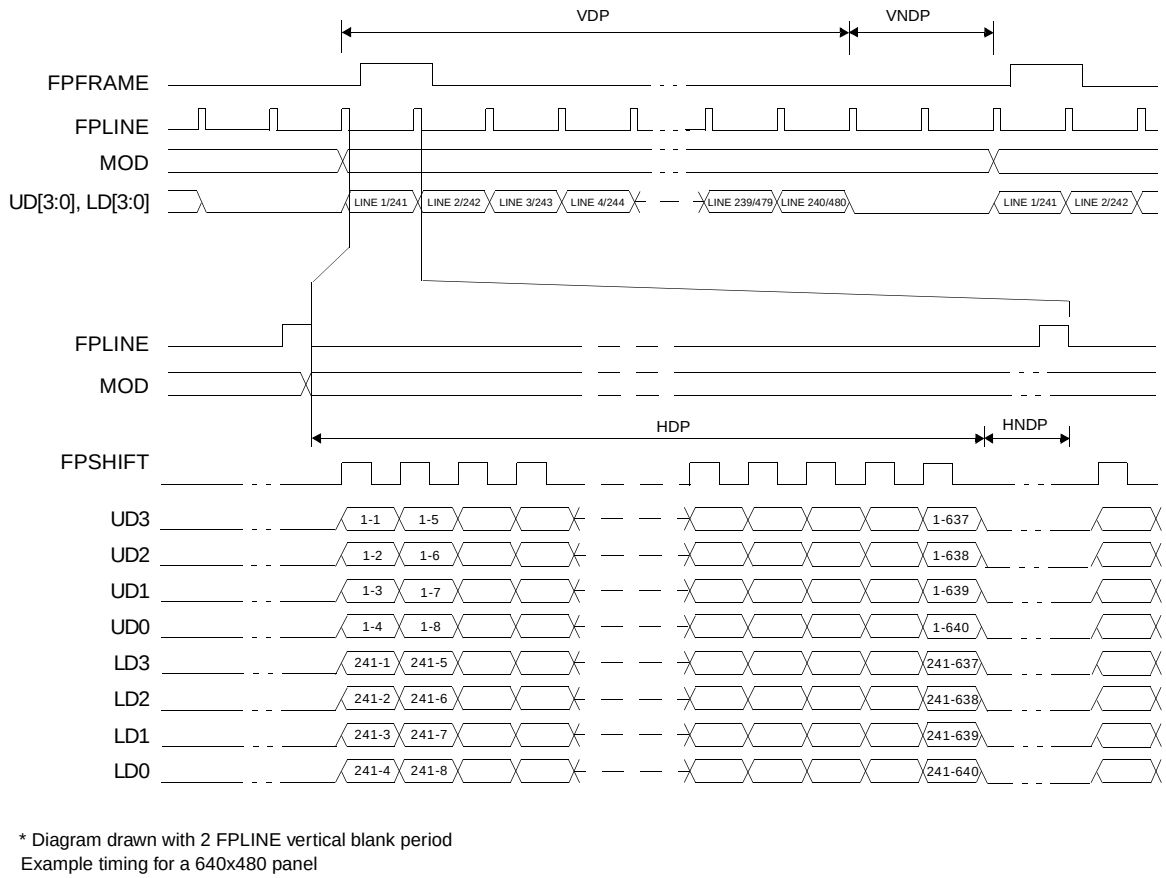


Figure 7-31: Dual Monochrome 8-Bit Panel Timing

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1)*8Ts

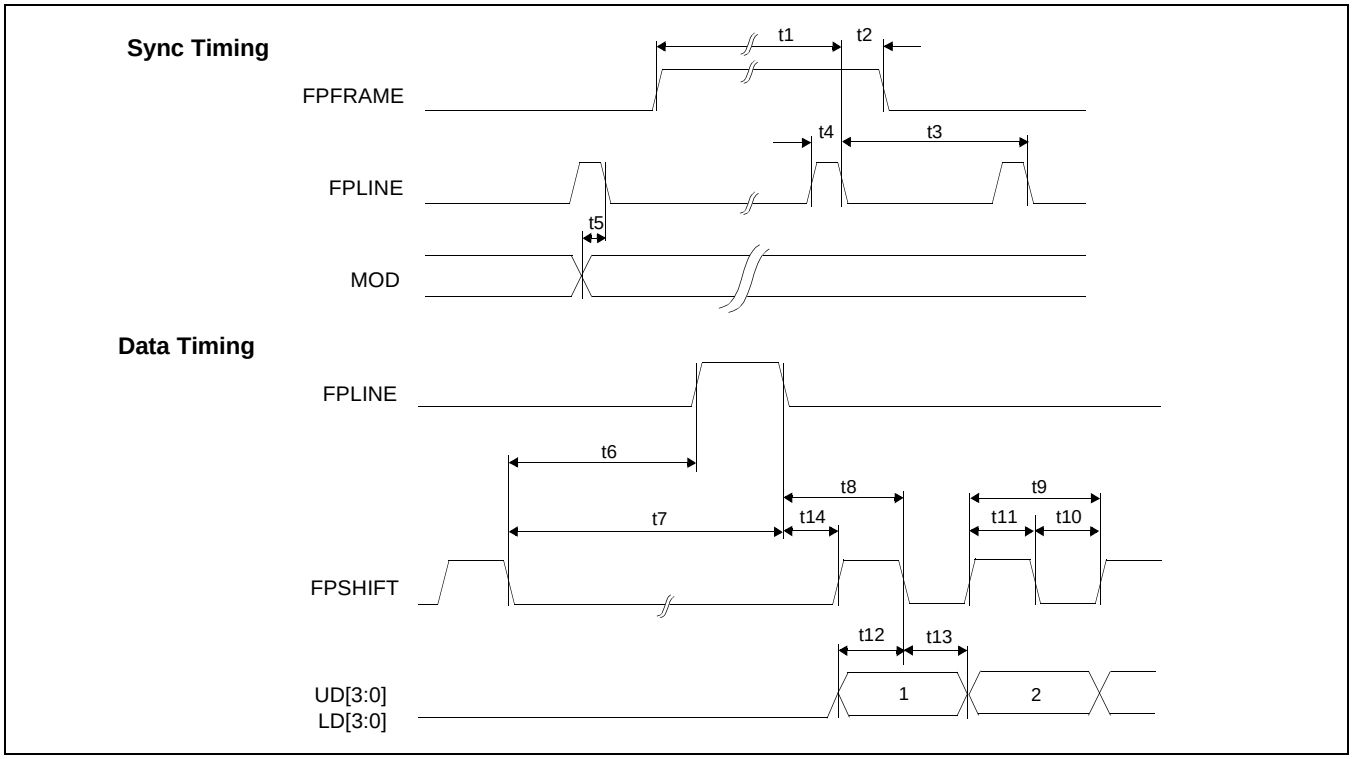


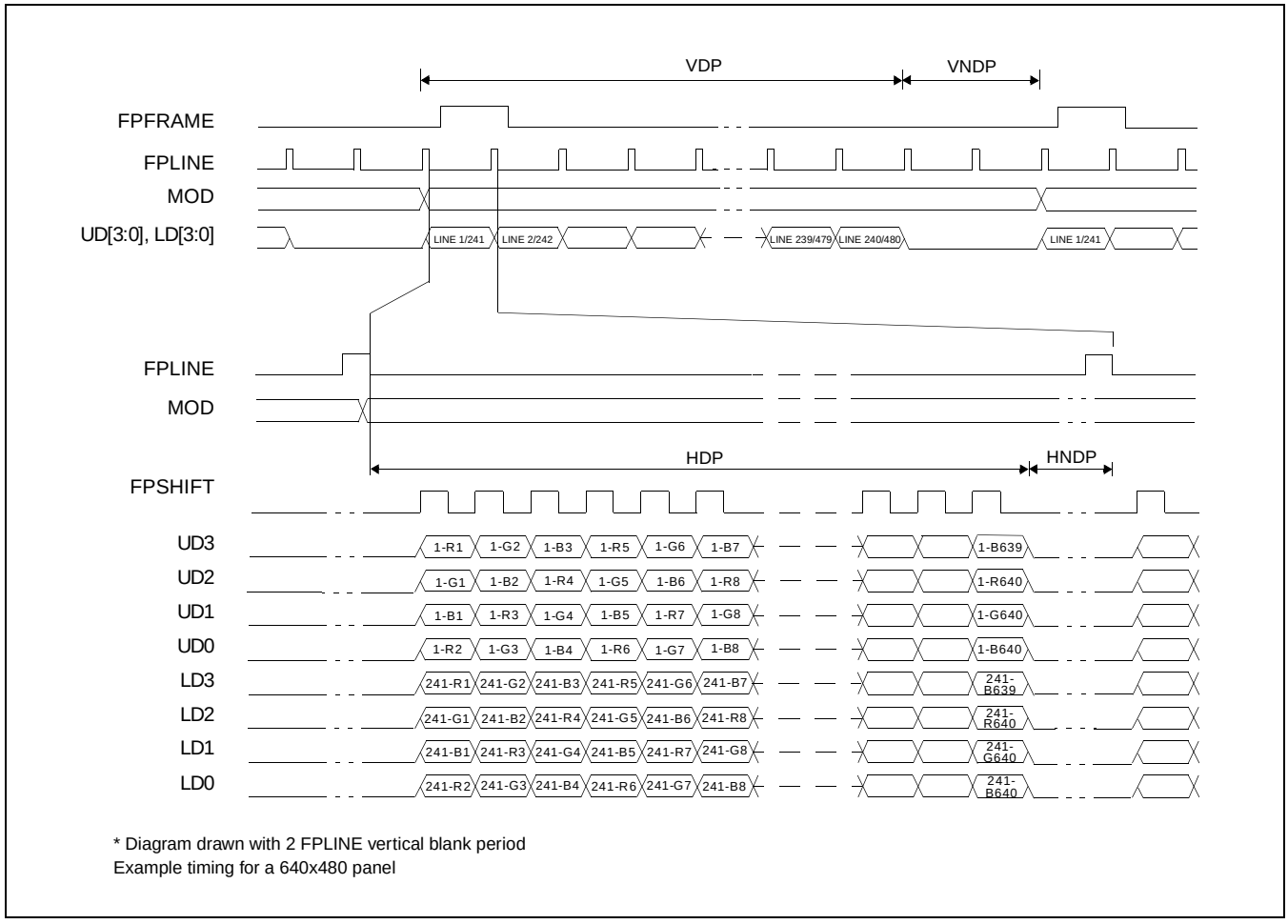
Figure 7-32: Dual Monochrome 8-Bit Panel A.C. Timing

Table 7-25: Dual Monochrome 8-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			
t2	FPFRAME hold from FPLINE falling edge	9			Ts (note 1)
t3	FPLINE period	note 3			
t4	FPLINE pulse width	9			Ts
t5	MOD transition to FPLINE falling edge	33		note 4	Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 5			
t7	FPSHIFT falling edge to FPLINE falling edge	note 6			
t8	FPLINE falling edge to FPSHIFT falling edge	t14 + 2			Ts
t9	FPSHIFT period	4			Ts
t10	FPSHIFT pulse width low	2			Ts
t11	FPSHIFT pulse width high	2			Ts
t12	UD[3:0], LD[3:0] setup to FPSHIFT falling edge	2			Ts
t13	UD[3:0], LD[3:0] hold to FPSHIFT falling edge	2			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	10			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t3_{min}$ - 9Ts
3. $t3_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] + 33 Ts
4. $t5_{min}$ = [((REG[04h] bits [6:0])+1)*8 - 1] Ts
5. $t6_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 17] Ts
6. $t7_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 8] Ts

7.4.10 Dual Color 8-Bit Panel Timing



* Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 640x480 panel

Figure 7-33: Dual Color 8-Bit Panel Timing

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1)*8Ts

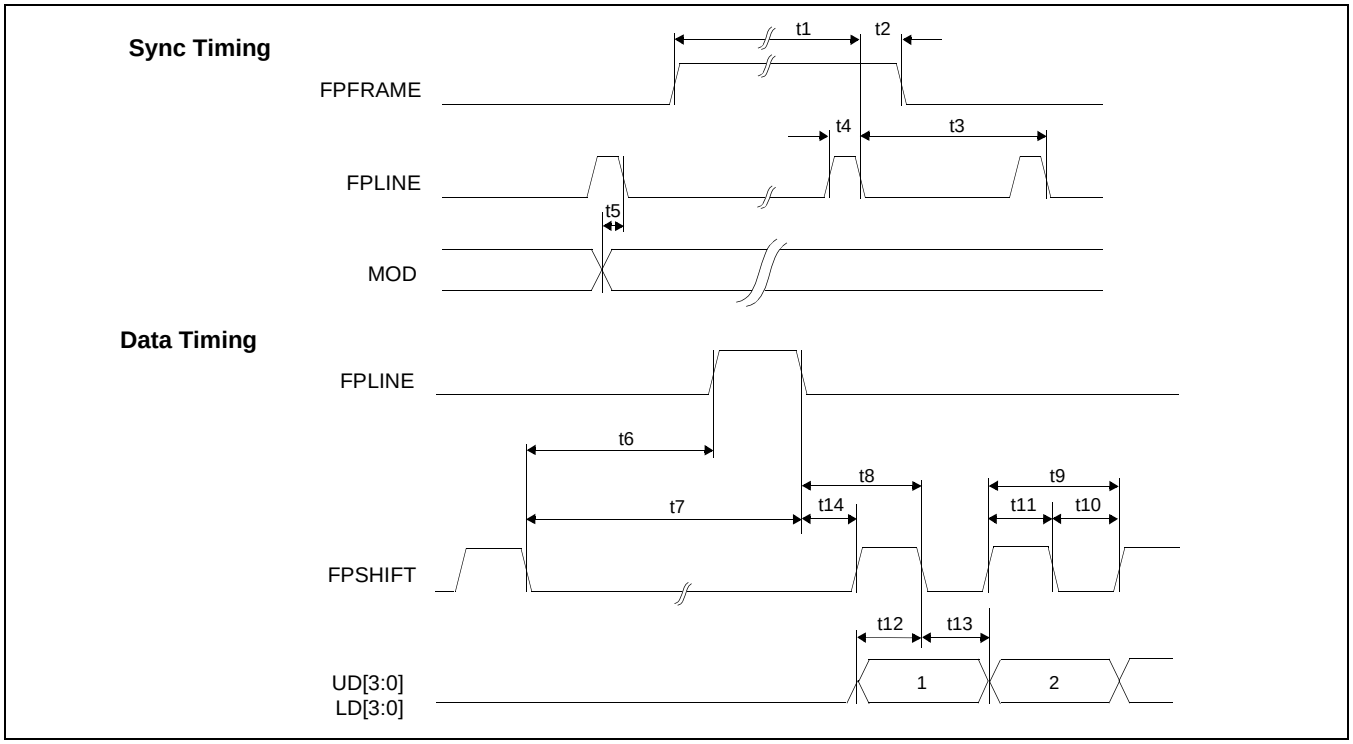


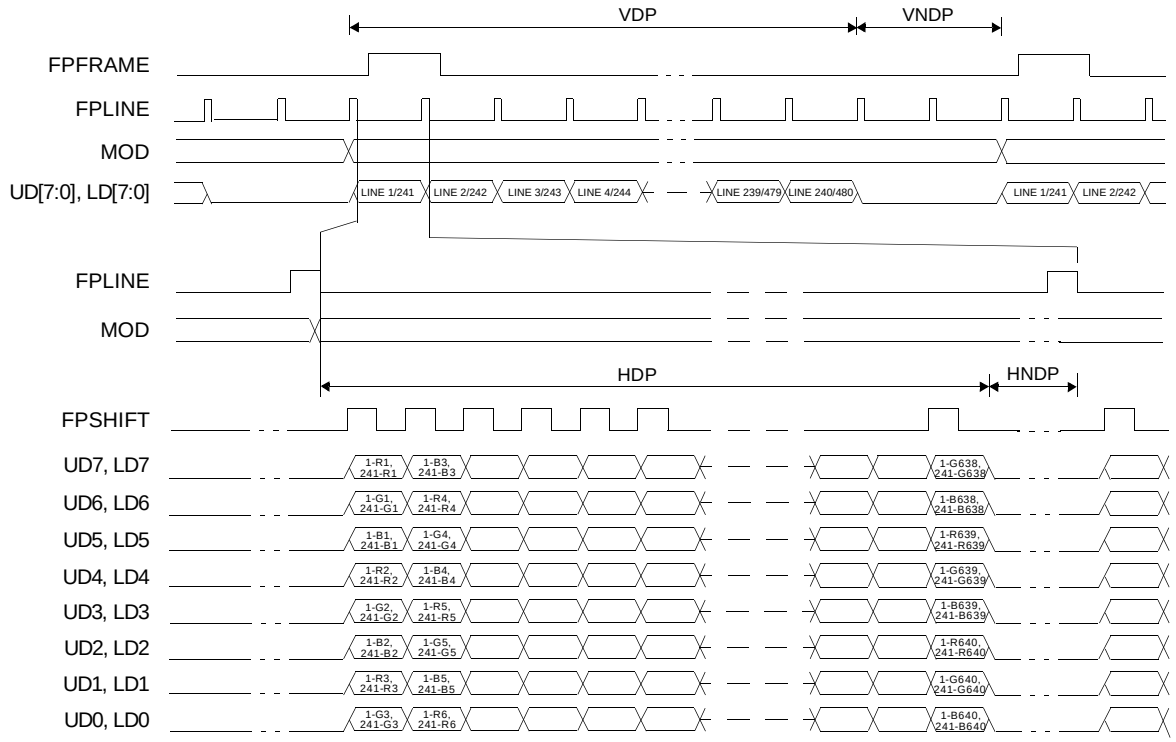
Figure 7-34: Dual Color 8-Bit Panel A.C. Timing

Table 7-26: Dual Color 8-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			
t2	FPFRAME hold from FPLINE falling edge	9			Ts (note 1)
t3	FPLINE period	note 3			
t4	FPLINE pulse width	9			Ts
t5	MOD transition to FPLINE falling edge	33		note 4	Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 5			
t7	FPSHIFT falling edge to FPLINE falling edge	note 6			
t8	FPLINE falling edge to FPSHIFT falling edge	t14 + 1			Ts
t9	FPSHIFT period	1			Ts
t10	FPSHIFT pulse width low	0.45			Ts
t11	FPSHIFT pulse width high	0.45			Ts
t12	UD[3:0], LD[3:0] setup to FPSHIFT falling edge	0.45			Ts
t13	UD[3:0], LD[3:0] hold to FPSHIFT falling edge	0.45			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	11			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t3_{min}$ - 9Ts
3. $t3_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] + 33 Ts
4. $t5_{min}$ = [((REG[04h] bits [6:0])+1)*8 - 1] Ts
5. $t6_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 18] Ts
6. $t7_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 9] Ts

7.4.11 Dual Color 16-Bit Panel Timing



* Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 640x480 panel

Figure 7-35: Dual Color 16-Bit Panel Timing

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1)*8Ts

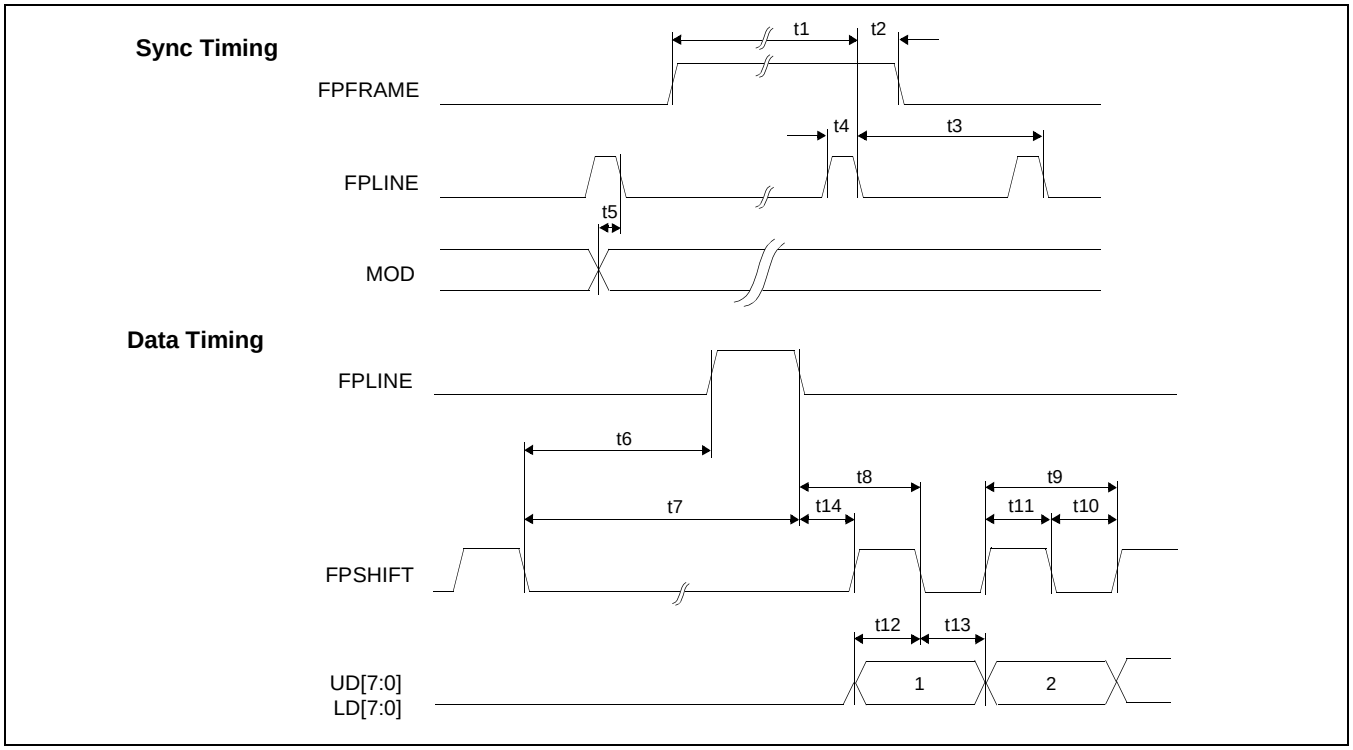


Figure 7-36: Dual Color 16-Bit Panel A.C. Timing

Table 7-27: Dual Color 16-Bit Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE falling edge	note 2			
t2	FPFRAME hold from FPLINE falling edge	9			Ts (note 1)
t3	FPLINE period	note 3			
t4	FPLINE pulse width	9			Ts
t5	MOD transition to FPLINE falling edge	33		note 4	Ts
t6	FPSHIFT falling edge to FPLINE rising edge	note 5			
t7	FPSHIFT falling edge to FPLINE falling edge	note 6			
t8	FPLINE falling edge to FPSHIFT falling edge	t14 + 2			
t9	FPSHIFT period	2			Ts
t10	FPSHIFT pulse width low	1			Ts
t11	FPSHIFT pulse width high	1			Ts
t12	UD[7:0], LD[7:0] setup to FPSHIFT falling edge	1			Ts
t13	UD[7:0], LD[7:0] hold to FPSHIFT falling edge	1			Ts
t14	FPLINE falling edge to FPSHIFT rising edge	10			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t3_{min}$ - 9Ts
3. $t3_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] + 33 Ts
4. $t5_{min}$ = [((REG[04h] bits [6:0])+1)*8 - 1] Ts
5. $t6_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 18] Ts
6. $t7_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 9] Ts

7.4.12 16-Bit TFT Panel Timing

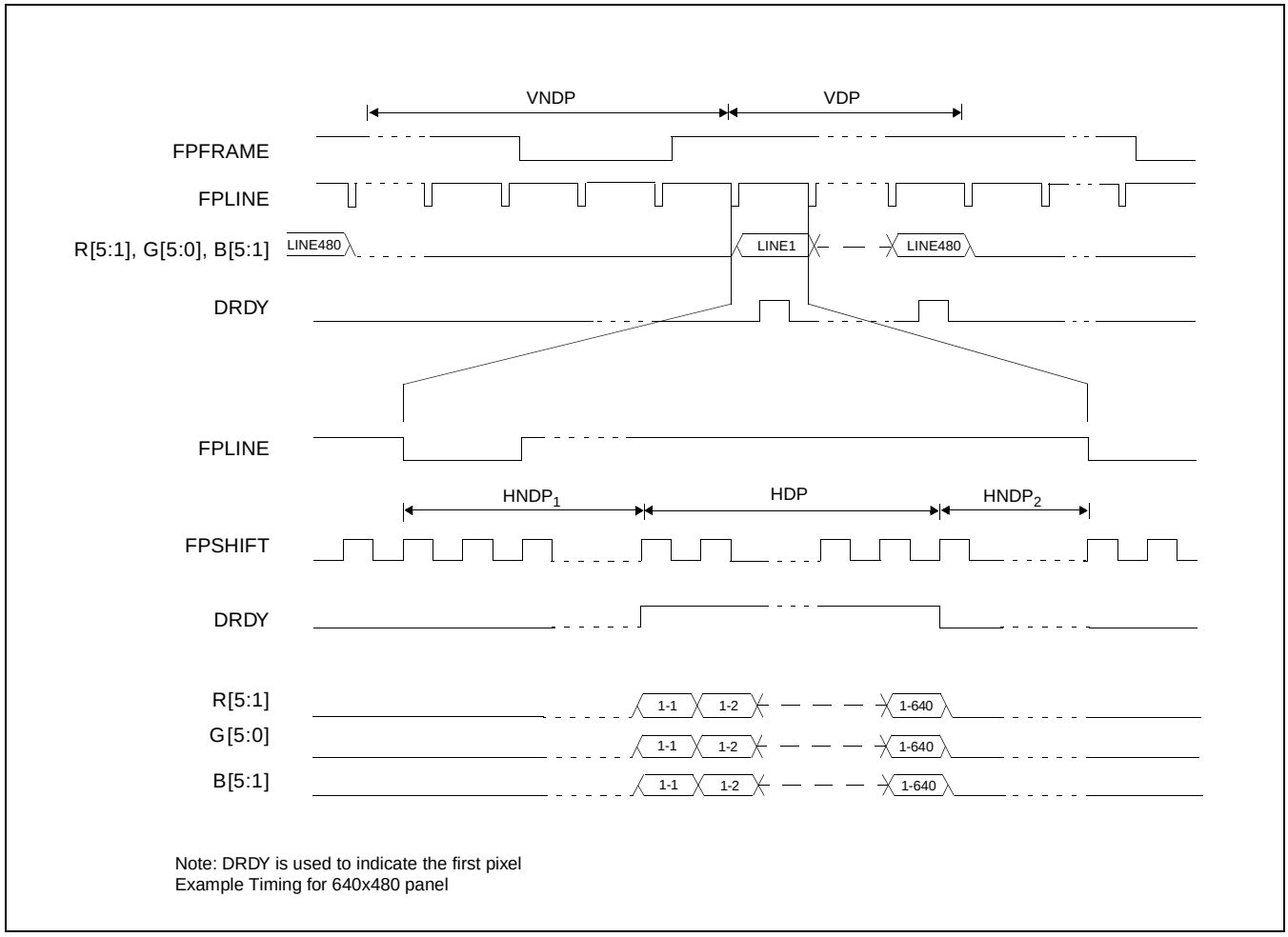


Figure 7-37: 16-Bit TFT Panel Timing

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= $HNDP_1 + HNDP_2$ = ((REG[05h] bits [4:0]) + 1)*8Ts

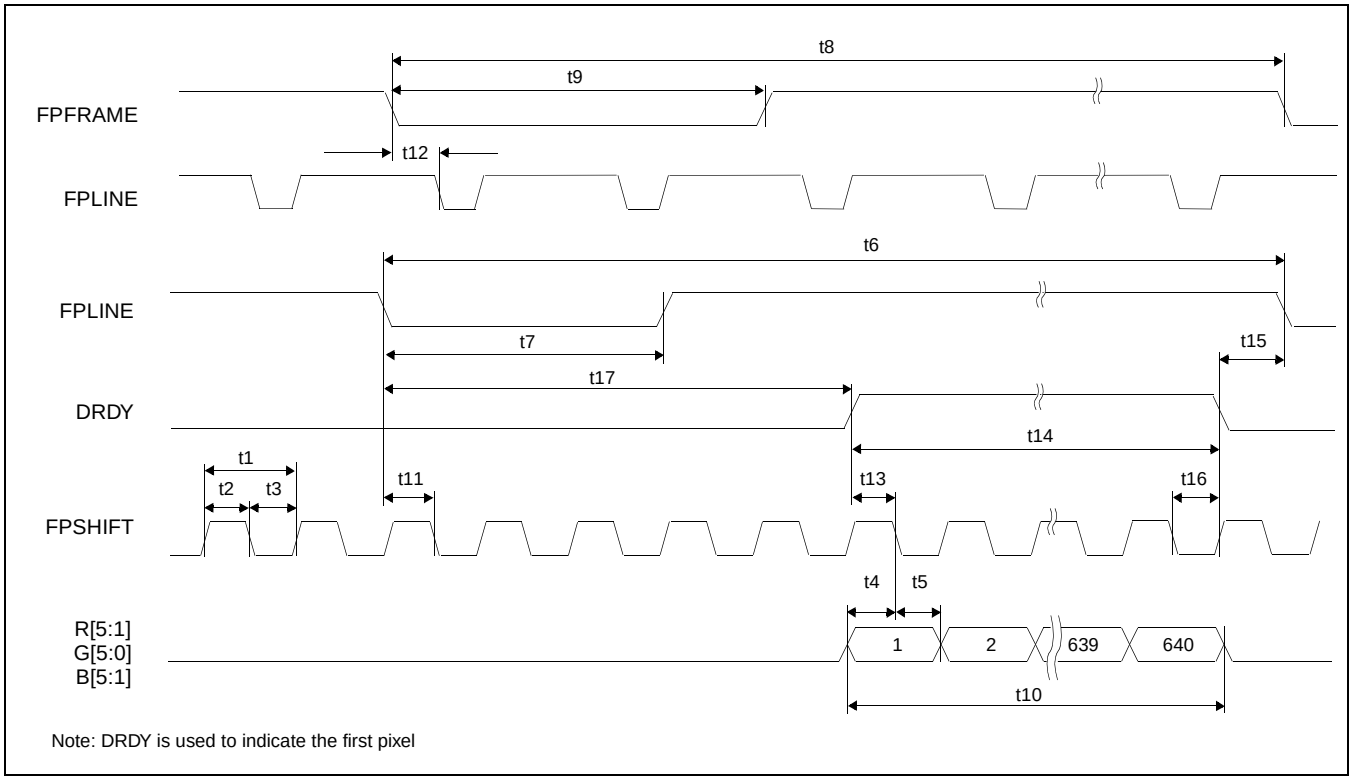


Figure 7-38: TFT A.C. Timing

Table 7-28: TFT A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPSHIFT period	1			Ts (note 1)
t2	FPSHIFT pulse width high	0.45			Ts
t3	FPSHIFT pulse width low	0.45			Ts
t4	data setup to FPSHIFT falling edge	0.45			Ts
t5	data hold from FPSHIFT falling edge	0.45			Ts
t6	FPLINE cycle time	note 2			
t7	FPLINE pulse width low	note 3			
t8	FPFRAME cycle time	note 4			
t9	FPFRAME pulse width low	note 5			
t10	horizontal display period	note 6			
t11	FPLINE setup to FPSHIFT falling edge	0.45			Ts
t12	FPFRAME falling edge to FPLINE falling edge phase difference	note 7			
t13	DRDY to FPSHIFT falling edge setup time	0.45			Ts
t14	DRDY pulse width	note 8			
t15	DRDY falling edge to FPLINE falling edge	note 9			
t16	DRDY hold from FPSHIFT falling edge	0.45			Ts
t17	FPLINE Falling edge to DRDY active	note 10		250	Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t6_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0])+1)*8] Ts
3. $t7_{min}$ = [((REG[07h] bits [3:0])+1)*8] Ts
4. $t8_{min}$ = [((REG[09h] bits [1:0], REG[08h] bits [7:0])+1) + ((REG[0Ah] bits [5:0])+1)] lines
5. $t9_{min}$ = [((REG[0Ch] bits [2:0])+1)] lines
6. $t10_{min}$ = [((REG[04h] bits [6:0])+1)*8] Ts
7. $t12_{min}$ = [((REG[06h] bits [4:0])+1)*8] Ts
8. $t14_{min}$ = [((REG[04h] bits [6:0])+1)*8] Ts
9. $t15_{min}$ = [((REG[06h] bits [4:0])+1)*8 - 2] Ts
10. $t17_{min}$ = [((REG[05h] bits [4:0])+1)*8 - ((REG[06h] bits [4:0])+1)*8 + 2]

7.4.13 CRT Timing

Example Timing for 640x480 CRT

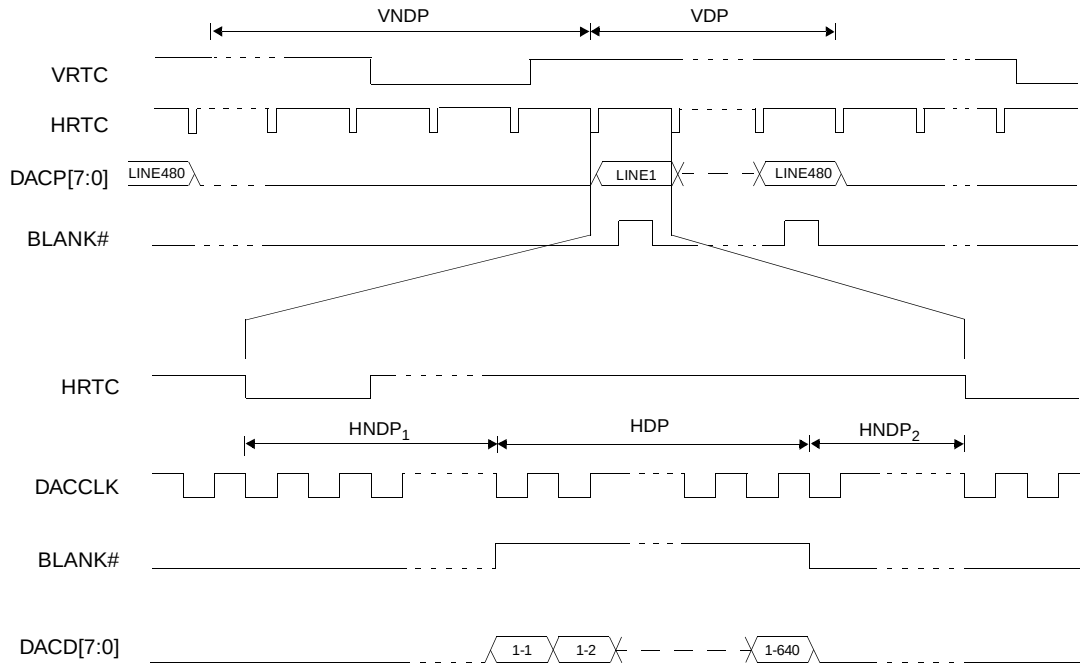


Figure 7-39: CRT Timing

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= $HNDP_1$ + $HNDP_2$ = ((REG[05h] bits [4:0]) + 1)*8Ts

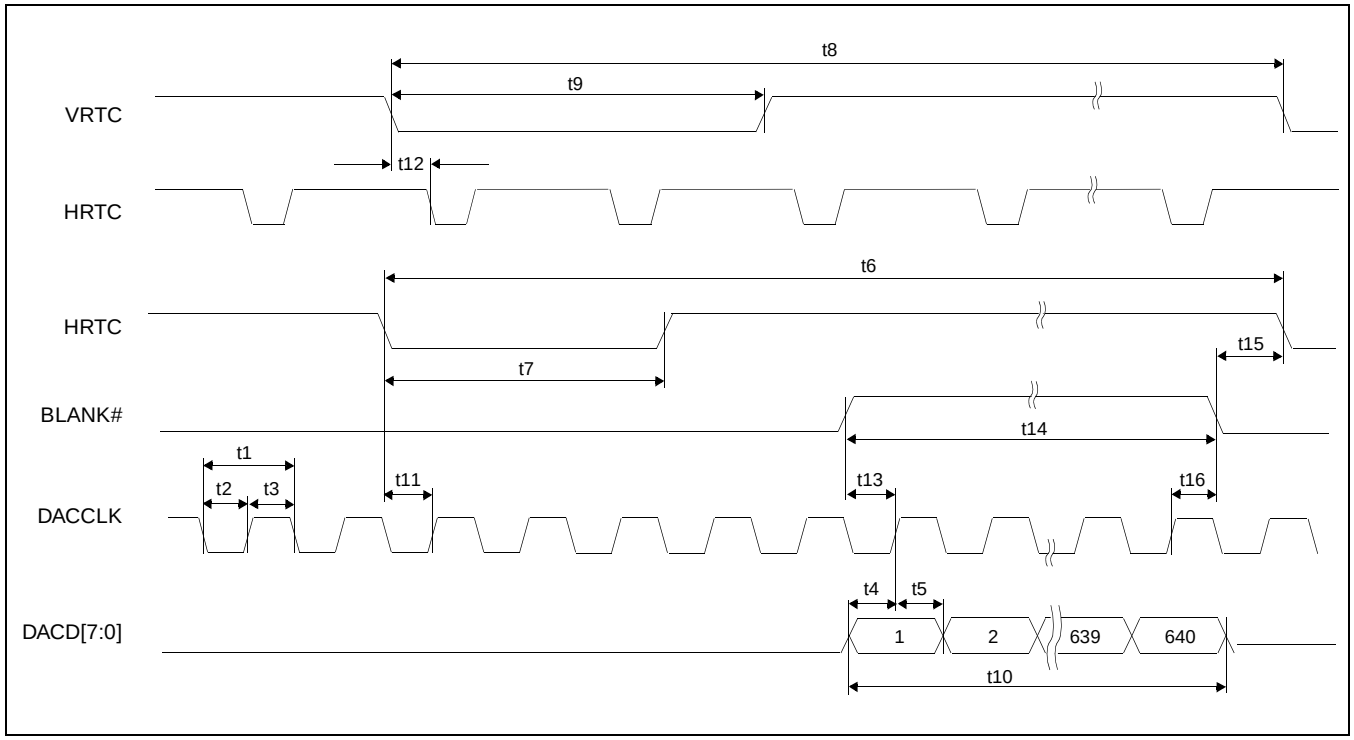


Figure 7-40: CRT A.C. Timing

Table 7-29: CRT A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	DACCLK period	1			Ts (note 1)
t2	DACCLK pulse width high	0.45			Ts
t3	DACCLK pulse width low	0.45			Ts
t4	data setup to DACCLK rising edge	0.45			Ts
t5	data hold from DACCLK rising edge	0.45			Ts
t6	HRTC cycle time	note 2			
t7	HRTC pulse width (shown active low)	note 3			
t8	VRTC cycle time	note 4			
t9	VRTC pulse width (shown active low)	note 5			
t10	horizontal display period	note 6			
t11	HRTC setup to DACCLK rising edge	0.45			Ts
t12	VRTC falling edge to FPLINE falling edge phase difference	note 7			
t13	BLANK# to DACCLK rising edge setup time	0.45			Ts
t14	BLANK# pulse width	note 8			
t15	BLANK# falling edge to HRTC falling edge	note 9			
t16	BLANK# hold from DACCLK rising edge	0.45			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t6_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0])+1)*8] Ts
3. $t7_{min}$ = [((REG[07h] bits [3:0])+1)*8] Ts
4. $t8_{min}$ = [((REG[09h] bits [1:0], REG[08h] bits [7:0])+1) + ((REG[0Ah] bits [6:0])+1)] lines
5. $t9_{min}$ = [((REG[0Ch] bits [2:0])+1)] lines
6. $t10_{min}$ = [((REG[04h] bits [6:0])+1)*8] Ts
7. $t12_{min}$ = [((REG[06h] bits [4:0])+1)*8] Ts
8. $t14_{min}$ = [((REG[04h] bits [6:0])+1)*8] Ts
9. $t15_{min}$ = [((REG[06h] bits [4:0])+1)*8 - 2] Ts

7.4.14 External RAMDAC Read / Write Timing

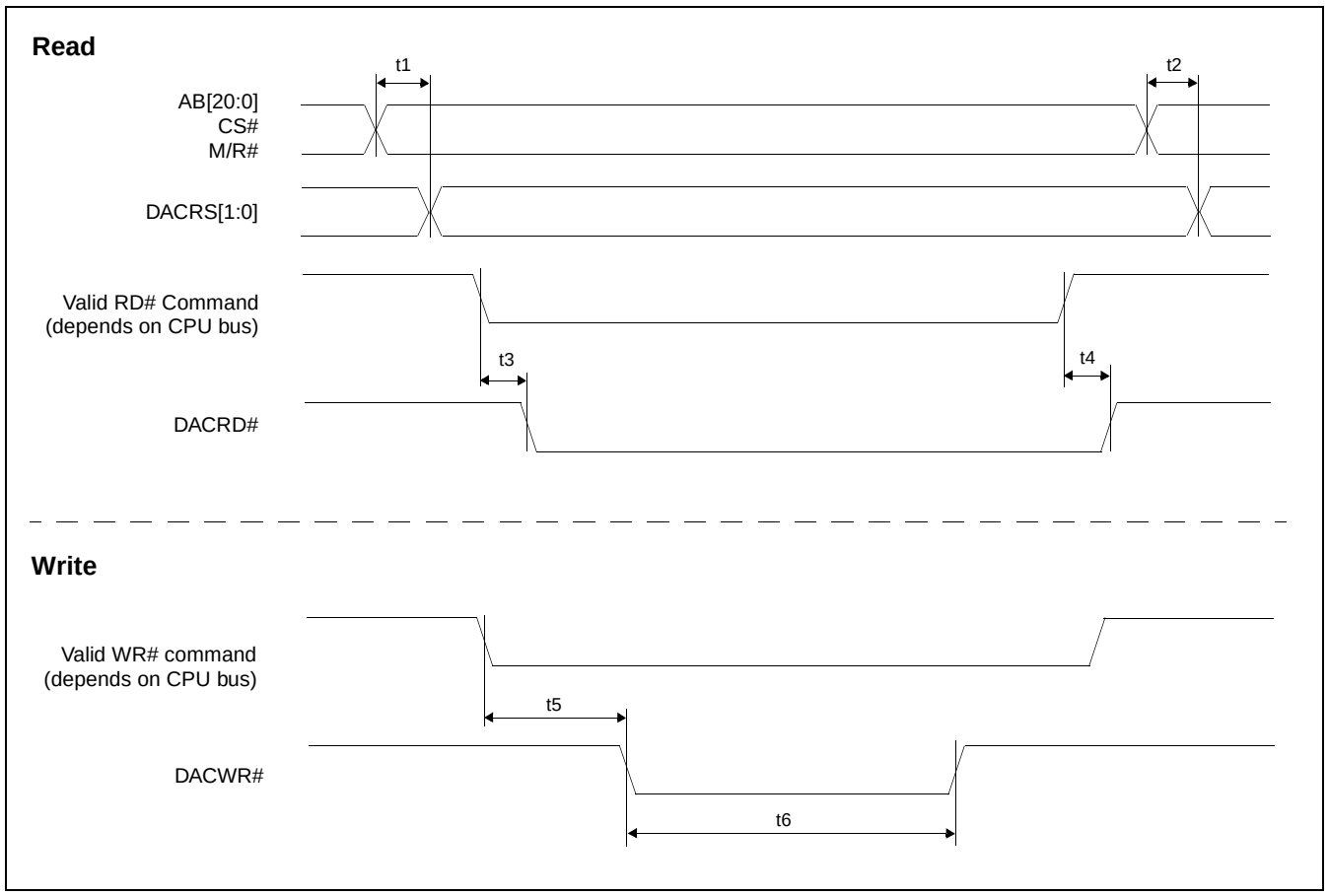


Figure 7-41: Generic Bus RAMDAC Read / Write Timing

Table 7-30: Generic Bus RAMDAC Read / Write Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{BCLK}	Bus clock period	30			ns
t1	AB[20:0], CS#, M/R# delay to DACRS[1:0]			10	ns
t2	DACRS[1:0] hold from AB[20:0], CS#, M/R# negated			10	ns
t3	Valid RD# command to DACRS[1:0] delay	8		33	ns
t4	DACRD# hold from valid RD# command negated	3		14	ns
t5	Valid WR# command to DACWR# delay	2 T_{BCLK}			ns
t6	DACWR# pulse width low	2.45 T_{BCLK}		2.55 T_{BCLK}	ns

8 Registers

8.1 Register Mapping

The S1D13504 registers are all memory mapped. The system must provide the external address decoding through the CS# and M/R# input pins. When CS# = 0 and M/R# = 0, the registers are mapped by address bits AB[5:0], e.g. REG[00h] is mapped to AB[5:0] = 000000, REG[01h] is mapped to AB[5:0] = 000001. See the table below:

Table 8-1: S1D13504 Addressing

CS#	M/R#	Access
0	0	Register access: • REG[00h] is addressed when AB[5:0] = 0 • REG[01h] is addressed when AB[5:0] = 1 • REG[n] is addressed when AB[5:0] = n
0	1	Memory access: the 2M byte display buffer is addressed by AB[20:0]
1	X	S1D13504 not selected

8.2 Register Descriptions

Note

Unless specified otherwise, all register bits are reset to 0 during power up. Reserved bits should be written 0 when programming unless otherwise noted.

8.2.1 Revision Code Register

Revision Code Register REG[00h]							RO
Product Code Bit 5	Product Code Bit 4	Product Code Bit 3	Product Code Bit 2	Product Code Bit 1	Product Code Bit 0	Revision Code Bit 1	Revision Code Bit 0

bits 7-2 Product Code Bits [5:0]
This is a read-only register that indicates the product code of the chip. The product code is 000001.

bits 1-0 Revision Code Bits [1:0]
This is a read-only register that indicates the revision code of the chip. The revision code is 00.

8.2.2 Memory Configuration Registers

Memory Configuration Register REG[01h]							RW
n/a	Refresh Rate Bit 2	Refresh Rate Bit 1	Refresh Rate Bit 0	n/a	WE# Control	n/a	Memory Type

bits 6-4 DRAM Refresh Rate Select Bits [2:0]
These bits specify the amount of divide from the input clock (CLKI) to generate the DRAM refresh clock rate, which is equal to $2^{(ValueOfTheseBits + 6)}$.

Table 8-2: DRAM Refresh Rate Selection

Refresh Rate Bits [2:0]	CLKI Divide Amount	Refresh Rate for 33MHz CLKI	DRAM Refresh Time/256 Cycles
000	64	520 kHz	0.5 ms
001	128	260 kHz	1 ms
010	256	130 kHz	2 ms
011	512	65 kHz	4 ms
100	1024	33 kHz	8 ms
101	2048	16 kHz	16 ms
110	4096	8 kHz	32 ms
111	8192	4 kHz	64 ms

bit 2 WE# Control
When this bit = 1, 2-WE# DRAM is selected. When this bit = 0 2-CAS# DRAM is selected.

bit 0 Memory Type
When this bit = 1, FPM-DRAM is selected. When this bit = 0, EDO-DRAM is selected.
This bit should be changed only when there are no read/write DRAM cycles. This condition occurs when both the Display FIFO is disabled (REG[23h] bit 7 = 1) and the Half Frame Buffer is disabled (REG[1Bh] bit 0 = 1). For programming information, see *S1D13504 Programming Notes and Examples*, document number X19A-G-002-xx.

8.2.3 Panel/Monitor Configuration Registers

Panel Type Register REG[02h]							RW
n/a	n/a	Panel Data Width Bit 1	Panel Data Width Bit 0	Panel Data Format Select	Color/Mono Panel Select	Dual/Single Panel Select	TFT/Passive LCD Panel Select

bits 5-4 Panel Data Width Bits [1:0]
These bits select passive LCD/TFT panel data width size.

Table 8-3: Panel Data Width Selection

Panel Data Width Bits [1:0]	Passive LCD Panel Data Width Size	TFT Panel Data Width Size
00	4-bit	9-bit
01	8-bit	12-bit
10	16-bit	16-bit
11	Reserved	Reserved

bit 3 Panel Data Format Select
When this bit = 1, 8-bit single color passive LCD panel data format 2 is selected. This bit must be set to 0 for all other LCD panel formats.

bit 2 Color/Mono Panel Select
When this bit = 1, color passive LCD panel is selected. When this bit = 0, monochrome passive LCD panel is selected.

bit 1 Dual/Single Panel Select
When this bit = 1, dual passive LCD panel is selected. When this bit = 0, single passive LCD panel is selected.
Setting this bit for single panel mode should be done only when the Half Frame Buffer is idle. The Half Frame Buffer is idle during vertical non-display periods or while in suspend mode. For programming information, see *S1D13504 Programming Notes and Examples*, document number X19A-G-002-xx.

bit 0 TFT/Passive LCD Panel Select
When this bit = 1, TFT panel is selected. When this bit = 0, passive LCD panel is selected.

MOD Rate Register REG[03h]							RW
n/a	n/a	MOD Rate Bit 5	MOD Rate Bit 4	MOD Rate Bit 3	MOD Rate Bit 2	MOD Rate Bit 1	MOD Rate Bit 0

bits 5-0 MOD Rate Bits [5:0]
For a non-zero value these bits specify the number of FPLINE between toggles of the MOD output signal. When these bits are all 0's the MOD output signal toggles every FPFRAME. These bits are for passive LCD panels only.

Horizontal Display Width Register
REG[04h] RW

n/a	Horizontal Display Width Bit 6	Horizontal Display Width Bit 5	Horizontal Display Width Bit 4	Horizontal Display Width Bit 3	Horizontal Display Width Bit 2	Horizontal Display Width Bit 1	Horizontal Display Width Bit 0

bits 6-0 Horizontal Display Width Bits [6:0]
These bits specify the LCD panel and/or the CRT horizontal display width as follows.

Contents of this Register = (Horizontal Display Width ÷ 8) - 1

For passive LCD panels the Horizontal Display Width must be divisible by 16, and for TFT LCD panels/CRTs the Horizontal Display Width must be divisible by 8. The maximum horizontal display width is 1024 pixels.

Note
This register must be programmed such that REG[04h] ≥ 3 (32 pixels)

Horizontal Non-Display Period Register
REG[05h] RW

n/a	n/a	n/a	Horizontal Non-Display Period Bit 4	Horizontal Non-Display Period Bit 3	Horizontal Non-Display Period Bit 2	Horizontal Non-Display Period Bit 1	Horizontal Non-Display Period Bit 0

bits 4-0 Horizontal Non-Display Period Bits [4:0]
These bits specify the horizontal non-display period width in 8-pixel resolution as follows.

Contents of this Register = (Horizontal Non-Display Period ÷ 8) - 1

The minimum value which should be programmed into this register is 3 (32 pixels). The maximum value which can be programmed into this register is 1F, which gives a horizontal non-display period width of 256 pixels.

Note
This register must be programmed such that
REG[05h] ≥ 3 and (REG[05h] + 1) ≥ (REG[06h] + 1) + (REG[07h] bits [3:0] + 1)

HRTC/FPLINE Start Position Register
REG[06h] RW

n/a	n/a	n/a	HRTC/ FPLINE Start Position Bit 4	HRTC/ FPLINE Start Position Bit 3	HRTC/ FPLINE Start Position Bit 2	HRTC/ FPLINE Start Position Bit 1	HRTC/ FPLINE Start Position Bit 0

bits 4-0 HRTC/FPLINE Start Position Bits [4:0]
For CRTs and TFTs, these bits specify the delay from the start of the horizontal non-display period to the leading edge of the HRTC pulse and FPLINE pulse respectively.

Contents of this Register = (HRTC/FPLINE Start Position ÷ 8) - 1

The maximum HRTC start delay is 256 pixels.

Note
This register must be programmed such that
(REG[05h] + 1) ≥ (REG[06h] + 1) + (REG[07h] bits [3:0] + 1)

HRTC/FPLINE Pulse Width Register REG[07h]							RW
HRTC Polarity Select	FPLINE Polarity Select	n/a	n/a	HRTC/ FPLINE Pulse Width Bit 3	HRTC/ FPLINE Pulse Width Bit 2	HRTC/ FPLINE Pulse Width Bit 1	HRTC/ FPLINE Pulse Width Bit 0

bit 7 HRTC Polarity Select

For CRTs, this bit selects the polarity of the HRTC. When this bit = 1, the HRTC pulse is active high. When this bit = 0, the HRTC pulse is active low.

bit 6 FPLINE Polarity Select

This bit selects the polarity of the FPLINE for TFT and passive LCD. When this bit = 1, the FPLINE pulse is active high for TFT and active low for passive LCD. When this bit = 0, the FPLINE pulse is active low for TFT and active high for passive LCD.

Table 8-4: FPLINE Polarity Selection

FPLINE Polarity Select	Passive LCD FPLINE Polarity	TFT FPLINE Polarity
0	active high	active low
1	active low	active high

bits 3-0 HRTC/FPLINE Pulse Width Bits [3:0]

For CRTs and TFTs, these bits specify the pulse width of HRTC and FPLINE respectively. For passive LCDs, FPLINE is automatically created and these bits have no effect.

HRTC/FPLINE pulse width (pixels) = (HRTC/FPLINE Pulse Width Bits [3:0] + 1) × 8.

The maximum HRTC pulse width is 128 pixels.

Note

This register must be programmed such that
(REG[05h] + 1) ≥ (REG[06h] + 1) + (REG[07h] bits [3:0] + 1)

Vertical Display Height Register 0 REG[08h]							RW
Vertical Display Height Bit 7	Vertical Display Height Bit 6	Vertical Display Height Bit 5	Vertical Display Height Bit 4	Vertical Display Height Bit 3	Vertical Display Height Bit 2	Vertical Display Height Bit 1	Vertical Display Height Bit 0

Vertical Display Height Register 1 REG[09h]							RW
n/a	n/a	n/a	n/a	n/a	n/a	Vertical Display Height Bit 9	Vertical Display Height Bit 8

REG[08h] bits 7-0 Vertical Display Height Bits [9:0]
REG[09h] bits 1-0

These bits specify the LCD panel and/or the CRT vertical display height, in 1-line resolution. For a dual LCD panel only configuration, this register should be programmed to half the panel size.

Vertical display height in number of lines = (ContentsOfThisRegister) + 1.
The maximum vertical display height is 1024 lines.

Vertical Non-Display Period Register
REG[0Ah] RW

Vertical Non-Display Period Status (RO)	n/a	Vertical Non-Display Period Bit 5	Vertical Non-Display Period Bit 4	Vertical Non-Display Period Bit 3	Vertical Non-Display Period Bit 2	Vertical Non-Display Period Bit 1	Vertical Non-Display Period Bit 0

bit 7 Vertical Non-Display Period Status

This is a read-only status bit. A “1” indicates that a vertical non-display period is occurring. A “0” indicates that display output is in a vertical display period.

Note

When configured for a dual panel, this bit will toggle at twice the frame rate.

bits 5-0 Vertical Non-Display Period Bits [5:0]

These bits specify the vertical non-display period height in 1-line resolution.

Vertical non-display period height in number of lines = (ContentsOfThisRegister) + 1.

The maximum vertical non-display period height is 64 lines.

Note

This register must be programmed such that
REG[0Ah] ≥ 1 and (REG[0Ah] bits [5:0] + 1) ≥ (REG[0Bh] + 1) + (REG[0Ch] bits [2:0] + 1)

VRTC/FPFRAME Start Position Register
REG[0Bh] RW

n/a	n/a	VRTC/ FPFRAME Start Position Bit 5	VRTC/ FPFRAME Start Position Bit 4	VRTC/ FPFRAME Start Position Bit 3	VRTC/ FPFRAME Start Position Bit 2	VRTC/ FPFRAME Start Position Bit 1	VRTC/ FPFRAME Start Position Bit 0

bits 5-0 VRTC/FPFRAME Start Position Bits [5:0]

For CRTs and TFTs, these bits specify the delay in lines from the start of the vertical non-display period to the leading edge of the VRTC pulse and FPFRAME pulse respectively. For passive LCDs, FPFRAME is automatically created and these bits have no effect.

VRTC/FPFRAME start position (lines) = VRTC/FPFRAME Start Position Bits [5:0] + 1.

The maximum VRTC start delay is 64 lines.

Note

This register must be programmed such that
(REG[0Ah] bits [5:0] + 1) ≥ (REG[0Bh] + 1) + (REG[0Ch] bits [2:0] + 1)

VRTC/FPFRAME Pulse Width Register REG[0Ch]							RW
VRTC Polarity Select	FPFRAME Polarity Select	n/a	n/a	n/a	VRTC/ FPFRAME Pulse Width Bit 2	VRTC/ FPFRAME Pulse Width Bit 1	VRTC/ FPFRAME Pulse Width Bit 0

bit 7 VRTC Polarity Select

For CRTs, this bit selects the polarity of the VRTC. When this bit = 1, the VRTC pulse is active high. When this bit = 0, the VRTC pulse is active low.

bit 6 FPFRAME Polarity Select

This bit selects the polarity of the FPFRAME for TFT and passive LCD. When this bit = 1, the FPFRAME pulse is active high for TFT and active low for passive LCD. When this bit = 0, the FRAME pulse is active low for TFT and active high for passive LCD.

Table 8-5: FPFRAME Polarity Selection

FPFRAME Polarity Select	Passive LCD FPFRAME Polarity	TFT FPFRAME Polarity
0	active high	active low
1	active low	active high

bits 2-0 VRTC/FPFRAME Pulse Width Bits [2:0]

For CRTs and TFTs, these bits specify the pulse width of VRTC and FPFRAME respectively. For passive LCDs, FPFRAME is automatically created and these bits have no effect.

VRTC/FPFRAME pulse width (lines) = VRTC/FPFRAME Pulse Width Bits [2:0] + 1.

The maximum VRTC pulse width is 8 lines.

Note

This register must be programmed such that
(REG[0Ah] bits [5:0] + 1) ≥ (REG[0Bh] + 1) + (REG[0Ch] bits [2:0] + 1)

8.2.4 Display Configuration Registers

Display Mode Register REG[0Dh]							RW
n/a	Simultaneous Display Option Select Bit 1	Simultaneous Display Option Select Bit 0	Number Of Bits/Pixel Select Bit 2	Number Of Bits/Pixel Select Bit 1	Number Of Bits/Pixel Select Bit 0	CRT Enable	LCD Enable

bits 6-5 Simultaneous Display Option Select Bits [1:0]
These bits are used to select one of four different simultaneous display mode options: Normal, Line Doubling, Interlace, or Even Scan Only. The purpose of these modes is to manipulate the vertical resolution of the image so that it fits on both CRT, typically 640 x 480, and LCD. The following gives descriptions of the four modes using a 640x480 CRT as an example:

Table 8-6: Simultaneous Display Option Selection

Simultaneous Display Option Select Bits [1:0]	Simultaneous Display Option
00	Normal
01	Line Doubling
10	Interlace
11	Even Scan Only

Note

1. Line doubling option is not supported with dual panel.
2. Dual Panel Considerations
   When configured for a dual panel LCD and using Simultaneous Display, the Half Frame Buffer Disable, REG[1Bh] bit 0, must be set to 1. This will result in a lower contrast on the LCD panel, which then may require adjustment.

Normal - the image is the same on both displays, i.e. 640x240. CRT parameters determine the LCD image. The LCD image will appear to be washed out due to the 1/525 duty cycle of the CRT.

Line Doubling - each line is sent to the CRT twice, giving a 640x480 image which has a long aspect ratio. The image on the LCD has each line sent twice but only one FPLINE. This gives a duty cycle of 2/525, which is very close to the LCD only mode duty cycle of 1/242, so the image on the LCD will have almost the same contrast as that of a single LCD.

Interlace - odd frames receive odd scan lines and even frames receive even scan lines. The 640x480 image on the CRT will be normal while the image on the 640x240 LCD will appear to be squashed, though text will be readable.

Even Scan Only - the 640x480 image on the CRT is normal. The LCD (640x240) only receives the even scan lines. The image on the LCD does not flicker, but it may be hard to read text.

bits 4-2 Number of Bits-Per-Pixel Select Bits [2:0]
These bits select the number of bits-per-pixel (bpp) for the displayed data.

Note
15 and 16-bpp modes bypass the LUT and are supported as 12-bpp on passive panels and 15/16-bpp on TFT panels. These modes are not supported on CRT. See Figure 10-2: "15/16 Bit-Per-Pixel Format Memory Organization," on page 116 for a description of passive panel support.

Table 8-7: Number of Bits-Per-Pixel Selection

Number Of Bits-Per-Pixel Select Bits [2:0]	Number of Bits-Per-Pixel
000	1
001	2
010	4
011	8
100	15
101	16
110-111	Reserved

bit 1 CRT Enable
This bit enables the CRT control signals.

Note
REG[02h] bit 1 must = 0 when in CRT only mode.

bit 0 LCD Enable
This bit enables the LCD control signals. Programming this bit from a 0 to a 1 starts the LCD power-on sequence. Programming this bit from a 1 to a 0 starts the LCD power-off sequence.

Screen 1 Line Compare Register 0 REG[0Eh]							RW
Screen 1 Line Compare Bit 7	Screen 1 Line Compare Bit 6	Screen 1 Line Compare Bit 5	Screen 1 Line Compare Bit 4	Screen 1 Line Compare Bit 3	Screen 1 Line Compare Bit 2	Screen 1 Line Compare Bit 1	Screen 1 Line Compare Bit 0

Screen 1 Line Compare Register 1 REG[0Fh]							RW
n/a	n/a	n/a	n/a	n/a	n/a	Screen 1 Line Compare Bit 9	Screen 1 Line Compare Bit 8

REG[0Eh] bits 7-0
REG[0Fh] bits 1-0

Screen 1 Line Compare Bits [9:0]

In split screen mode, the panel is divided into screen 1 and screen 2, with screen 1 above screen 2. These registers form a 10-bit value that specify the screen 1 size in 1-line resolution. The maximum screen 1 vertical size is 1024 lines. Screen 2 is visible only if the screen 1 line compare is less than the vertical panel size. The starting address for screen 1 is given by the Screen 1 Display Start Address registers (REG[10h], REG[11h], REG[12h]). The starting address for screen 2 is given by the Screen 2 Display Start Address registers (REG[13h], REG[14h], REG[15h]).

For normal operation (no split screen):

this register must be set greater than the vertical display height REG[08h] and REG[09h] (e.g. set to 3FFh).

For split screen on a single panel:

Split screen 1 vertical size in number of lines = (ContentsOfThisRegister) + 1

For split screen on a dual panel:

Split screen 1 vertical size in number of lines = (ContentsOfThisRegister) + 1,
if (ContentsOfThisRegister) ≤ 00EFh
or
Split screen 1 vertical size in number of lines = (ContentsOfThisRegister) + 2,
if (ContentsOfThisRegister) > 00EFh

Note

For further details, see Section 10.2, *"Image Manipulation"* on page 117 and the *S1D13504 Programming Notes and Examples*, document number X19A-G-002-xx.

Screen 1 Display Start Address Register 0 REG[10h]							RW
Start Address Bit 7	Start Address Bit 6	Start Address Bit 5	Start Address Bit 4	Start Address Bit 3	Start Address Bit 2	Start Address Bit 1	Start Address Bit 0

Screen 1 Display Start Address Register 1 REG[11h]							RW
Start Address Bit 15	Start Address Bit 14	Start Address Bit 13	Start Address Bit 12	Start Address Bit 11	Start Address Bit 10	Start Address Bit 9	Start Address Bit 8

Screen 1 Display Start Address Register 2 REG[12h]							RW
n/a	n/a	n/a	n/a	Start Address Bit 19	Start Address Bit 18	Start Address Bit 17	Start Address Bit 16

REG[10h] bits 7-0 Screen 1 Start Address Bits [19:0]
REG[11h] bits 7-0 This register forms the 20-bit address for the starting word of the screen 1 image in the display
REG[12h] bits 3-0 buffer. Note that this is a word address. An entry of 0000h into these registers represents the first word of display memory, an entry of 0001h represents the second word of display memory, and so on. See Section 10, *"Display Configuration"* on page 115 for details.

Screen 2 Display Start Address Register 0 RW REG[13h]							RW
Start Address Bit 7	Start Address Bit 6	Start Address Bit 5	Start Address Bit 4	Start Address Bit 3	Start Address Bit 2	Start Address Bit 1	Start Address Bit 0

Screen 2 Display Start Address Register 1 REG[14h]							RW
Start Address Bit 15	Start Address Bit 14	Start Address Bit 13	Start Address Bit 12	Start Address Bit 11	Start Address Bit 10	Start Address Bit 9	Start Address Bit 8

Screen 2 Display Start Address Register 2 REG[15h]							RW
n/a	n/a	n/a	n/a	Start Address Bit 19	Start Address Bit 18	Start Address Bit 17	Start Address Bit 16

REG[13h] bits 7-0 Screen 2 Start Address Bits [19:0]
REG[14h] bits 7-0 This register forms the 20-bit address for the starting word of the screen 2 image in the display
REG[15h] bits 3-0 buffer. Note that this is a word address. An entry of 0000h into these registers represents the first word of display memory, an entry of 0001h represents the second word of display memory, and so on. See Section 10, *"Display Configuration"* on page 115 for details.

Memory Address Offset Register 0 REG[16h]							RW
Memory Address Offset Bit 7	Memory Address Offset Bit 6	Memory Address Offset Bit 5	Memory Address Offset Bit 4	Memory Address Offset Bit 3	Memory Address Offset Bit 2	Memory Address Offset Bit 1	Memory Address Offset Bit 0

Memory Address Offset Register 1 REG[17h]							RW
n/a	n/a	n/a	n/a	n/a	n/a	Memory Address Offset Bit 9	Memory Address Offset Bit 8

REG[16] bits 7-0 Memory Address Offset Bits [9:0]
REG[17] bits 1-0 These bits are the 10-bit address offset from the starting word of line "n" to the starting word of line "n + 1". This value is applied to both screen 1 and screen 2.

Note
This value is in words and must be programmed ≥ REG[04h].

A virtual image can be formed by setting this register to a value greater than the width of the display. The displayed image is a window into the larger virtual image.

See Section 10, *"Display Configuration"* on page 115 for details.

Pixel Panning Register REG[18h]							RW
Screen 2 Pixel Panning Bit 3	Screen 2 Pixel Panning Bit 2	Screen 2 Pixel Panning Bit 1	Screen 2 Pixel Panning Bit 0	Screen 1 Pixel Panning Bit 3	Screen 1 Pixel Panning Bit 2	Screen 1 Pixel Panning Bit 1	Screen 1 Pixel Panning Bit 0

This register is used to control the horizontal pixel panning of screen 1 and screen 2. Each screen can be independently panned to the left by programming its respective Pixel Panning Bits to a non-zero value. This value represents the number of pixels panned. The maximum pan value is dependent on the display mode as shown in the table below.

Table 8-8: Pixel Panning Selection

Number of Bits-Per-Pixel	Screen 2 Pixel Panning Bits Used
1	Bits [3:0]
2	Bits [2:0]
4	Bits [1:0]
8	Bit 0
15/16	---

Smooth horizontal panning can be achieved by a combination of this register and the Display Start Address register. See Section 10, *"Display Configuration"* on page 115 and S1D13504 Programming Notes and Examples, document number X19A-G-002-xx, Section 4 for details.

bits 7-4 Screen 2 Pixel Panning Bits [3:0]
Pixel panning bits for screen 2.

bits 3-0 Screen 1 Pixel Panning Bits [3:0]
Pixel panning bits for screen 1.

8.2.5 Clock Configuration Register

Clock Configuration Register REG[19h]							RW
n/a	n/a	n/a	n/a	n/a	MCLK Divide Select	PCLK Divide Select Bit 1	PCLK Divide Select Bit 0

bit 2 MCLK Divide Select
When this bit = 1 the memory clock (MCLK) frequency is half of the input clock frequency. When this bit = 0 the memory clock frequency is equal to the input clock frequency.

bits 1-0 PCLK Divide Select Bits [1:0]
These bits determine the amount of divide from the memory clock to generate the pixel clock (PCLK):

Table 8-9: PCLK Divide Selection

PCLK Divide Select Bits [1:0]	MCLK/PCLK Frequency Ratio
00	1
01	2
10	3
11	4

See Section 11.2, *"Frame Rate Calculation"* on page 119 for selection of PCLK frequency.

8.2.6 Power Save Configuration Registers

Power Save Configuration Register REG[1Ah]							RW
n/a	n/a	n/a	n/a	LCD Power Disable	Suspend Refresh Select Bit 1	Suspend Refresh Select Bit 0	Software Suspend Mode Enable

bit 3 LCD Power Disable
When this bit = 1 the LCDPWR output is directly forced to the Off state. The LCDPWR "On/Off" state is configured by MD10 at the rising edge of RESET#. When this bit = 0 the LCDPWR output is controlled by the panel on/off sequencing logic. See Table 5-8: "Summary of Power On / Reset Options," on page 30.

bits 2-1 Suspend Refresh Select Bits [1:0]
These bits specify the type of DRAM refresh to use in Suspend mode.

Table 8-10: Suspend Refresh Selection

Suspend Refresh Select Bits [1:0]	DRAM Refresh Type
00	CBR Refresh
01	Self-Refresh
1x	No Refresh

Note
These bits should not be changed when suspend mode is enabled.

bit 0 Software Suspend Mode Enable
When this bit = 1 software suspend mode is enabled. When this bit = 0 software suspend mode is disabled.

8.2.7 Miscellaneous Registers

Miscellaneous Disable Register REG[1Bh]							RW
Host Interface Disable	n/a	n/a	n/a	n/a	n/a	n/a	Half Frame Buffer Disable

bit 7 Host Interface Disable

This bit must be programmed to 0 to enable the Host Interface. This bit goes high on reset. When this bit is high, all memory and all registers except REG[1Ah] (read-only), REG[28h] through REG[2Fh], and REG[1Bh] are inaccessible.

bit 0 Half Frame Buffer Disable

This bit is used to disable the Half Frame Buffer.

When this bit = 1, the Half Frame Buffer is disabled. When this bit = 0, the Half Frame Buffer is enabled. When a single panel is selected, the Half Frame Buffer is automatically disabled and this bit has no hardware effect.

The Half Frame Buffer is needed to fully support dual panels. Disabling the Half Frame Buffer reduces memory bandwidth requirements and increases the supportable pixel clock frequency, but results in reduced contrast on the LCD panel. This mode is not normally used except in special circumstances such as simultaneous display on a CRT and dual panel LCD. See Section 11.2 on page 119 for details.

Note

The Half Frame Buffer should be disabled only when idle. The Half Frame Buffer is idle during vertical non-display periods (i.e. when REG[0Ah] bit 7 = 1), or while in suspend mode. For programming information, see *S1D13504 Programming Notes and Examples*, document number X19A-G-002-xx.

MD Configuration Readback Register 0 REG[1Ch]							RO
MD7 Status	MD6 Status	MD5 Status	MD4 Status	MD3 Status	MD2 Status	MD1 Status	MD0 Status

MD Configuration Readback Register 1 REG[1Dh]							RO
MD15 Status	MD14 Status	MD13 Status	MD12 Status	MD11 Status	MD10 Status	MD9 Status	MD8 Status

REG[1Ch] bits 7-0 MD[15:0] Configuration Status
REG[1Dh] bits 7-0

These are read-only status bits for the MD[15:0] pins configuration status at the rising edge of RESET#.

See Table 5-8: “Summary of Power On / Reset Options,” on page 30.

GPIO Configuration Register 0 REG[1Eh]							RW
GPIO7 Pin IO Config.	GPIO6 Pin IO Config.	GPIO5 Pin IO Config.	GPIO4 Pin IO Config.	GPIO3 Pin IO Config.	GPIO2 Pin IO Config.	GPIO1 Pin IO Config.	GPIO0 Pin IO Config.

bit 7 GPIO7 Pin IO Configuration
When this bit = 1, GPIO7 is configured as an output. When this bit = 0 (default), GPIO7 is configured as an input. Note the MD8 pin must be high at the rising edge of RESET# to enable GPIO7, otherwise the DACWR# pin is controlled automatically and this bit will have no effect on hardware.

bit 6 GPIO6 Pin IO Configuration
When this bit = 1, GPIO6 is configured as an output. When this bit = 0 (default), GPIO6 is configured as an input. Note the MD8 pin must be high at the rising edge of RESET# to enable GPIO6, otherwise the DACP0 pin is controlled automatically and this bit will have no effect on hardware.

bit 5 GPIO5 Pin IO Configuration
When this bit = 1, GPIO5 is configured as an output. When this bit = 0 (default), GPIO5 is configured as an input. Note the MD8 pin must be high at the rising edge of RESET# to enable GPIO5, otherwise the BLANK# pin is controlled automatically and this bit will have no effect on hardware.

bit 4 GPIO4 Pin IO Configuration
When this bit = 1, GPIO4 is configured as an output. When this bit = 0 (default), GPIO4 is configured as an input. Note the MD8 pin must be high at the rising edge of RESET# to enable GPIO4, otherwise the DACRD# pin is controlled automatically and this bit will have no effect on hardware.

bit 3 GPIO3 Pin IO Configuration
When this bit = 1, GPIO3 is configured as an output. When this bit = 0 (default), GPIO3 is configured as an input. Note the MD[7:6] pins must be properly configured at the rising edge of RESET# to enable GPIO3, otherwise the MA9 pin is controlled automatically and this bit will have no effect on hardware.

bit 2 GPIO2 Pin IO Configuration
When this bit = 1, GPIO2 is configured as an output. When this bit = 0 (default), GPIO2 is configured as an input. Note the MD[7:6] pins must be properly configured at the rising edge of RESET# to enable GPIO2, otherwise the MA11 pin is controlled automatically and this bit will have no effect on hardware.

bit 1 GPIO1 Pin IO Configuration
When this bit = 1, GPIO1 is configured as an output. When this bit = 0 (default), GPIO1 is configured as an input. Note the MD[7:6] pins must be properly configured at the rising edge of RESET# to enable GPIO1, otherwise the MA10 pin is controlled automatically and this bit will have no effect on hardware.

bit 0 GPIO0 Pin IO Configuration
When this bit = 1, GPIO0 is configured as an output. When this bit = 0 (default), GPIO0 is configured as an input.

GPIO Configuration Register 1 REG[1Fh]							RW
n/a	n/a	n/a	n/a	GPIO11 Pin IO Config.	GPIO10 Pin IO Config.	GPIO9 Pin IO Config.	GPIO8 Pin IO Config.

bit 3 GPIO11 Pin IO Configuration

When this bit = 1, GPIO11 is configured as an output. When this bit = 0 (default), GPIO11 is configured as an input. Note the MD8 pin must be high at the rising edge of RESET# to enable GPIO11, otherwise the VRTC pin is controlled automatically and this bit will have no effect on hardware.

bit 2 GPIO10 Pin IO Configuration

When this bit = 1, GPIO10 is configured as an output. When this bit = 0 (default), GPIO10 is configured as an input. Note the MD8 pin must be high at the rising edge of RESET# to enable GPIO10, otherwise the HRTC pin is controlled automatically and this bit will have no effect on hardware.

bit 1 GPIO9 Pin IO Configuration

When this bit = 1, GPIO9 is configured as an output. When this bit = 0 (default), GPIO9 is configured as an input.

Note

GPIO9 and GPIO8 must always be set to the same function (both to input or both to output).

The MD8 pin must be high at the rising edge of RESET# to enable GPIO9, otherwise the DACRS1 pin is controlled automatically and this bit will have no effect on hardware.

bit 0 GPIO8 Pin IO Configuration

When this bit = 1, GPIO8 is configured as an output. When this bit = 0 (default), GPIO8 is configured as an input.

Note

GPIO8 and GPIO9 must always be set to the same function (both to input or both to output).

The MD8 pin must be high at the rising edge of RESET# to enable GPIO8, otherwise the DACRS0 pin is controlled automatically and this bit will have no effect on hardware.

GPIO Status / Control Register 0 REG[20h]							RW
GPIO7 Pin IO Status	GPIO6 Pin IO Status	GPIO5 Pin IO Status	GPIO4 Pin IO Status	GPIO3 Pin IO Status	GPIO2 Pin IO Status	GPIO1 Pin IO Status	GPIO0 Pin IO Status

bit 7 GPIO7 Pin IO Status
When GPIO7 is configured as an output, a “1” in this bit drives GPIO7 to high and a “0” in this bit drives GPIO7 to low. When GPIO7 is configured as an input, a read from this bit returns the status of GPIO7. Note the MD8 pin must be high at the rising edge of RESET# to enable GPIO7, otherwise the DACWR# pin is controlled automatically and this bit will have no effect on hardware.

bit 6 GPIO6 Pin IO Status
When GPIO6 is configured as an output, a “1” in this bit drives GPIO6 to high and a “0” in this bit drives GPIO6 to low. When GPIO6 is configured as an input, a read from this bit returns the status of GPIO6. Note the MD8 pin must be high at the rising edge of RESET# to enable GPIO6, otherwise the DACP0 pin is controlled automatically and this bit will have no effect on hardware.

bit 5 GPIO5 Pin IO Status
When GPIO5 is configured as an output, a “1” in this bit drives GPIO5 to high and a “0” in this bit drives GPIO5 to low. When GPIO5 is configured as an input, a read from this bit returns the status of GPIO5. Note the MD8 pin must be high at the rising edge of RESET# to enable GPIO5, otherwise the BLANK# pin is controlled automatically and this bit will have no effect on hardware.

bit 4 GPIO4 Pin IO Status
When GPIO4 is configured as an output, a “1” in this bit drives GPIO4 to high and a “0” in this bit drives GPIO4 to low. When GPIO4 is configured as an input, a read from this bit returns the status of GPIO4. Note the MD8 pin must be high at the rising edge of RESET# to enable GPIO4, otherwise the DACRD# pin is controlled automatically and this bit will have no effect on hardware.

bit 3 GPIO3 Pin IO Status
When GPIO3 is configured as an output, a “1” in this bit drives GPIO3 to high and a “0” in this bit drives GPIO3 to low. When GPIO3 is configured as an input, a read from this bit returns the status of GPIO3. Note the MD[7:6] pins must be properly configured at the rising edge of RESET# to enable GPIO3, otherwise the MA9 pin is controlled automatically and this bit will have no effect on hardware.

bit 2 GPIO2 Pin IO Status
When GPIO2 is configured as an output, a “1” in this bit drives GPIO2 to high and a “0” in this bit drives GPIO2 to low. When GPIO2 is configured as an input, a read from this bit returns the status of GPIO2. Note the MD[7:6] pins must be properly configured at the rising edge of RESET# to enable GPIO2, otherwise the MA11 pin is controlled automatically and this bit will have no effect on hardware.

bit 1 GPIO1 Pin IO Status
When GPIO1 is configured as an output, a “1” in this bit drives GPIO1 to high and a “0” in this bit drives GPIO1 to low. When GPIO1 is configured as an input, a read from this bit returns the status of GPIO1. Note the MD[7:6] pins must be properly configured at the rising edge of RESET# to enable GPIO1, otherwise the MA10 pin is controlled automatically and this bit will have no effect on hardware.

bit 0 GPIO0 Pin IO Status
When GPIO0 is configured as an output, a “1” in this bit drives GPIO0 to high and a “0” in this bit drives GPIO0 to low. When GPIO0 is configured as an input, a read from this bit returns the status of GPIO0.

GPIO Status / Control Register 1 REG[21h]							RW
GPO Control	n/a	n/a	n/a	GPIO11 Pin IO Status	GPIO10 Pin IO Status	GPIO9 Pin IO Status	GPIO8 Pin IO Status

bit 7 GPO Control

This bit is used to control the state of the SUSPEND# pin when it is configured as GPO. The SUSPEND# pin can be used as a power-down input (SUSPEND#) or as an output (GPO) possibly used for controlling the LCD backlight power:

- When MD9 = 0 at rising edge of RESET#, SUSPEND# is an active-low Schmitt input used to put the S1D13504 into suspend mode - see Section 13, *"Power Save Modes"* on page 127 for details.
- When MD[10:9] = 01 at rising edge of RESET#, SUSPEND# is an output with a reset state of 1.
- When MD[10:9] = 11 at rising edge of RESET#, SUSPEND# is an output with a reset state of 0.

When this bit = 0 the GPO output is set to the reset state. When this bit = 1 the GPO output pin is set to the inverse of the reset state.

bit 3 GPIO11 Pin IO Status

When GPIO11 is configured as an output, a "1" in this bit drives GPIO11 to high and a "0" in this bit drives GPIO11 to low. When GPIO11 is configured as an input, a read from this bit returns the status of GPIO11. Note the MD8 pin must be high at the rising edge of RESET# to enable GPIO11, otherwise the VRTC pin is controlled automatically and this bit will have no effect on hardware.

bit 2 GPIO10 Pin IO Status

When GPIO10 is configured as an output, a "1" in this bit drives GPIO10 to high and a "0" in this bit drives GPIO10 to low. When GPIO10 is configured as an input, a read from this bit returns the status of GPIO10. Note the MD8 pin must be high at the rising edge of RESET# to enable GPIO10, otherwise the HRTC pin is controlled automatically and this bit will have no effect on hardware.

bit 1 GPIO9 Pin IO Status

When GPIO9 is configured as an output, a "1" in this bit drives GPIO9 to high and a "0" in this bit drives GPIO9 to low. When GPIO9 is configured as an input, a read from this bit returns the status of GPIO9. Note the MD8 pin must be high at the rising edge of RESET# to enable GPIO9, otherwise the DACRS1 pin is controlled automatically and this bit will have no effect on hardware.

bit 0 GPIO8 Pin IO Status

When GPIO8 is configured as an output, a "1" in this bit drives GPIO8 to high and a "0" in this bit drives GPIO8 to low. When GPIO8 is configured as an input, a read from this bit returns the status of GPIO8. Note the MD8 pin must be high at the rising edge of RESET# to enable GPIO8, otherwise the DACRS0 pin is controlled automatically and this bit will have no effect on hardware.

Performance Enhancement Register 0 REG[22h]							RW
EDO Read-Write Delay	RC Timing Value Bit 1	RC Timing Value Bit 0	RAS# to CAS# Delay	RAS# Precharge Timing Bit 1	RAS# Precharge Timing Bit 0	n/a	Reserved

Note

Changing this register to non-zero value, or to a different non-zero value, should be done only when there are no read/write DRAM cycles. This condition occurs when both the Display FIFO is disabled (REG[23h] bit 7 = 1) and the Half Frame Buffer is disabled (REG[1Bh] bit 0 = 1). For programming information, see *S1D13504 Programming Notes and Examples*, document number X19A-G-002-xx.

bit 7 EDO Read-Write Delay

This bit is used for EDO-DRAM to select the delay during the read-write transition. A "0" selects 2 MCLK delay for the read-write transition. A "1" selects 1 MCLK delay for the read-write DRAM. This bit has no effect for FPM-DRAM which always uses 1 MCLK delay for the read-write transition. This bit may be programmed to 1 when the MCLK frequency is less than 30MHz.

bits 6-5 RC Timing Value (N_{RC}) Bits [1:0]

These bits select the DRAM random-cycle timing parameter, t_{RC}. These bits specify the number (N_{RC}) of MCLK periods (T_M) used to create t_{RC}. N_{RC} should be chosen to meet t_{RC} as well as t_{RAS}, the RAS pulse width. Use the following two formulae to calculate N_{RC} then choose the larger value. Note, these formulae assume an MCLK duty cycle of 50 +/- 5%.

N_{RC} = Round-Up (t_{RC}/T_M)

N_{RC} = Round-Up ($t_{RAS}/T_M + N_{RP}$) if N_{RP} = 1 or 2
= Round-Up (t_{RAS}/T_M + 1.55) if N_{RP} = 1.5

The resulting t_{RC} is related to N_{RC} as follows:

t_{RC} = (N_{RC}) T_M

Table 8-11: Minimum Memory Timing Selection

REG[22h] Bits [6:5]	N_{RC}	Minimum Random Cycle Width (t_{RC})
00	5	5 T_M
01	4	4 T_M
10	3	3 T_M
11	Reserved	Reserved

bit 4

RAS# to CAS# Delay (N_{RCD})

This bit selects the DRAM RAS# to CAS# delay parameter, t_{RCD}. This bit specifies the number (N_{RCD}) of MCLK periods (T_M) used to create t_{RCD}. N_{RCD} must be chosen to satisfy the RAS# access time, t_{RAC}. Note, these formulae assume an MCLK duty cycle of 50 +/- 5%.

N_{RCD}	= Round-Up((t_{RAC} + 5)/T_M - 1)	if EDO and N_{RP} = 1 or 2
	= 2	if EDO and N_{RP} = 1.5
	= Round-Up(t_{RAC}/T_M - 1)	if FPM and N_{RP} = 1 or 2
	= Round-Up(t_{RAC}/T_M - 0.45)	if FPM and N_{RP} = 1.5

Note that for EDO-DRAM and N_{RP} = 1.5, this bit is automatically forced to 0 to select 2 MCLK for N_{RCD}. This is done to satisfy the CAS# address setup time, t_{ASC}.

The resulting t_{RC} is related to N_{RCD} as follows:

t_{RC}	= (N_{RCD}) T_M	if EDO and N_{RP} = 1 or 2
t_{RC}	= (1.5) T_M	if EDO and N_{RP} = 1.5
t_{RC}	= (N_{RCD} + 0.5) T_M	if FPM and N_{RP} = 1 or 2
t_{RC}	= (N_{RCD}) T_M	if FPM and N_{RP} = 1.5

Table 8-12: RAS-to-CAS Delay Timing Select

REG[22h] Bit 4	N_{RCD}	RAS# to CAS# Delay (t_{RCD})
0	2	2 T_M
1	1	1 T_M

bits 3-2

RAS# Precharge Timing (N_{RP}) Bits [1:0]

Minimum Memory Timing for RAS precharge

These bits select the DRAM RAS# Precharge timing parameter, t_{RP}. These bits specify the number (N_{RP}) of MCLK periods (T_M) used to create t_{RP} - see the following formulae. Note, these formulae assume an MCLK duty cycle of 50 +/- 5%.

N_{RP}	= 1	if (t_{RP}/T_M) < 1
	= 1.5	if 1 ≤ (t_{RP}/T_M) < 1.45
	= 2	if (t_{RP}/T_M) ≥ 1.45

The resulting t_{RC} is related to N_{RP} as follows:

t_{RC}	= (N_{RP} + 0.5) T_M	if FPM refresh cycle and N_{RP} = 1 or 2
t_{RC}	= (N_{RP}) T_M	for all other

Table 8-13: RAS Precharge Timing Select

REG[22h] Bits [3:2]	N_{RP}	RAS# Precharge Width (t_{RP})
00	2	2 T_M
01	1.5	1.5 T_M
10	1	1 T_M
11	Reserved	Reserved

Optimal DRAM Timing

The following table contains the optimally programmed values of N_{RC}, N_{RP}, and N_{RCD} for different DRAM types, at maximum MCLK frequencies.

Table 8-14: Optimal N_{RC}, N_{RP}, and N_{RCD} Values at Maximum MCLK Frequency

DRAM Type	DRAM Speed (ns)	T_M (ns)	N_{RC} (#MCLK)	N_{RP} (#MCLK)	N_{RCD} (#MCLK)
EDO	50	25	4	1.5	2
	60	30	4	1.5	2
	70	33	5	2	2
FPM	60	40	4	1.5	2
	70	50	3	1.5	1

bit 0 Reserved
Must be set to 0.

Performance Enhancement Register 1 REG[23h]							
Display FIFO Disable	n/a	n/a	Display FIFO Threshold Bit 4	Display FIFO Threshold Bit 3	Display FIFO Threshold Bit 2	Display FIFO Threshold Bit 1	Display FIFO Threshold Bit 0

bit 7 Display FIFO Disable
When this bit = 1 the display FIFO is disabled and all data outputs are forced to zero (i.e. the screen is blanked). This allows the S1D13504 to be dedicated to service CPU to memory accesses. When this bit = 0 the display FIFO is enabled.

bits 4-0 Display FIFO Threshold Bits [4:0]
These bits should be set to a value of 10h upon initialization as this provides the best overall performance for all display modes.

8.2.8 Look-Up Table Registers

The S1D13504 has three internal 16 position, 4-bit wide Look-Up Tables. The 4-bit value programmed into each table position determines the color weighting of display data; the output gray shade is derived from the Green Look-Up Table. These tables are bypassed in 15/16-bpp mode.

These three 16 position Look-Up Tables can be arranged in many different configurations to accommodate all the gray shade / color display modes.

Look-Up Table Address Register
REG[24h] RW

n/a	n/a	RGB Index Bit 1	RGB Index Bit 0	LUT Address Bit 3	LUT Address Bit 2	LUT Address Bit 1	LUT Address Bit 0

bits 5-4 RGB Index Bits [1:0]
These bits are also used to provide access to the three internal Look-Up Tables (RGB).

Table 8-15: RGB Index Selection

RGB Index Bits [1:0]	Look-Up Table Access	Pointer Sequence
00	Auto-Increment R, G, B LUT	R[n], G[n], B[n], R[n+1], G[n+1] . . .
01	Auto-Increment Red LUT only	R[n], R[n+1], R[n+2] . . .
10	Auto-Increment Green LUT only	G[n], G[n+1], G[n+2] . . .
11	Auto-Increment Blue LUT only	B[n], B[n+1], B[n+2] . . .

A write to this register with RGB Index bits = 00 selected will position the internal pointer to the Red LUT. Each read/write access to the LUT data will increment the counter to point to the next LUT in order (R to G to B to R...). A read/write access to the Blue LUT will also automatically increment the LUT address by 1. This provides an efficient method for sequential writing of RGB data.

When the RGB Index bits = 01, 10, or 11, the internal pointer always points to the respective R, G, or B LUT. A read/write access to the LUT data will increment the LUT address by 1.

bits 3-0 LUT Address Bits [3:0]
These 4 bits provide a pointer into the 16 position Look-Up Table currently selected for CPU read/write access.

The Look-Up Table configuration (e.g. 1/2/4 banks) does not affect the read/write access from the CPU as all 16 positions can be accessed sequentially.

Look-Up Table Data Register
REG[26h] RW

n/a	n/a	n/a	n/a	LUT Data Bit 3	LUT Data Bit 2	LUT Data Bit 1	LUT Data Bit 0

bits 3-0 LUT Data Bits [3:0]
These 4 bits are the gray shade/color values used for display data output. They are programmed into the 4-bit Look-Up Table positions pointed to by LUT Address bits [3:0] and RGB Index bits [1:0] (if in color display modes).

For example: in a 16-level gray shade display mode, a data value of 0001b (4 bits-per-pixel) will point to Look-Up Table position one and display the 4-bit gray shade corresponding to the value programmed into that location.

Look-Up Table Bank Select Register REG[27h]							RW
n/a	n/a	Red Bank Select Bit 1	Red Bank Select Bit 0	Blue Bank Select Bit 1	Blue Bank Select Bit 0	Green Bank Select Bit 1	Green Bank Select Bit 0

bit 5-4 Red Bank Select Bits [1:0]
In 2-bpp mode, the 16 position Red LUT is arranged into four, 4 position "banks." These two bits control which bank is currently selected.

In 8-bpp mode, the 16 position Red LUT is arranged into two, 8 position "banks." Only bit 0 of these two bits controls which bank is currently selected.

These bits have no effect in 1-bpp, 4-bpp, 15/16-bpp mode, or all monochrome modes.

bit 3-2 Blue Bank Select Bits [1:0]
In both 2-bpp and 8-bpp modes, the 16 position Blue LUT is arranged into four 4 position "banks." These two bits control which bank is currently selected.

These bits have no effect in 1-bpp, 4-bpp, 15/16-bpp mode, or all monochrome modes.

bits 1-0 Green Bank Select Bits [1:0]
In 2-bpp mode, the 16 position Green LUT is arranged into four, 4 position "banks." These two bits control which bank is currently selected.

In 8-bpp mode, the 16 position Green LUT is arranged into two, 8 position "banks." Only bit 0 of these two bits controls which bank is currently selected.

These bits have no effect in 1-bpp, 4-bpp, and 15/16-bpp modes.

8.2.9 External RAMDAC Control Registers

Note

1. In a Little-Endian architecture, the RAMDAC should be connected to the low byte of the CPU data bus and the following registers are accessed at the lower address given for each register (28h, 2Ah, 2Ch, and 2Eh).
   In a Big-Endian architecture, the RAMDAC should be connected to the high byte of the CPU data bus and the following registers are accessed at the higher address given for each register (29h, 2Bh, 2Dh, and 2Fh).
2. When accessing the External RAMDAC Control registers with either of the architectures described in note 1, accessing the adjacent unused registers is prohibited.
3. To access the RAMDAC registers the CRT enable bit, REG[0Dh] bit 1, must be set to 1.

RAMDAC Pixel Read Mask Register REG[28h] or REG[29h]							RW
RAMDAC Data Bit 7	RAMDAC Data Bit 6	RAMDAC Data Bit 5	RAMDAC Data Bit 4	RAMDAC Data Bit 3	RAMDAC Data Bit 2	RAMDAC Data Bit 1	RAMDAC Data Bit 0

bits 7-0 RAMDAC Pixel Read Mask Bits [7:0]
A CPU read or write to this register will generate a DACRD# or DACWR# pulse and DACRS1 = 1 and DACRS0 = 0 to the external RAMDAC for a pixel read mask register access. The RAMDAC data must be transferred directly between the system data bus and the external RAMDAC through either data bus bits [7:0] in a Little-Endian system or data bus bits [15:8] in a Big-Endian system.

RAMDAC Read Mode Address Register
REG[2Ah] or REG[2Bh] RW

RAMDAC Address Bit 7	RAMDAC Address Bit 6	RAMDAC Address Bit 5	RAMDAC Address Bit 4	RAMDAC Address Bit 3	RAMDAC Address Bit 2	RAMDAC Address Bit 1	RAMDAC Address Bit 0

bits 7-0 RAMDAC Read Mode Address Bits [7:0]
A CPU read or write to this register will generate a DACRD# or DACWR# pulse and DACRS1 = 1 and DACRS0 = 1 to the external RAMDAC for a read-mode address register access. The RAMDAC address must be transferred directly between the system data bus and the external RAMDAC through either data bus bits [7:0] in a Little-Endian system or data bus bits [15:8] in a Big-Endian system.

RAMDAC Write Mode Address Register
REG[2Ch] or REG[2Dh] RW

RAMDAC Address Bit 7	RAMDAC Address Bit 6	RAMDAC Address Bit 5	RAMDAC Address Bit 4	RAMDAC Address Bit 3	RAMDAC Address Bit 2	RAMDAC Address Bit 1	RAMDAC Address Bit 0

bits 7-0 RAMDAC Write Mode Address Bits [7:0]
A CPU read or write to this register will generate a DACRD# or DACWR# pulse and DACRS1 = 0 and DACRS0 = 0 to the external RAMDAC for a write-mode address register access. The RAMDAC address must be transferred directly between the system data bus and the external RAMDAC through either data bus bits [7:0] in a Little-Endian system or data bus bits [15:8] in a Big-Endian system.

RAMDAC Palette Data Register
REG[2Eh] or REG[2Fh] RW

RAMDAC Data Bit 7	RAMDAC Data Bit 6	RAMDAC Data Bit 5	RAMDAC Data Bit 4	RAMDAC Data Bit 3	RAMDAC Data Bit 2	RAMDAC Data Bit 1	RAMDAC Data Bit 0

bits 7-0 RAMDAC Palette Data Bits [7:0]
A CPU read or write to this register will generate a DACRD# or DACWR# pulse and DACRS1 = 0 and DACRS0 = 1 to the external RAMDAC for a palette data register access. The RAMDAC data must be transferred directly between the system data bus and the external RAMDAC through either data bus bits [7:0] in a Little-Endian system or data bus bits [15:8] in a Big-Endian system.

9 Display Buffer

The system addresses the display buffer through the CS#, M/R#, and AB[20:0] input pins. When CS# = 0 and M/R# = 1, the display buffer is addressed by bits AB[20:0] as shown in the following table.

Table 9-1: S1D13504 Addressing

CS#	M/R#	Access
0	0	Register access: • REG[00h] is addressed when AB[5:0] = 0 • REG[01h] is addressed when AB[5:0] = 1 • REG[n] is addressed when AB[5:0] = n
0	1	Memory access: the 2M byte display buffer is addressed by AB[20:0]
1	X	S1D13504 not selected

The display buffer address space is always 2M bytes. However, the physical display buffer may be either 512K bytes or 2M bytes. See Section 5.5, *"Summary of Configuration Options"* on page 30.

The 512K byte display buffer is replicated in the 2M byte address space as shown below.

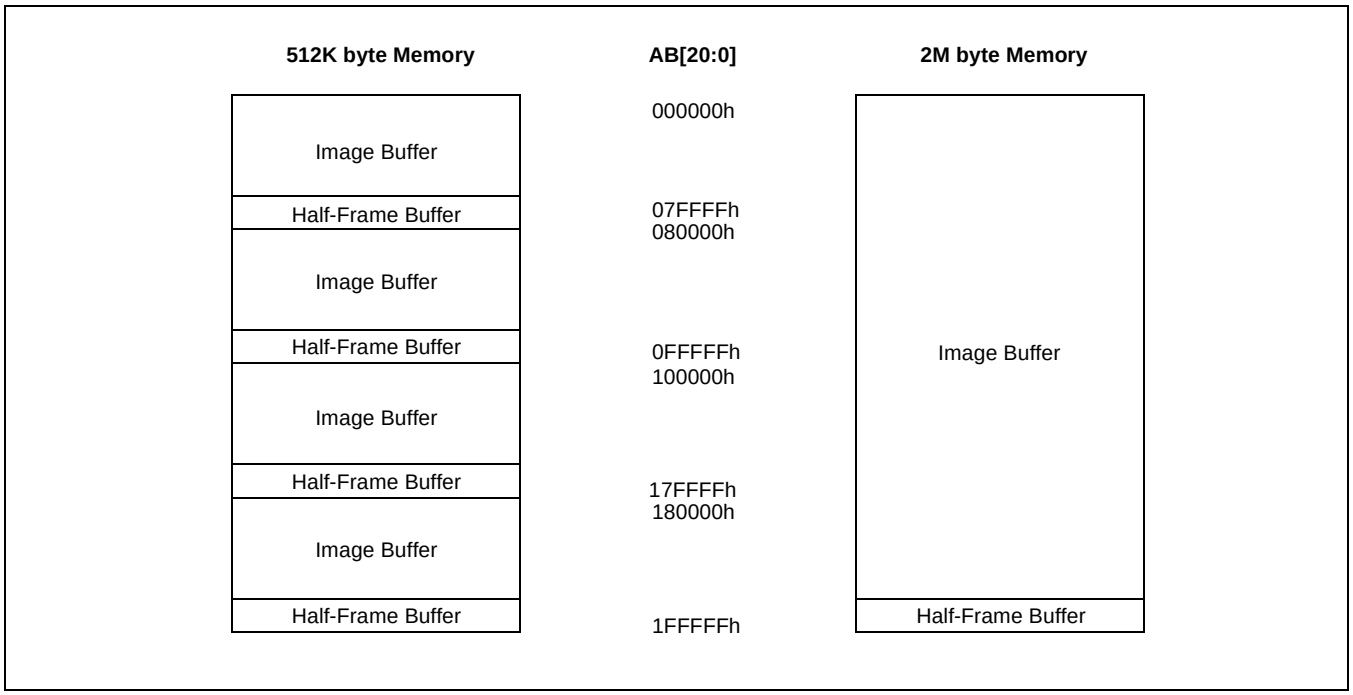


Figure 9-1: Display Buffer Addressing

The display buffer will contain an image buffer and may also contain a half-frame buffer.

9.1 Image Buffer

The image buffer contains the formatted display data - see Section 10.1, *"Display Mode Data Format"* on page 115.

The displayed image(s) may take up only a portion of the image buffer; the remaining area can be used for multiple images - possibly for animation or general storage. See Section 10, *"Display Configuration"* on page 115 for details on the relationship between the image buffer and the display.

9.2 Half Frame Buffer

In dual panel mode, with the half frame buffer enabled, the top of the display buffer is allocated to the half-frame buffer. The size of the half frame buffer is a function of the panel resolution and whether the panel is color or monochrome:

Half Frame Buffer Size (in bytes) = (panel width x panel length) * factor / 16

where factor = 4 for color panel
= 1 for monochrome panel

For example, for a 640x480 8 bpp color panel the half frame buffer size is 75K bytes. In a 512K byte display buffer, the half-frame buffer resides from 6D400h to 7FFFFh. In a 2M byte display buffer, the half-frame buffer resides from 1ED400h to 1FFFFFh.

10 Display Configuration

10.1 Display Mode Data Format

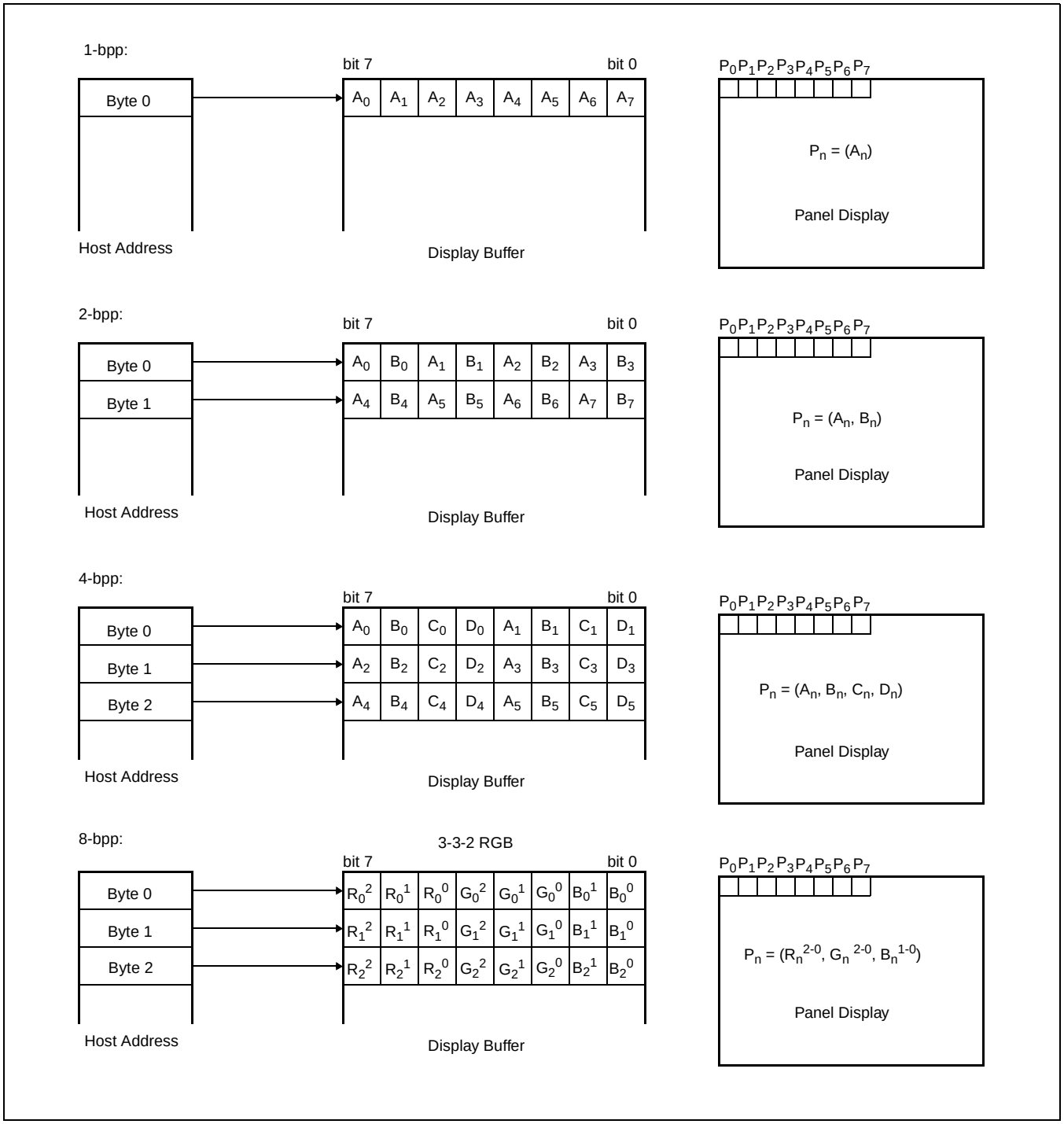


Figure 10-1: 1/2/4/8 Bit-Per-Pixel Format Memory Organization

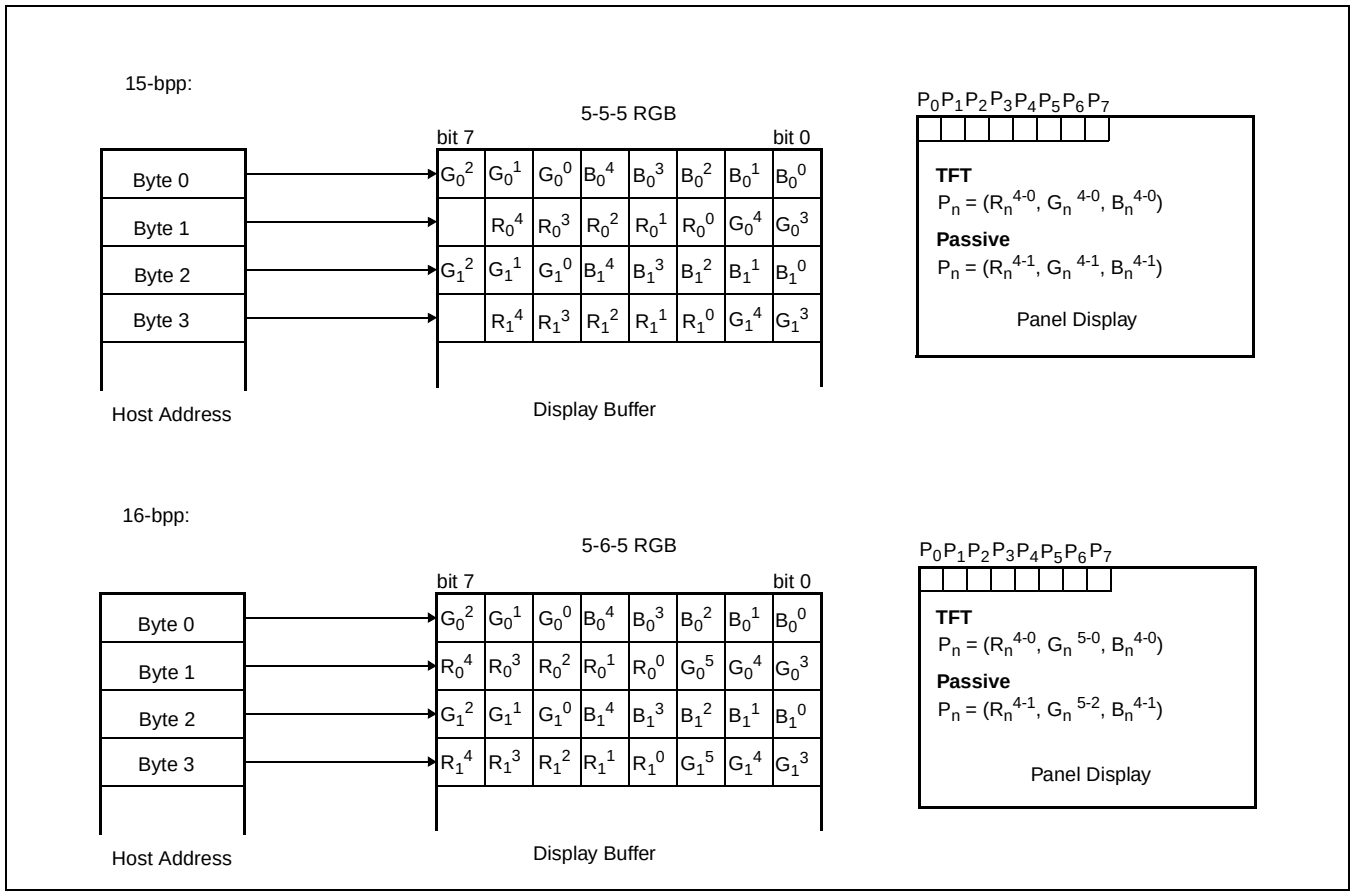


Figure 10-2: 15/16 Bit-Per-Pixel Format Memory Organization

Note

1. The Host-to-Display mapping described here assumes that a Little-Endian interface is being used.
2. For 8/15/16 bit-per-pixel formats, R_n, G_n, B_n represent the red, green, and blue color components.

10.2 Image Manipulation

The figure below shows how screen 1 and screen 2 images stored in the image buffer are positioned on the display. The screen 1 and screen 2 images can be parts of a larger virtual image or images.

- (REG[17h], REG[16h]) defines the width of the virtual image(s).
- (REG[12h], REG[11h], REG[10h]) defines the starting word of the screen 1, (REG[15h], REG[14h], REG[13h]) defines the starting word of the screen 2.
- REG[18h] bits [3:0] define the starting pixel within the starting word for screen 1, REG[18h] bits[7:4] define the starting pixel within the starting word for screen 2.
- (REG[0Fh],REG[0Eh]) define the last line of screen 1, the remainder of the display is taken up by screen 2.

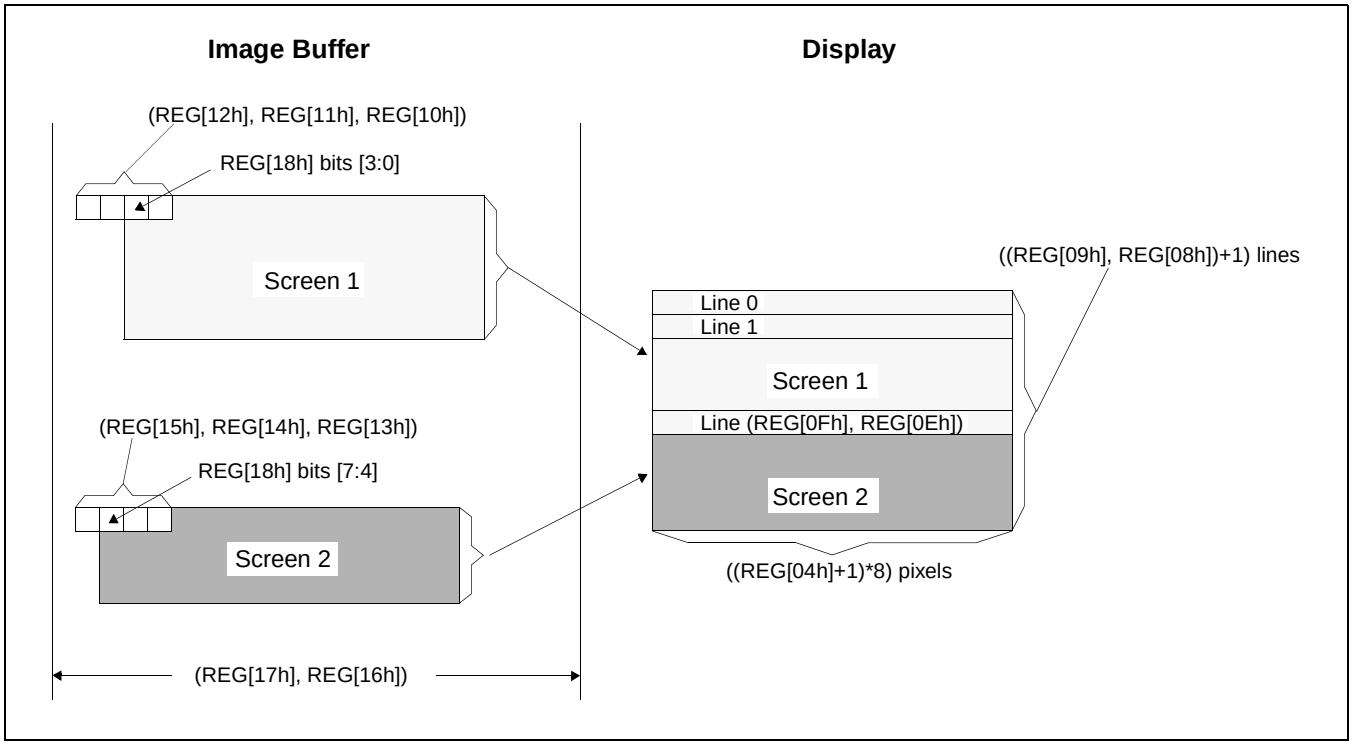


Figure 10-3: Image Manipulation

11 Clocking

11.1 Maximum MCLK: PCLK Ratios

Table 11-1: Maximum PCLK Frequency with EDO-DRAM

Display type	N_{RC}	Maximum PCLK Allowed				
		1 bpp	2 bpp	4 bpp	8 bpp	16 bpp
• Single Panel. • CRT. • Dual Monochrome/Color Panel with Half Frame Buffer Disabled. • Simultaneous CRT + Single Panel. • Simultaneous CRT + Dual Monochrome/Color Panel with Half Frame Buffer Disabled.	5, 4, 3	MCLK				
• Dual Monochrome Panel with Half Frame Buffer Enabled. • Simultaneous CRT + Dual Monochrome Panel with Half Frame Buffer Enable.	5	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
	4	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
	3	MCLK	MCLK	MCLK/2	MCLK/2	MCLK/2
• Dual Color Panel with Half Frame Buffer Enabled. • Simultaneous CRT + Dual Color Panel with Half Frame Buffer Enable.	5	MCLK/2	MCLK/2	MCLK/2	MCLK/3	MCLK/3
	4	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
	3	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3

Table 11-2: Maximum PCLK Frequency with FPM-DRAM

Display type	N_{RC}	Maximum PCLK allowed				
		1 bpp	2 bpp	4 bpp	8 bpp	16 bpp
• Single Panel. • CRT. • Dual Monochrome/Color Panel with Half Frame Buffer Disabled. • Simultaneous CRT + Single Panel. • Simultaneous CRT + Dual Monochrome/Color Panel with Half Frame Buffer Disabled.	5, 4, 3	MCLK				
• Dual Monochrome Panel with Half Frame Buffer Enabled. • Simultaneous CRT + Dual Monochrome Panel with Half Frame Buffer Enable.	5	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
	4	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/2
	3	MCLK	MCLK	MCLK	MCLK/2	MCLK/2
• Dual Color Panel with Half Frame Buffer Enabled. • Simultaneous CRT + Dual Color Panel with Half Frame Buffer Enable.	5	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
	4	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
	3	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/2

11.2 Frame Rate Calculation

The frame rate is calculated using the following formula:

$$\text{FrameRate} = \frac{\text{PCLK}_{max}}{(\text{HDP} + \text{HNDP}) \times (\text{VDP} + \text{VNDP})}$$

Where:

VDP	= Vertical Display Period	= REG[09h] bits [1:0], REG[08h] bits [7:0] + 1
VNDP	= Vertical Non-Display Period	= REG[0Ah] bits [5:0] + 1 = in table below
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1) * 8Ts
HNDP	= Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1) * 8Ts = given in table below
Ts	= Pixel Clock	= PCLK

Table 11-3: Example Frame Rates

DRAM Type[1] (Speed Grade)	Display	Resolution	Color Depth (bpp)	Maximum Pixel Clock (MHz)	Minimum Panel HNDP(T_s)	Maximum Frame Rate (Hz)	
						Panel[4]	CRT
50ns EDO-DRAM MClk = 40MHz N_{RC} = 4 N_{RP} = 1.5 N_{RCD} = 2	• Single Panel. • CRT. • Dual Monochrome/Color Panel with Half Frame Buffer Disabled.[5] • Simultaneous CRT + Single Panel. • Simultaneous CRT + Dual Monochrome/Color Panel with Half Frame Buffer Disabled.[5]	800x600[2]	1/2/4/8	40	32	80	60
			16		56	78	60
		640x480	1/2/4/8		32	123	85
			16		56	119	85
		640x240	1/2/4/8		32	247	-
			16		56	242	-
		480x320	1/2/4/8		32	243	-
			16		56	232	-
		320x240	1/2/4/8		32	471	-
			16		56	441	-
	• Dual Color with Half Frame Buffer Enabled. • Dual Mono with Half Frame Buffer Enabled.	800x600[2,3]	1/2/4/8	20	32	80	-
			16	13.3	32	53	-
		640x480	1/2/4/8	20	32	123	-
			16	13.3	32	82	-

Table 11-3: Example Frame Rates

DRAM Type[1] (Speed Grade)	Display	Resolution	Color Depth (bpp)	Maximum Pixel Clock (MHz)	Minimum Panel HNDP(T_s)	Maximum Frame Rate (Hz)	
						Panel[4]	CRT
60ns EDO-DRAM MClk = 33MHz N_{RC} = 4 N_{RP} = 1.5 N_{RCD} = 2	• Single Panel. • CRT. • Dual Mono/Color Panel with Half Frame Buffer Disabled.[5] • Simultaneous CRT + Single Panel. • Simultaneous CRT + Dual Mono/Color Panel with Half Frame Buffer Disabled.[5]	800x600[2]	1/2/4/8	33	32	66	55
			16		56	65	55
		640x480	1/2/4/8		32	101	78
			16		56	98	78
		640x240	1/2/4/8		32	203	-
			16		56	200	-
		480x320	1/2/4/8		32	200	-
			16		56	196	-
		320x240	1/2/4/8		32	388	-
			16		56	380	-
	• Dual Color with Half Frame Buffer Enabled. • Dual Mono with Half Frame Buffer Enabled.	800x600[2,3]	1/2/4/8	16.5	32	66	-
			16	11	32	43	-
		640x480	1/2/4/8	16.5	32	103	-
			16	11	32	68	-
60ns FPM-DRAM MClk = 25MHz N_{RC} = 4 N_{RP} = 1.5 N_{RCD} = 2	• Single Panel. • CRT. • Dual Mono/Color Panel with Half Frame Buffer Disabled.[5] • Simultaneous CRT + Single Panel. • Simultaneous CRT + Dual Mono/Color Panel with Half Frame Buffer Disabled.[5]	800x600[2]	1/2/4/8	25	32	50	-
			16		56	48	-
		640x480	1/2/4/8		32	77	60
			16		56	75	60
		640x240	1/2/4/8		32	142	-
			16		56	136	-
		480x320	1/2/4/8		32	152	-
			16		56	145	-
		320x240	1/2/4/8		32	294	-
			16		56	280	-
	• Dual Mono with Half Frame Buffer Enabled.	800x600[2]	1/2/4/8/16	12.5	32	50	-
		640x480	1/2/4/8/16	12.5	32	77	-
		640x400	1/2/4/8/16	12.5	32	92	-
	• Dual Color with Half Frame Buffer Enabled.	800x600[2,3]	1/2/4/8	12.5	32	50	-
			16	8.33	32	33	-
		640x480	1/2/4/8	12.5	32	77	-
			16	8.33	32	51	-

1. Must set N_{RC} = 4MCLK. See REG[22h], “Performance Enhancement Register 0”.
2. 800x600 @ 16 bpp requires 2M bytes of display buffer for all display types.
3. 800x600 @ 8 bpp on a dual color panel requires 2M bytes of display buffer if the half frame buffer is enabled.
4. Optimum frame rates for panels range from 60Hz to 150Hz. If the maximum refresh rate is too high for a panel, MCLK should be reduced or PCLK should be divided down.
5. Half Frame Buffer disabled by REG[1Bh] bit 0.

12 Look-Up Table Architecture

Table 12-1: Look-Up Table Configurations

Display Mode	4-Bit Wide Look-Up Table		
	RED	GREEN	BLUE
Black & White		1 bank of 2 entries	
4-level gray		4 banks of 4 entries	
16-level gray		1 bank of 16 entries	
2 color	1 bank of 2 entries	1 bank of 2 entries	1 bank of 2 entries
4 color	4 banks of 4 entries	4 banks of 4 entries	4 banks of 4 entries
16 color	1 bank of 16 entries	1 bank of 16 entries	1 bank of 16 entries
256 color	2 banks of 8 entries	2 banks of 8 entries	4 banks of 4 entries

Indicates the look-up table is not used for that display mode

The following depictions are intended to show the display data output path only. The CPU R/W access to the individual Look-Up Tables is not affected by the various “banking” configurations.

12.1 Gray Shade Display Modes

1 Bit-Per-Pixel Mode

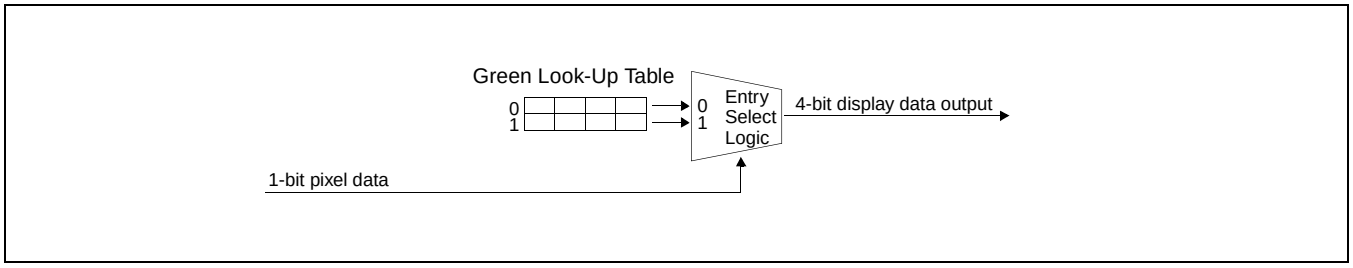
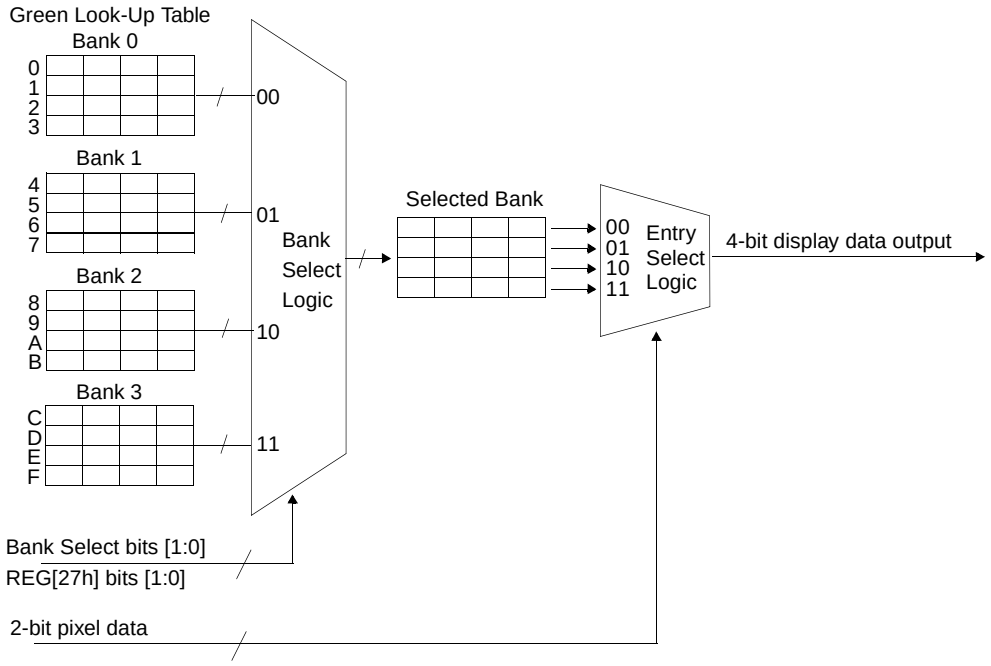


Figure 12-1: 1 Bit-Per-Pixel – 2-Level Gray-Shade Mode Look-Up Table Architecture

2 Bit-Per-Pixel Mode



Note: the above depiction is intended to show the display data output path only. The CPU R/W access to the individual Look-Up Tables is not affected by the various "banking" configurations.

Figure 12-2: 2 Bit-Per-Pixel – 4-Level Gray-Shade Mode Look-Up Table Architecture

4 Bit-Per-Pixel Mode

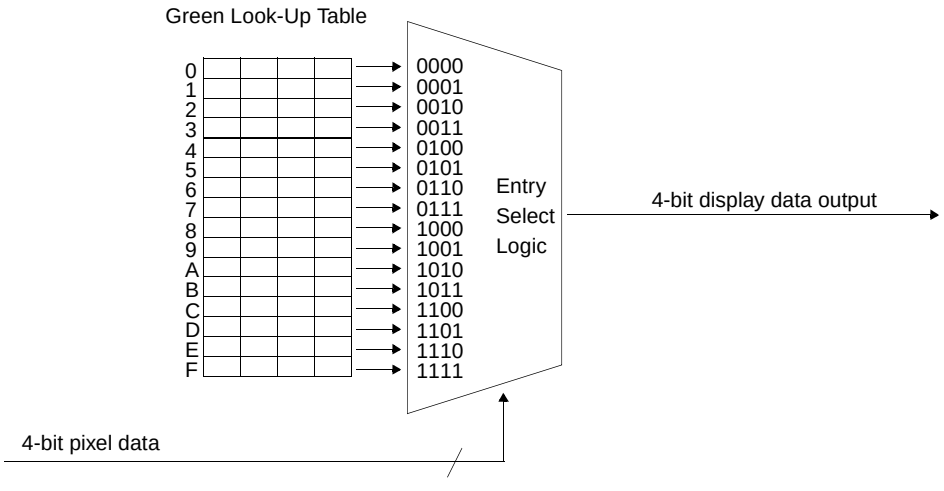


Figure 12-3: 4 Bit-Per-Pixel – 16-Level Gray-Shade Mode Look-Up Table Architecture

12.2 Color Display Modes

1 Bit-Per-Pixel Color Mode

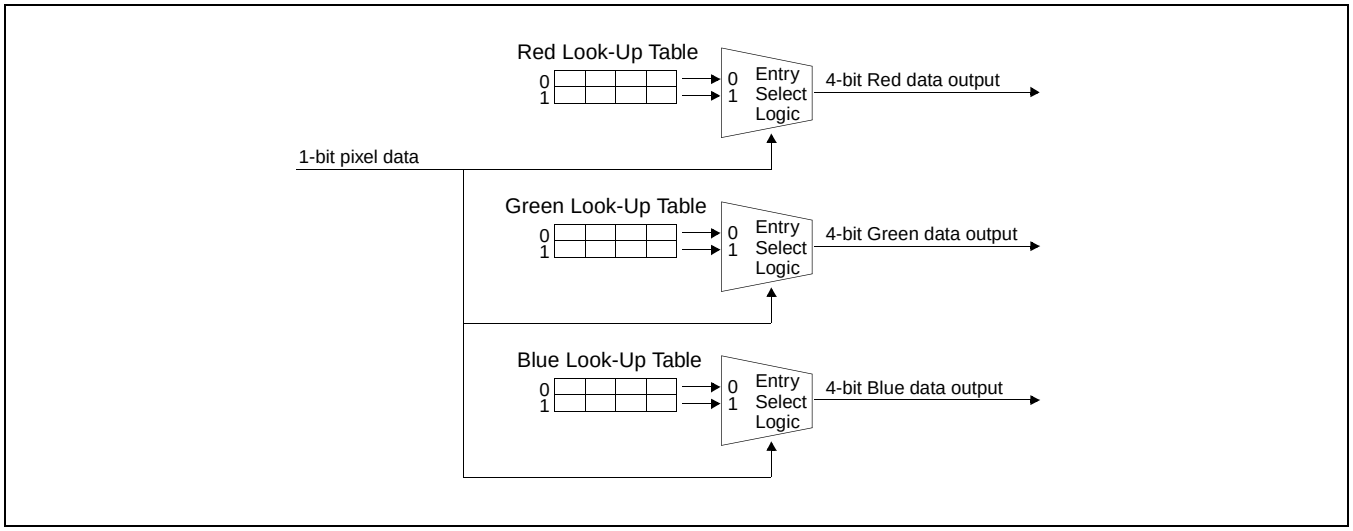


Figure 12-4: 1 Bit-Per-Pixel – 2-Level Color Look-Up Table Architecture

2 Bit-Per-Pixel Color Mode

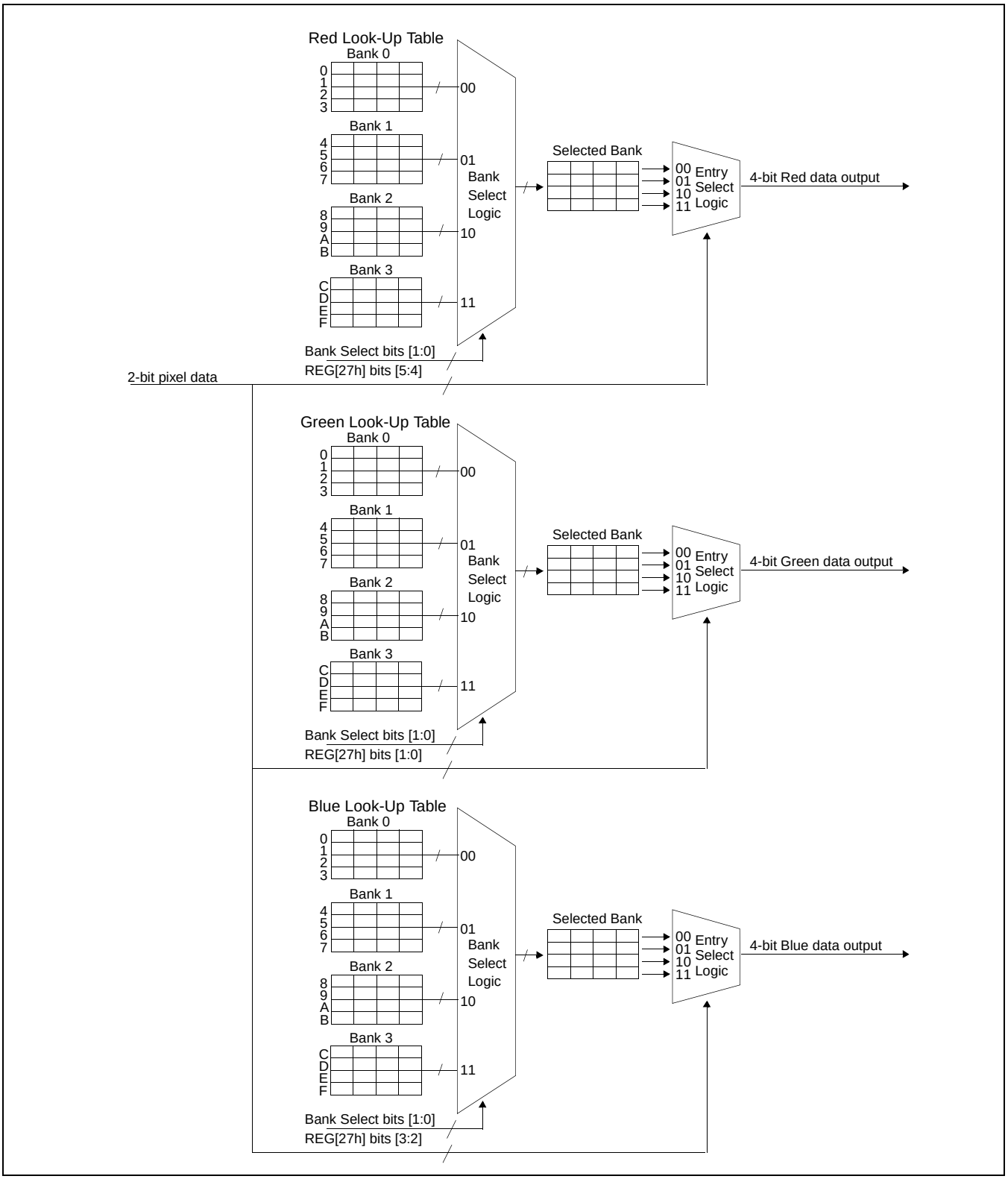


Figure 12-5: 2 Bit-Per-Pixel – 4-Level Color Mode Look-Up Table Architecture

4 Bit-Per-Pixel Color Mode

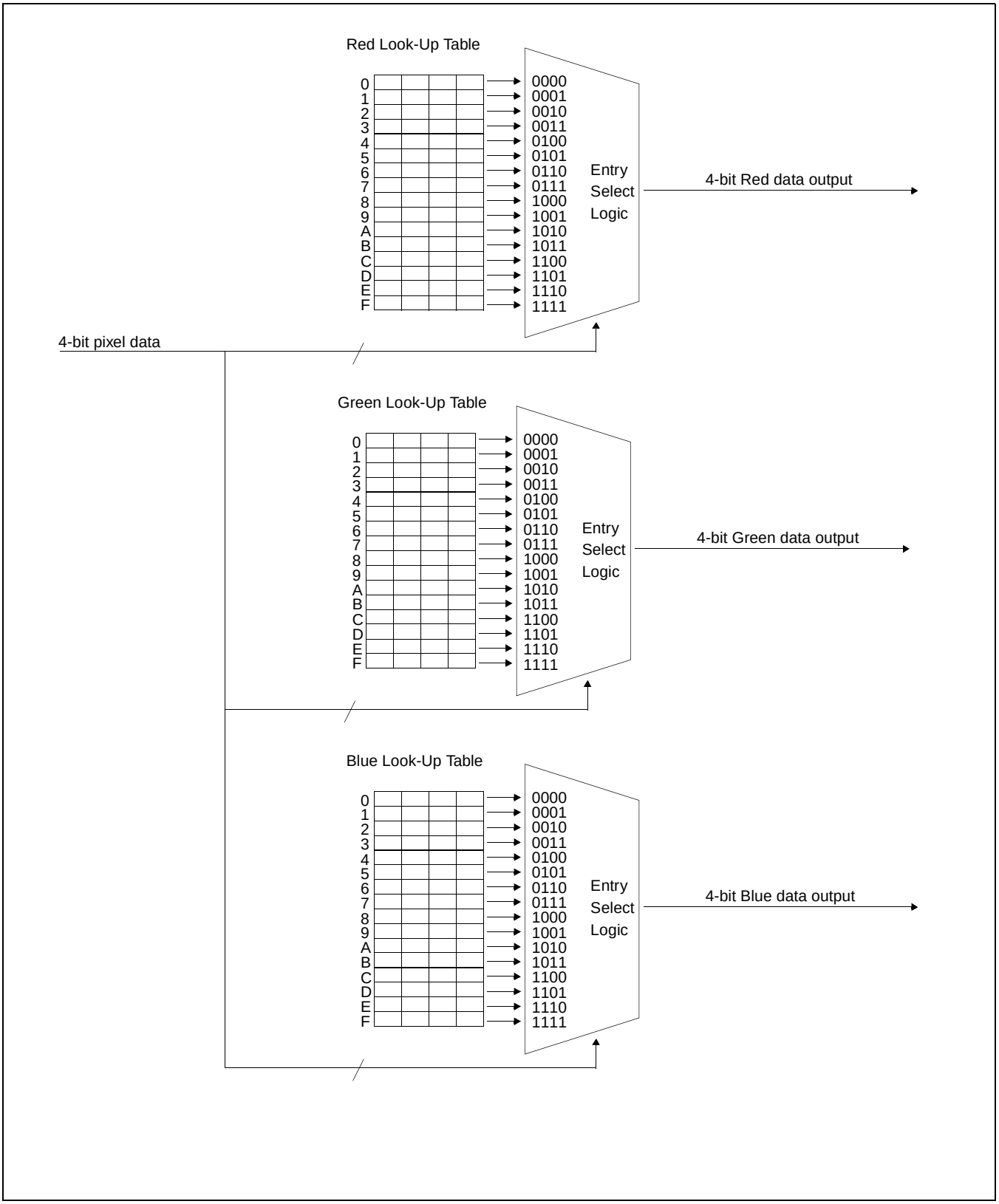


Figure 12-6: 4 Bit-Per-Pixel – 16-Level Color Mode Look-Up Table Architecture

8 Bit-Per-Pixel Color Mode

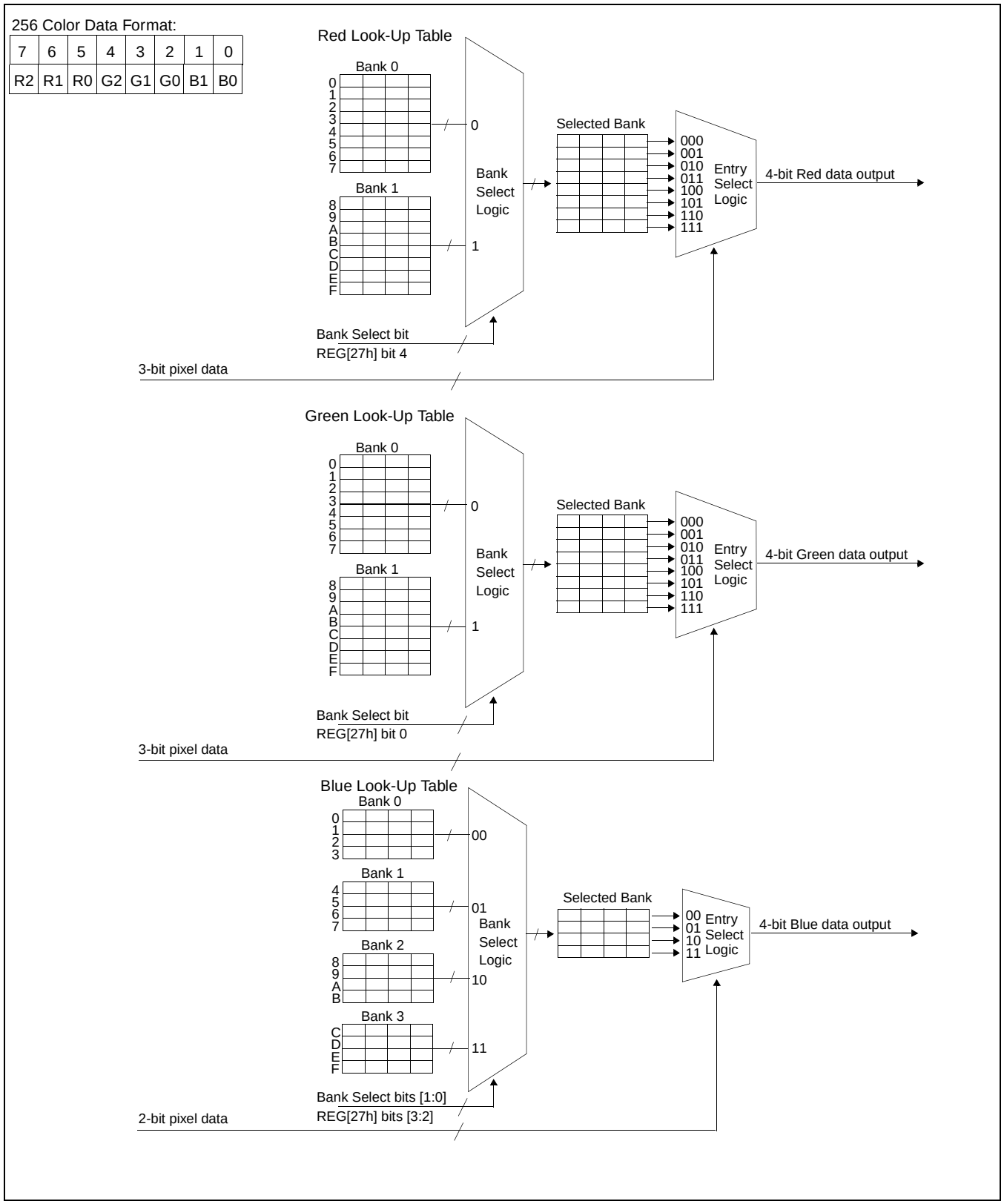


Figure 12-7: 8 Bit-Per-Pixel – 256-Level Color Mode Look-Up Table Architecture

13 Power Save Modes

Two Power Save Modes have been incorporated into the S1D13504 to accommodate the important need for power reduction in the hand-held devices market. These modes are hardware suspend and software suspend.

13.1 Hardware Suspend

- Register read/write disallowed.
- Memory read/write disallowed.
- LCD outputs are forced low (see Note 1 of Section 13.4, *"Pin States in Power Save Modes"* on page 128).
- LCDPWR forced to Off state.
- CRT outputs are disabled.
- If suspend mode CBR refresh is selected, all internal modules and clocks except the Memory I/F are shut down.
- If suspend mode self-refresh or no-refresh is selected, all internal modules and clocks are shut down.

13.2 Software Suspend

- Register read/write allowed except for RAMDAC registers.
- Memory read/write disallowed.
- LCD outputs are forced low (see Note 1 of Section 13.4, *"Pin States in Power Save Modes"* on page 128).
- LCDPWR forced to Off state.
- CRT outputs are disabled.
- If suspend mode CBR refresh is selected, all internal modules and clocks except the Host Bus I/F and the Memory I/F are shut down.
- If suspend mode self-refresh or no-refresh is selected, all internal modules and clocks except the Host Bus I/F are shut down.

13.3 Power Save Mode Function Summary

Table 13-1: Power Save Mode Function Summary

Function	Power Save Mode (PSM)		
	Normal (Active)	**Software Suspend**	**Hardware Suspend**
Display Active?	Yes	No	No
Register Access Possible?	Yes	Yes (1)	No
Memory Access Possible?	Yes	No	No
Host Bus Interface Running?	Yes	Yes	No
Memory Interface Running?	Yes	No (2)	No (2)

Note

(1) except for RAMDAC registers.
(2) Yes if CBR suspend mode refresh is selected.

13.4 Pin States in Power Save Modes

Table 13-2: Pin States in Power Save Modes

Pins	Pin State		
	Normal (Active)	**Software Suspend**	**Hardware Suspend**
LCD outputs	Active	Forced Low (1)	Forced Low (1)
LCDPWR	On	Off	Off
DRAM outputs	Active	Refresh Only (2)	Refresh Only (2)
CRT / DAC outputs	Active	Disabled (3)	Disabled (3)
Host Interface outputs	Active	Active (4)	Disabled

Note

1. FPFRAME and FPLINE are forced to their inactive states as defined by REG[0Ch] bit 6 and REG[07h] bit 6 respectively.
2. Selectable: may be CBR refresh, self-refresh or no refresh at all.
3. DACWR#, DACRD#, DACRS0, DACRS1 are active but DACCLK is disabled.
4. Active for non-DAC register access only.

14 Mechanical Data

14.1 QFP15-128 (S1D13504F00A)

QFP15 - 128 pin **Unit: mm**

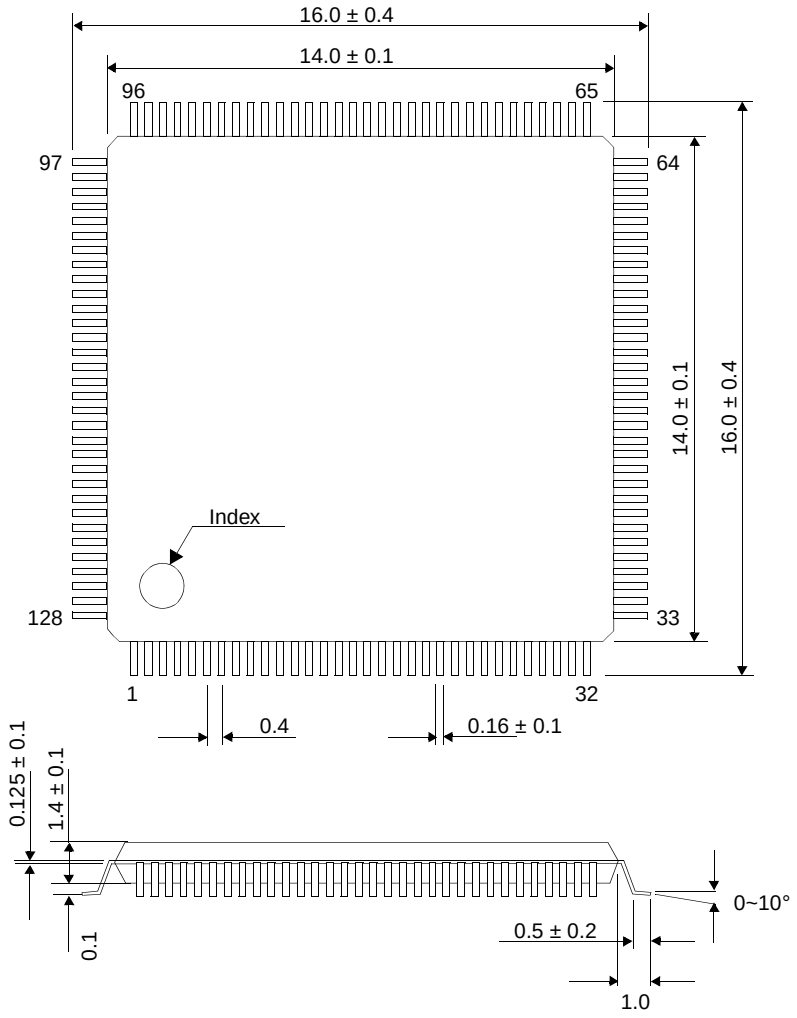


Figure 14-1: Mechanical Drawing QFP15-128

14.2 TQFP15-128 (S1D13504F01A)

TQFP15 - 128 pin **Unit: mm**

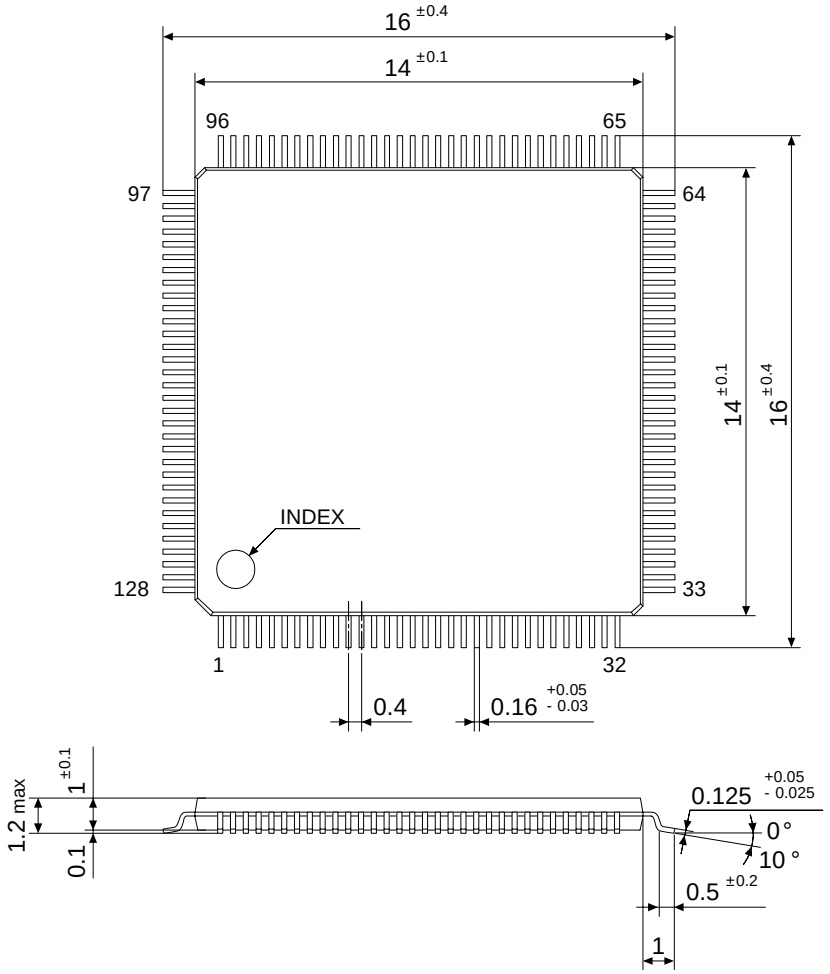


Figure 14-2: Mechanical Drawing TQFP15-128

14.3 QFP20-144 (S1D13504F02A)

QFP20 - 144 pin **Unit: mm**

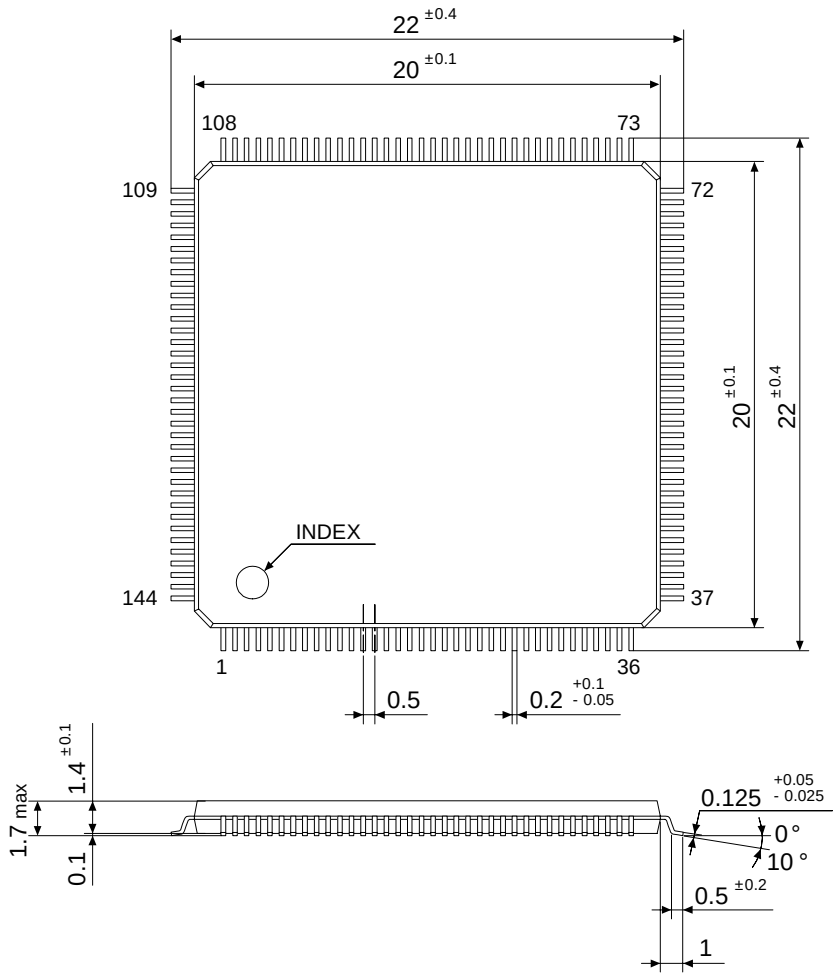


Figure 14-3: Mechanical Drawing QFP20-144

15 References

The following documents contain additional information related to the S1D13504. Document numbers are listed in parenthesis after the document name. All documents can be found at the Epson Research and Development Website at **www.erd.epson.com**.

- S1D13504 Product Brief (X19A-C-002-xx)
- S1D13504 Windows CE v2.x Display Drivers (X19A-E-001-xx)
- S1D13504 Wind River WindML v2.0 Display Drivers (X19A-E-002-xx)
- S1D13504 Wind River UGL v1.2 Display Drivers (X19A-E-003-xx)
- S1D13504 Programming Notes And Examples (X19A-G-002-xx)
- S5U13504B00C Evaluation Board User Manual (X19A-G-004-xx)
- Interfacing to the Philips MIPS PR31500/PR31700 Microprocessor (X19A-G-005-xx)
- S1D13504 Power Consumption (X19A-G-006-xx)
- Interfacing to the NEC VR4102 Microprocessors (X19A-G-007-xx)
- Interfacing to the ODO Display Card Interface (X19A-G-008-xx)
- Interfacing to the PC Card Bus (X19A-G-009-xx)
- Interfacing to the Motorola MPC821 Microprocessor (X19A-G-010-xx)
- Interfacing to the Motorola MCF5307 “Coldfire” Microprocessors (X19A-G-011-xx)
- Interfacing to the Toshiba TX3912 Microprocessor (X19A-G-012-xx)
- Interfacing to the Motorola MC68328 “Dragonball” Microprocessor (X19A-G-013-xx)
- S1D13504 Register Summary (X19A-Q-001-xx)

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