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S1D13505 Embedded RAMDAC LCD/CRT Controller

Hardware Functional Specification

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1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13505 Embedded RAMDAC LCD/CRT Controller. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

This specification will be updated as appropriate. Please check the Epson Electronics America Website at http://www.eea.epson.com or the Epson Research and Development website at http://www.erd.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

1.2 Overview Description

The S1D13505 is a color/monochrome LCD/CRT graphics controller interfacing to a wide range of CPUs and display devices. The S1D13505 architecture is designed to meet the low cost, low power requirements of the embedded markets, such as Mobile Communications, Hand-Held PCs, and Office Automation.

The S1D13505 supports multiple CPUs, all LCD panel types, CRT, and additionally provides a number of differentiating features. Products requiring a “Portrait” mode display can take advantage of the SwivelView™ feature. Simultaneous, Virtual and Split Screen Display are just some of the display modes supported, while the Hardware Cursor, Ink Layer, and the Memory Enhancement Registers offer substantial performance benefits. These features, combined with the S1D13505’s Operating System independence, make it an ideal display solution for a wide variety of applications.

2 Features

2.1 Memory Interface

- 16-bit DRAM interface:
  - EDO-DRAM up to 40MHz data rate (80M bytes/sec.).
  - FPM-DRAM up to 25MHz data rate (50M bytes/sec.).
- Memory size options:
  - 512K bytes using one 256K×16 device.
  - 2M bytes using one 1M×16 device.
- Performance Enhancement Register to tailor the memory control output timing for the DRAM device.

2.2 CPU Interface

- Supports the following interfaces:
  - 8/16-bit SH-4 bus interface.
  - 8/16-bit SH-3 bus interface.
  - 8/16-bit interface to 8/16/32-bit MC68000 microprocessors/microcontrollers.
  - 8/16-bit interface to 8/16/32-bit MC68030 microprocessors/microcontrollers.
  - Philips PR31500/PR31700 (MIPS).
  - Toshiba TX3912 (MIPS)
  - 16-bit Power PC (MPC821) microprocessor.
  - 16-bit Epson E0C33 microprocessor.
  - PC Card (PCMCIA).
  - StrongARM (PC Card).
  - NEC VR41xx (MIPS).
  - ISA bus.
- Supports the following interface with external logic:
  - GX486 microprocessor.
- One-stage write buffer for minimum wait-state CPU writes.
- Registers are memory-mapped – the M/R# pin selects between the display buffer and register address space.
- The complete 2M byte display buffer address space is addressable as a single linear address space through the 21-bit address bus.

2.3 Display Support

- 4/8-bit monochrome passive LCD interface.
- 4/8/16-bit color passive LCD interface.
- Single-panel, single-drive displays.
- Dual-panel, dual-drive displays.
- Direct support for 9/12-bit TFT/D-TFD; 18-bit TFT/D-TFD is supported up to 64K color depth (16-bit data).
- Embedded RAMDAC (DAC)with direct analog CRT drive.
- Simultaneous display of CRT and passive or TFT/D-TFD panels.

2.4 Display Modes

- 1/2/4/8/15/16 bit-per-pixel (bpp) support on LCD/CRT.
- Up to 16 shades of gray using FRM on monochrome passive LCD panels.
- Up to 4096 colors on passive LCD panels; three 256x4 Look-Up Tables (LUT) are used to map 1/2/4/8 bpp modes into these colors, 15/16 bpp modes are mapped directly using the 4 most significant bits of the red, green and blue colors.
- Up to 64K colors on TFT/D-TFD LCD panels and CRT; three 256x4 Look-Up Tables are used to map 1/2/4/8 bpp modes into 4096 colors, 15/16 bpp modes are mapped directly.

2.5 Display Features

- SwivelView™: direct hardware 90° rotation of display image for “portrait” mode display.
- Split Screen Display: allows two different images to be simultaneously viewed on the same display.
- Virtual Display Support: displays images larger than the display size through the use of panning.
- Double Buffering/multi-pages: provides smooth animation and instantaneous screen update.
- Acceleration of screen updates by allocating full display memory bandwidth to CPU (see REG[23h] bit 7).
- Hardware 64x64 pixel 2-bit cursor or full screen 2-bit ink layer.
- Simultaneous display of CRT and passive panel or TFT/D-TFD panel.
  - Normal mode for cases where LCD and CRT screen sizes are identical.
  - Line-doubling for simultaneous display of 240-line images on 240-line LCD and 480-line CRT.
  - Even-scan or interlace modes for simultaneous display of 480-line images on 240-line LCD and 480-line CRT.

2.6 Clock Source

- Single clock input for both the pixel and memory clocks.
- Memory clock can be input clock or (input clock/2), providing flexibility to use CPU bus clock as input.
- Pixel clock can be the memory clock, (memory clock/2), (memory clock/3) or (memory clock/4).

2.7 Miscellaneous

- The memory data bus, MD[15:0], is used to configure the chip at power-on.
- Three General Purpose Input/Output pins, GPIO[3:1], are available if the upper Memory Address pins are not required for asymmetric DRAM support.
- Suspend power save mode can be initiated by either hardware or software.
- The SUSPEND# pin is used either as an input to initiate Suspend mode, or as a General Purpose Output that can be used to control the LCD backlight. Power-on polarity is selected by an MD configuration pin.
- Operating voltages from 2.7 volts to 5.5 volts are supported
- 128-pin QFP15 surface mount package

3 Typical System Implementation Diagrams

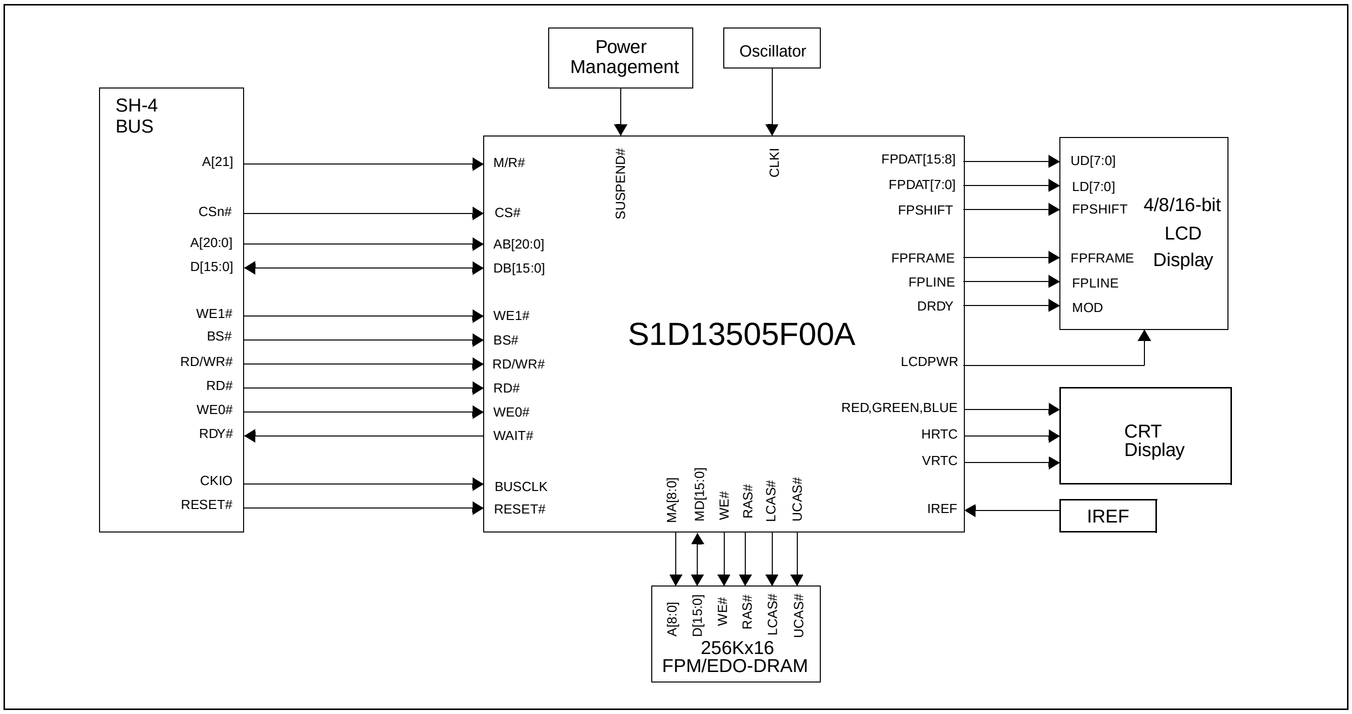


Figure 3-1: Typical System Diagram (SH-4 Bus)

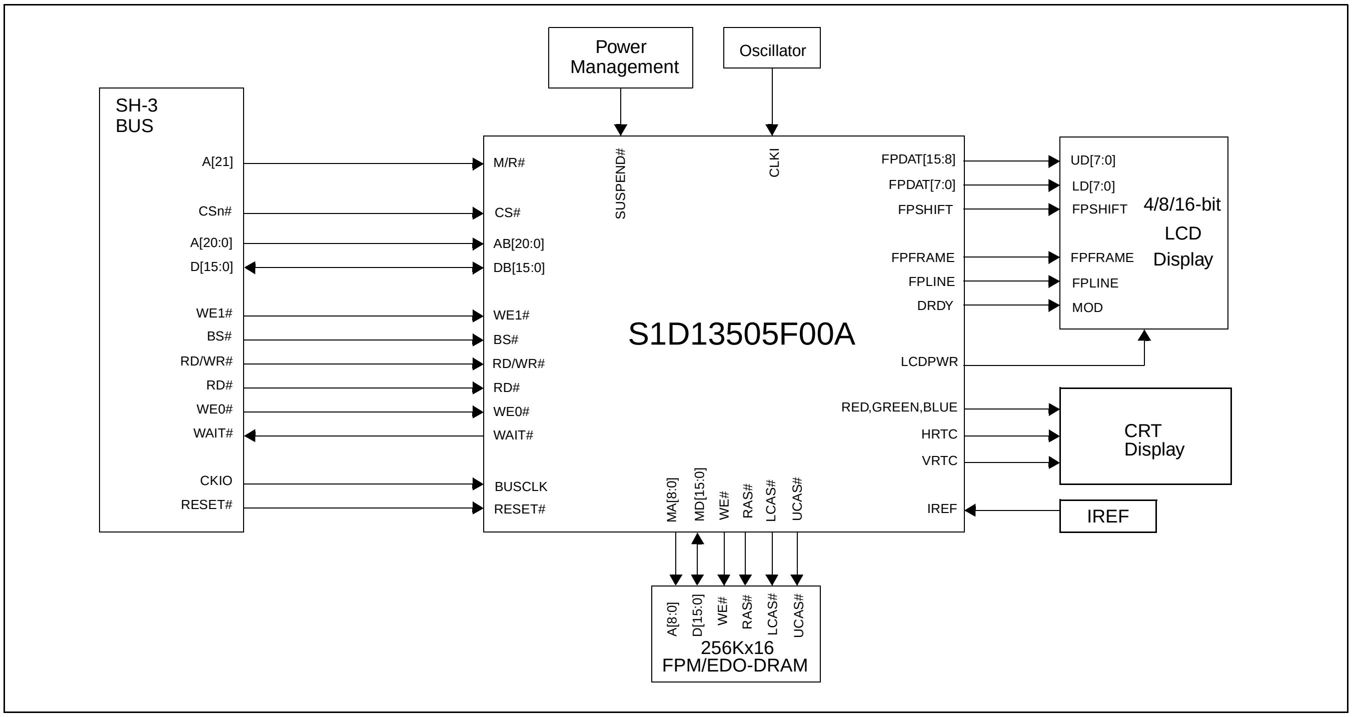


Figure 3-2: Typical System Diagram (SH-3 Bus)

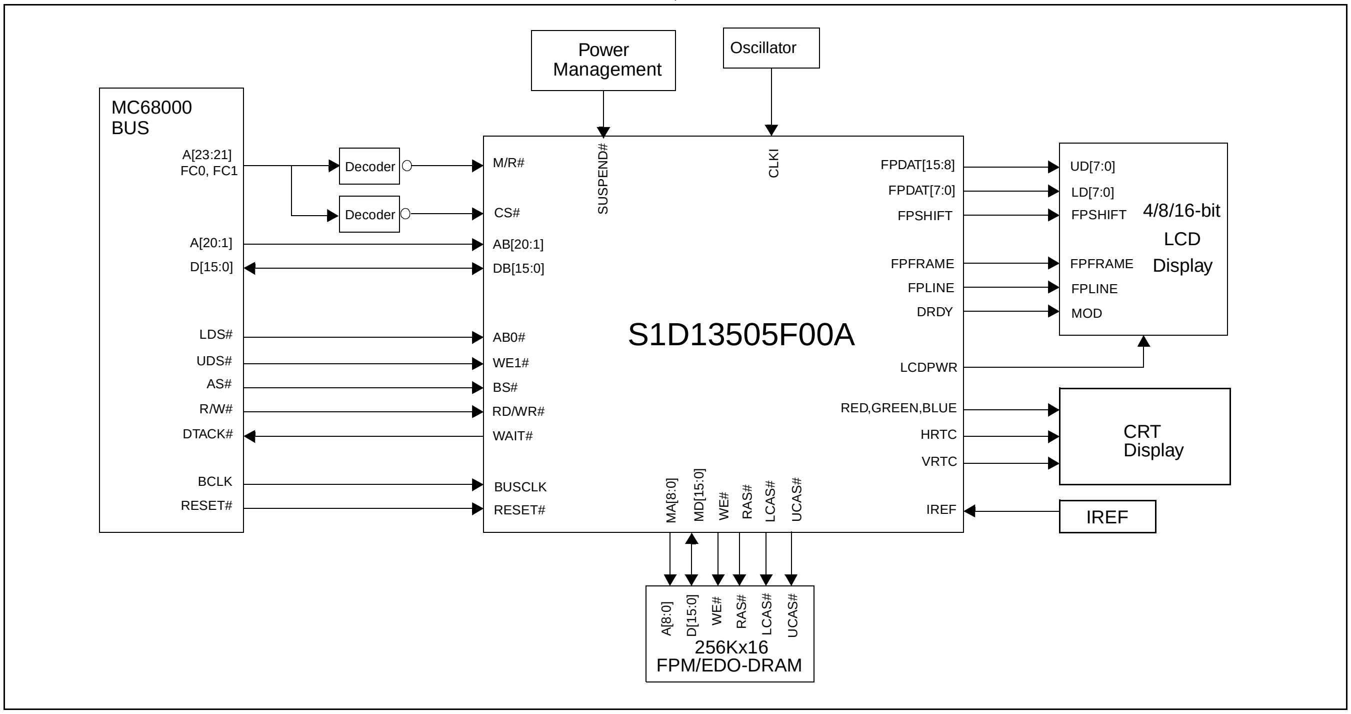


Figure 3-3: Typical System Diagram (MC68K Bus 1, 16-Bit 68000)

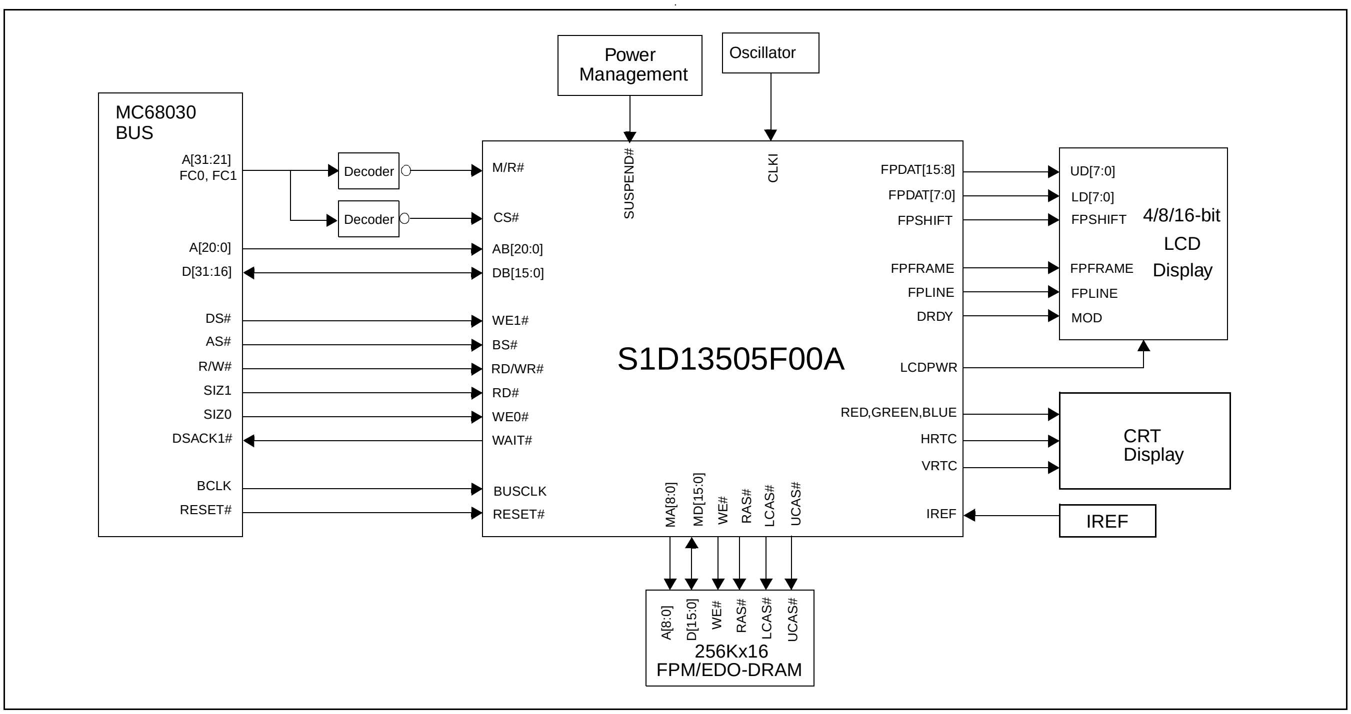


Figure 3-4: Typical System Diagram (MC68K Bus 2, 32-Bit 68030)

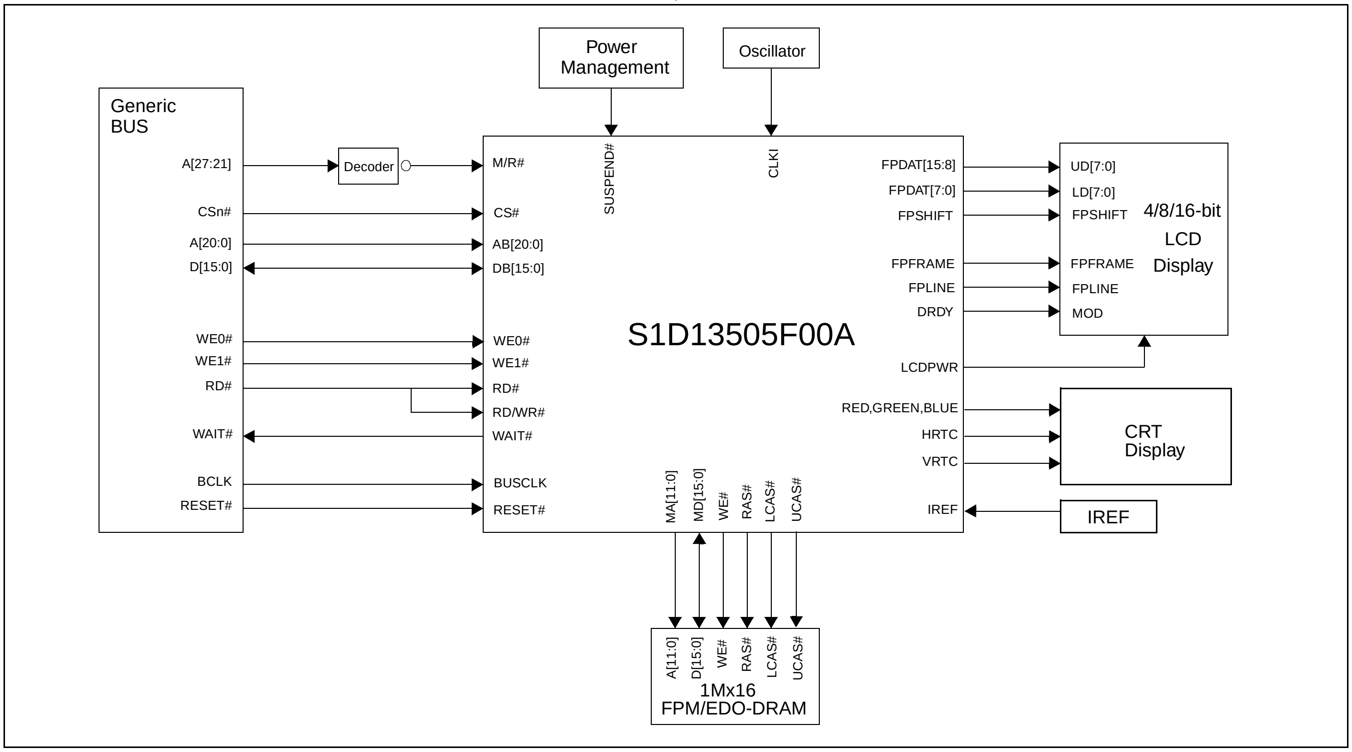


Figure 3-5: Typical System Diagram (Generic Bus)

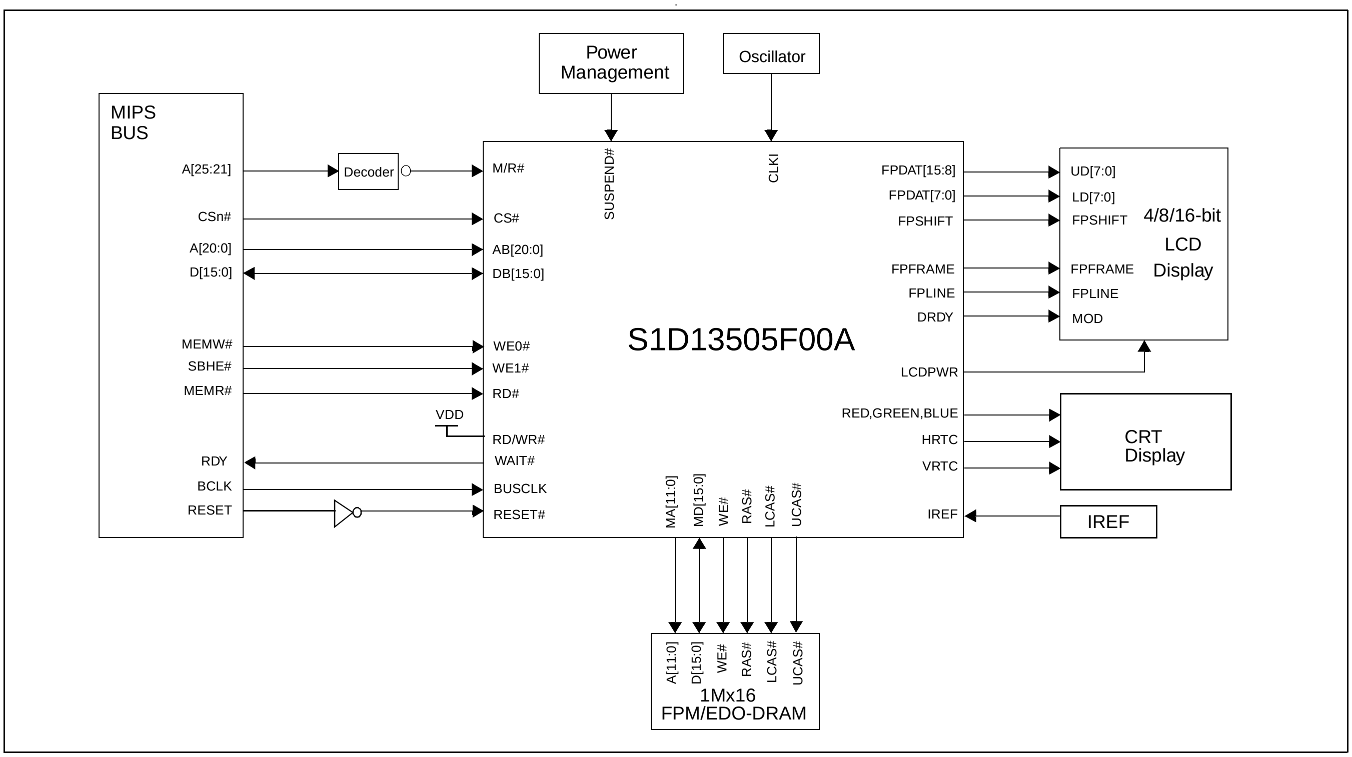


Figure 3-6: Typical System Diagram (NEC VR41xx (MIPS) Bus)

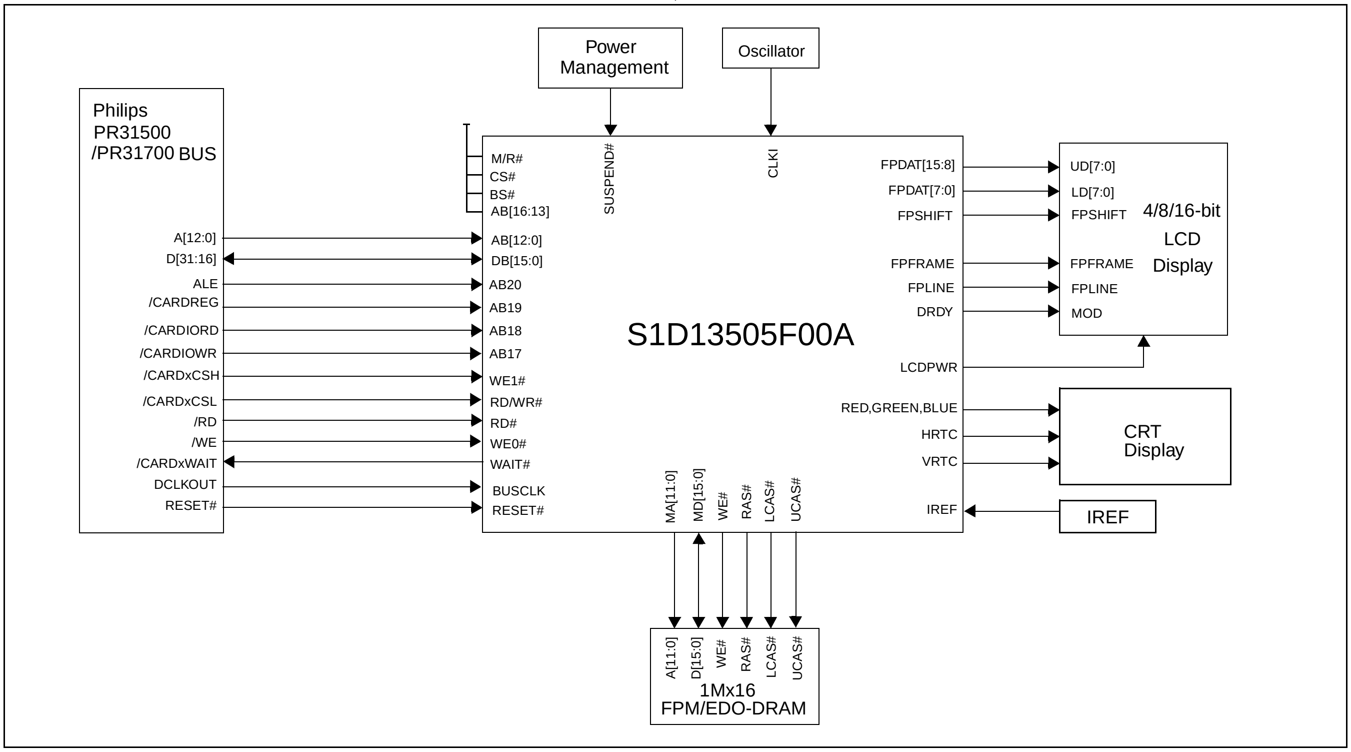


Figure 3-7: Typical System Diagram (Philips PR31500/PR31700 Bus)

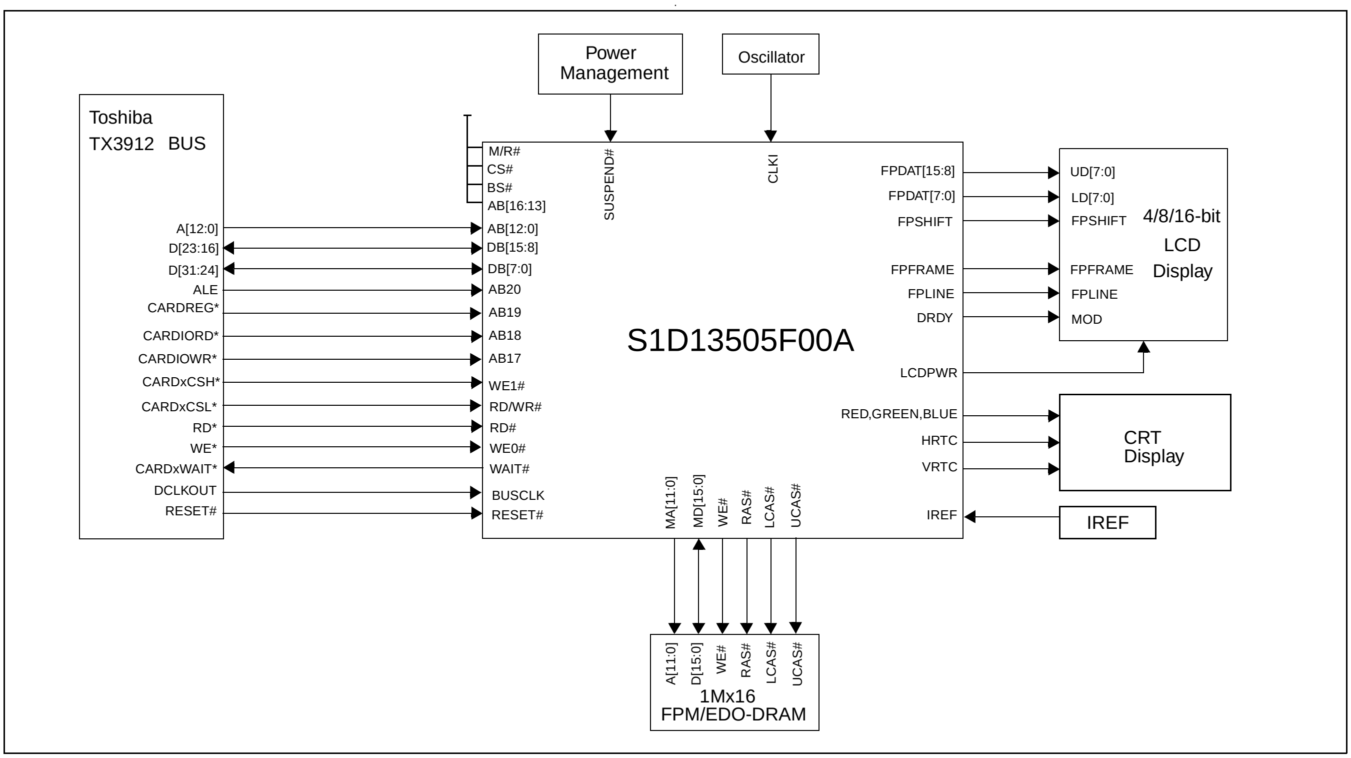


Figure 3-8: Typical System Diagram (Toshiba TX3912 Bus)

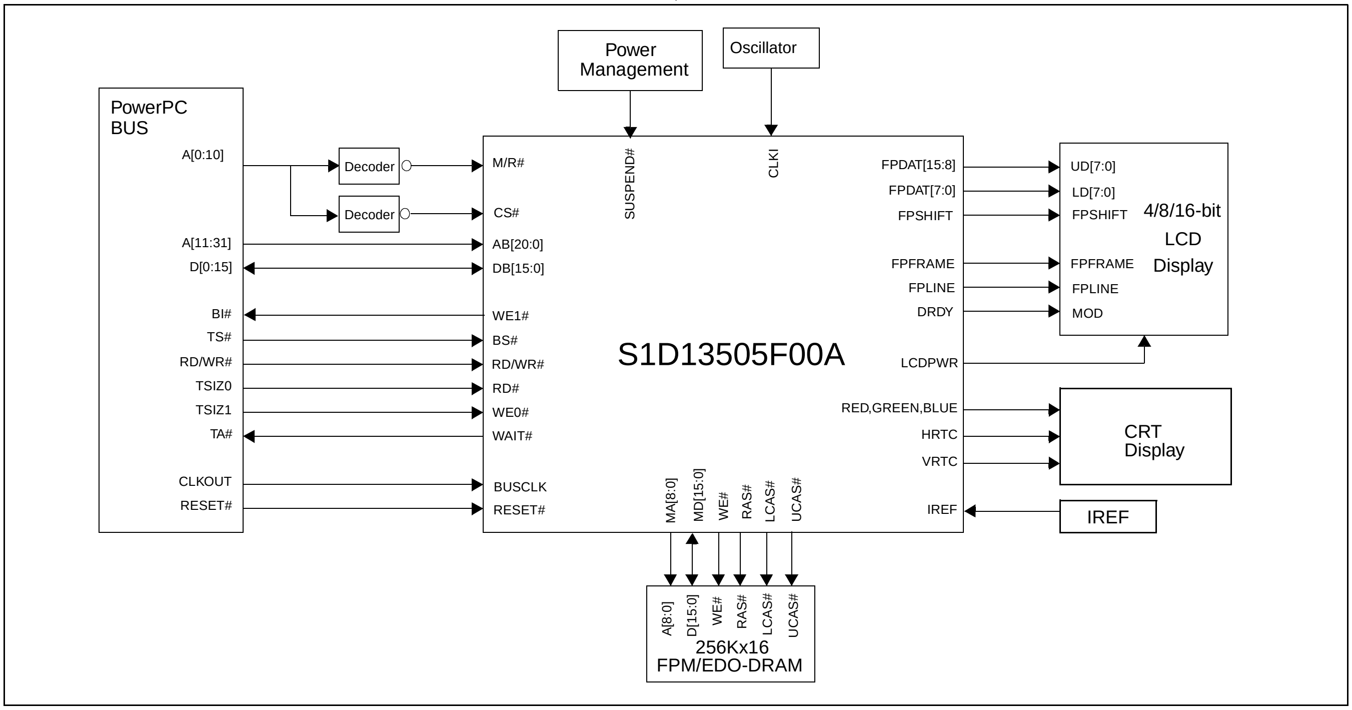


Figure 3-9: Typical System Diagram (Power PC Bus)

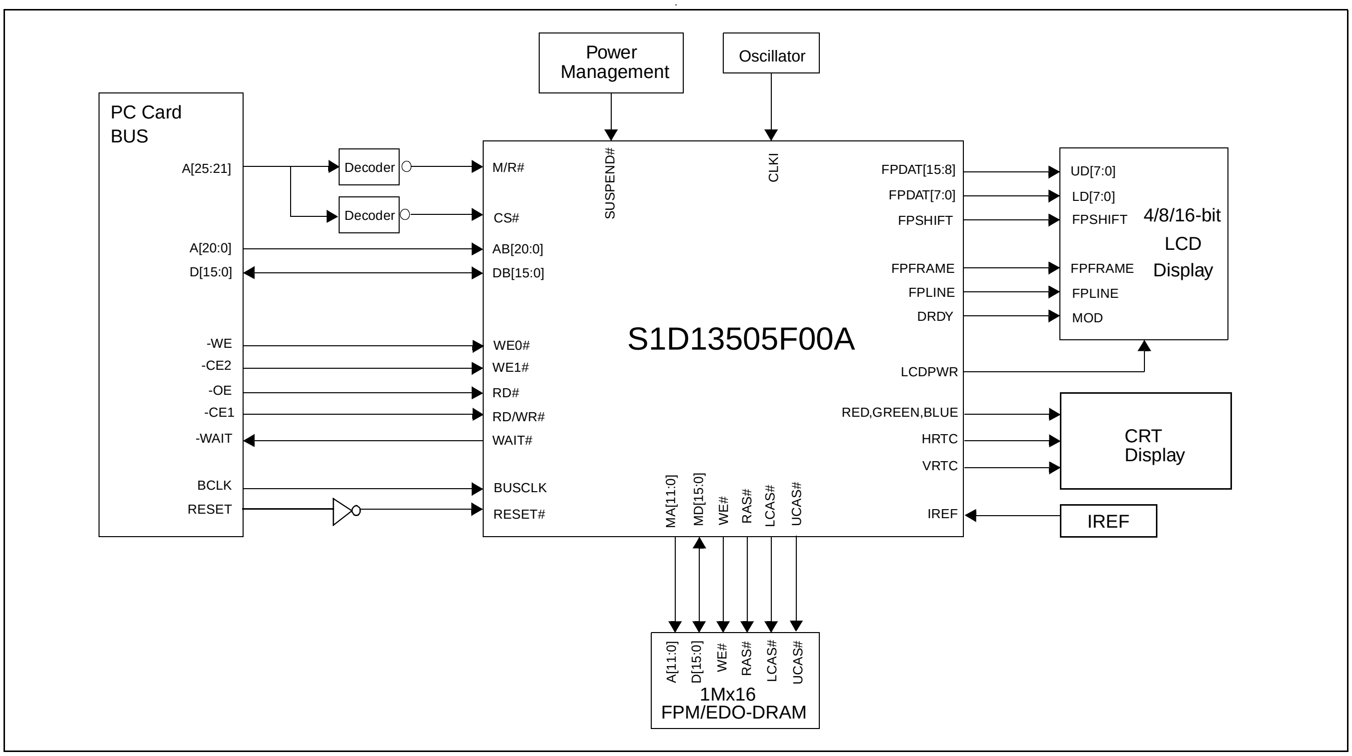
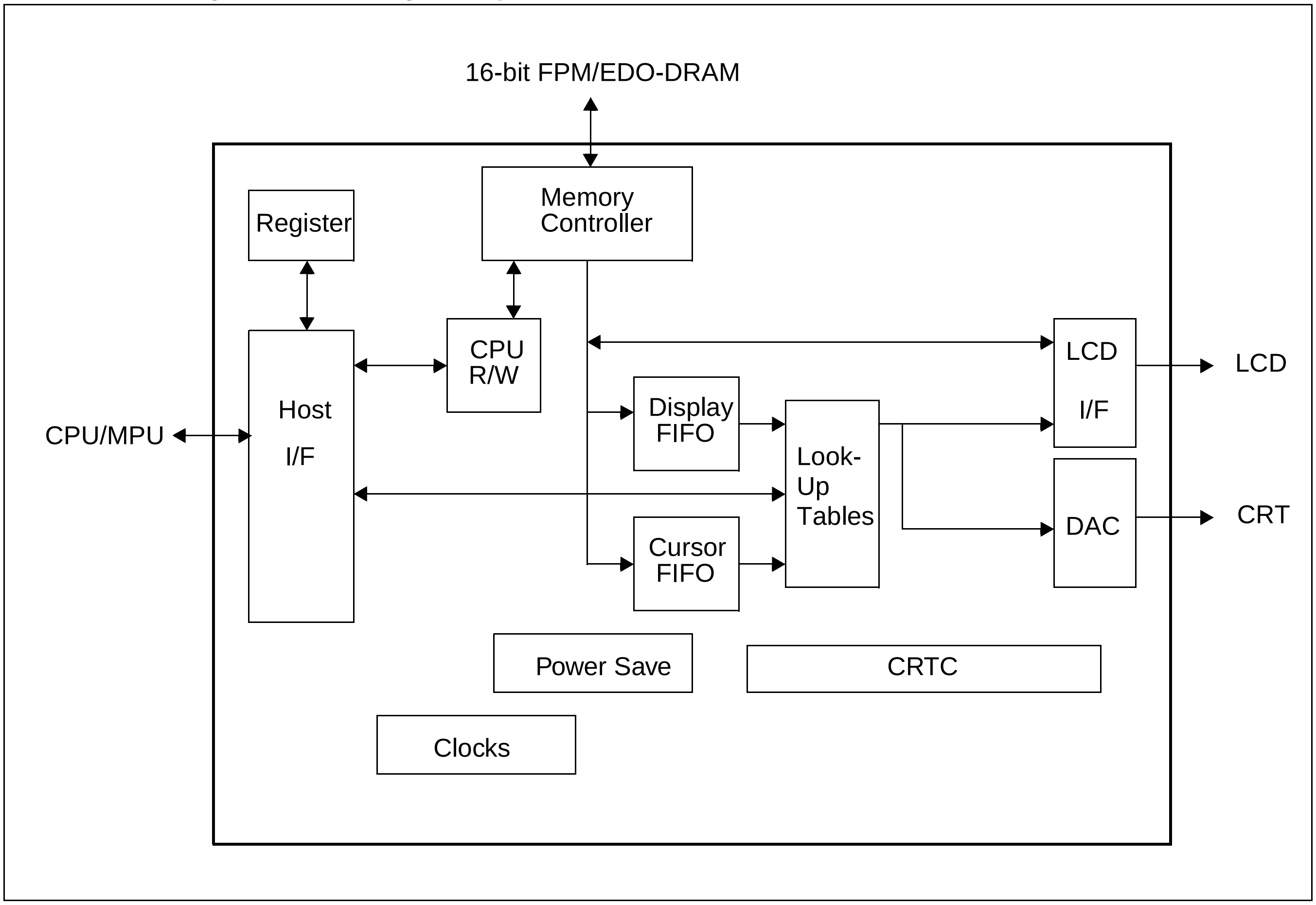


Figure 3-10: Typical System Diagram (PC Card (PCMCIA) Bus)

4 Internal Description

4.1 Block Diagram Showing Datapaths



4.2 Block Descriptions

4.2.1 Register

The Register block contains all the register latches

4.2.2 Host Interface

The Host Interface (I/F) block provides the means for the CPU/MPU to communicate with the display buffer and internal registers via one of the supported bus interfaces.

4.2.3 CPU R/W

The CPU R/W block synchronizes the CPU requests for display buffer access. If SwivelView is enabled, the data is rotated in this block.

4.2.4 Memory Controller

The Memory Controller block arbitrates between CPU accesses and display refresh accesses as well as generates the necessary signals to interface to one of the supported 16-bit memory devices (FPM-DRAM or EDO-DRAM).

4.2.5 Display FIFO

The Display FIFO block fetches display data from the Memory Controller for display refresh.

4.2.6 Cursor FIFO

The Cursor FIFO block fetches Cursor/ink data from the Memory Controller for display refresh.

4.2.7 Look-Up Tables

The Look-Up Tables block contains three 256x4 Look-Up Tables (LUT), one for each primary color. In monochrome mode, only the green LUT is selected and used. This block contains anti-sparkle circuitry. The cursor/ink and display data are merged in this block.

4.2.8 CRTC

The CRTC generates the sync timing for the LCD and CRT, defining the vertical and horizontal display periods.

4.2.9 LCD Interface

The LCD Interface block performs Frame Rate Modulation (FRM) for passive LCD panels and generates the correct data format and timing control signals for various LCD and TFT/D-TFD panels.

4.2.10 DAC

The DAC is the Digital to Analog converter for analog CRT support.

4.2.11 Power Save

The Power Save block contains the power save mode circuitry.

4.2.12 Clocks

The Clocks module is the source of all clocks in the chip.

5 Pins

5.1 Pinout Diagram

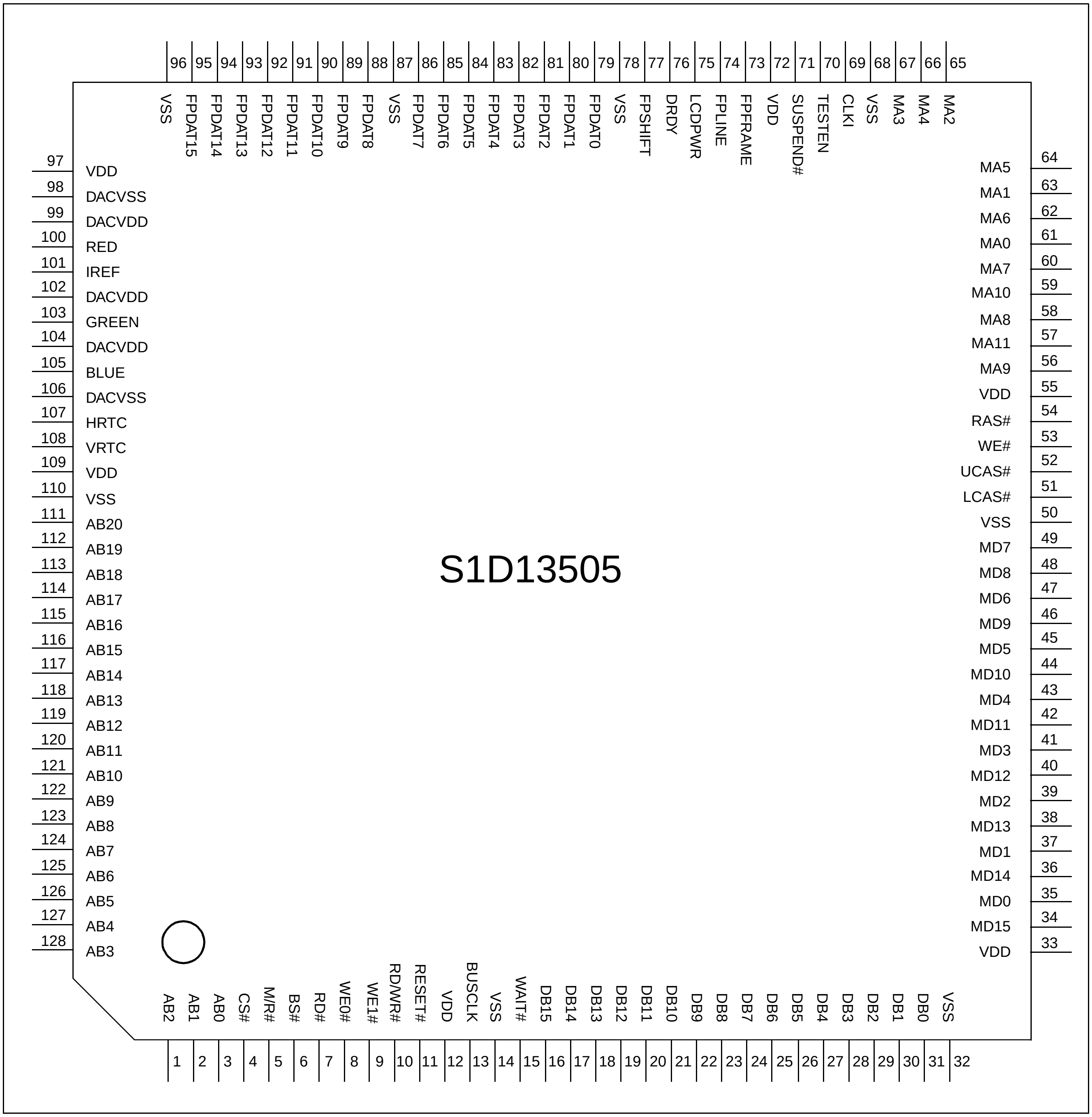


Figure 5-1: Pinout Diagram

128-pin QFP15 surface mount package

5.2 Pin Description

Key:

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
A	=	Analog
P	=	Power pin
C	=	CMOS level input
CD	=	CMOS level input with pull down resistor (typical values of 100KΩ/180KΩ at 5V/3.3V respectively)
CS	=	CMOS level Schmitt input
COx	=	CMOS output driver, x denotes driver type (see tables 6-3, 6-4, 6-5 for details)
TSx	=	Tri-state CMOS output driver, x denotes driver type (see tables 6-3, 6-4, 6-5 for details)
TSxD	=	Tri-state CMOS output driver with pull down resistor (typical values of 100KΩ/180KΩ at 5V/3.3V) respectively), x denotes driver type (see tables 6-3, 6-4, 6-5 for details)
CNx	=	CMOS low-noise output driver, x denotes driver type (see tables 6-3, 6-4, 6-5 for details)

5.2.1 Host Interface

Table 5-1: Host Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
AB0	I	3	CS	Hi-Z	• For SH-3/SH-4 Bus, this pin inputs system address bit 0 (A0). • For MC68K Bus 1, this pin inputs the lower data strobe (LDS#). • For MC68K Bus 2, this pin inputs system address bit 0 (A0). • For Generic Bus, this pin inputs system address bit 0 (A0). • For MIPS/ISA Bus, this pin inputs system address bit 0 (SA0). • For Philips PR31500/31700 Bus, this pin inputs system address bit 0 (A0). • For Toshiba TX3912 Bus, this pin inputs system address bit 0 (A0). • For PowerPC Bus, this pin inputs system address bit 31 (A31). • For PC Card (PCMCIA) Bus, this pin inputs system address bit 0 (A0). See *"Host Bus Interface Pin Mapping"* for summary. See the respective AC Timing diagram for detailed functionality.
AB[12:1]	I	119-128, 1, 2	C	Hi-Z	• For PowerPC Bus, these pins input the system address bits 19 through 30 (A[19:30]). • For all other busses, these pins input the system address bits 12 through 1 (A[12:1]). See *"Host Bus Interface Pin Mapping"* for summary. See the respective AC Timing diagram for detailed functionality.

Table 5-1: Host Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #	Cell	RESET# State	Description
AB[16:13]	I	115-118	C	Hi-Z	• For Philips PR31500/31700 Bus, these pins are connected to V_{DD}. • For Toshiba TX3912 Bus, these pins are connected to V_{DD}. • For PowerPC Bus, these pins input the system address bits 15 through 18 (A[15:18]). • For all other busses, these pins input the system address bits 16 through 13 (A[16:13]). See *“Host Bus Interface Pin Mapping”* for summary. See the respective AC Timing diagram for detailed functionality.
AB17	I	114	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin inputs the IO write command (/CARDIOWR). • For Toshiba TX3912 Bus, this pin inputs the IO write command (CARDIOWR*). • For PowerPC Bus, this pin inputs the system address bit 14 (A14). • For all other busses, this pin inputs the system address bit 17 (A17). See *“Host Bus Interface Pin Mapping”* for summary. See the respective AC Timing diagram for detailed functionality.
AB18	I	113	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin inputs the IO read command (/CARDIORD). • For Toshiba TX3912 Bus, this pin inputs the IO read command (CARDIORD*). • For PowerPC Bus, this pin inputs the system address bit 13 (A13). • For all other busses, this pin inputs the system address bit 18 (A18). See *“Host Bus Interface Pin Mapping”* for summary. See the respective AC Timing diagram for detailed functionality.
AB19	I	112	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin inputs the card control register access (/CARDREG). • For Toshiba TX3912 Bus, this pin inputs the card control register (CARDREG*). • For PowerPC Bus, this pin inputs the system address bit 12 (A12). • For all other busses, this pin inputs the system address bit 19 (A19). See *“Host Bus Interface Pin Mapping”* for summary. See the respective AC Timing diagram for detailed functionality.
AB20	I	111	C	Hi-Z	• For the MIPS/ISA Bus, this pin inputs system address bit 20. Note that for the ISA Bus, the unlatched LA20 must first be latched before input to AB20. • For Philips PR31500/31700 Bus, this pin inputs the address latch enable (ALE). • For Toshiba TX3912 Bus, this pin inputs the address latch enable (ALE). • For PowerPC Bus, this pin inputs the system address bit 11 (A11). • For all other busses, this pin inputs the system address bit 20 (A20). See *“Host Bus Interface Pin Mapping”* for summary. See the respective AC Timing diagram for detailed functionality.

Table 5-1: Host Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #	Cell	RESET# State	Description
DB[15:0]	IO	16-31	C/TS2	Hi-Z	These pins are the system data bus. For 8-bit bus modes, unused data pins should be tied to V_{DD}. • For SH-3/SH-4 Bus, these pins are connected to D[15:0]. • For MC68K Bus 1, these pins are connected to D[15:0]. • For MC68K Bus 2, these pins are connected to D[31:16] for 32-bit devices (e.g. MC68030) or D[15:0] for 16-bit devices (e.g. MC68340). • For Generic Bus, these pins are connected to D[15:0]. • For MIPS/ISA Bus, these pins are connected to SD[15:0]. • For Philips PR31500/31700 Bus, these pins are connected to D[31:16]. • For Toshiba TX3912 Bus, pins [15:8] are connected to D[23:16] and pins [7:0] are connected to D[31:24]. • For PowerPC Bus, these pins are connected to D[0:15]. • For PC Card (PCMCIA) Bus, these pins are connected to D[15:0]. See *“Host Bus Interface Pin Mapping”* for summary. See the respective AC Timing diagram for detailed functionality.
WE1#	IO	9	CS/TS2	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the write enable signal for the upper data byte (WE1#). • For MC68K Bus 1, this pin inputs the upper data strobe (UDS#). • For MC68K Bus 2, this pin inputs the data strobe (DS#). • For Generic Bus, this pin inputs the write enable signal for the upper data byte (WE1#). • For MIPS/ISA Bus, this pin inputs the system byte high enable signal (SBHE#). • For Philips PR31500/31700 Bus, this pin inputs the odd byte access enable signal (/CARDxCSH). • For Toshiba TX3912 Bus, this pin inputs the odd byte access enable signal (CARDxCSH*). • For PowerPC Bus, this pin outputs the burst inhibit signal (BI#). • For PC Card (PCMCIA) Bus, this pin inputs the card enable 2 signal (-CE2). See *“Host Bus Interface Pin Mapping”* for summary. See the respective AC Timing diagram for detailed functionality.
M/R#	I	5	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin is connected to V_{DD}. • For Toshiba TX3912 Bus, this pin is connected to V_{DD}. • For all other busses, this input pin is used to select between the display buffer and register address spaces of the S1D13505. M/R# is set high to access the display buffer and low to access the registers. See *Register Mapping*. See Table 5-6:, “CPU Interface Pin Mapping,” on page 34.
CS#	I	4	C	Hi-Z	• For Philips PR31500/31700 Bus, this pin is connected to V_{DD}. • For Toshiba TX3912 Bus, this pin is connected to V_{DD}. • For all other busses, this is the Chip Select input. See Table 5-6:, “CPU Interface Pin Mapping,” on page 34. See the respective AC Timing diagram for detailed functionality.

Table 5-1: Host Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #	Cell	RESET# State	Description
BUSCLK	I	13	C	Hi-Z	This pin inputs the system bus clock. It is possible to apply a 2x clock and divide it by 2 internally - see MD12 in *Summary of Configuration Options*. • For SH-3/SH-4 Bus, this pin is connected to CKIO. • For MC68K Bus 1, this pin is connected to CLK. • For MC68K Bus 2, this pin is connected to CLK. • For Generic Bus, this pin is connected to BCLK. • For MIPS/ISA Bus, this pin is connected to CLK. • For Philips PR31500/31700 Bus, this pin is connected to DCLKOUT. • For Toshiba TX3912 Bus, this pin is connected to DCLKOUT. • For PowerPC Bus, this pin is connected to CLKOUT. • For PC Card (PCMCIA) Bus, this pin is connected to CLKI. See *"Host Bus Interface Pin Mapping"* for summary. See the respective AC Timing diagram for detailed functionality.
BS#	I	6	CS	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the bus start signal (BS#). • For MC68K Bus 1, this pin inputs the address strobe (AS#). • For MC68K Bus 2, this pin inputs the address strobe (AS#). • For Generic Bus, this pin is connected to V_{DD}. • For MIPS/ISA Bus, this pin is connected to V_{DD}. • For Philips PR31500/31700 Bus, this pin is connected to V_{DD}. • For Toshiba TX3912 Bus, this pin is connected to V_{DD}. • For PowerPC Bus, this pin inputs the Transfer Start signal (TS#). • For PC Card (PCMCIA) Bus, this pin is connected to V_{DD}. See *"Host Bus Interface Pin Mapping"* for summary. See the respective AC Timing diagram for detailed functionality.
RD/WR#	I	10	CS	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the read write signal (RD/WR#). The S1D13505 needs this signal for early decode of the bus cycle. • For MC68K Bus 1, this pin inputs the read write signal (R/W#). • For MC68K Bus 2, this pin inputs the read write signal (R/W#). • For Generic Bus, this pin inputs the read command for the upper data byte (RD1#). • For MIPS/ISA Bus, this pin is connected to V_{DD}. • For Philips PR31500/31700 Bus, this pin inputs the even byte access enable signal (/CARDxCSL). • For Toshiba TX3912 Bus, this pin inputs the even byte access enable signal (CARDxCSL*). • For PowerPC Bus, this pin inputs the read write signal (RD/WR#). • For PC Card (PCMCIA) Bus, this pin inputs the card enable 1 signal (-CE1). See *"Host Bus Interface Pin Mapping"* for summary. See the respective AC Timing diagram for detailed functionality.

Table 5-1: Host Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #	Cell	RESET# State	Description
RD#	I	7	CS	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the read signal (RD#). • For MC68K Bus 1, this pin is connected to V_{DD}. • For MC68K Bus 2, this pin inputs the bus size bit 1 (SIZ1). • For Generic Bus, this pin inputs the read command for the lower data byte (RD0#). • For MIPS/ISA Bus, this pin inputs the memory read signal (MEMR#). • For Philips PR31500/31700 Bus, this pin inputs the memory read command (/RD). • For Toshiba TX3912 Bus, this pin inputs the memory read command (RD*). • For PowerPC Bus, this pin inputs the transfer size 0 signal (TSIZ0). • For PC Card (PCMCIA) Bus, this pin inputs the output enable signal (-OE). See *"Host Bus Interface Pin Mapping"* for summary. See the respective AC Timing diagram for detailed functionality.
WE0#	I	8	CS	Hi-Z	This is a multi-purpose pin: • For SH-3/SH-4 Bus, this pin inputs the write enable signal for the lower data byte (WE0#). • For MC68K Bus 1, this pin must be connected to V_{DD} • For MC68K Bus 2, this pin inputs the bus size bit 0 (SIZ0). • For Generic Bus, this pin inputs the write enable signal for the lower data byte (WE0#). • For MIPS/ISA Bus, this pin inputs the memory write signal (MEMW#). • For Philips PR31500/31700 Bus, this pin inputs the memory write command (/WE). • For Toshiba TX3912 Bus, this pin inputs the memory write command (WE*). • For PowerPC Bus, this pin inputs the Transfer Size 1 signal (TSIZ1). • For PC Card (PCMCIA) Bus, this pin inputs the write enable signal (-WE). See *"Host Bus Interface Pin Mapping"* for summary. See the respective AC Timing diagram for detailed functionality.

Table 5-1: Host Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #	Cell	RESET# State	Description
WAIT#	O	15	TS2	Hi-Z	The active polarity of the WAIT# output is configurable; the state of MD5 on the rising edge of RESET# defines the active polarity of WAIT# - see *"Summary of Configuration Options"*. • For SH-3 Bus, this pin outputs the wait request signal (WAIT#); MD5 must be pulled low during reset by the internal pull-down resistor. • For SH-4 Bus, this pin outputs the ready signal (RDY#); MD5 must be pulled high during reset by an external pull-up resistor. • For MC68K Bus 1, this pin outputs the data transfer acknowledge signal (DTACK#); MD5 must be pulled high during reset by an external pull-up resistor. • For MC68K Bus 2, this pin outputs the data transfer and size acknowledge bit 1 (DSACK1#); MD5 must be pulled high during reset by an external pull-up resistor. • For Generic Bus, this pin outputs the wait signal (WAIT#); MD5 must be pulled low during reset by the internal pull-down resistor. • For MIPS/ISA Bus, this pin outputs the IO channel ready signal (IOCHRDY); MD5 must be pulled low during reset by the internal pull-down resistor. • For Philips PR31500/31700 Bus, this pin outputs the wait state signal (/CARDxWAIT); MD5 must be pulled low during reset by the internal pull-down resistor. • For Toshiba TX3912 Bus, this pin outputs the wait state signal (CARDxWAIT*); MD5 must be pulled low during reset by the internal pull-down resistor. • For PowerPC Bus, this pin outputs the transfer acknowledge signal (TA#); MD5 must be pulled high during reset by an external pull-up resistor. • For PC Card (PCMCIA) Bus, this pin outputs the wait signal (-WAIT); MD5 must be pulled low during reset by the internal pull-down resistor. See *"Host Bus Interface Pin Mapping"* for summary. See the respective AC Timing diagram for detailed functionality.
RESET#	I	11	CS	0	Active low input that clears all internal registers and forces all outputs to their inactive states. Note that active high RESET signals must be inverted before input to this pin.

5.2.2 Memory Interface

Table 5-2: Memory Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
LCAS#	O	51	CO1	1	• For dual-CAS# DRAM, this is the column address strobe for the lower byte (LCAS#). • For single-CAS# DRAM, this is the column address strobe (CAS#). See *“Memory Interface Pin Mapping”* for summary. See *Memory Interface Timing* for detailed functionality.
UCAS#	O	52	CO1	1	This is a multi-purpose pin: • For dual-CAS# DRAM, this is the column address strobe for the upper byte (UCAS#). • For single-CAS# DRAM, this is the write enable signal for the upper byte (UWE#). See *“Memory Interface Pin Mapping”* for summary. See *Memory Interface Timing* for detailed functionality.
WE#	O	53	CO1	1	• For dual-CAS# DRAM, this is the write enable signal (WE#). • For single-CAS# DRAM, this is the write enable signal for the lower byte (LWE#). See *“Memory Interface Pin Mapping”* for summary. See *Memory Interface Timing* for detailed functionality.
RAS#	O	54	CO1	1	Row address strobe - see *Memory Interface Timing* for detailed functionality.
MD[15:0]	IO	34, 36, 38, 40, 42, 44, 46, 48, 49, 47, 45, 43, 41, 39, 37, 35	C/TS 1D	Hi-Z	Bi-Directional memory data bus. During reset, these pins are inputs and their states at the rising edge of RESET# are used to configure the chip - see *Summary of Configuration Options*. Internal pull-down resistors (typical values of 100KΩ/180KΩ at 5V/3.3V respectively) pull the reset states to 0. External pull-up resistors can be used to pull the reset states to 1. See *Memory Interface Timing* for detailed functionality.

Table 5-2: Memory Interface Pin Descriptions (Continued)

Pin Name	Type	Pin #	Cell	RESET# State	Description
MA[8:0]	O	58, 60, 62, 64, 66, 67, 65, 63, 61	CO1	0utput	Multiplexed memory address - see *Memory Interface Timing* for functionality.
MA9	IO	56	C/TS 1	0utput	This is a multi-purpose pin: • For 2M byte DRAM, this is memory address bit 9 (MA9). • For asymmetrical 512K byte DRAM, this is memory address bit 9 (MA9). • For symmetrical 512K byte DRAM, this pin can be used as general purpose IO pin 3 (GPIO3). Note that unless configured otherwise, this pin defaults to an input and must be driven to a valid logic level. See *“Memory Interface Pin Mapping”* for summary. See *Memory Interface Timing* for detailed functionality.
MA10	IO	59	C/TS 1	0utput	This is a multi-purpose pin: • For asymmetrical 2M byte DRAM this is memory address bit 10 (MA10). • For symmetrical 2M byte DRAM and all 512K byte DRAM this pin can be used as general purpose IO pin 1 (GPIO1). Note that unless configured otherwise, this pin defaults to an input and must be driven to a valid logic level. See *“Memory Interface Pin Mapping”* for summary. See *Memory Interface Timing* for detailed functionality.
MA11	IO	57	C/TS 1	0utput	This is a multi-purpose pin: • For asymmetrical 2M byte DRAM this is memory address bit 11 (MA11). • For symmetrical 2M byte DRAM and all 512K byte DRAM this pin can be used as general purpose IO pin 2 (GPIO2). Note that unless configured otherwise, this pin defaults to an input and must be driven to a valid logic level. See *“Memory Interface Pin Mapping”* for summary. See *Memory Interface Timing* for detailed functionality.

5.2.3 LCD Interface

Table 5-2: LCD Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
FPDAT[15:0]	O	95-88, 86-79	CN3	0utput	Panel data bus. Not all pins are used for some panels - see *LCD Interface Pin Mapping* for details. Unused pins are driven low.
FPFRAME	O	73	CN3	0utput	Frame pulse
FPLINE	O	74	CN3	0utput	Line pulse
FPSHIFT	O	77	CO3	0utput	Shift clock
LCDPWR	O	75	CO1	0utput if MD[10]=0 1 if MD[10]=1	LCD power control output. The active polarity of this output is selected by the state of MD10 at the rising edge of RESET# - see *Summary of Configuration Options*. This output is controlled by the power save mode circuitry - see *Power Save Modes* for details.
DRDY	O	76	CN3	0utput	This is a multi-purpose pin: • For TFT/D-TFD panels this is the display enable output (DRDY). • For passive LCD with Format 1 interface this is the 2nd Shift Clock (FPSHIFT2) • For all other LCD panels this is the LCD backplane bias signal (MOD). See *LCD Interface Pin Mapping* and REG[02h] for details.

5.2.4 CRT Interface

Table 5-3: CRT Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET # State	Description
HRTC	IO	107	CN3	0utput	Horizontal retrace signal for CRT
VRTC	IO	108	CN3	0utput	Vertical retrace signal for CRT
RED	O	100	A		Analog output for CRT color Red
GREEN	O	103	A		Analog output for CRT color Green
BLUE	O	105	A		Analog output for CRT color Blue
IREF	I	101	A		Current reference for DAC - see *Analog Pins*. This pin must be left unconnected if the DAC is not needed.

5.2.5 Miscellaneous

Table 5-4: Miscellaneous Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
SUSPEND#	IO	71	CS/TS1	Hi-Z if MD[9]=0 High if MD[10:9]=01 Low if MD[10:9]=11	This pin can be used as a power-down input (SUSPEND#) or as an output possibly used for controlling the LCD backlight power: • When MD9 = 0 at rising edge of RESET#, this pin is an active-low Schmitt input used to put the S1D13505 into Hardware Suspend mode - see Section 15, “Power Save Modes” for details. • When MD[10:9] = 01 at rising edge of RESET#, this pin is an output (GPO) with a reset state of 1. The state of GPO is controlled by REG[21h] bit 7. • When MD[10:9] = 11 at rising edge of RESET#, this pin is an output (GPO) with a reset state of 0. The state of GPO is controlled by REG[21h] bit 7.
CLKI	I	69	C		Input clock for the internal pixel clock (PCLK) and memory clock (MCLK). PCLK and MCLK are derived from CLKI - see REG[19h] for details.
TESTEN	I	70	CD	Hi-Z	Test Enable. This pin should be connected to V_{SS} for normal operation.
VDD	P	12, 33, 55, 72, 97, 109	P		V_{DD}
DACVDD	P	99, 102, 104	P		DAC V_{DD}
VSS	P	14, 32, 50, 68, 78, 87, 96, 110	P		V_{SS}
DACVSS	P	98, 106	P		DAC V_{SS}

5.3 Summary of Configuration Options

Table 5-5: Summary of Power On/Reset Options

<table>
<tr><th>Pin Name</th><th colspan="2">value on this pin at rising edge of RESET# is used to configure: (1/0)</th></tr>
<tr><td></td><td>1</td><td>0</td></tr>
<tr><td>MD0</td><td>8-bit host bus interface</td><td>16-bit host bus interface</td></tr>
<tr><td>MD[3:1]</td><td colspan="2">Select host bus interface:MD[11] = 0:
000 = SH-3/SH-4 bus interface
001 = MC68K Bus 1
010 = MC68K Bus 2
011 = Generic
100 = Reserved
101 = MIPS/ISA
110 = PowerPC
111 = PC Card (when MD11 = 1 Philips PR31500/PR31700 or Toshiba TX3912 Bus)</td></tr>
<tr><td>MD4</td><td>Little Endian</td><td>Big Endian</td></tr>
<tr><td>MD5</td><td>WAIT# is active high (1 = insert wait state)</td><td>WAIT# is active low (0 = insert wait state)</td></tr>
<tr><td>MD[7:6]</td><td colspan="2">Memory Address/GPIO configuration:
00 = symmetrical 256K×16 DRAM. MA[8:0] = DRAM address. MA[11:9] = GPIO2,1,3 pins.
01 = symmetrical 1M×16 DRAM. MA[9:0] = DRAM address. MA[10:11] = GPIO2,1 pins.
10 = asymmetrical 256K×16 DRAM. MA[9:0] = DRAM address. MA[10:11] = GPIO2,1 pins.
11 = asymmetrical 1M×16 DRAM. MA[11:0] = DRAM address.</td></tr>
<tr><td>MD8</td><td colspan="2">Not used</td></tr>
<tr><td>MD9</td><td>SUSPEND# pin configured as GPO output</td><td>SUSPEND# pin configured as SUSPEND# input</td></tr>
<tr><td>MD10</td><td>Active low LCDPWR polarity or
active high GPO polarity</td><td>Active high LCDPWR polarity or
active low GPO polarity</td></tr>
<tr><td>MD11</td><td>Alternate Host Bus Interface Selected</td><td>Primary Host Bus Interface Selected</td></tr>
<tr><td>MD12</td><td>BUSCLK input divided by 2</td><td>BUSCLK input not divided</td></tr>
<tr><td>MD[15:13]</td><td colspan="2">Not used</td></tr>
</table>

5.4 Multiple Function Pin Mapping

Table 5-6: CPU Interface Pin Mapping

S1D13505 Pin Names	SH-3	SH-4	MC68K Bus 1	MC68K Bus 2	Generic	MIPS/ISA	Philips PR31500 /PR31700	Toshiba TX3912	PowerPC	PC Card (PCMCIA)
AB20	A20	A20	A20	A20	A20	LatchA20	ALE	ALE	A11	A20
AB19	A19	A19	A19	A19	A19	SA19	/CARDREG	CARDREG*	A12	A19
AB18	A18	A18	A18	A18	A18	SA18	/CARDIORD	CARDIORD*	A13	A18
AB17	A17	A17	A17	A17	A17	SA17	/CARDIOWR	CARDIOWR*	A14	A17
AB[16:13]	A[16:13]	A[16:13]	A[16:13]	A[16:13]	A[16:13]	SA[16:13]	V_{DD}	V_{DD}	A[15:18]	A[16:13]
AB[12:1]	A[12:1]	A[12:1]	A[12:1]	A[12:1]	A[12:1]	SA[12:1]	A[12:1]	A[12:1]	A[19:30]	A[12:1]
AB0	A0[1]	A0	LDS#	A0	A0[1]	SA0	A0[1]	A0[1]	A31	A0[1]
DB[15:8]	D[15:8]	D[15:8]	D[15:8]	D[31:24]	D[15:8]	SD[15:8]	D[31:24]	D[31:24]	D[0:7]	D[15:8]
DB[7:0]	D[7:0]	D[7:0]	D[7:0]	D[23:16]	D[7:0]	SD[7:0]	D[23:16]	D[23:16]	D[8:15	D[7:0]
WE1#	WE1#	WE1#	UDS#	DS#	WE1#	SBHE#	/CARDxCSH	CARDxCSH*	BI#	-CE2
M/R#	External Decode						V_{DD}		External Decode	
CS#	External Decode						V_{DD}		External Decode	
BUSCLK	CKIO	CKIO	CLK	CLK	BCLK	CLK	DCLKOUT	DCLKOUT	CLKOUT	CLKI
BS#	BS#	BS#	AS#	AS#	V_{DD}	V_{DD}	V_{DD}	V_{DD}	TS#	V_{DD}
RD/WR#	RD/WR#	RD/WR#	R/W#	R/W#	RD1#	V_{DD}	/CARDxCSL	CARDxCSL*	RD/WR#	-CE1
RD#	RD#	RD#	V_{DD}	SIZ1	RD0#	MEMR#	/RD	RD*	TSIZ0	-OE
WE0#	WE0#	WE0#	V_{DD}	SIZ0	WE0#	MEMW#	/WE	WE*	TSIZ1	-WE
WAIT#	WAIT#	RDY	DTACK#	DSACK1#	WAIT#	IOCHRDY	/CARDxWAIT	CARDxWAIT*	TA#	-WAIT
RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	inverted RESET	RESET#	PON*	RESET#	inverted RESET

Note
[1] The bus signal A0 is not used by the S1D13505 internally.

Table 5-7: Memory Interface Pin Mapping

S1D13505 Pin Names	FPM/EDO-DRAM							
	Sym 256Kx16		Asym 256Kx16		Sym 1Mx16		Asym 1Mx16	
	2-CAS#	2-WE#	2-CAS#	2-WE#	2-CAS#	2-WE#	2-CAS#	2-WE#
MD[15:0]	D[15:0]							
MA[8:0]	A[8:0]							
MA9	GPIO3		A9				A9	
MA10	GPIO1						A10	
MA11	GPIO2						A11	
UCAS#	UCAS#	UWE#	UCAS#	UWE#	UCAS#	UWE#	UCAS#	UWE#
LCAS#	LCAS#	CAS#	LCAS#	CAS#	LCAS#	CAS#	LCAS#	CAS#
WE#	WE#	LWE#	WE#	LWE#	WE#	LWE#	WE#	LWE#
RAS#	RAS#							

Note

All GPIO pins default to input on reset and unless programmed otherwise, should be connected to either V_{SS} or IO V_{DD} if not used.

Table 5-8: LCD Interface Pin Mapping

S1D13505 Pin Names	Monochrome Passive Panel			Color Passive Panel						Color TFT/D-TFD Panel		
	Single		Dual	Single	Single Format 1	Single Format 2	Single	Dual				
	4-bit	8-bit	8-bit	4-bit	8-bit	8-bit	16-Bit	8-bit	16-bit	9-bit	12-bit	18-bit
FPFRAME	FPFRAME											
FPLINE	FPLINE											
FPSHIFT	FPSHIFT											
DRDY	MOD				FPSHIFT 2	MOD				DRDY		
FPDAT0	driven 0	D0	LD0	driven 0	D0	D0	D0	LD0	LD0	R2	R3	R5
FPDAT1	driven 0	D1	LD1	driven 0	D1	D1	D1	LD1	LD1	R1	R2	R4
FPDAT2	driven 0	D2	LD2	driven 0	D2	D2	D2	LD2	LD2	R0	R1	R3
FPDAT3	driven 0	D3	LD3	driven 0	D3	D3	D3	LD3	LD3	G2	G3	G5
FPDAT4	D0	D4	UD0	D0	D4	D4	D4	UD0	UD0	G1	G2	G4
FPDAT5	D1	D5	UD1	D1	D5	D5	D5	UD1	UD1	G0	G1	G3
FPDAT6	D2	D6	UD2	D2	D6	D6	D6	UD2	UD2	B2	B3	B5
FPDAT7	D3	D7	UD3	D3	D7	D7	D7	UD3	UD3	B1	B2	B4
FPDAT8	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D8	driven 0	LD4	B0	B1	B3
FPDAT9	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D9	driven 0	LD5	driven 0	R0	R2
FPDAT10	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D10	driven 0	LD6	driven 0	driven 0	R1
FPDAT11	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D11	driven 0	LD7	driven 0	G0	G2
FPDAT12]	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D12	driven 0	UD4	driven 0	driven 0	G1
FPDAT13	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D13	driven 0	UD5	driven 0	driven 0	G0
FPDAT14	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D14	driven 0	UD6	driven 0	B0	B2
FPDAT15	driven 0	driven 0	driven 0	driven 0	driven 0	driven 0	D15	driven 0	UD7	driven 0	driven 0	B1

5.5 CRT Interface

The following figure shows the external circuitry for the CRT interface.

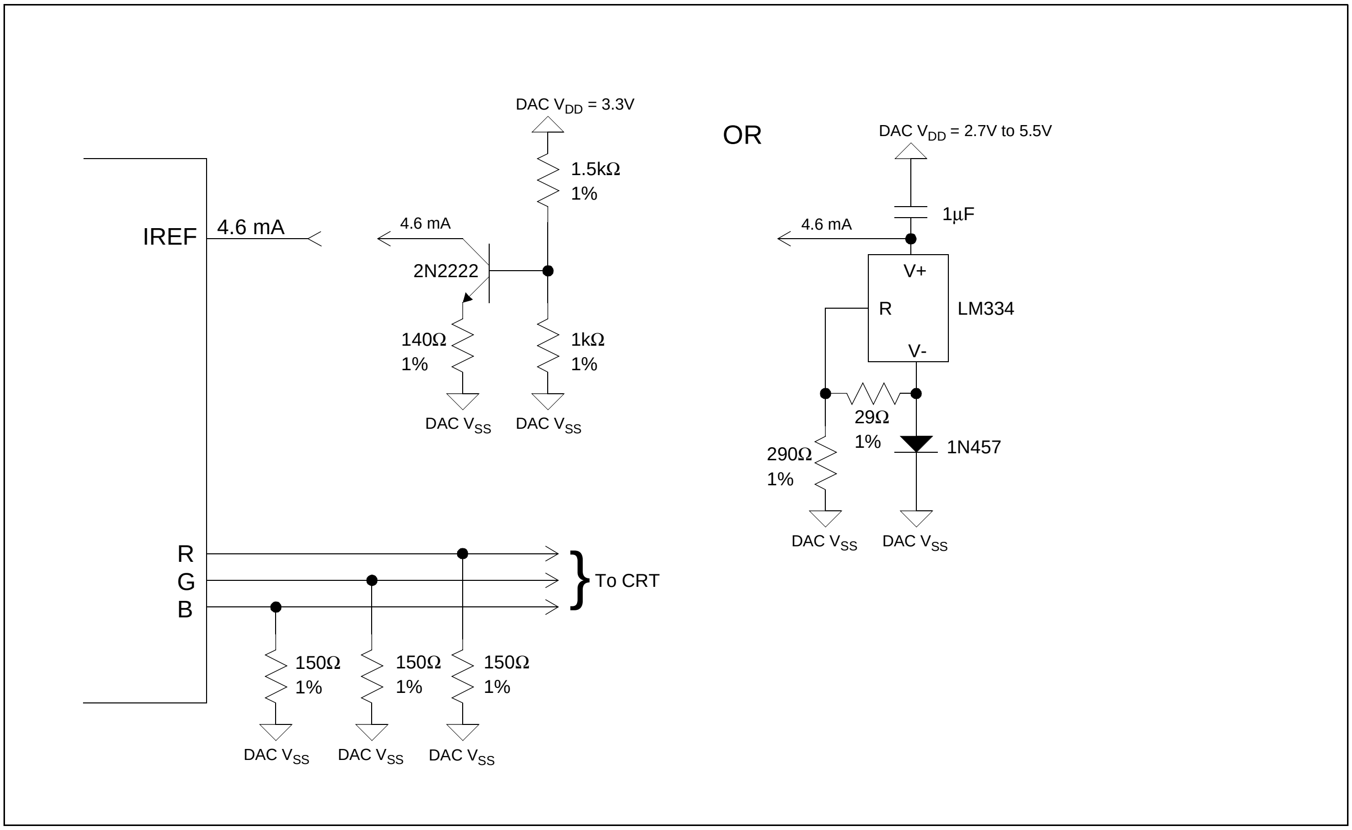


Figure 5-3: External Circuitry for CRT Interface

6 D.C. Characteristics

Table 6-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DD}	Supply Voltage	V_{SS} - 0.3 to 6.0	V
DAC V_{DD}	Supply Voltage	V_{SS} - 0.3 to 6.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.5	V
T_{STG}	Storage Temperature	-65 to 150	° C
T_{SOL}	Solder Temperature/Time	260 for 10 sec. max at lead	° C

Table 6-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Supply Voltage	V_{SS} = 0 V	2.7	3.0/3.3/5.0	5.5	V
V_{IN}	Input Voltage		V_{SS}		V_{DD}	V
T_{OPR}	Operating Temperature		-40	25	85	° C

Table 6-3: Electrical Characteristics for VDD = 5.0V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions			400	uA
I_{IZ}	Input Leakage Current		-1		1	μA
I_{OZ}	Output Leakage Current		-1		1	μA
V_{OH}	High Level Output Voltage	VDD = min I_{OL} = -4mA (Type1), -8mA (Type2) -12mA (Type3)	V_{DD} - 0.4			V
V_{OL}	Low Level Output Voltage	VDD = min I_{OL} = 4mA (Type1), 8mA (Type2) 12mA (Type3)			0.4	V
V_{IH}	High Level Input Voltage	CMOS level, V_{DD} = max	3.5			V
V_{IL}	Low Level Input Voltage	CMOS level, V_{DD} = min			1.0	V
V_{T+}	High Level Input Voltage	CMOS Schmitt, V_{DD} = 5.0V			4.0	V
V_{T-}	Low Level Input Voltage	CMOS Schmitt, V_{DD} = 5.0V	0.8			V
V_{H1}	Hysteresis Voltage	CMOS Schmitt, V_{DD} = 5.0V	0.3			V
R_{PD}	Pull Down Resistance	$V_I = V_{DD}$	50	100	200	kΩ
C_I	Input Pin Capacitance				12	pF
C_O	Output Pin Capacitance				12	pF
C_{IO}	Bi-Directional Pin Capacitance				12	pF

Table 6-4: Electrical Characteristics for VDD = 3.3V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions			290	uA
I_{IZ}	Input Leakage Current		-1		1	µA
I_{OZ}	Output Leakage Current		-1		1	µA
V_{OH}	High Level Output Voltage	VDD = min I_{OL} = -2mA (Type1), -4mA (Type2) -6mA (Type3)	V_{DD} - 0.3			V
V_{OL}	Low Level Output Voltage	VDD = min I_{OL} = 2mA (Type1), 4mA (Type2) 6mA (Type3)			0.3	V
V_{IH}	High Level Input Voltage	CMOS level, V_{DD} = max	2.2			V
V_{IL}	Low Level Input Voltage	CMOS level, V_{DD} = min			0.8	V
V_{T+}	High Level Input Voltage	CMOS Schmitt, V_{DD} = 3.3V			2.4	V
V_{T-}	Low Level Input Voltage	CMOS Schmitt, V_{DD} = 3.3V	0.6			V
V_{H1}	Hysteresis Voltage	CMOS Schmitt, V_{DD} = 3.3V	0.1			V
R_{PD}	Pull Down Resistance	$V_I = V_{DD}$	90	180	360	kΩ
C_I	Input Pin Capacitance				12	pF
C_O	Output Pin Capacitance				12	pF
C_{IO}	Bi-Directional Pin Capacitance				12	pF

Table 6-5: Electrical Characteristics for VDD = 3.0V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions			260	uA
I_{IZ}	Input Leakage Current		-1		1	μA
I_{OZ}	Output Leakage Current		-1		1	μA
V_{OH}	High Level Output Voltage	VDD = min I_{OL} = -1.8mA (Type1), -3.5mA (Type2) -5mA (Type3)	V_{DD} - 0.3			V
V_{OL}	Low Level Output Voltage	VDD = min I_{OL} = 1.8mA (Type1), 3.5mA (Type2) 5mA (Type3)			0.3	V
V_{IH}	High Level Input Voltage	CMOS level, V_{DD} = max	2.0			V
V_{IL}	Low Level Input Voltage	CMOS level, V_{DD} = min			0.8	V
V_{T+}	High Level Input Voltage	CMOS Schmitt, V_{DD} = 3.0V			2.3	V
V_{T-}	Low Level Input Voltage	CMOS Schmitt, V_{DD} = 3.0V	0.5			V
V_{H1}	Hysteresis Voltage	CMOS Schmitt, V_{DD} = 3.0V	0.1			V
R_{PD}	Pull Down Resistance	$V_I = V_{DD}$	100	200	400	kΩ
C_I	Input Pin Capacitance				12	pF
C_O	Output Pin Capacitance				12	pF
C_{IO}	Bi-Directional Pin Capacitance				12	pF

7 A.C. Characteristics

Conditions: V_{DD} = 3.0V ± 10% and V_{DD} = 5.0V ± 10%
T_A = -40° C to 85° C
T_{rise} and T_{fall} for all inputs must be ≤ 5 nsec (10% ~ 90%)
C_L = 50pF (CPU Interface), unless noted
C_L = 100pF (LCD Panel Interface)
C_L = 10pF (Display Buffer Interface)
C_L = 10pF (CRT Interface)

7.1 CPU Interface Timing

7.1.1 SH-4 Interface Timing

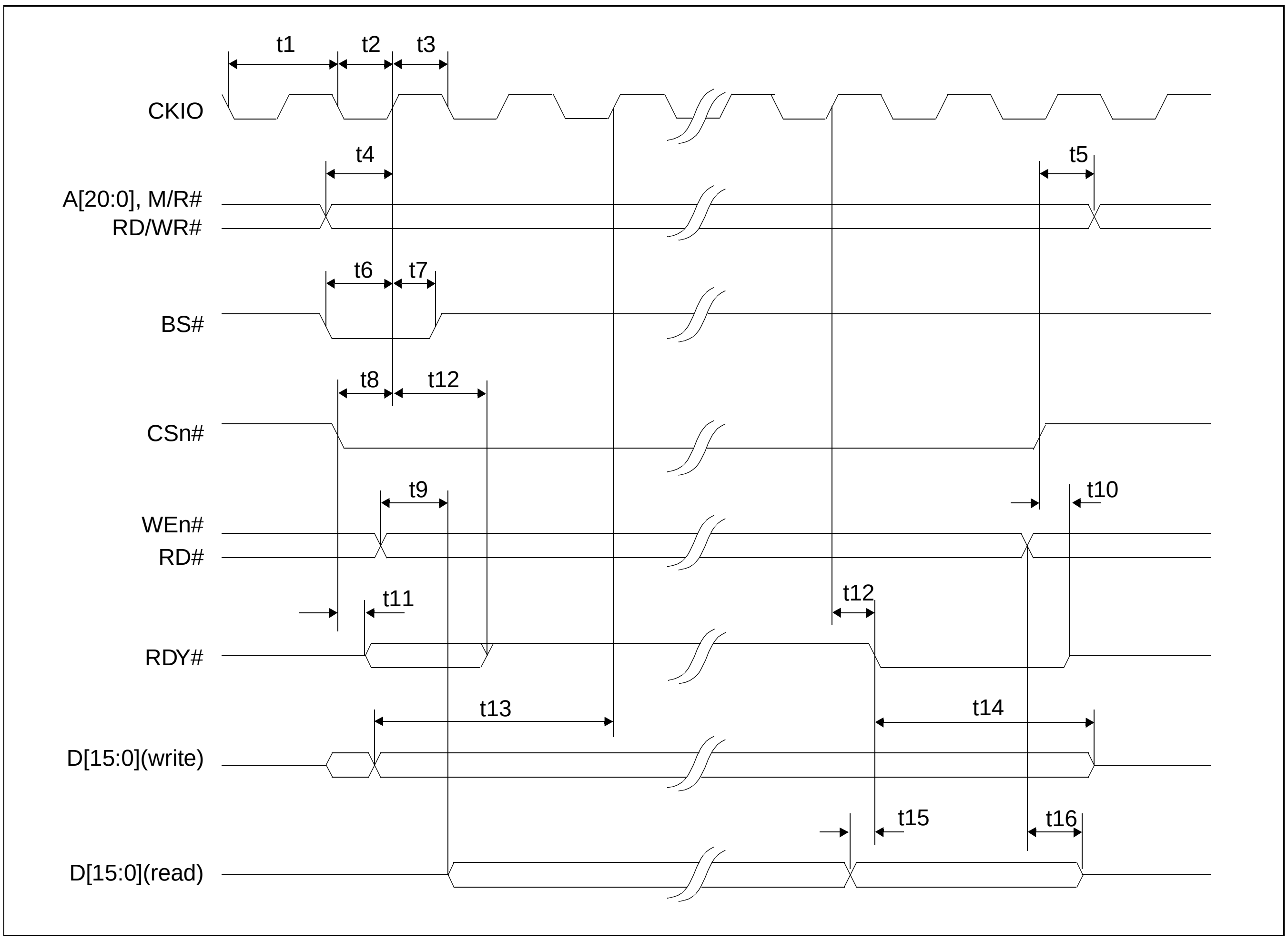


Figure 7-1: SH-4 Timing

Note
The above timing diagram is not applicable if the BUSCLK divided by 2 configuration option is selected.

Note

The SH-4 Wait State Control Register for the area in which the S1D13505 resides must be set to a non-zero value. The SH-4 read-to-write cycle transition must be set to a non-zero value (with reference to BUSCLK).

Table 7-1: SH-4 Timing

		3.0V[a]		5.0V[b]		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
t1	Clock period	15		15		ns
t2	Clock pulse width high	6		6		ns
t3	Clock pulse width low	6		6		ns
t4	A[20:0], M/R#, RD/WR# setup to CKIO	3		3		ns
t5	A[20:0], M/R#, RD/WR# hold from CS#	0		0		ns
t6	BS# setup	4		4		ns
t7	BS# hold	1		1		ns
t8	CSn# setup	4		4		ns
t9[2]	Falling edge RD# to D[15:0] driven	0		0		ns
t10	Rising edge CSn# to RDY# tri-state	5	25	2.5	10	ns
t11[1]	Falling edge CSn# to RDY# driven	0	15	0	10	ns
t12	CKIO to WAIT# delay	4	20	3.6	12	ns
t13	D[15:0] setup to 2nd CKIO after BS# (write cycle)	10		10		ns
t14	D[15:0] hold (write cycle)	0		0		ns
t15	D[15:0] valid to RDY# falling edge (read cycle)	0		0		ns
t16	Rising edge RD# to D[15:0] tri-state (read cycle)	5	25	2.5	10	ns

[a] Two Software WAIT States Required
[b] One Software WAIT State Required

1. If the S1D13505 host interface is disabled, the timing for RDY# driven is relative to the falling edge of CSn# or the first positive edge of CKIO after A[20:0], M/R# becomes valid, whichever one is later.

2. If the S1D13505 host interface is disabled, the timing for D[15:0] driven is relative to the falling edge of RD# or the first positive edge of CKIO after A[20:0], M/R# becomes valid, whichever one is later.

7.1.2 SH-3 Interface Timing

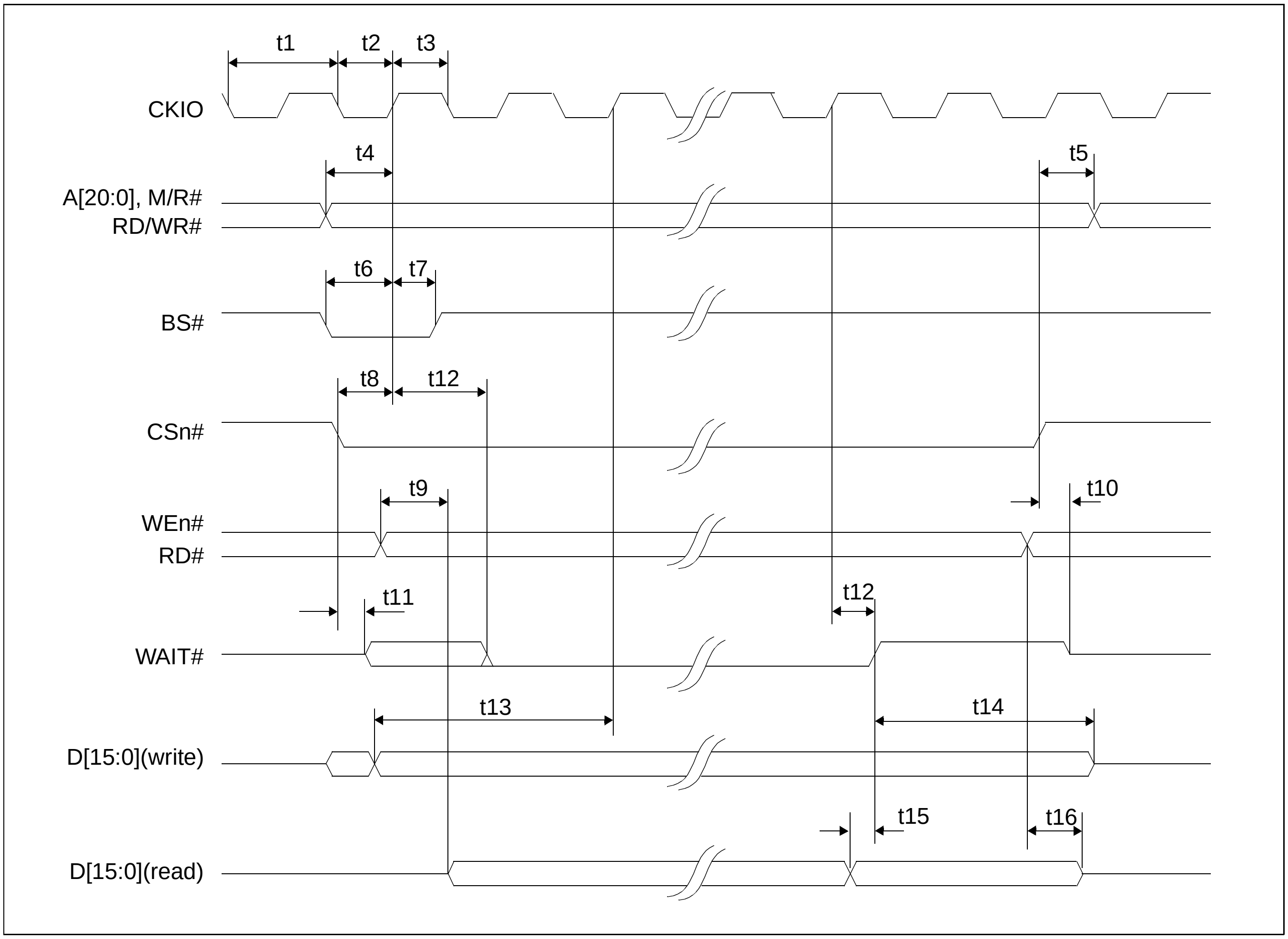


Figure 7-2: SH-3 Timing

Note
The above timing diagram is not applicable if the BUSCLK divided by 2 configuration option is selected.

Note
The SH-3 Wait State Control Register for the area in which the S1D13505 resides must be set to a non-zero value.

Table 7-2: SH-3 Timing

		3.0V[a]		5.0V[b]		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
t1	Clock period	15.1		15.1		ns
t2	Clock pulse width high	6		6		ns
t3	Clock pulse width low	6		6		ns
t4	A[20:0], M/R#, RD/WR# setup to CKIO	3		3		ns
t5	A[20:0], M/R#, RD/WR# hold from CS#	0		0		ns
t6	BS# setup	4		4		ns
t7	BS# hold	1		1		ns
t8	CSn# setup	4		4		ns
t9[2]	Falling edge RD# to D[15:0] driven	0		0		ns
t10	Rising edge CSn# to WAIT# tri-state	5	25	2.5	10	ns
t11[1]	Falling edge CSn# to WAIT# driven	0	15	0	10	ns
t12	CKIO to WAIT# delay	4	20	3.6	12	ns
t13	D[15:0] setup to 2nd CKIO after BS# (write cycle)	10		10		ns
t14	D[15:0] hold (write cycle)	0		0		ns
t15	D[15:0] valid to WAIT# rising edge (read cycle)	0		0		ns
t16	Rising edge RD# to D[15:0] tri-state (read cycle)	5	25	2.5	10	ns

[a] Two Software WAIT States Required
[b] One Software WAIT State Required

1. If the S1D13505 host interface is disabled, the timing for WAIT# driven is relative to the falling edge of CSn# or the first positive edge of CKIO after A[20:0], M/R# becomes valid, whichever one is later.
2. If the S1D13505 host interface is disabled, the timing for D[15:0] driven is relative to the falling edge of RD# or the first positive edge of CKIO after A[20:0], M/R# becomes valid, whichever one is later.

7.1.3 MC68K Bus 1 Interface Timing (e.g. MC68000)

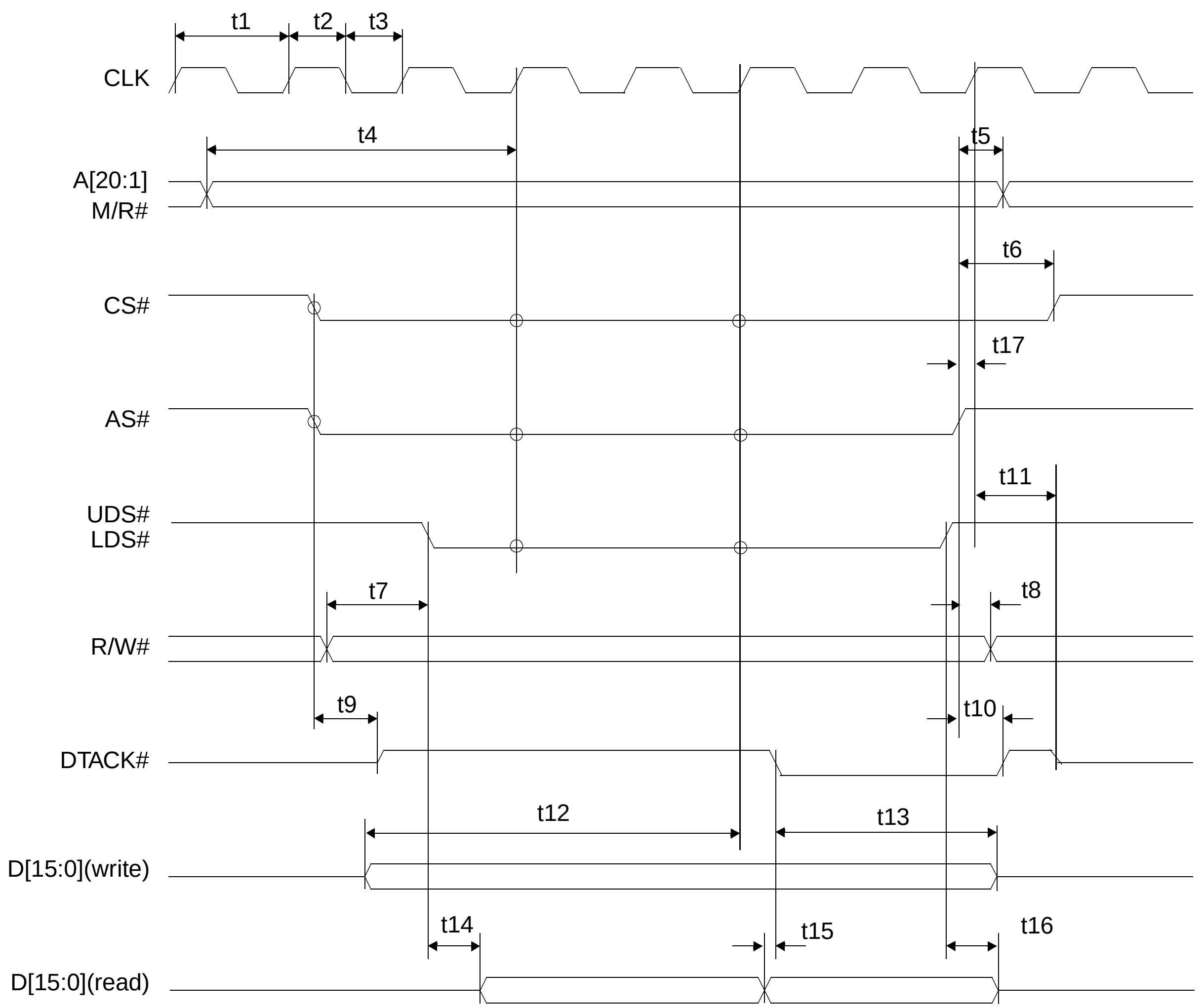


Figure 7-3: MC68000 Timing

Note
The above timing diagram is not applicable if the BUSCLK divided by 2 configuration option is selected.

Table 7-3: MC68000 Timing

Symbol	Parameter	3.0V Min	3.0V Max	5.0V Min	5.0V Max	Units
t1	Clock period	20		20		ns
t2	Clock pulse width high	6		6		ns
t3	Clock pulse width low	6		6		ns
t4	A[20:1], M/R# setup to first CLK where CS# = 0 AS# = 0, and either UDS#=0 or LDS# = 0	10		10		ns
t5	A[20:1], M/R# hold from AS#	0		0		ns
t6	CS# hold from AS#	0		0		ns
t7	R/W# setup to before to either UDS#=0 or LDS# = 0	10		10		ns
t8	R/W# hold from AS#	0		0		ns
t9[1]	AS# = 0 and CS# = 0 to DTACK# driven high	0		0		ns
t10	AS# high to DTACK# high	3	18	3	12	ns
t11	First BCLK where AS# = 1 to DTACK# high impedance		25		10	ns
t12	D[15:0] valid to third CLK where CS# = 0 AS# = 0, and either UDS#=0 or LDS# = 0 (write cycle)	10		10		ns
t13	D[15:0] hold from falling edge of DTACK# (write cycle)	0		0		ns
t14[2]	Falling edge of UDS#=0 or LDS#=0 to D[15:0] driven (read cycle)	0		0		ns
t15	D[15:0] valid to DTACK# falling edge (read cycle)	0		0		ns
t16	UDS# and LDS# high to D[15:0] invalid/high impedance (read cycle)	5	25	2.5	10	ns
t17	AS# high setup to CLK	2		2		ns

1. If the S1D13505 host interface is disabled, the timing for DTACK# driven high is relative to the falling edge of CS#, AS# or the first positive edge of CLK after A[20:1], M/R# becomes valid,
whichever one is later.

2. If the S1D13505 host interface is disabled, the timing for D[15:0] driven is relative to the falling edge of UDS#, LDS# or the first positive edge of CLK after A[20:1], M/R# becomes valid, whichever one is later.

7.1.4 MC68K Bus 2 Interface Timing (e.g. MC68030)

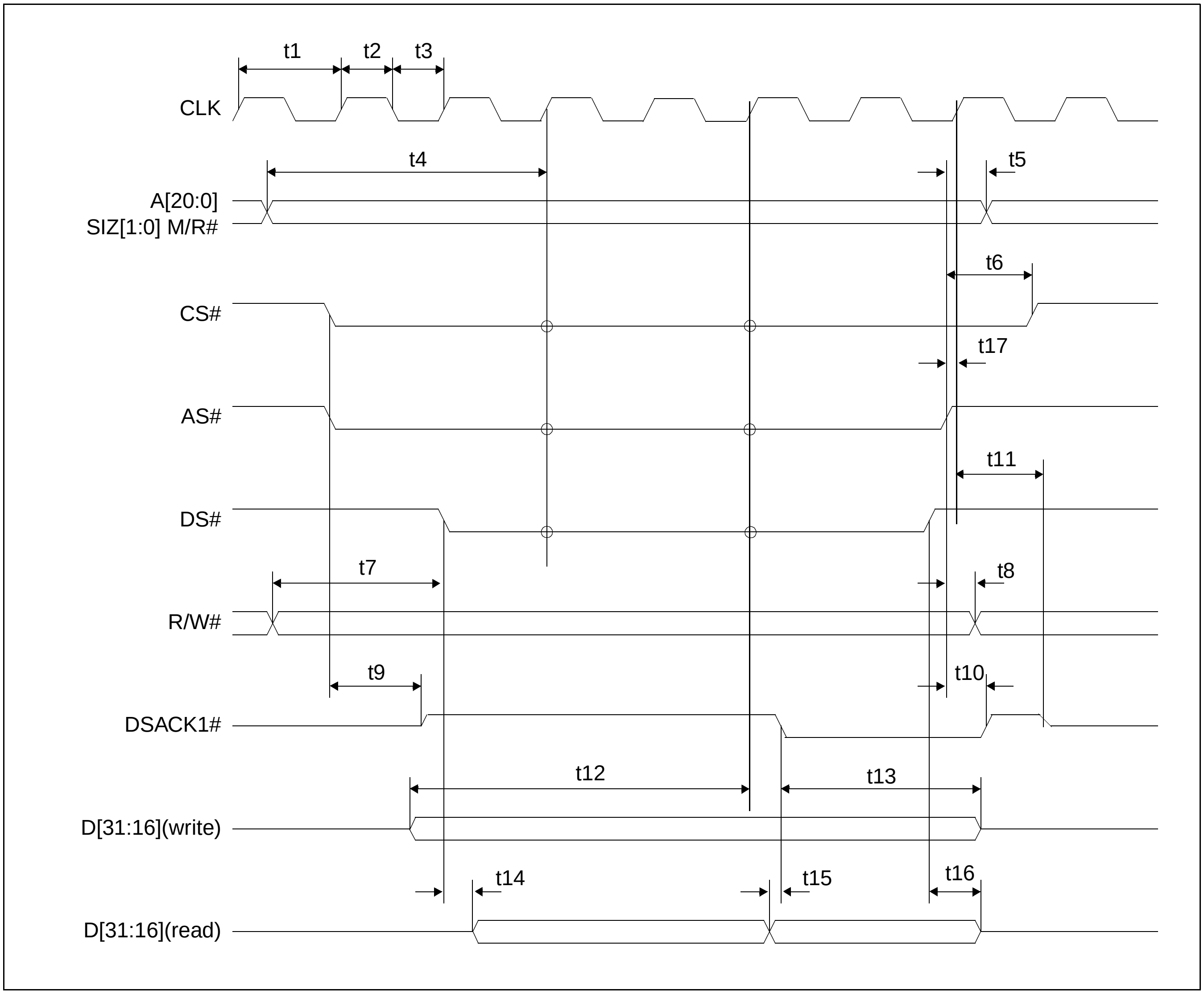


Figure 7-4: MC68030 Timing

Note

The above timing diagram is not applicable if the BUSCLK divided by 2 configuration option is selected.

Table 7-4: MC68030 Timing

		3.0V		5.0V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
t1	Clock period	20		20		ns
t2	Clock pulse width high	6		6		ns
t3	Clock pulse width low	6		6		ns
t4	A[20:0], SIZ[1:0], M/R# setup to first CLK where CS# = 0 AS# = 0, and either UDS#=0 or LDS# = 0	10		10		ns
t5	A[20:0], SIZ[1:0], M/R# hold from AS#	0		0		ns
t6	CS# hold from AS#	0		0		ns
t7	R/W# setup to DS#	10		10		ns
t8	R/W# hold from AS#	0		0		ns
t9[1]	AS# = 0 and CS# = 0 to DSACK1# driven high	0		0		ns
t10	AS# high to DSACK1# high	3	18	3	12	ns
t11	First BCLK where AS# = 1 to DSACK1# high impedance	5	25	2.5	10	ns
t12	D[31:16] valid to third CLK where CS# = 0 AS# = 0, and either UDS#=0 or LDS# = 0 (write cycle)	10		10		ns
t13	D[31:16] hold from falling edge of DSACK1# (write cycle)	0		0		ns
t14[2]	Falling edge of UDS#=0 or LDS# = 0 to D[31:16] driven (read cycle)	0		0		ns
t15	D[31:16] valid to DSACK1# falling edge (read cycle)	0		0		ns
t16	UDS# and LDS# high to D[31:16] invalid/high impedance (read cycle)	5	25	2.5	10	ns
t17	AS# high setup to CLK	2		2		ns

1. If the S1D13505 host interface is disabled, the timing for DSACK1# driven high is relative to the falling edge of CS#, AS# or the first positive edge of CLK after A[20:0], M/R# becomes valid, whichever one is later.
2. If the S1D13505 host interface is disabled, the timing for D[31:16] driven is relative to the falling edge of UDS#, LDS# or the first positive edge of CLK after A[20:0], M/R# becomes valid, whichever one is later.

7.1.5 PC Card Interface Timing

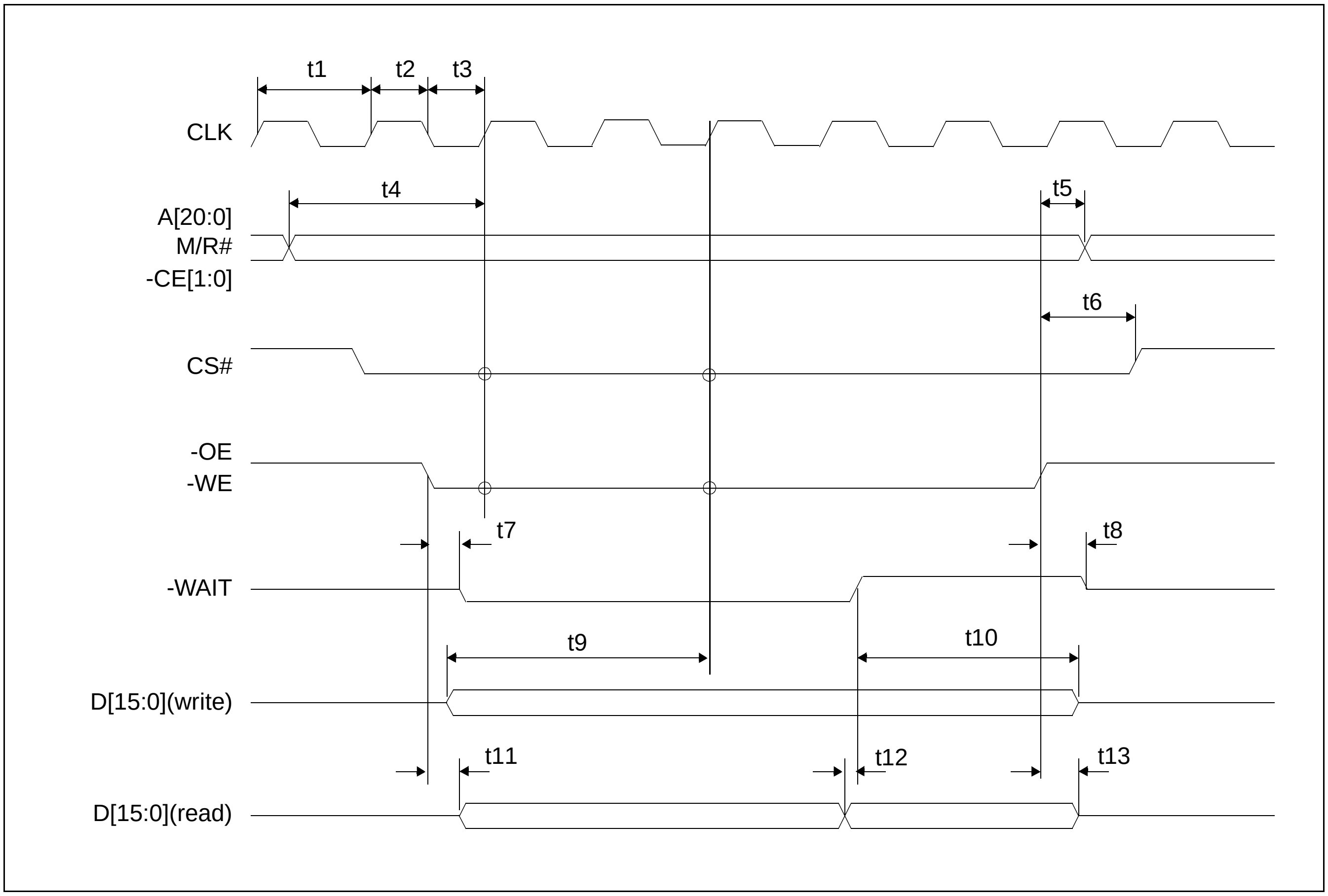


Figure 7-5: PC Card Timing

Note

The above timing diagram is not applicable if the BUSCLK divided by 2 configuration option is selected.

Table 7-5: PC Card Timing

Symbol	Parameter	3.0V Min	3.0V Max	5.0V Min	5.0V Max	Units
t1	Clock period	20		20		ns
t2	Clock pulse width high	6		6		ns
t3	Clock pulse width low	6		6		ns
t4	A[20:0], M/R# setup to first CLK where CS# = 0 and either -OE = 0 or -WE = 0	10		10		ns
t5	A[20:0], M/R# hold from rising edge of either -OE or -WE	0		0		ns
t6	CS# hold from rising edge of either -OE or -WE	0		0		ns
t7[1]	Falling edge of either -OE or -WE to -WAIT driven low	0	15	0	10	ns
t8	Rising edge of either -OE or -WE to -WAIT tri-state	5	25	2.5	10	ns
t9	D[15:0] setup to third CLK where CS# = 0 and -WE = 0 (write cycle)	10		10		ns
t10	D[15:0] hold (write cycle)	0		0		ns
t11[2]	Falling edge -OE to D[15:0] driven (read cycle)	0		0		ns
t12	D[15:0] setup to rising edge -WAIT (read cycle)	0		0		ns
t13	Rising edge of -OE to D[15:0] tri-state (read cycle)	5	25	5	10	ns

1. If the S1D13505 host interface is disabled, the timing for -WAIT driven low is relative to the falling edge of -OE, -WE or the first positive edge of CLK after A[20:0], M/R# becomes valid, whichever one is later.

2. If the S1D13505 host interface is disabled, the timing for D[15:0] driven is relative to the falling edge of -OE or the first positive edge of CLK after A[20:0], M/R# becomes valid, whichever one is later.

7.1.6 Generic Interface Timing

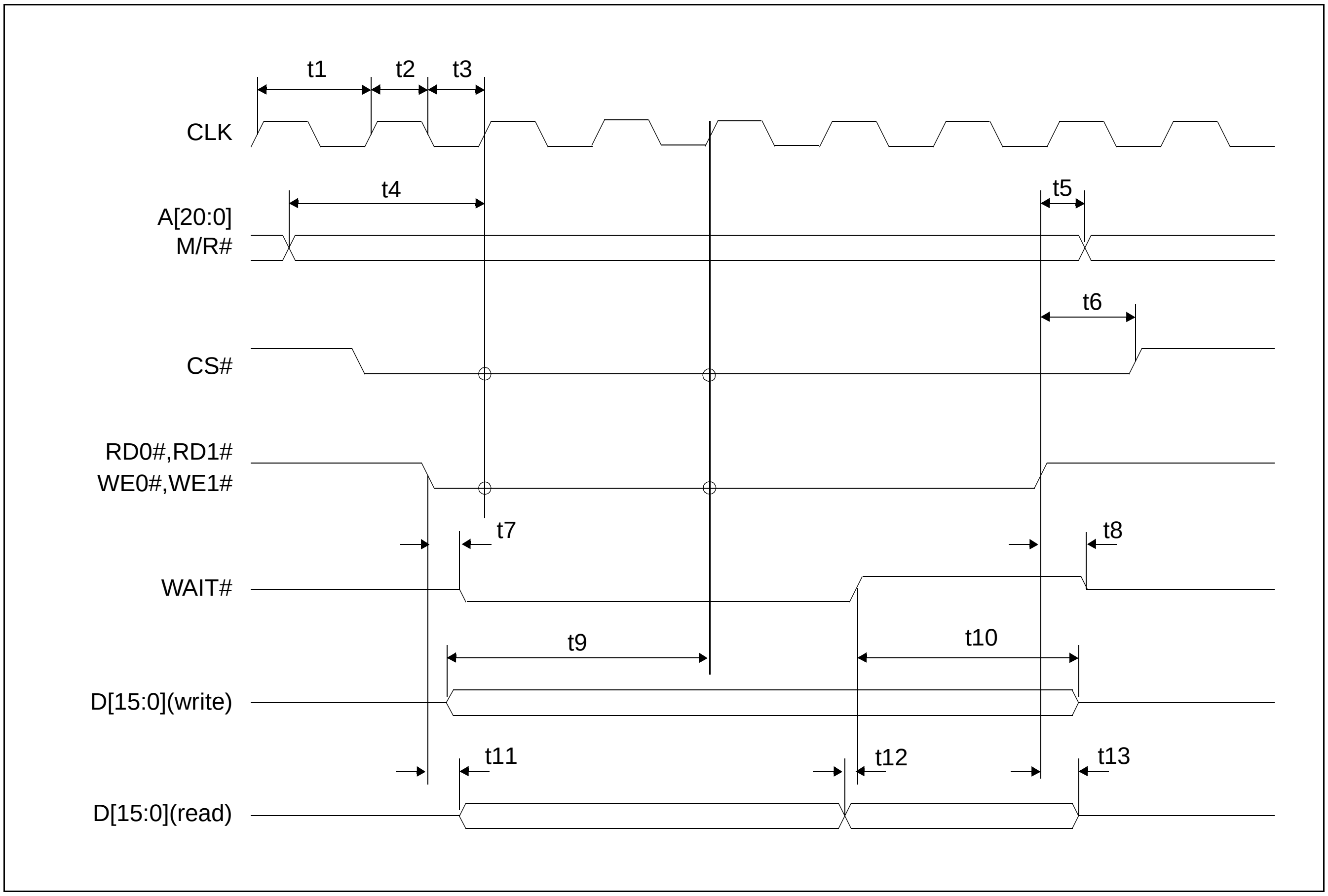


Figure 7-6: Generic Timing

Note

The above timing diagram is not applicable if the BUSCLK divided by 2 configuration option is selected.

Table 7-6: Generic Timing

Symbol	Parameter	3.0V Min	3.0V Max	5.0V Min	5.0V Max	Units
t1	Clock period	20		20		ns
t2	Clock pulse width high	6		6		ns
t3	Clock pulse width low	6		6		ns
t4	A[20:0], M/R# setup to first CLK where CS# = 0 and either RD0#,RD1#,WE0# or WE1# = 0	10		10		ns
t5	A[20:0], M/R# hold from rising edge of either RD0#,RD1#,WE0# or WE1# = 0	0		0		ns
t6	CS# hold from rising edge of either RD0#,RD1#,WE0# or WE1# = 0	0		0		ns
t7[1]	Falling edge of either RD0#,RD1#,WE0# or WE1# to WAIT# driven low	0	15	0	10	ns
t8	Rising edge of either RD0#,RD1#,WE0# or WE1# to WAIT# tri-state	5	25	2.5	10	ns
t9	D[15:0] setup to third CLK where CS# = 0 and WE0#,WE1# = 0 (write cycle)	10		10		ns
t10	D[15:0] hold (write cycle)	0		0		ns
t11[2]	Falling edge RD0#,RD1# to D[15:0] driven (read cycle)	0		0		ns
t12	D[15:0] setup to rising edge WAIT# (read cycle)	0		0		ns
t13	Rising edge of RD0#,RD1# to D[15:0] tri-state (read cycle)	5	25	5	10	ns

1. If the S1D13505 host interface is disabled, the timing for WAIT# driven low is relative to the falling edge of RD0#, RD1#, WE0#, WE1# <u>or</u> the first positive edge of CLK after A[20:0], M/R# becomes valid, whichever one is later.

2. If the S1D13505 host interface is disabled, the timing for D[15:0] driven is relative to the falling edge of RD0#, RD1# <u>or</u> the first positive edge of CLK after A[20:0], M/R# becomes valid, whichever one is later.

7.1.7 MIPS/ISA Interface Timing

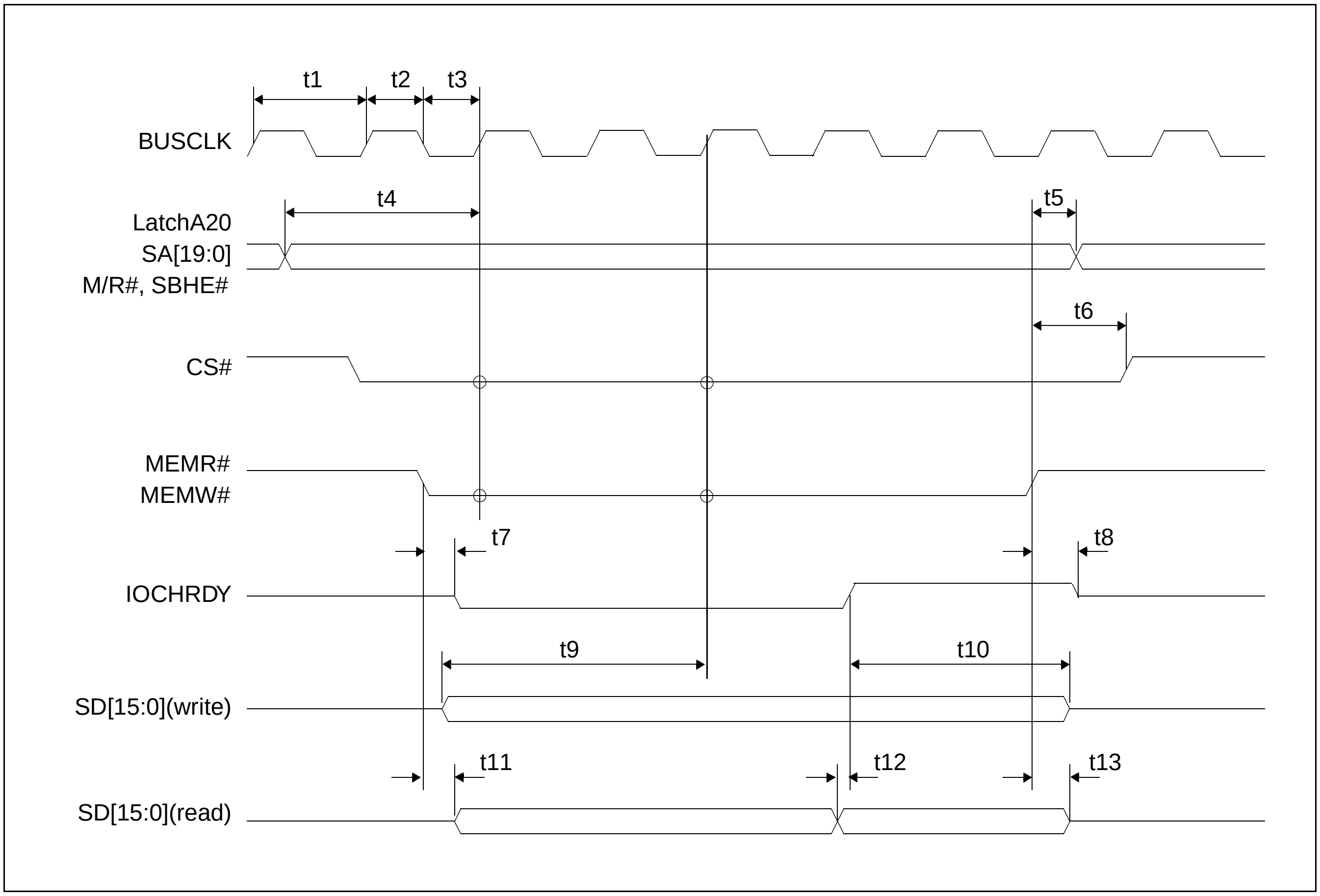


Figure 7-7: MIPS/ISA Timing

Note

The above timing diagram is not applicable if the BUSCLK divided by 2 configuration option is selected.

Table 7-7: MIPS/ISA Timing

		3.0V		5.0V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
t1	Clock period	20		20		ns
t2	Clock pulse width high	6		6		ns
t3	Clock pulse width low	6		6		ns
t4	LatchA20, SA[19:0], M/R#, SBHE# setup to first BUSCLK where CS# = 0 and either MEMR# = 0 or MEMW# = 0	10		10		ns
t5	LatchA20, SA[19:0], M/R#, SBHE# hold from rising edge of either MEMR# or MEMW#	0		0		ns
t6	CS# hold from rising edge of either MEMR# or MEMW#	0		0		ns
t7[1]	Falling edge of either MEMR# or MEMW# to IOCHRDY# driven low	0		0		ns
t8	Rising edge of either MEMR# or MEMW# to IOCHRDY# tri-state	5	25	2.5	10	ns
t9	SD[15:0] setup to third BUSCLK where CS# = 0 MEMW# = 0 (write cycle)	10		10		ns
t10	SD[15:0] hold (write cycle)	0		0		ns
t11[2]	Falling edge MEMR# to SD[15:0] driven (read cycle)	0		0		ns
t12	SD[15:0] setup to rising edge IOCHRDY# (read cycle)	0		0		ns
t13	Rising edge of MEMR# toSD[15:0] tri-state (read cycle)	5	25	5	10	ns

1. If the S1D13505 host interface is disabled, the timing for IOCHRDY driven low is relative to the falling edge of MEMR#, MEMW# or the first positive edge of BUSCLK after LatchA20, SA[19:0], M/R# becomes valid, whichever one is later.
2. If the S1D13505 host interface is disabled, the timing for SD[15:0] driven is relative to the falling edge of MEMR# or the first positive edge of BUSCLK after LatchA20, SA[19:0], M/R# becomes valid, whichever one is later.

7.1.8 Philips Interface Timing (e.g. PR31500/PR31700)

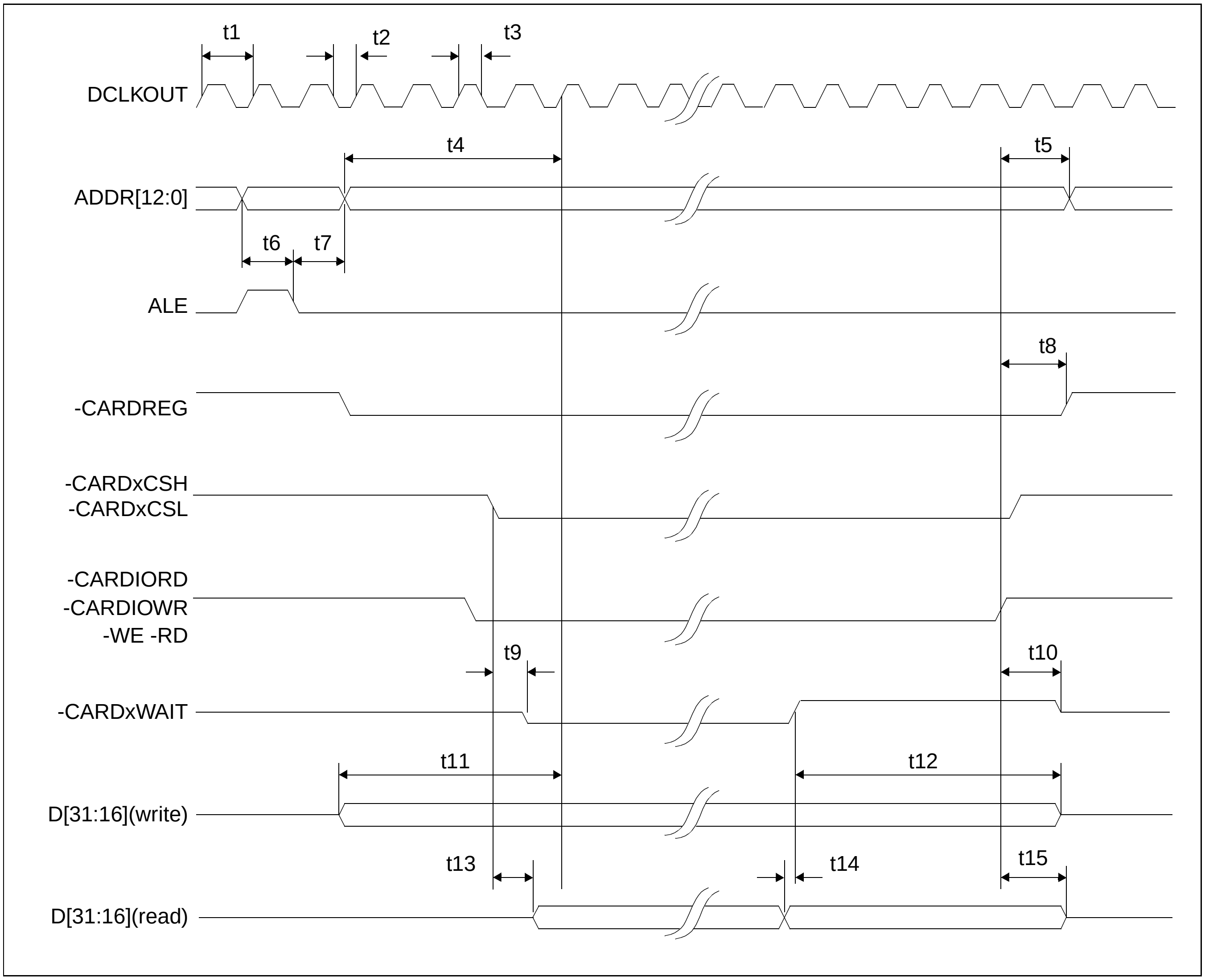


Figure 7-8: Philips Timing

Table 7-8: Philips Timing

Symbol	Parameter	3.0V Min	3.0V Max	5.0V Min	5.0V Max	Units
t1	Clock period	13.3		13.3		ns
t2	Clock pulse width low	6		6		ns
t3	Clock pulse width high	6		6		ns
t4	ADDR[12:0] setup to first CLK of cycle	10		10		ns
t5	ADDR[12:0] hold from command invalid	0		0		ns
t6	ADDR[12:0] setup to falling edge ALE	10		10		ns
t7	ADDR[12:0] hold from falling edge ALE	5		5		ns
t8	-CARDREG hold from command invalid	0		0		ns
t9[1]	Falling edge of chip select to -CARDxWAIT driven	0	15	0	9	ns
t10	Command invalid to -CARDxWAIT tri-state	5	25	2.5	10	ns
t11	D[31:16] valid to first CLK of cycle (write cycle)	10		10		ns
t12	D[31:16] hold from rising edge of -CARDxWAIT	0		0		
t13[2]	Chip select to D[31:16] driven (read cycle)	1		1		ns
t14	D[31:16] setup to rising edge -CARDxWAIT (read cycle)	0		0		ns
t15	Command invalid to D[31:16] tri-state (read cycle)	5	25	2.5	10	ns

1. If the S1D13505 host interface is disabled, the timing for -CARDxWAIT driven is relative to the falling edge of chip select or the second positive edge of DCLKOUT after ADDR[12:0] becomes valid, whichever one is later.

2. If the S1D13505 host interface is disabled, the timing for D[31:16] driven is relative to the falling edge of chip select or the second positive edge of DCLKOUT after ADDR[12:0] becomes valid, whichever one is later.

Note
The Philips interface has different clock input requirements as follows:

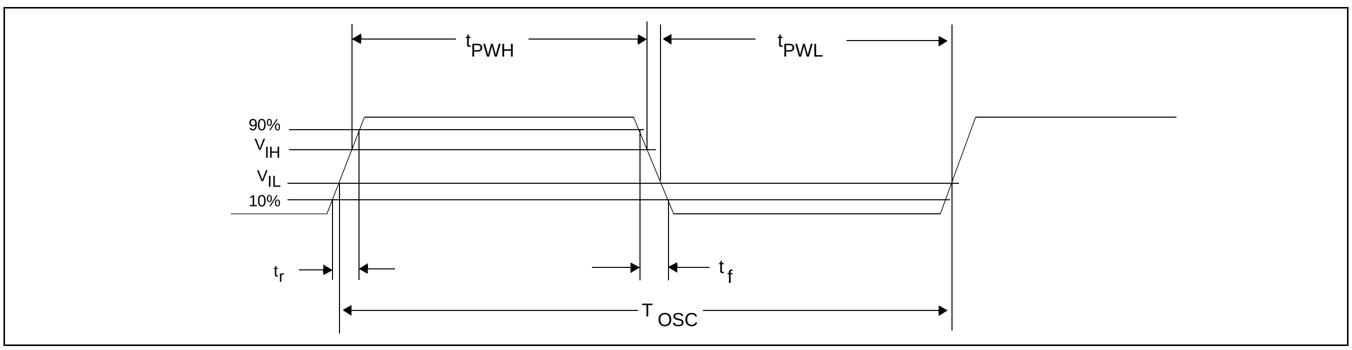


Figure 7-9: Clock Input Requirement

Table 7-9: Clock Input Requirements for BUSCLK using Philips local bus

Symbol	Parameter	Min	Max	Units
T_{OSC}	Input Clock Period)	13.3		ns
t_{PWH}	Input Clock Pulse Width High	6		ns
t_{PWL}	Input Clock Pulse Width Low	6		ns
t_f	Input Clock Fall Time (10% - 90%)		5	ns
t_r	Input Clock Rise Time (10% - 90%)		5	ns

7.1.9 Toshiba Interface Timing (e.g. TX3912)

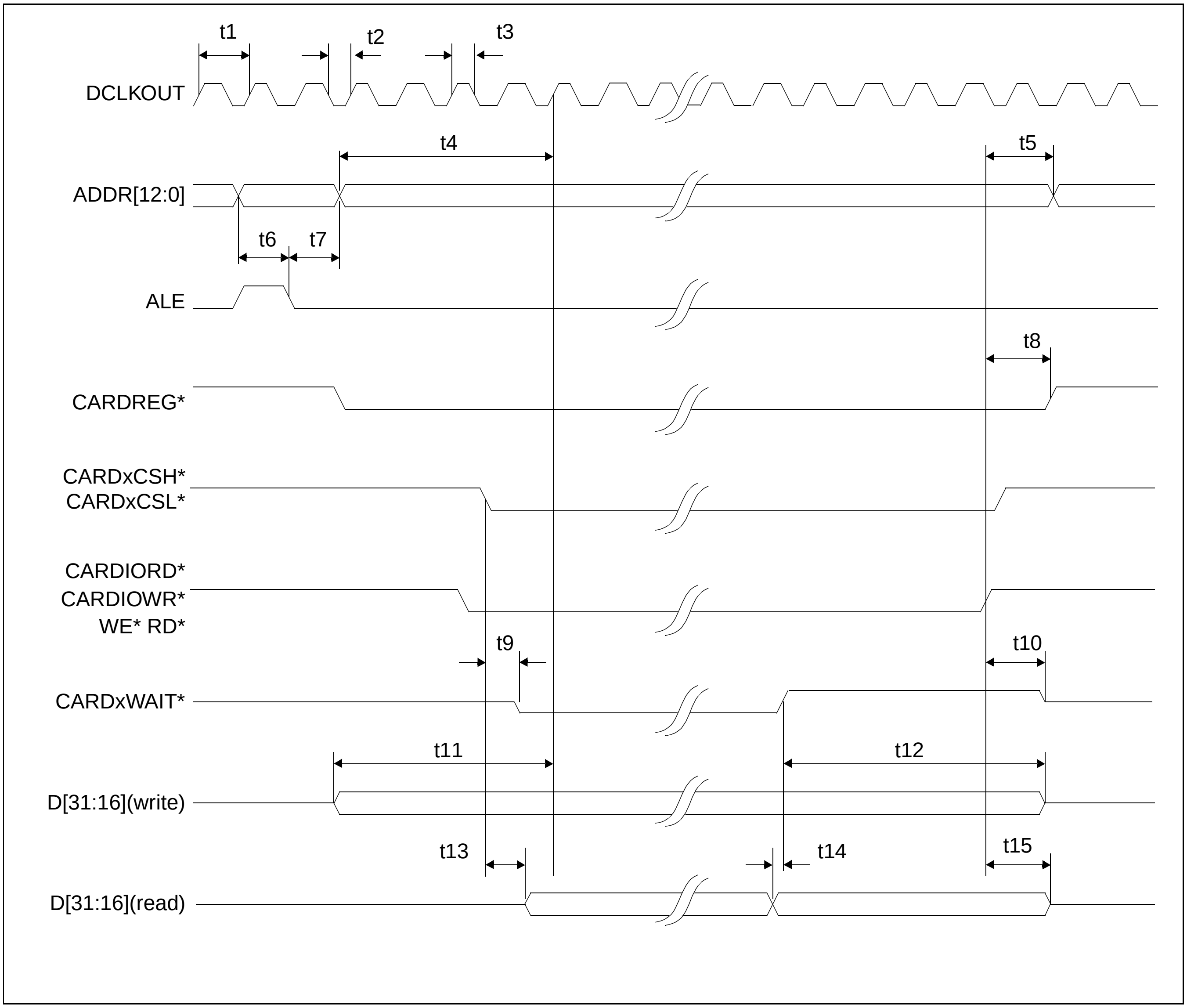


Figure 7-10: Toshiba Timing

Table 7-10: Toshiba Timing

Symbol	Parameter	3.0V Min	3.0V Max	5.0V Min	5.0V Max	Units
t1	Clock period	13.3		13.3		ns
t2	Clock pulse width low	5.4		5.4		ns
t3	Clock pulse width high	5.4		5.4		ns
t4	ADDR[12:0] setup to first CLK of cycle	10		10		ns
t5	ADDR[12:0] hold from command invalid	0		0		ns
t6	ADDR[12:0] setup to falling edge ALE	10		10		ns
t7	ADDR[12:0] hold from falling edge ALE	5		5		ns
t8	CARDREG* hold from command invalid	0		0		ns
t9[1]	Falling edge of chip select to CARDxWAIT* driven	0	15	0	9	ns
t10	Command invalid to CARDxWAIT* tri-state	5	25	2.5	10	ns
t11	D[31:16] valid to first CLK of cycle (write cycle)	10		10		ns
t12	D[31:16] hold from rising edge of CARDxWAIT*	0		0		
t13[2]	Chip select to D[31:16] driven (read cycle)	1		1		ns
t14	D[31:16] setup to rising edge CARDxWAIT* (read cycle)	0		0		ns
t15	Command invalid to D[31:16] tri-state (read cycle)	5	25	2.5	10	ns

1. If the S1D13505 host interface is disabled, the timing for CARDxWAIT* driven is relative to the falling edge of chip select or the second positive edge of DCLKOUT after ADDR[12:0] becomes valid, whichever one is later.
2. If the S1D13505 host interface is disabled, the timing for D[31:16] driven is relative to the falling edge of chip select or the second positive edge of DCLKOUT after ADDR[12:0] becomes valid, whichever one is later.

Note
The Toshiba interface has different clock input requirements as follows:

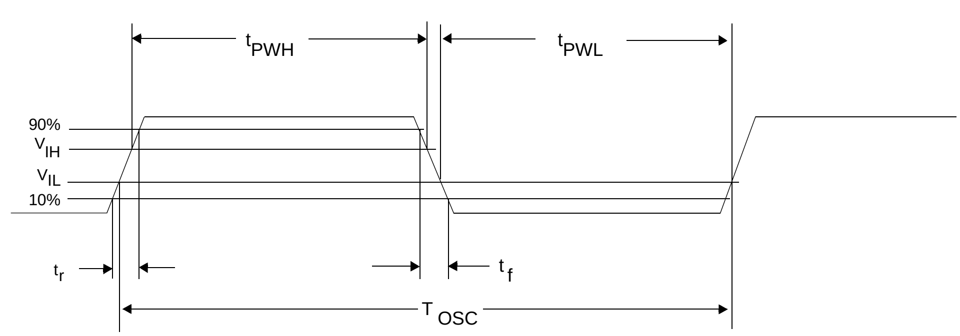


Figure 7-11: Clock Input Requirement

Table 7-11: Clock Input Requirements for BUSCLK using Toshiba local bus

Symbol	Parameter	Min	Max	Units
T_{OSC}	Input Clock Period)	13.3		ns
t_{PWH}	Input Clock Pulse Width High	5.4		ns
t_{PWL}	Input Clock Pulse Width Low	5.4		ns
t_f	Input Clock Fall Time (10% - 90%)		5	ns
t_r	Input Clock Rise Time (10% - 90%)		5	ns

7.1.10 Power PC Interface Timing (e.g. MPC8xx, MC68040, Coldfire)

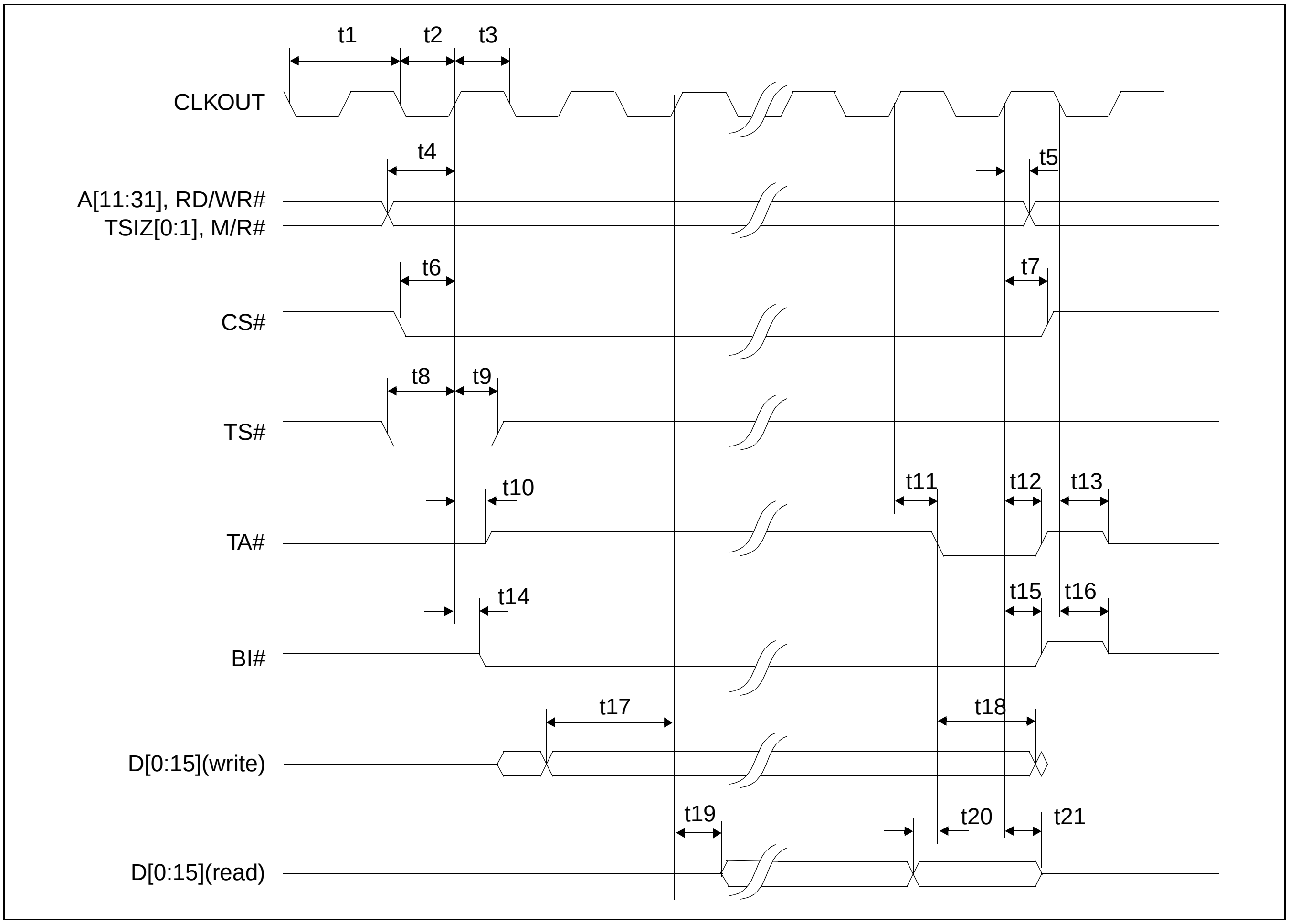


Figure 7-12: Power PC Timing

Note

The above timing diagram is not applicable if the BUSCLK divided by 2 configuration option is selected.

Table 7-12: Power PC Timing

Symbol	Parameter	3.0V Min	3.0V Max	5.0V Min	5.0V Max	Units
t1	Clock period	25		20		ns
t2	Clock pulse width low	6		6		ns
t3	Clock pulse width high	6		6		ns
t4	AB[11:31], RD/WR#, TSIZ[0:1], M/R# setup	10		10		ns
t5	AB[11:31], RD/WR#, TSIZ[0:1], M/R# hold	0		0		ns
t6	CS# setup	10		10		ns
t7	CS# hold	0		0		ns
t8	TS# setup	7		10		ns
t9	TS# hold	5		0		ns
t10	CLKOUT to TA# driven	0		0		ns
t11	CLKOUT to TA# low	3	19	3	12	ns
t12	CLKOUT to TA# high	3	19.7	3	13	ns
t13	negative edge CLKOUT to TA# tri-state	5	25	2.5	10	ns
t14	CLKOUT to BI# driven	0	18	0	11	ns
t15	CLKOUT to BI# high	3	16	3	10	ns
t16	negative edge CLKOUT to BI# tri-state	5	25	2.5	10	ns
t17	D[0:15] setup to 2nd CLKOUT after TS# = 0 (write cycle)	10		10		ns
t18	D[0:15] hold (write cycle)	0		0		ns
t19	CLKOUT to D[0:15] driven (read cycle)	0		0		ns
t20	D[0:15] valid to TA# falling edge (read cycle)	0		0		ns
t21	CLKOUT to D[0:15] tri-state (read cycle)	5	25	2.5	10	ns

7.2 Clock Input Requirements

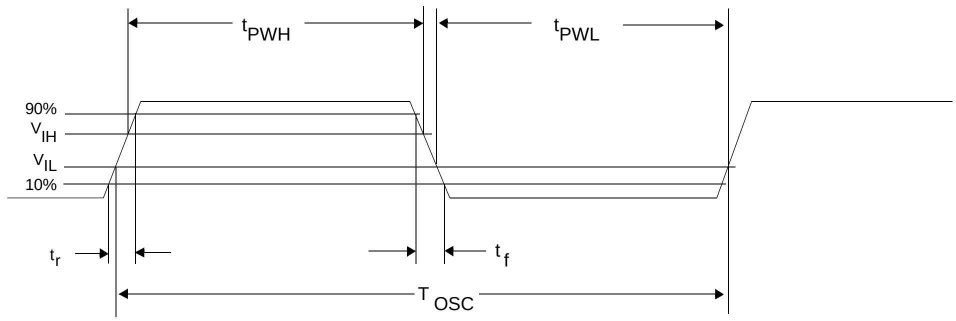


Figure 7-13: Clock Input Requirement

Table 7-13: Clock Input Requirements for CLKI divided down internally (MCLK = CLKI/2)

Symbol	Parameter	Min	Max	Units
T_{OSC}	Input Clock Period	12.5		ns
t_{PWH}	Input Clock Pulse Width High	5.6		ns
t_{PWL}	Input Clock Pulse Width Low	5.6		ns
t_f	Input Clock Fall Time (10% - 90%)		5	ns
t_r	Input Clock Rise Time (10% - 90%)		5	ns

Table 7-14: Clock Input Requirements for CLKI

Symbol	Parameter	Min	Max	Units
T_{OSC}	Input Clock Period	25		ns
t_{PWH}	Input Clock Pulse Width High	11.3		ns
t_{PWL}	Input Clock Pulse Width Low	11.3		ns
t_f	Input Clock Fall Time (10% - 90%)		5	ns
t_r	Input Clock Rise Time (10% - 90%)		5	ns

Note

When CLKI is more than 40MHz, REG[19h] bit 2 must be set to 1 (MCLK = CLKI/2).

7.3 Memory Interface Timing

7.3.1 EDO-DRAM Read/Write/Read-Write Timing

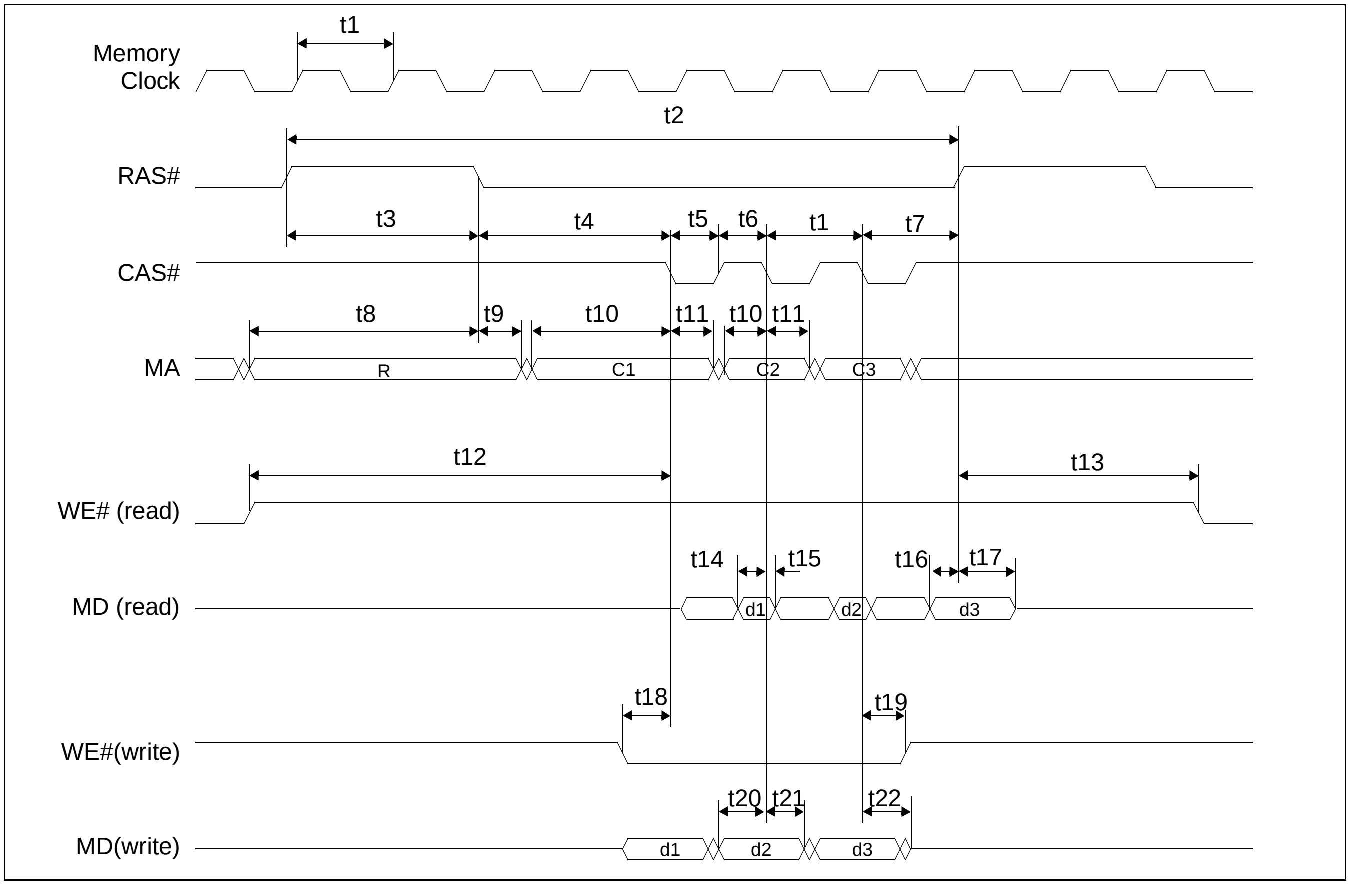


Figure 7-14: EDO-DRAM Read/Write Timing

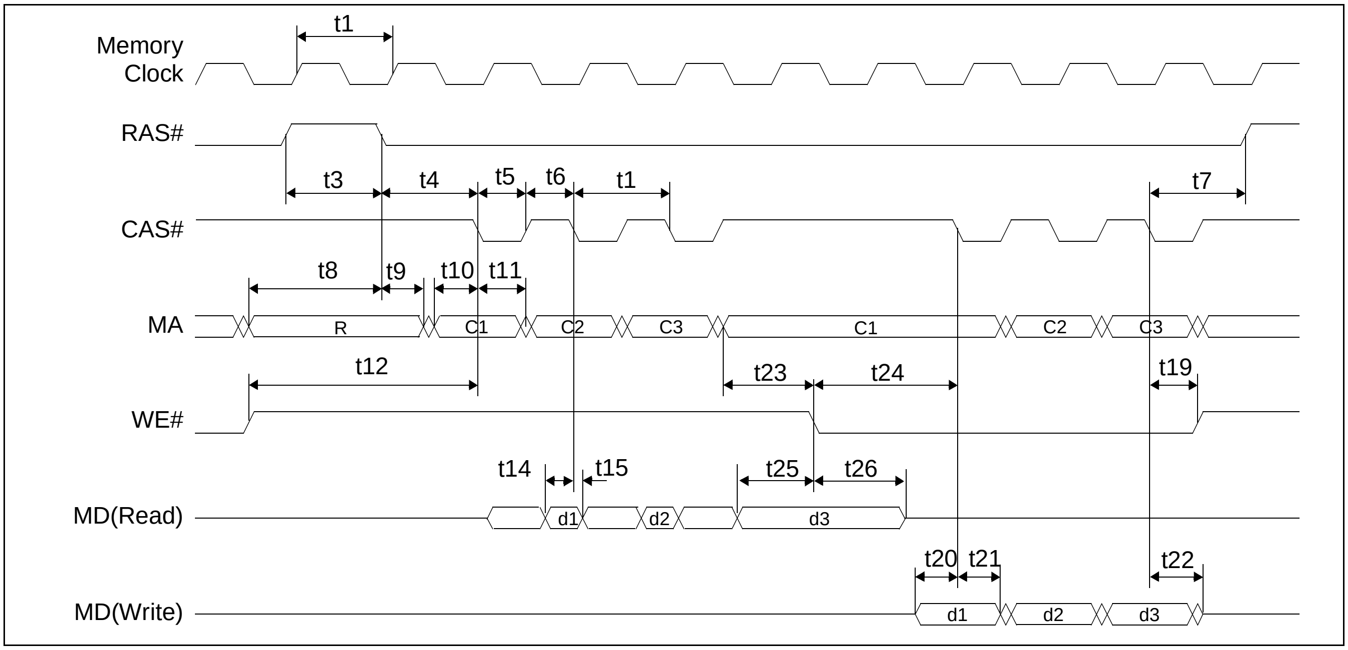


Figure 7-15: EDO-DRAM Read-Write Timing

Table 7-15: EDO-DRAM Read/Write/Read-Write Timing

Symbol	Parameter	Min	Max	Units
t1	Internal memory clock period	25		ns
t2	Random read cycle REG[22h] bit 6-5 == 00	5t1		ns
	Random read cycle REG[22h] bit 6-5 == 01	4t1		ns
	Random read cycle REG[22h] bit 6-5 == 10	3t1		ns
t3	RAS# precharge time (REG[22h] bits 3-2 = 00)	2t1 - 3		ns
	RAS# precharge time (REG[22h] bits 3-2 = 01)	1.45 t1 - 3		ns
	RAS# precharge time (REG[22h] bits 3-2 = 10)	1t1 - 3		ns
t4	RAS# to CAS# delay time (REG[22h] bit 4 = 0 and bits 3-2 = 00 or 10)	2t1 - 3		ns
	RAS# to CAS# delay time (REG[22h] bit 4 = 1 and bits 3-2 = 00 or 10)	1t1 - 3		ns
	RAS# to CAS# delay time (REG[22h] bits 3-2 = 01)	1.45 t1 - 3		ns
t5	CAS# precharge time	0.45 t1 - 3		ns
t6	CAS# pulse width	0.45 t1 - 3		ns
t7	RAS# hold time	1 t1 - 3		ns
t8	Row address setup time (REG[22h] bits 3-2 = 00)	2.45 t1		ns
	Row address setup time (REG[22h] bits 3-2 = 01)	2 t1		ns
	Row address setup time (REG[22h] bits 3-2 = 10)	1.45 t1		ns
t9	Row address hold time (REG[22h] bits 3-2 = 00 or 10)	0.45 t1 - 3		ns
	Row address hold time (REG[22h] bits 3-2 = 01)	1 t1 - 3		ns
t10	Column address setup time	0.45 t1 - 3		ns
t11	Column address hold time	0.45 t1 - 3		ns

Table 7-15: EDO-DRAM Read/Write/Read-Write Timing

Symbol	Parameter	Min	Max	Units
t12	Read Command Setup (REG[22h] bit 4 = 0 and bits 3-2 = 00)	4.45 t1 - 3		ns
	Read Command Setup (REG[22h] bit 4 = 0 and bits 3-2 = 10)	3.45 t1 - 3		ns
	Read Command Setup (REG[22h] bit 4 = 1 and bits 3-2 = 00)	3.45 t1 - 3		ns
	Read Command Setup (REG[22h] bit 4 = 1 and bits 3-2 = 10)	2.45 t1 - 3		ns
	Read Command Setup (REG[22h] bits 3-2 = 01)	3.45 t1 - 3		ns
t13	Read Command Hold (REG[22h] bit 4 = 0 and bits 3-2 = 00)	3.45 t1 - 3		ns
	Read Command Hold (REG[22h] bit 4 = 0 and bits 3-2 = 10)	2.45 t1 - 3		ns
	Read Command Hold (REG[22h] bit 4 = 1 and bits 3-2 = 00)	2.45 t1 - 3		ns
	Read Command Hold (REG[22h] bit 4 = 1 and bits 3-2 = 10)	1.45 t1 - 3		ns
	Read Command Hold (REG[22h] bits 3-2 = 01)	2.45 t1 - 3		ns
t14	Read Data Setup referenced from CAS#	5		ns
t15	Read Data Hold referenced from CAS#	3		ns
t16	Last Read Data Setup referenced from RAS#	5		ns
t17	Bus Turn Off from RAS#	3	t1- 5	ns
t18	Write Command Setup	0.45 t1- 3		ns
t19	Write Command Hold	0.45 t1 - 3		ns
t20	Write Data Setup	0.45 t1 - 3		ns
t21	Write Data Hold	0.45 t1 - 3		ns
t22	MD Tri-state	0.45 t1	0.45t1 + 21	ns
t23	CAS# to WE# active during Read-Write cycle	1 t1 - 3		ns
t24	Write Command Setup during Read-Write cycle	1.45 t1- 3		ns
t25	Last Read Data Setup referenced from WE# during Read-Write cycle	10		ns
t26	Bus Tri-state from WE# during Read-Write cycle	0	t1- 5	ns

7.3.2 EDO-DRAM CAS Before RAS Refresh Timing

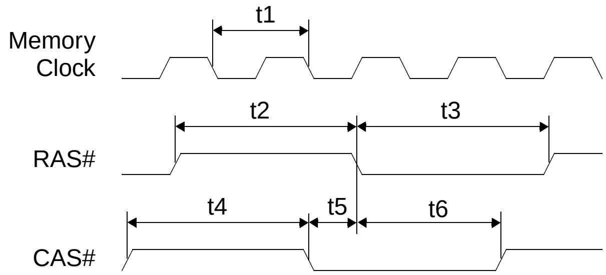


Figure 7-16: EDO-DRAM CAS Before RAS Refresh Timing

Table 7-16: EDO-DRAM CAS Before RAS Refresh Timing

Symbol	Parameter	Min	Max	Units
t1	Internal memory clock period	25		ns
t2	RAS# precharge time (REG[22h] bits 3-2 = 00)	2t1 - 3		ns
	RAS# precharge time (REG[22h] bits 3-2 = 01)	1.45t1 - 3		ns
	RAS# precharge time (REG[22h] bits 3-2 = 10)	1t1 - 3		ns
t3	RAS# pulse width (REG[22h] bit 6-5 = 00 and bits 3-2 = 00)	3 t1 - 3		ns
	RAS# pulse width (REG[22h] bit 6-5 = 00 and bits 3-2 = 01)	3.45 t1 - 3		ns
	RAS# pulse width (REG[22h] bit 6-5 = 00 and bits 3-2 = 10)	4 t1 - 3		ns
	RAS# pulse width (REG[22h] bit 6-5 = 01 and bits 3-2 = 00)	2 t1 - 3		ns
	RAS# pulse width (REG[22h] bit 6-5 = 01 and bits 3-2 = 01)	2.45 t1 - 3		ns
	RAS# pulse width (REG[22h] bit 6-5 = 01 and bits 3-2 = 10)	3 t1 - 3		ns
	RAS# pulse width (REG[22h] bit 6-5 = 10 and bits 3-2 = 00)	1 t1 - 3		ns
	RAS# pulse width (REG[22h] bit 6-5 = 10 and bits 3-2 = 01)	1.45 t1 - 3		ns
	RAS# pulse width (REG[22h] bit 6-5 = 10 and bits 3-2 = 10)	2 t1 - 3		ns
t4	CAS# pulse width	t2		ns
t5	CAS# setup time (REG[22h] bits 3-2 = 00 or 10)	0.45 t1 - 3		ns
	CAS# setup time (REG[22h] bits 3-2 = 01)	1 t1 - 3		ns

Table 7-16: EDO-DRAM CAS Before RAS Refresh Timing

Symbol	Parameter	Min	Max	Units
t6	CAS# Hold to RAS# (REG[22h] bit 6-5 = 00 and bits 3-2 = 00)	2.45 t1 - 3		ns
	CAS# Hold to RAS# (REG[22h] bit 6-5 = 00 and bits 3-2 = 01)	3 t1 - 3		ns
	CAS# Hold to RAS# (REG[22h] bit 6-5 = 00 and bits 3-2 = 10)	3.45 t1 - 3		ns
	CAS# Hold to RAS# (REG[22h] bit 6-5 = 01 and bits 3-2 = 00)	1.45 t1 - 3		ns
	CAS# Hold to RAS# (REG[22h] bit 6-5 = 01 and bits 3-2 = 01)	2 t1 - 3		ns
	CAS# Hold to RAS# (REG[22h] bit 6-5 = 01 and bits 3-2 = 10)	2.45 t1 - 3		ns
	CAS# Hold to RAS# (REG[22h] bit 6-5 = 10 and bits 3-2 = 00)	0.45 t1 - 3		ns
	CAS# Hold to RAS# (REG[22h] bit 6-5 = 10 and bits 3-2 = 01)	1 t1 - 3		ns
	CAS# Hold to RAS# (REG[22h] bit 6-5 = 10 and bits 3-2 = 10)	1.45 t1 - 3		ns

7.3.3 EDO-DRAM Self-Refresh Timing

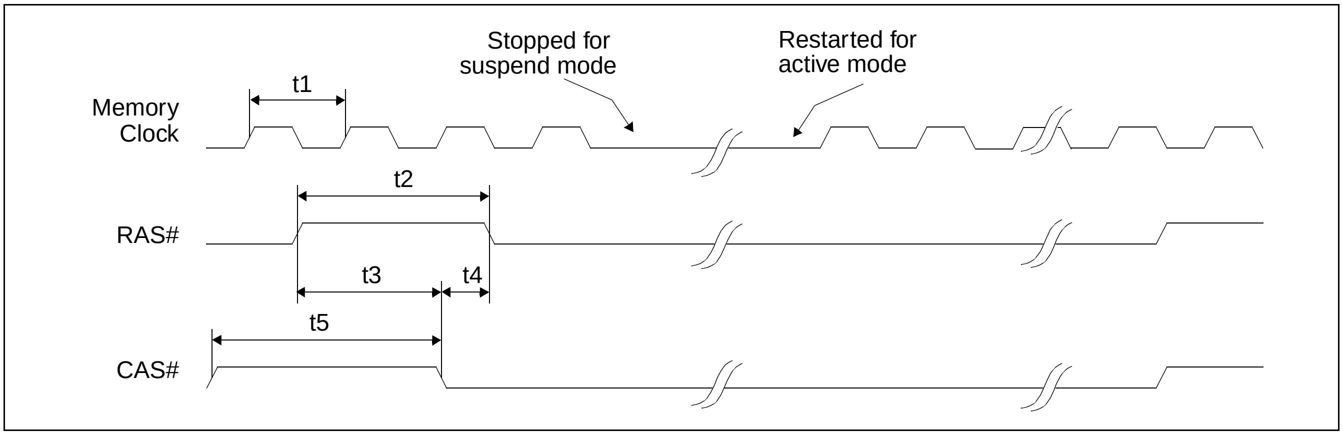


Figure 7-17: EDO-DRAM Self-Refresh Timing

Table 7-17: EDO-DRAM Self-Refresh Timing

Symbol	Parameter	Min	Max	Units
t1	Internal memory clock period	25		ns
t2	RAS# precharge time (REG[22h] bits 3-2 = 00)	2 t1 - 3		ns
	RAS# precharge time (REG[22h] bits 3-2 = 01)	1.45t1 - 3		ns
	RAS# precharge time (REG[22h] bits 3-2 = 10)	1 t1 - 3		ns
t3	RAS# to CAS# precharge time (REG[22h] bits 3-2 = 00)	1.45t1 - 3		ns
	RAS# to CAS# precharge time (REG[22h] bits 3-2 = 01 or 10)	0.45t1 - 3		ns
t4	CAS# setup time (REG[22h] bits 3-2 = 00 or 10)	0.45t1 - 3		ns
	CAS# setup time (REG[22h] bits 3-2 = 01)	1 t1 - 3		ns
t5	CAS# precharge time (REG[22h] bits 3-2 = 00)	2 t1 - 3		ns
	CAS# precharge time (REG[22h] bits 3-2 = 01 or 10)	1 t1 - 3		ns

7.3.4 FPM-DRAM Read/Write/Read-Write Timing

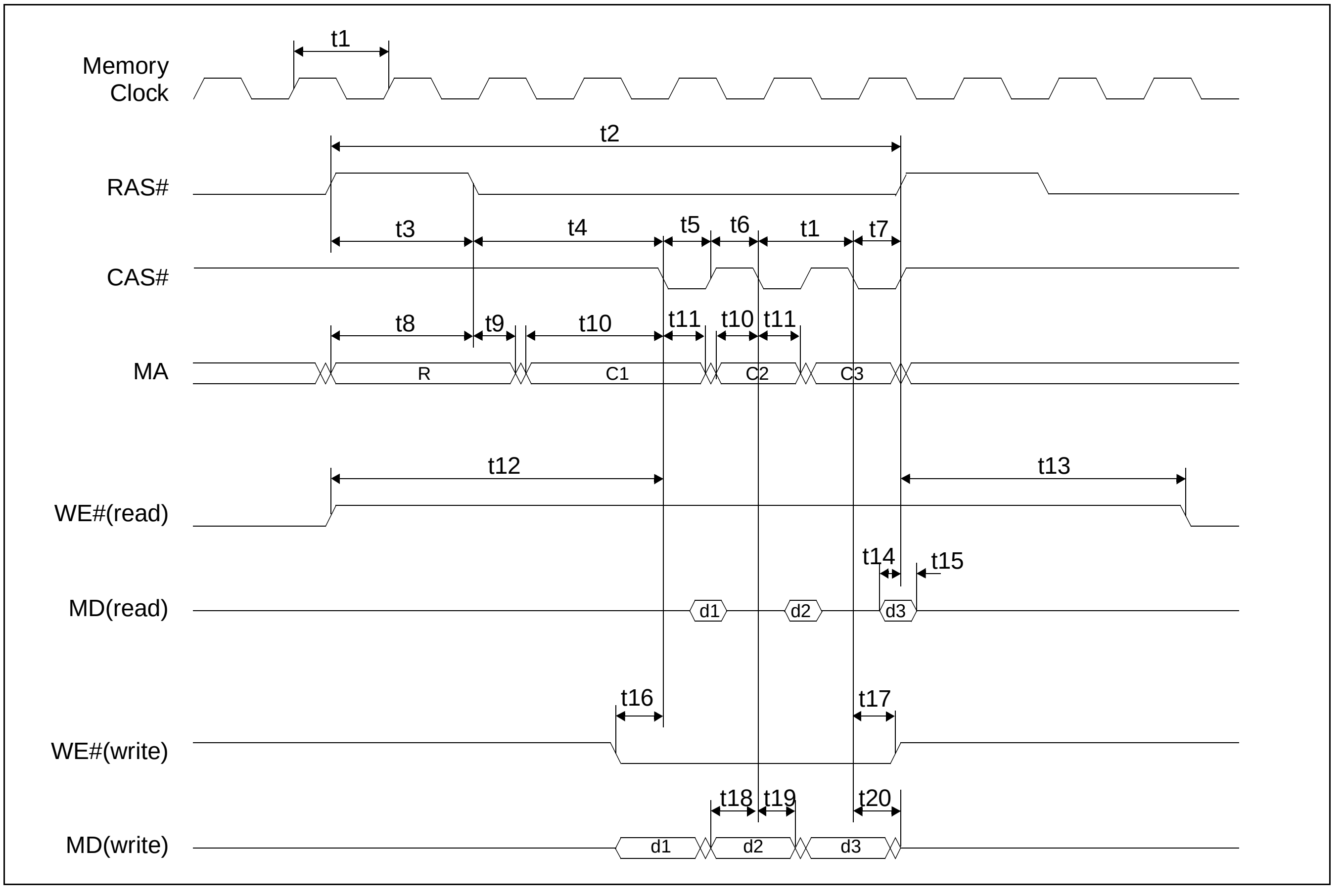


Figure 7-18: FPM-DRAM Read/Write Timing

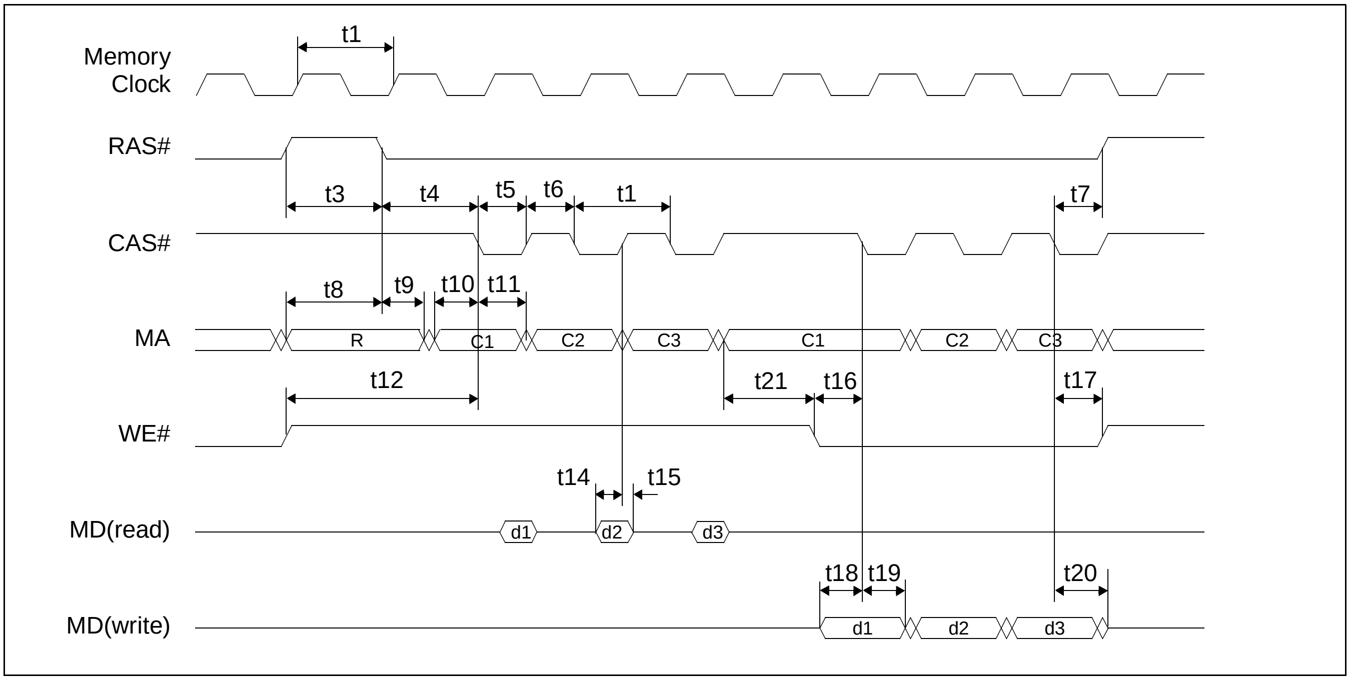


Figure 7-19: FPM-DRAM Read-Write Timing

Table 7-18: FPM-DRAM Read/Write/Read-Write Timing

Symbol	Parameter	Min	Max	Units
t1	Internal memory clock period	40		ns
t2	Random read cycle REG[22h] bit 6-5 == 00	5t1		ns
	Random read cycle REG[22h] bit 6-5 == 01	4t1		ns
	Random read cycle REG[22h] bit 6-5 == 10	3t1		ns
t3	RAS# precharge time (REG[22h] bits 3-2 = 00)	2 t1 - 3		ns
	RAS# precharge time (REG[22h] bits 3-2 = 01)	1.45 t1 - 3		ns
	RAS# precharge time (REG[22h] bits 3-2 = 10)	1 t1 - 3		ns
t4	RAS# to CAS# delay time (REG[22h] bit 4 = 1 and bits 3-2 = 00 or 10)	1.45 t1 - 3		ns
	RAS# to CAS# delay time (REG[22h] bit 4 = 0 and bits 3-2 = 00 or 10)	2.45 t1 - 3		ns
	RAS# to CAS# delay time (REG[22h] bit 4 = 1 and bits 3-2 = 01)	1t1 - 3		ns
	RAS# to CAS# delay time (REG[22h] bit 4 = 0 and bits 3-2 = 01)	2t1 - 3		ns
t5	CAS# precharge time	0.45 t1 - 3		ns
t6	CAS# pulse width	0.45 t1 - 3		ns
t7	RAS# hold time	0.45 t1 - 3		ns
t8	Row address setup time (REG[22h] bits 3-2 = 00)	2 t1 - 3		ns
	Row address setup time (REG[22h] bits 3-2 = 01)	1.45 t1 - 3		ns
	Row address setup time (REG[22h] bits 3-2 = 10)	1 t1 - 3		ns

Table 7-18: FPM-DRAM Read/Write/Read-Write Timing

Symbol	Parameter	Min	Max	Units
t9	Row address hold time (REG[22h] bits 3-2 = 00 or 10)	t1 - 3		ns
	Row address hold time (REG[22h] bits 3-2 = 01)	0.45 1t1 - 3		ns
t10	Column address setup time	0.45 t1 - 3		ns
t11	Column address hold time	0.45 t1 - 3		ns
t12	Read Command Setup (REG[22h] bit 4 = 0 and bits 3-2 = 00)	4.45 t1 - 3		ns
	Read Command Setup (REG[22h] bit 4 = 0 and bits 3-2 = 01 or 10)	3.45 t1 - 3		ns
	Read Command Setup (REG[22h] bit 4 = 1 and bits 3-2 = 00)	3.45 t1 - 3		ns
	Read Command Setup (REG[22h] bit 4 = 1 and bits 3-2 = 01 or 10)	2.45 t1 - 3		ns
t13	Read Command Hold (REG[22h] bit 4 = 0 and bits 3-2 = 00)	4 t1 - 3		ns
	Read Command Hold (REG[22h] bit 4 = 0 and bits 3-2 = 01 or 10)	3 t1 - 3		ns
	Read Command Hold (REG[22h] bit 4 = 1 and bits 3-2 = 00)	3 t1 - 3		ns
	Read Command Hold (REG[22h] bit 4 = 1 and bits 3-2 = 01 or 10)	2 t1 - 3		ns
t14	Read Data Setup referenced from CAS#	5		ns
t15	Bus Tri-State	3	t1- 5	ns
t16	Write Command Setup	0.45 t1- 3		ns
t17	Write Command Hold	0.45 t1 - 3		ns
t18	Write Data Setup	0.45 t1 - 3		ns
t19	Write Data Hold	0.45 t1 - 3		ns
t20	MD Tri-state	0.45 t1	0.45t1 + 21	ns
t21	CAS# to WE# active during Read-Write cycle	0.45 t1 - 3		ns

7.3.5 FPM-DRAM CAS Before RAS Refresh Timing

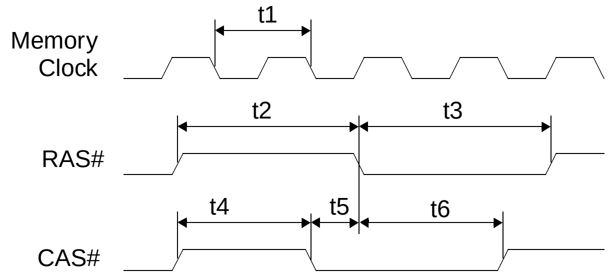


Figure 7-20: FPM-DRAM CAS Before RAS Refresh Timing

Table 7-19: FPM-DRAM CAS Before RAS Refresh Timing

Symbol	Parameter	Min	Max	Units
t1	Internal memory clock period	40		ns
t2	RAS# precharge time (REG[22h] bits 3-2 = 00)	2.45 t1 - 3		ns
	RAS# precharge time (REG[22h] bits 3-2 = 01 or 10)	1.45 t1 - 3		ns
t3	RAS# pulse width (REG[22h] bits 6-5 = 00 and bits 3-2 = 00)	2.45 t1 - 3		ns
	RAS# pulse width (REG[22h] bits 6-5 = 00 and bits 3-2 = 01 or 10)	3.45 t1 - 3		ns
	RAS# pulse width (REG[22h] bits 6-5 = 01 and bits 3-2 = 00)	1.45 t1 - 3		ns
	RAS# pulse width (REG[22h] bits 6-5 = 01 and bits 3-2 = 01 or 10)	2.45 t1 - 3		ns
	RAS# pulse width (REG[22h] bits 6-5 = 10 and bits 3-2 = 00)	0.45 t1 - 3		ns
	RAS# pulse width (REG[22h] bits 6-5 = 10 and bits 3-2 = 01 or 10)	1.45 t1 - 3		ns
t4	CAS# pulse width (REG[22h] bits 3-2 = 00)	2 t1 - 3		ns
	CAS# pulse width (REG[22h] bits 3-2 = 01 or 10)	1 t1 - 3		
t5	CAS# Setup to RAS#	0.45 t1 - 3		ns
t6	CAS# Hold to RAS# (REG[22h] bits 6-5 = 00 and bits 3-2 = 00)	2.45 t1 - 3		ns
	CAS# Hold to RAS# (REG[22h] bits 6-5 = 00 and bits 3-2 = 01 or 10)	3.45 t1 - 3		ns
	CAS# Hold to RAS# (REG[22h] bits 6-5 = 01 and bits 3-2 = 00)	1.45 t1 - 3		ns
	CAS# Hold to RAS# (REG[22h] bits 6-5 = 01 and bits 3-2 = 01 or 10)	2.45 t1 - 3		ns
	CAS# Hold to RAS# (REG[22h] bits 6-5 = 10 and bits 3-2 = 00)	0.45 t1 - 3		ns
	CAS# Hold to RAS# (REG[22h] bits 6-5 = 10 and bits 3-2 = 01 or 10)	1.45 t1 - 3		ns

7.3.6 FPM-DRAM Self-Refresh Timing

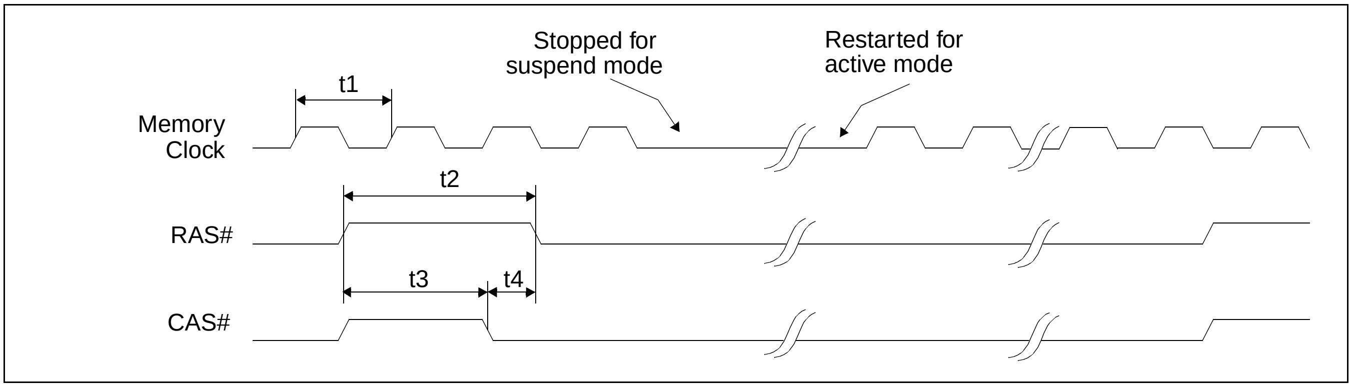


Figure 7-21: FPM-DRAM Self-Refresh Timing

Table 7-20: FPM-DRAM CBR Self-Refresh Timing

Symbol	Parameter	Min	Max	Units
t1	Internal memory clock	40		ns
t2	RAS# precharge time (REG[22h] bits 3-2 = 00)	2.45 t1 - 1		ns
	RAS# precharge time (REG[22h] bits 3-2 = 01 or 10)	1.45 t1 - 1		ns
t3	RAS# to CAS# precharge time (REG[22h] bits 3-2 = 00)	2 t1		ns
	RAS# to CAS# precharge time (REG[22h] bits 3-2 = 01 or 10)	1 t1		ns
t4	CAS# setup time (CAS# before RAS# refresh)	0.45 t1 - 2		ns

7.4 Power Sequencing

7.4.1 LCD Power Sequencing

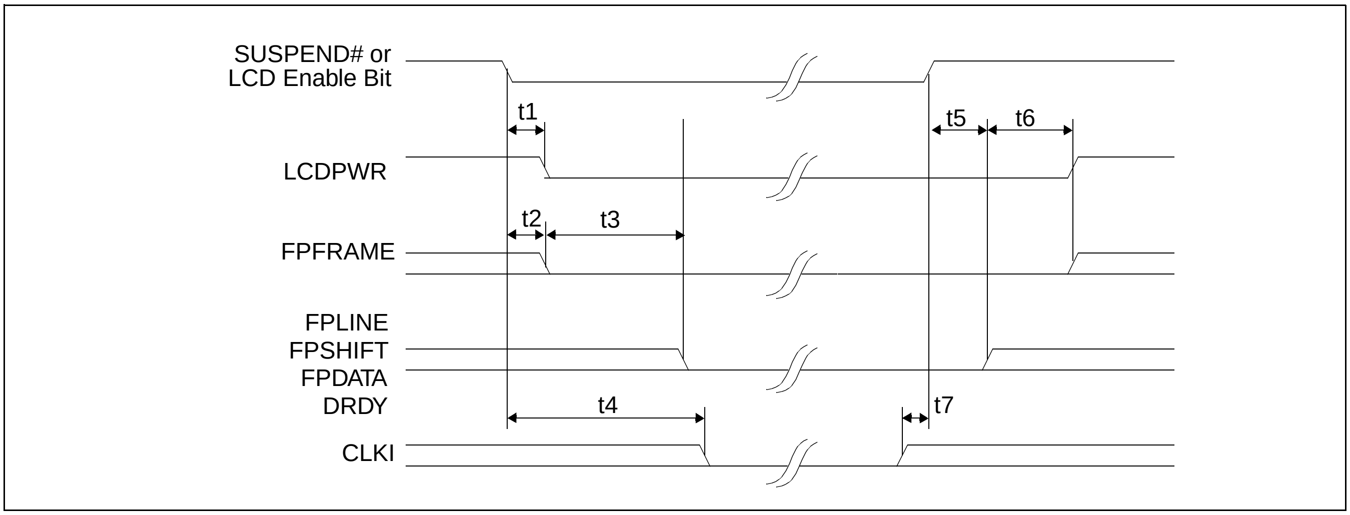


Figure 7-22: LCD Panel Power Off / Power On Timing. Drawn with LCDPWR set to active high polarity

Table 7-21: LCD Panel Power Off/ Power On

Symbol	Parameter	Min	Max	Units
t1	SUSPEND# or LCD ENABLE BIT low to LCDPWR off		$2T_{FPFRAME}$ + $8T_{PCLK}$	ns
t2	SUSPEND# or LCD ENABLE BIT low to FPFRAME inactive		1	Frames
t3	FPFRAME inactive to FPLINE, FPSHIFT, FPDATA, DRDY inactive	128		Frames
t4	SUSPEND# to CLKI inactive	130		Frames
t5	SUSPEND# or LCD ENABLE BIT high to FPLINE, FPSHIFT, FPDATA, DRDY active		$T_{FPFRAME}$ + $8T_{PCLK}$	ns
t6	FPLINE, FPSHIFT, FPDATA, DRDY active to LCDPWR, on and FPFRAME active	128		Frames
t7	CLKI active to SUSPEND# inactive	0		ns

Note

Where $T_{FPFRAME}$ is the period of FPFRAME and T_{PCLK} is the period of the pixel clock.

7.4.2 Power Save Status

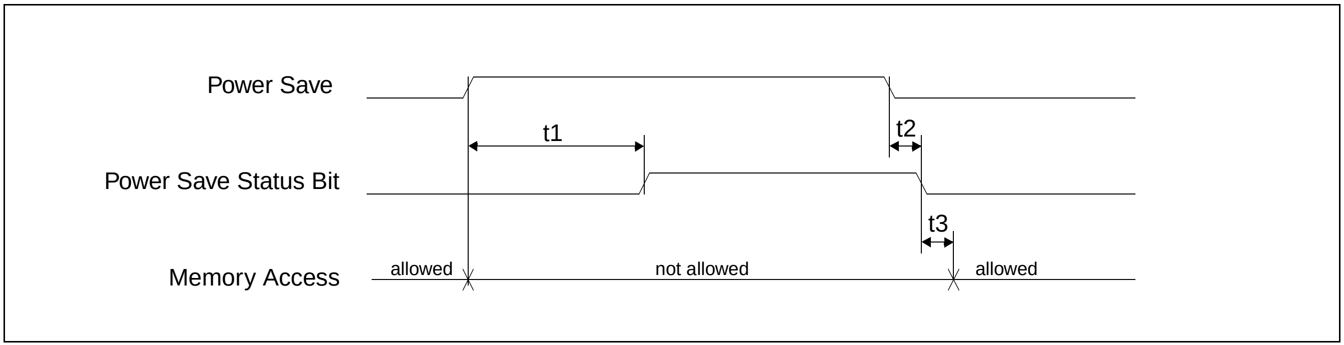


Figure 7-23: Power Save Status and Local Bus Memory Access Relative to Power Save Mode

Note
Power Save can be initiated through either the SUSPEND# pin or Software Suspend Enable Bit.

Table 7-22: Power Save Status and Local Bus Memory Access Relative to Power Save Mode

Symbol	Parameter	Min	Max	Units
t1	Power Save initiated to rising edge of Power Save Status and the last time memory access by the local bus may be performed.	129	130	Frames
t2	Power Save deactivated to falling edge of Power Save Status		12	MCLK
t3	Falling edge of Power Save Status to the earliest time the local bus may perform a memory access		8	MCLK

Note
It is recommended that memory access not be performed after a Power Save Mode has been initiated.

7.5 Display Interface

7.5.1 4-Bit Single Monochrome Passive LCD Panel Timing

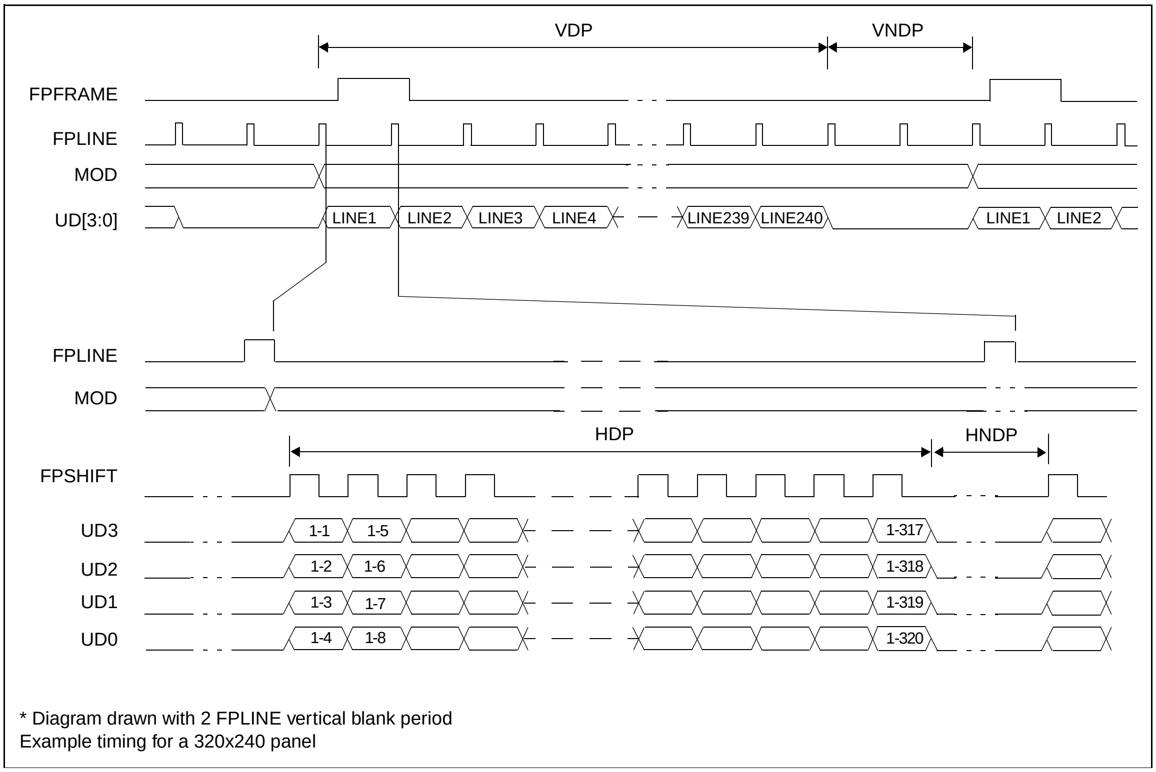


Figure 7-24: 4-Bit Single Monochrome Passive LCD Panel Timing

VDP =	Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP =	Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP =	Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP =	Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1)*8Ts

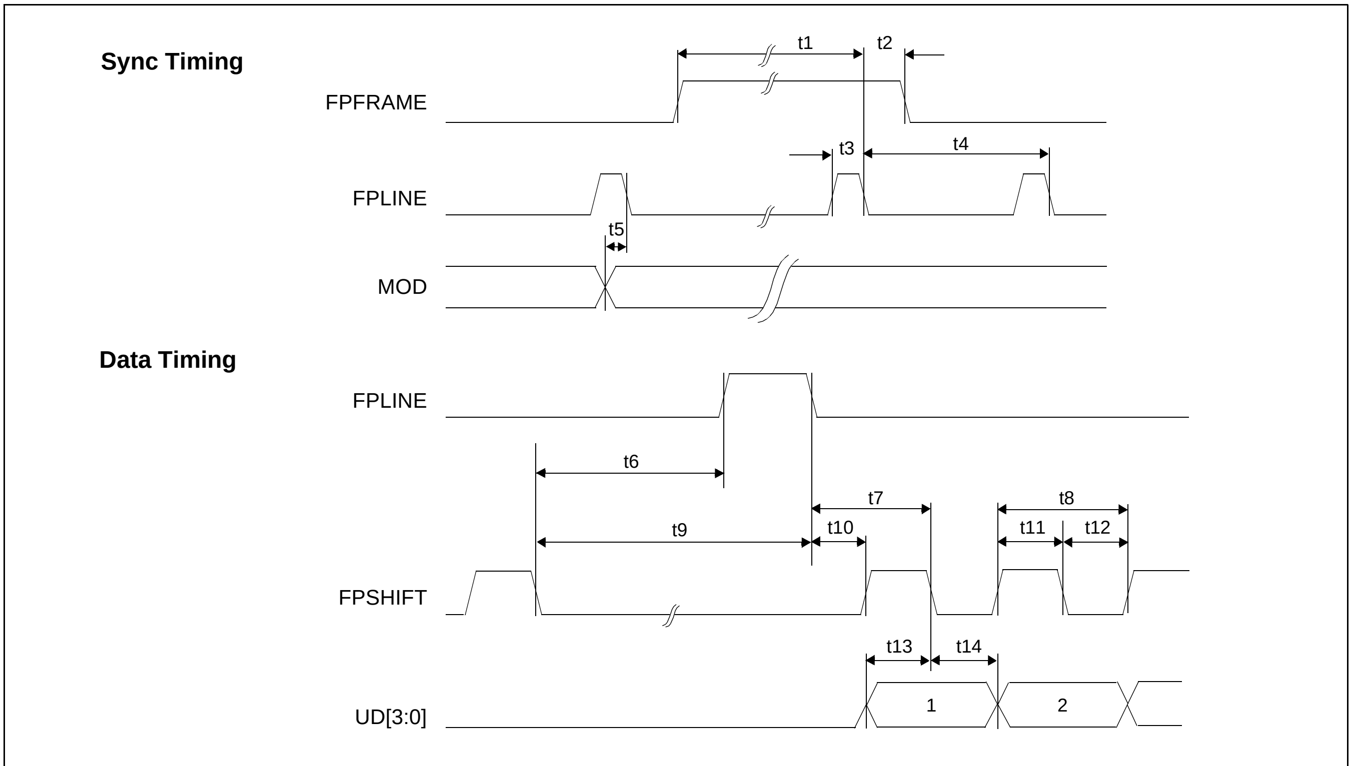


Figure 7-25: 4-Bit Single Monochrome Passive LCD Panel A.C. Timing

Table 7-23: 4-Bit Single Monochrome Passive LCD Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE pulse trailing edge	note 2			
t2	FPFRAME hold from FPLINE pulse trailing edge	14			Ts (note 1)
t3	FPLINE pulse width	9			Ts
t4	FPLINE period	note 3			
t5	MOD transition to FPLINE pulse trailing edge	1		note 4	Ts
t6	FPSHIFT falling edge to FPLINE pulse leading edge	note 5			
t7	FPLINE pulse trailing edge to FPSHIFT falling edge	t10 + t11			Ts
t8	FPSHIFT period	4			Ts
t9	FPSHIFT falling edge to FPLINE pulse trailing edge	note 6			
t10	FPLINE pulse trailing edge to FPSHIFT rising edge	20			Ts
t11	FPSHIFT pulse width high	2			Ts
t12	FPSHIFT pulse width low	2			Ts
t13	UD[3:0] setup to FPSHIFT falling edge	2			Ts
t14	UD[3:0] hold to FPSHIFT falling edge	2			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t4_{min}$ - 14Ts
3. $t4_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] + 33 Ts
4. $t5_{min}$ = [(((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8)-1] Ts
5. $t6_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 27] Ts
6. $t9_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 18] Ts

7.5.2 8-Bit Single Monochrome Passive LCD Panel Timing

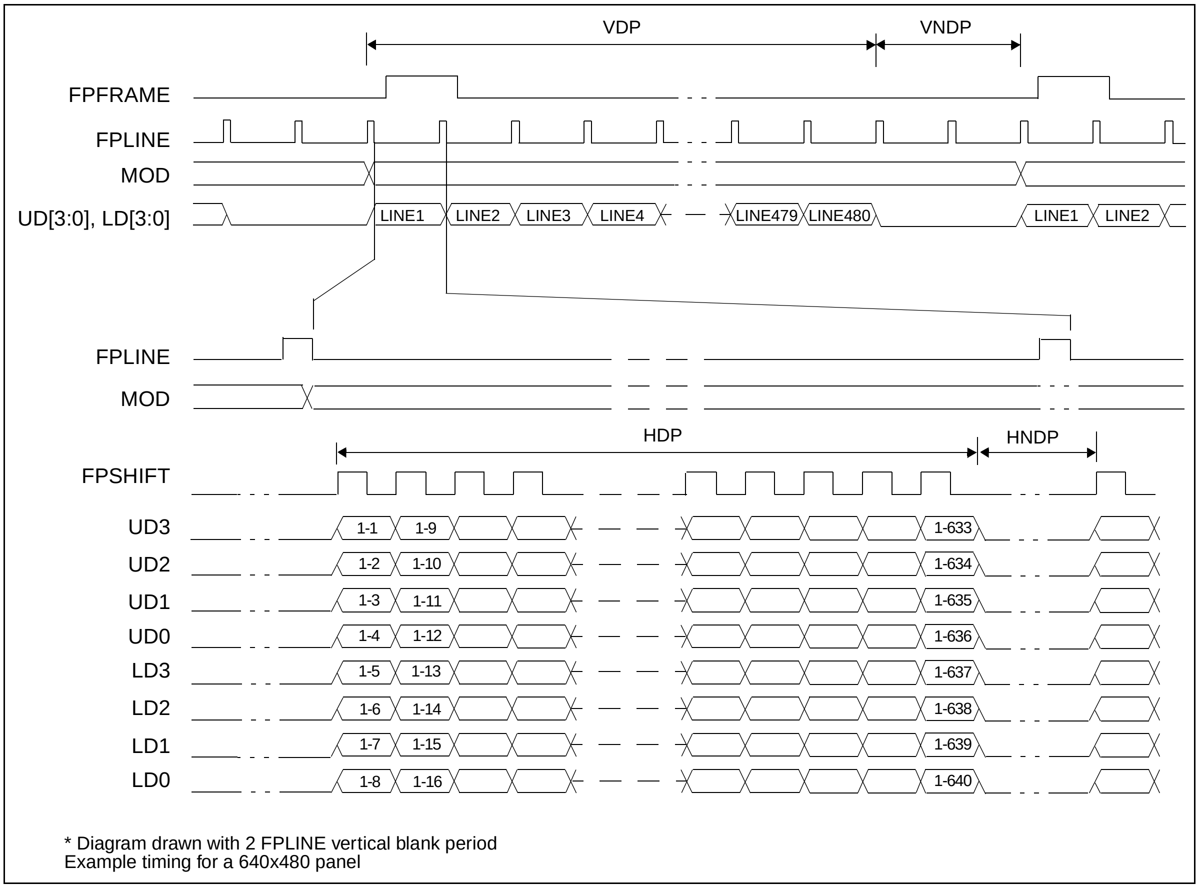


Figure 7-26: 8-Bit Single Monochrome Passive LCD Panel Timing

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1)*8Ts

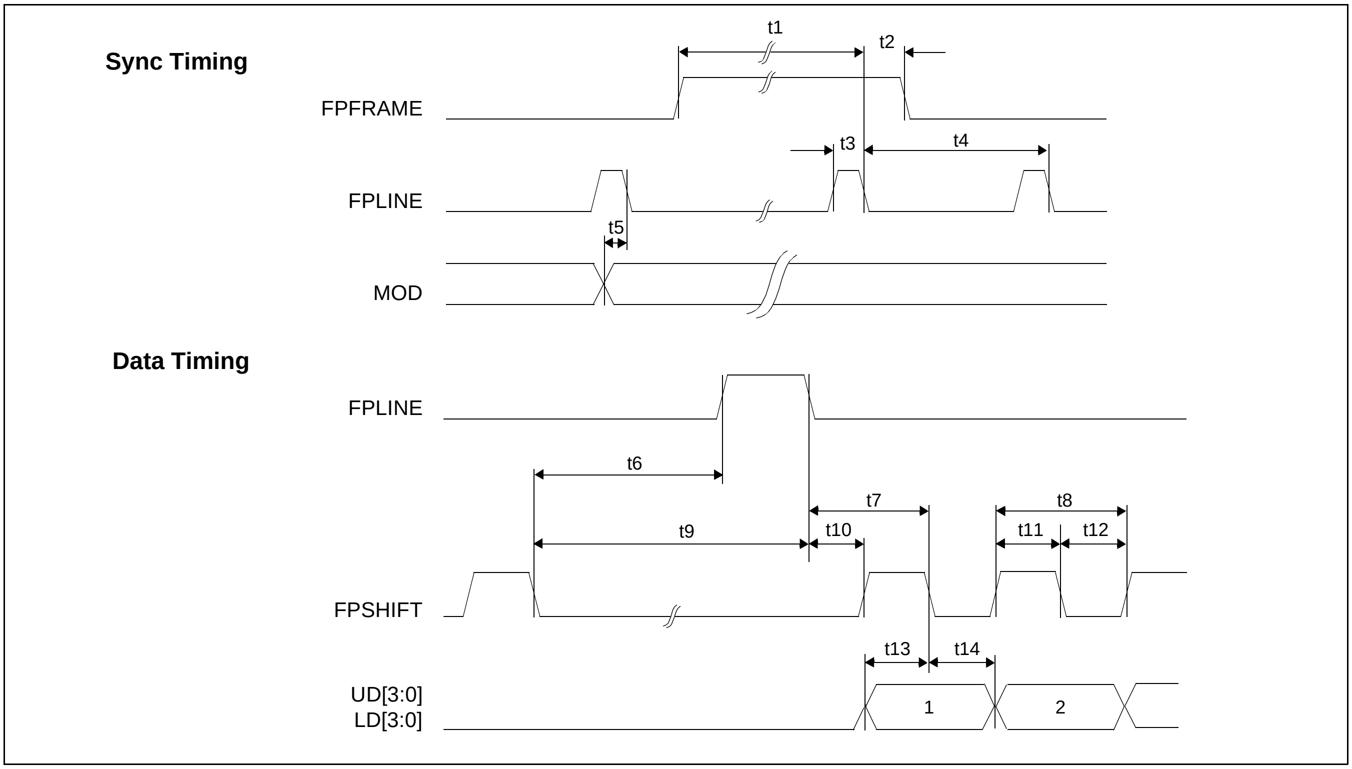


Figure 7-27: 8-Bit Single Monochrome Passive LCD Panel A.C. Timing

Table 7-24: 8-Bit Single Monochrome Passive LCD Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE pulse trailing edge	note 2			
t2	FPFRAME hold from FPLINE pulse trailing edge	14			Ts (note 1)
t3	FPLINE pulse width	9			Ts
t4	FPLINE period	note 3			
t5	MOD transition to FPLINE pulse trailing edge	1		note 4	Ts
t6	FPSHIFT falling edge to FPLINE pulse leading edge	note 5			
t7	FPLINE pulse trailing edge to FPSHIFT falling edge	t10 + t11			Ts
t8	FPSHIFT period	8			Ts
t9	FPSHIFT falling edge to FPLINE pulse trailing edge	note 6			
t10	FPLINE pulse trailing edge to FPSHIFT rising edge	20			Ts
t11	FPSHIFT pulse width high	4			Ts
t12	FPSHIFT pulse width low	4			Ts
t13	UD[3:0], LD[3:0] setup to FPSHIFT falling edge	4			Ts
t14	UD[3:0], LD[3:0] hold to FPSHIFT falling edge	4			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t4_{min}$ - 14Ts
3. $t4_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] + 33 Ts
4. $t5_{min}$ = [(((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8)-1] Ts
5. $t6_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 25] Ts
6. $t9_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 16] Ts

7.5.3 4-Bit Single Color Passive LCD Panel Timing

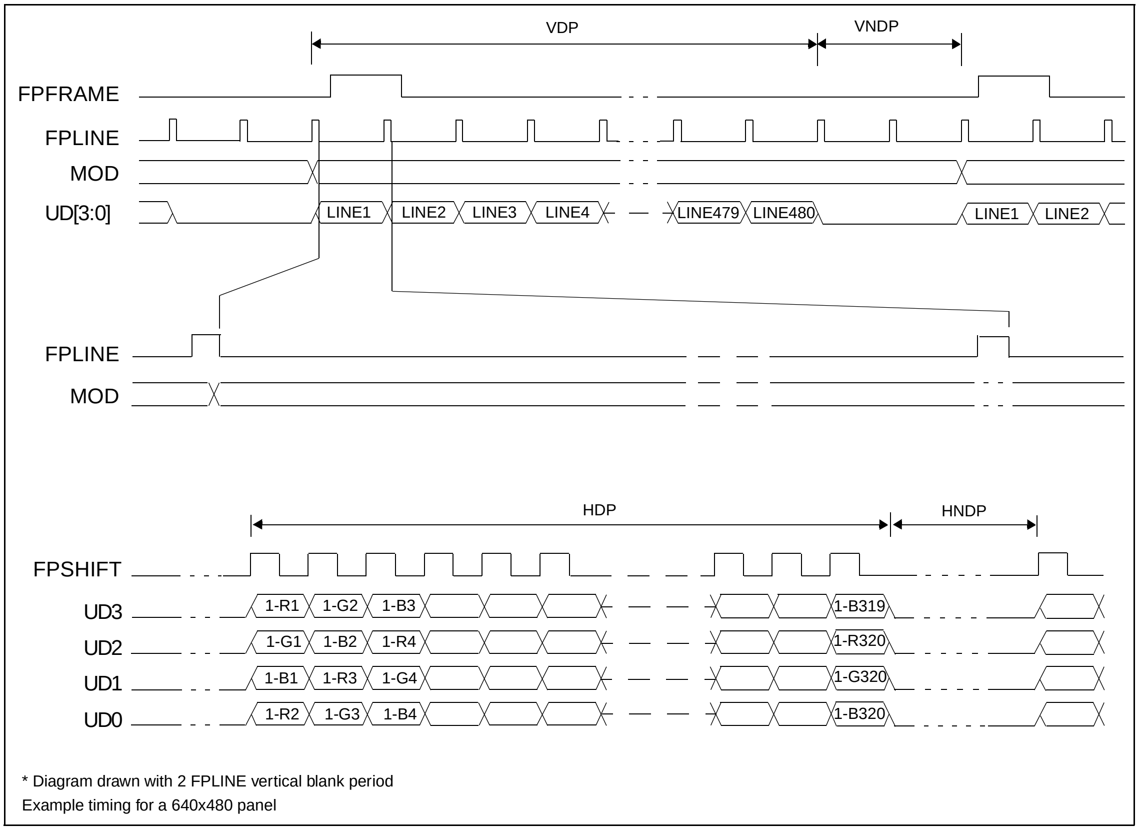


Figure 7-28: 4-Bit Single Color Passive LCD Panel Timing

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1)*8Ts

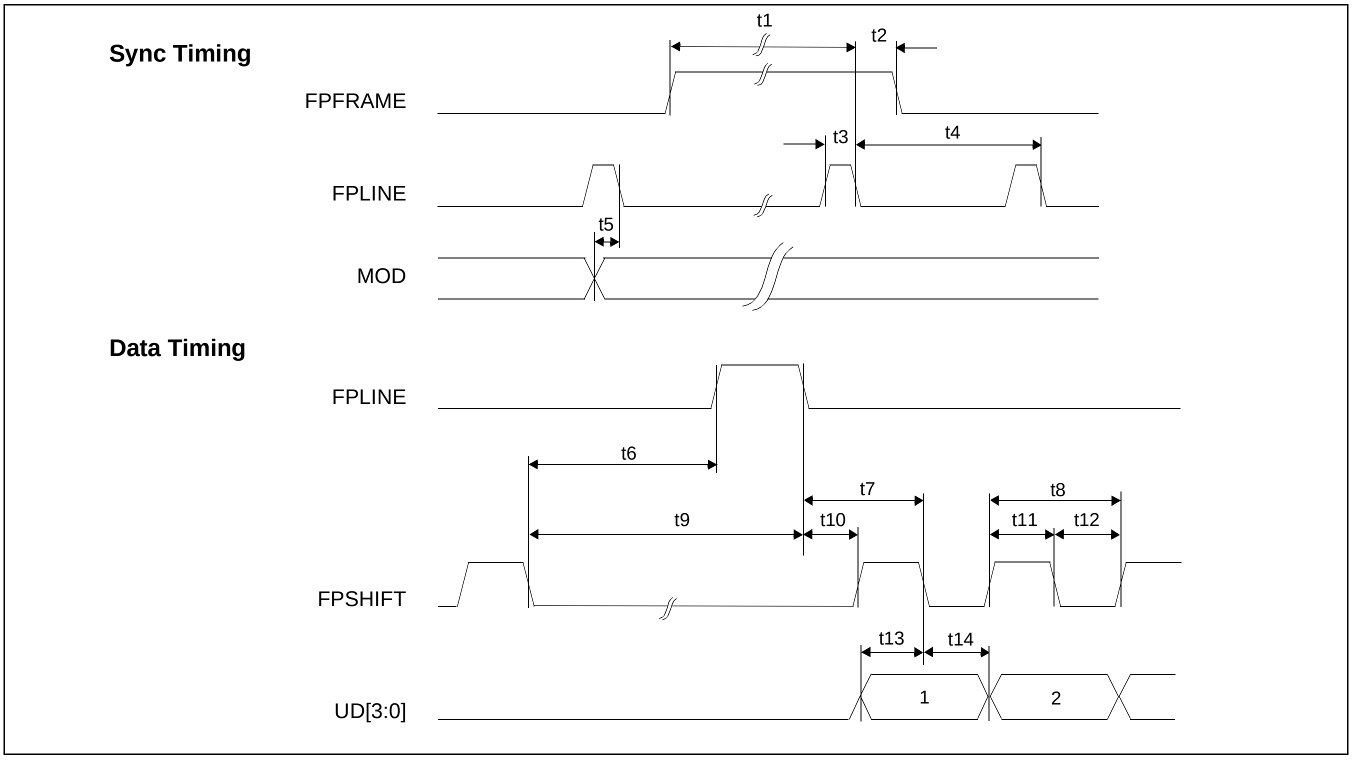


Figure 7-29: 4-Bit Single Color Passive LCD Panel A.C. Timing

Table 7-25: 4-Bit Single Color Passive LCD Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE pulse trailing edge	note 2			
t2	FPFRAME hold from FPLINE pulse trailing edge	14			Ts (note 1)
t3	FPLINE pulse width	9			Ts
t4	FPLINE period	note 3			
t5	MOD transition to FPLINE pulse trailing edge	1		note 4	Ts
t6	FPSHIFT falling edge to FPLINE pulse leading edge	note 5			
t7	FPLINE pulse trailing edge to FPSHIFT falling edge	t10 + t11			Ts
t8	FPSHIFT period	1			Ts
t9	FPSHIFT falling edge to FPLINE pulse trailing edge	note 6			
t10	FPLINE pulse trailing edge to FPSHIFT rising edge	21			Ts
t11	FPSHIFT pulse width high	0.45			Ts
t12	FPSHIFT pulse width low	0.45			Ts
t13	UD[3:0], setup to FPSHIFT falling edge	0.45			Ts
t14	UD[3:0], hold from FPSHIFT falling edge	0.45			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t4_{min}$ - 14Ts
3. $t4_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] + 33 Ts
4. $t5_{min}$ =[(((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8)-1] Ts
5. $t6_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 28] Ts
6. $t9_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 19] Ts

7.5.4 8-Bit Single Color Passive LCD Panel Timing (Format 1)

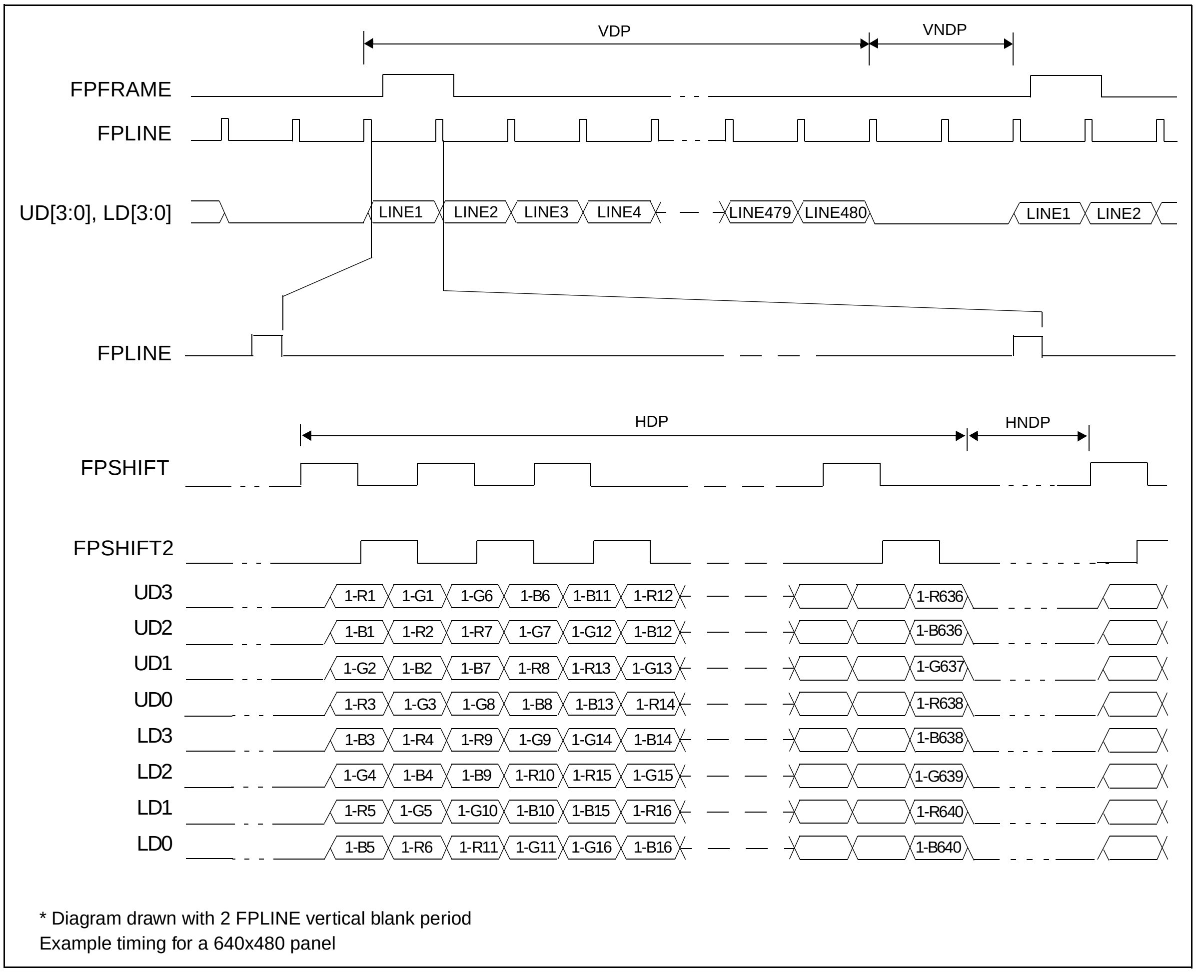


Figure 7-30: 8-Bit Single Color Passive LCD Panel Timing (Format 1)

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1)*8Ts

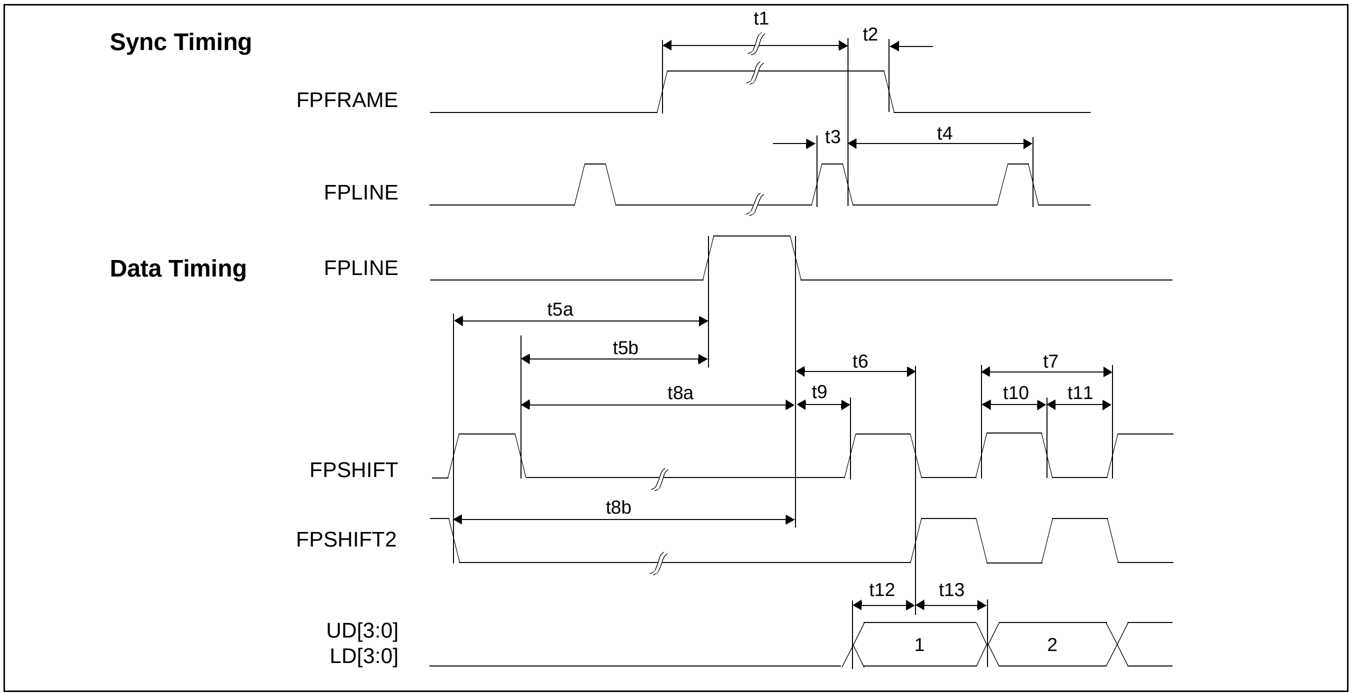


Figure 7-31: 8-Bit Single Color Passive LCD Panel A.C. Timing (Format 1)

Table 7-26: 8-Bit Single Color Passive LCD Panel A.C. Timing (Format 1)

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE pulse trailing edge	note 2			
t2	FPFRAME hold from FPLINE pulse trailing edge	14			Ts (note 1)
t3	FPLINE pulse width	9			Ts
t4	FPLINE period	note 3			
t5a	FPSHIFT2 falling edge to FPLINE pulse leading edge	note 4			
t5b	FPSHIFT falling edge to FPLINE pulse leading edge	note 5			
t6	FPLINE pulse trailing edge to FPSHIFT2 rising, FPSHIFT falling edge	t9 + t10			Ts
t7	FPSHIFT2, FPSHIFT period	4			Ts
t8a	FPSHIFT falling edge to FPLINE pulse trailing edge	note 6			
t8b	FPSHIFT2 falling edge to FPLINE pulse trailing edge	note 7			
t9	FPLINE pulse trailing edge to FPSHIFT rising edge	20			Ts
t10	FPSHIFT2, FPSHIFT pulse width high	2			Ts
t11	FPSHIFT2, FPSHIFT pulse width low	2			Ts
t12	UD[3:0], LD[3:0] setup to FPSHIFT2 rising, FPSHIFT falling edge	1			Ts
t13	UD[3:0], LD[3:0] hold from FPSHIFT2 rising, FPSHIFT falling edge	1			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t4_{min}$ - 14Ts
3. $t4_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] Ts
4. $t5_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 27] Ts
5. $t5_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 29] Ts
6. $t8_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 20] Ts
7. $t8_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 18] Ts

7.5.5 8-Bit Single Color Passive LCD Panel Timing (Format 2)

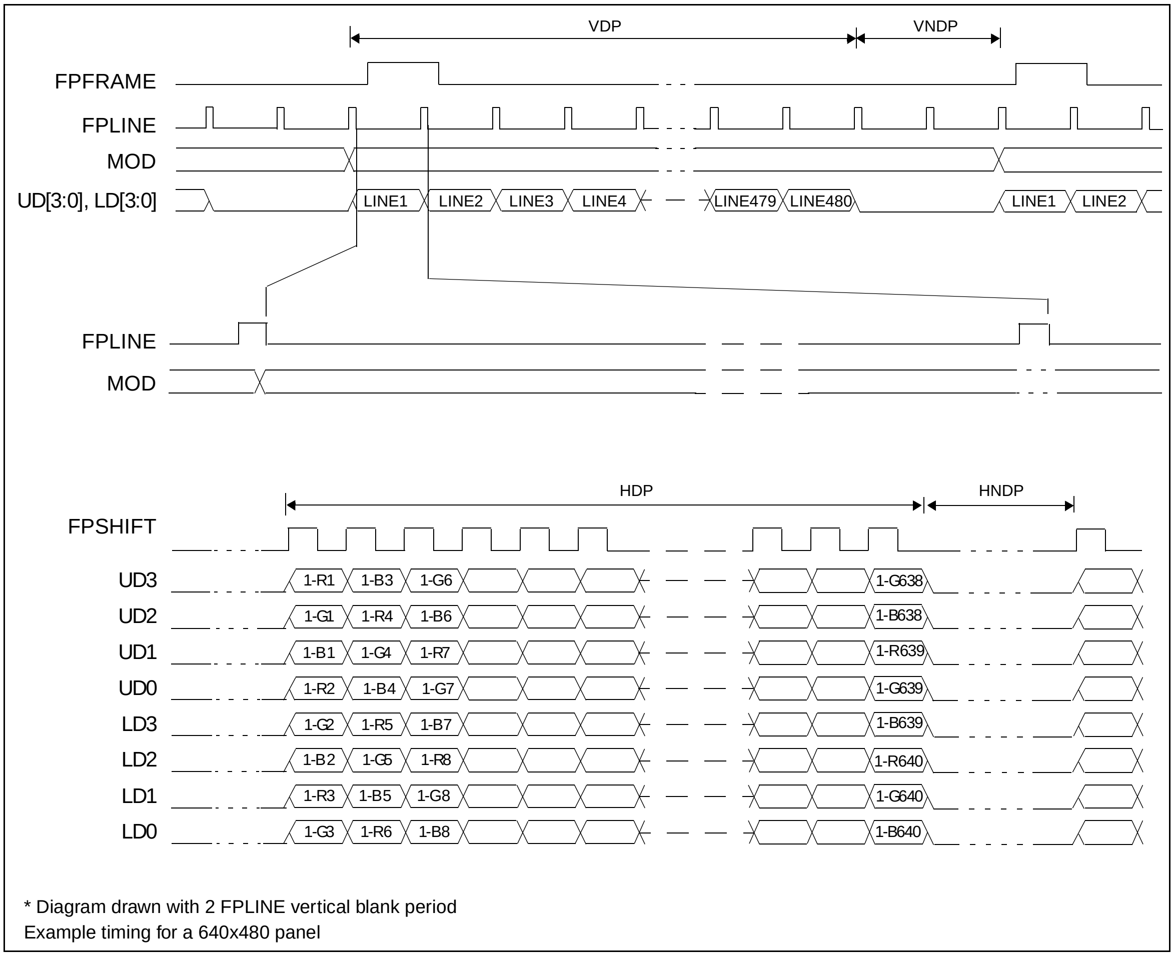


Figure 7-32: 8-Bit Single Color Passive LCD Panel Timing (Format 2)

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1)*8Ts

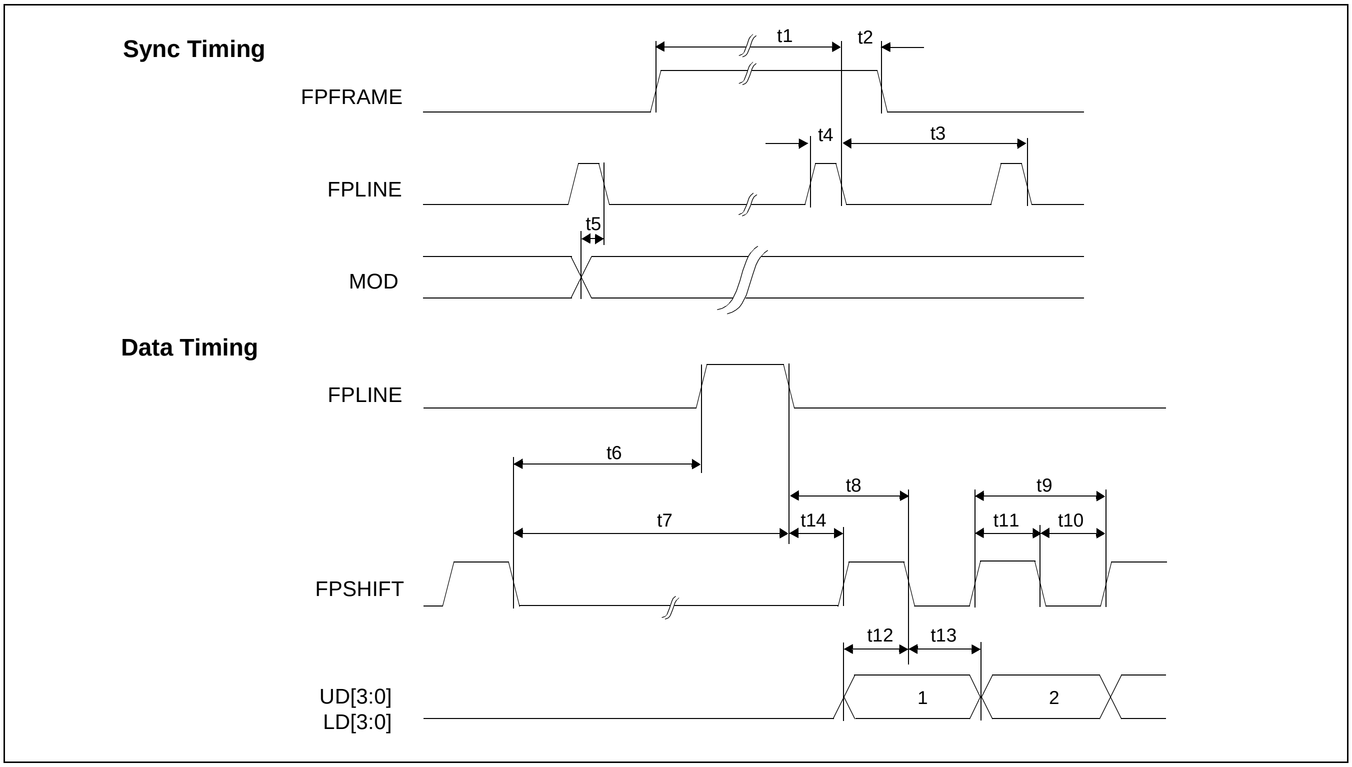


Figure 7-33: 8-Bit Single Color Passive LCD Panel A.C. Timing (Format 2)

Table 7-27: 8-Bit Single Color Passive LCD Panel A.C. Timing (Format 2)

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE pulse trailing edge	note 2			
t2	FPFRAME hold from FPLINE pulse trailing edge	14			Ts (note 1)
t3	FPLINE period	note 3			
t4	FPLINE pulse width	9			Ts
t5	MOD transition to FPLINE pulse trailing edge	1		note 4	Ts
t6	FPSHIFT falling edge to FPLINE pulse leading edge	note 5			
t7	FPSHIFT falling edge to FPLINE pulse trailing edge	note 6			
t8	FPLINE pulse trailing edge to FPSHIFT falling edge	t14 + 2			
t9	FPSHIFT period	2			Ts
t10	FPSHIFT pulse width low	1			Ts
t11	FPSHIFT pulse width high	1			Ts
t12	UD[3:0], LD[3:0] setup to FPSHIFT falling edge	1			Ts
t13	UD[3:0], LD[3:0] hold to FPSHIFT falling edge	1			Ts
t14	FPLINE pulse trailing edge to FPSHIFT rising edge	20			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t3_{min}$ - 14Ts
3. $t3_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] + 33 Ts
4. $t5_{min}$ = [(((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8)-1] Ts
5. $t6_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 28] Ts
6. $t7_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 19] Ts

7.5.6 16-Bit Single Color Passive LCD Panel Timing

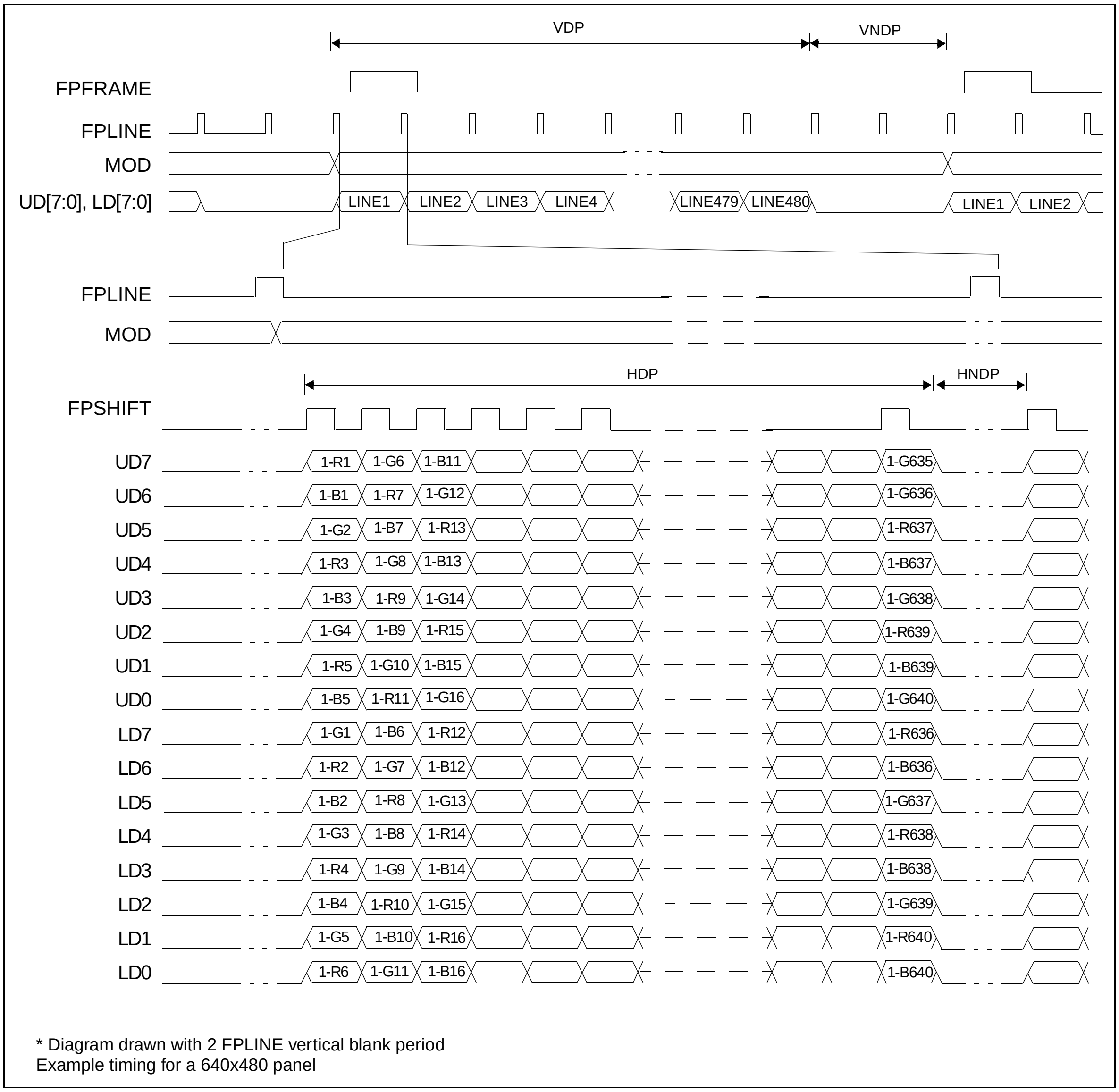


Figure 7-34: 16-Bit Single Color Passive LCD Panel Timing

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1)*8Ts

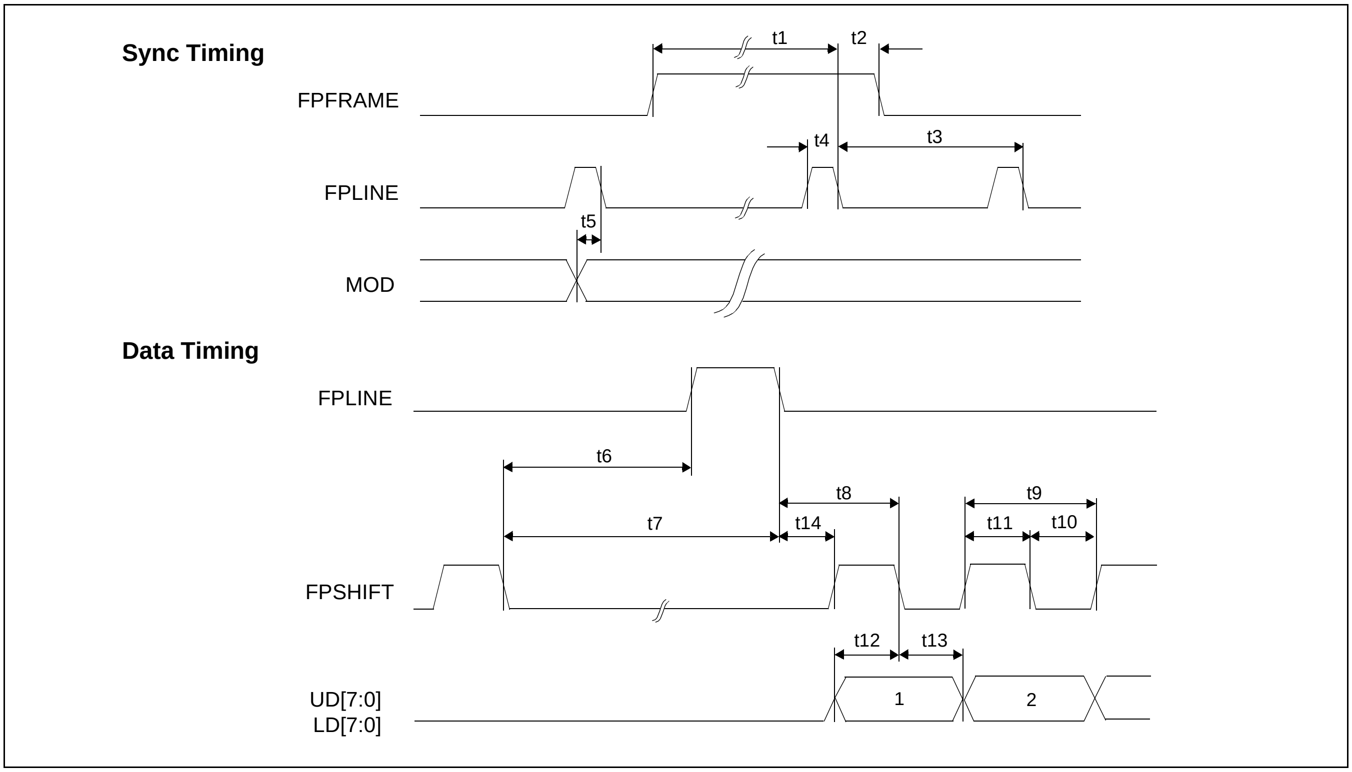


Figure 7-35: 16-Bit Single Color Passive LCD Panel A.C. Timing

Table 7-28: 16-Bit Single Color Passive LCD Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE pulse trailing edge	note 2			
t2	FPFRAME hold from FPLINE pulse trailing edge	14			Ts (note 1)
t3	FPLINE period	note 3			
t4	FPLINE pulse width	9			Ts
t5	MOD transition to FPLINE pulse trailing edge	1		note 4	Ts
t6	FPSHIFT falling edge to FPLINE pulse leading edge	note 5			
t7	FPSHIFT falling edge to FPLINE pulse trailing edge	note 6			
t8	FPLINE pulse trailing edge to FPSHIFT falling edge	t14 + 3			Ts
t9	FPSHIFT period	5			Ts
t10	FPSHIFT pulse width low	2			Ts
t11	FPSHIFT pulse width high	2			Ts
t12	UD[7:0], LD[7:0] setup to FPSHIFT falling edge	2			Ts
t13	UD[7:0], LD[7:0] hold to FPSHIFT falling edge	2			Ts
t14	FPLINE pulse trailing edge to FPSHIFT rising edge	20			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t3_{min}$ - 14Ts
3. $t3_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] + 33 Ts
4. $t5_{min}$ = [(((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8)-1] Ts
5. $t6_{min}$ = [(REG[05h] bits [4:0]) + 1)*8 - 27] Ts
6. $t7_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 18] Ts

7.5.7 8-Bit Dual Monochrome Passive LCD Panel Timing

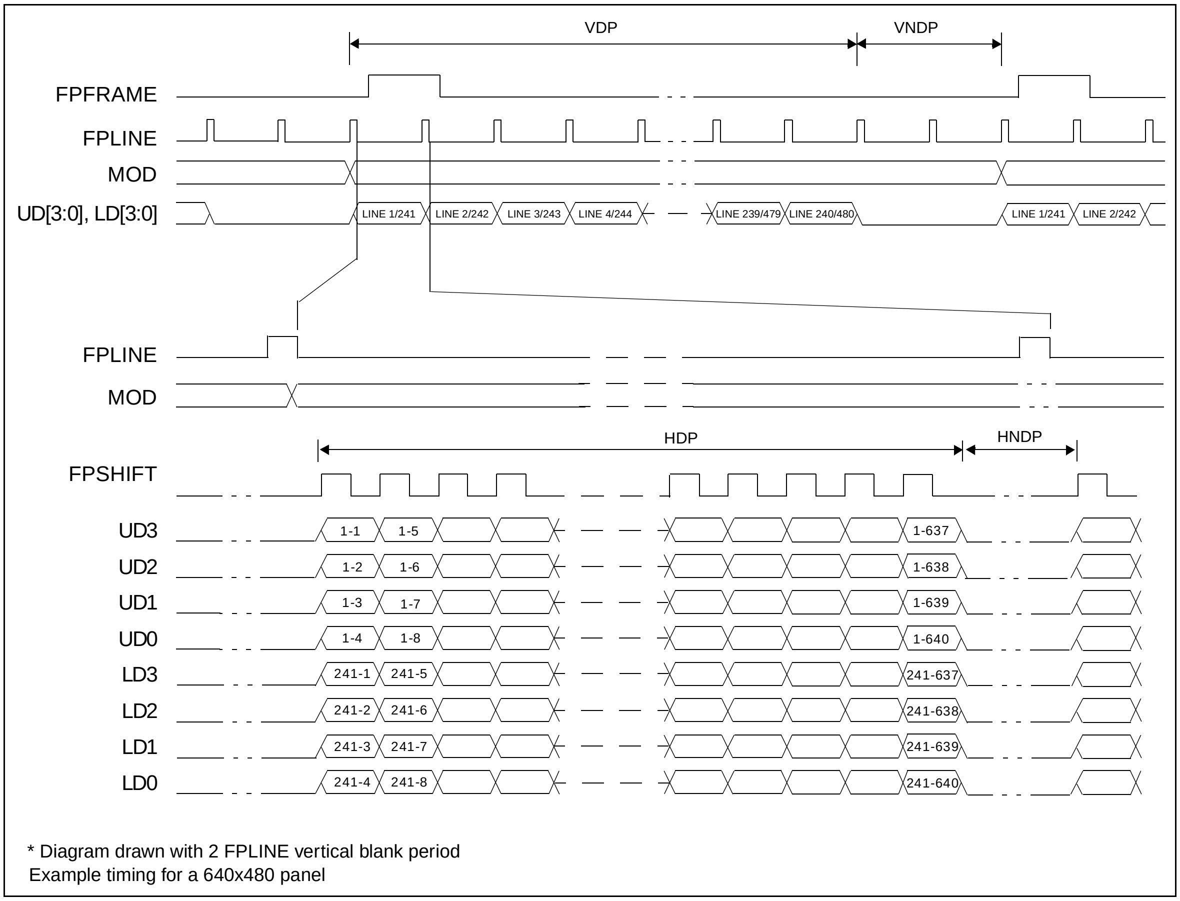


Figure 7-36: 8-Bit Dual Monochrome Passive LCD Panel Timing

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1)*8Ts

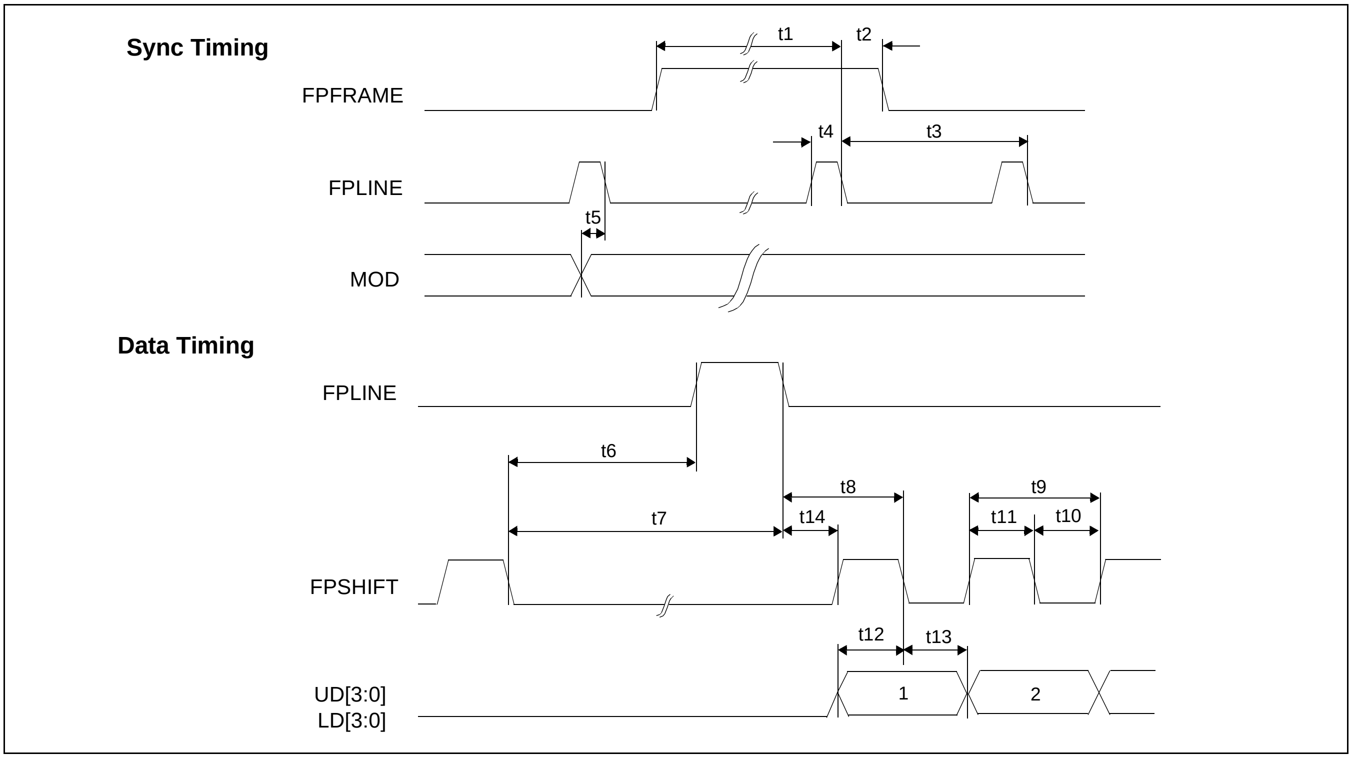


Figure 7-37: 8-Bit Dual Monochrome Passive LCD Panel A.C. Timing

Table 7-29: 8-Bit Dual Monochrome Passive LCD Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE pulse trailing edge	note 2			
t2	FPFRAME hold from FPLINE pulse trailing edge	14			Ts (note 1)
t3	FPLINE period	note 3			
t4	FPLINE pulse width	9			Ts
t5	MOD transition to FPLINE pulse trailing edge	1		note 4	Ts
t6	FPSHIFT falling edge to FPLINE pulse leading edge	note 5			
t7	FPSHIFT falling edge to FPLINE pulse trailing edge	note 6			
t8	FPLINE pulse trailing edge to FPSHIFT falling edge	t14 + 2			Ts
t9	FPSHIFT period	4			Ts
t10	FPSHIFT pulse width low	2			Ts
t11	FPSHIFT pulse width high	2			Ts
t12	UD[3:0], LD[3:0] setup to FPSHIFT falling edge	2			Ts
t13	UD[3:0], LD[3:0] hold to FPSHIFT falling edge	2			Ts
t14	FPLINE pulse trailing edge to FPSHIFT rising edge	12			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t3_{min}$ - 14Ts
3. $t3_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] + 33 Ts
4. $t5_{min}$ = [(((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8)-1] Ts
5. $t6_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 19] Ts
6. $t7_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 10] Ts

7.5.8 8-Bit Dual Color Passive LCD Panel Timing

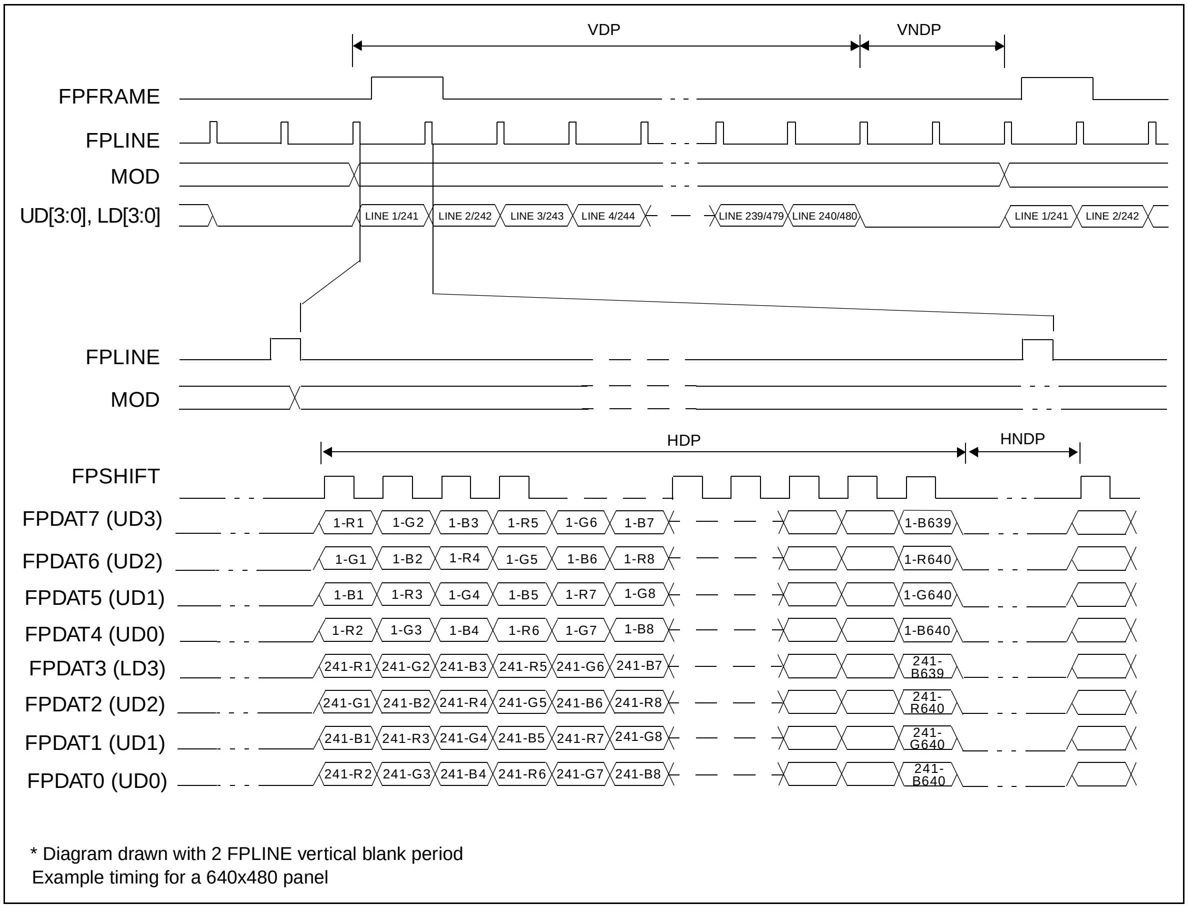


Figure 7-38: 8-Bit Dual Color Passive LCD Panel Timing

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1)*8Ts

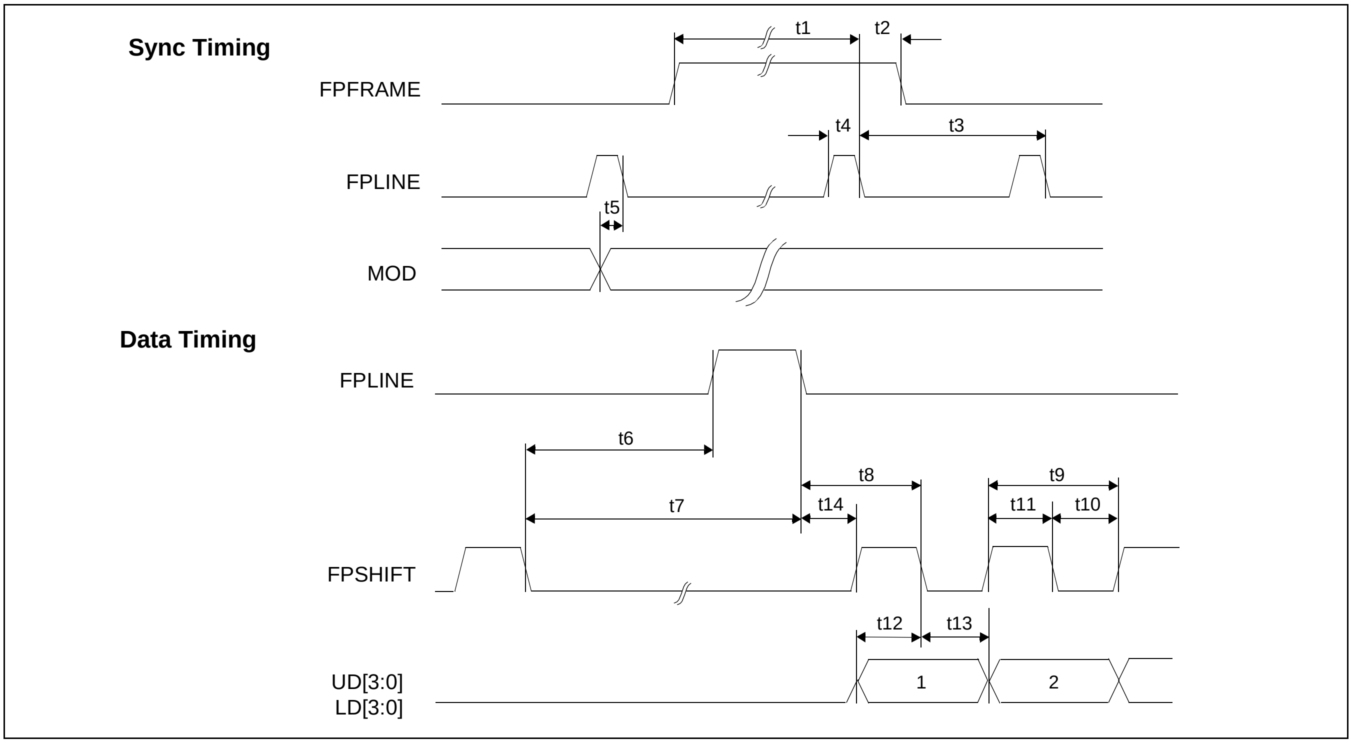


Figure 7-39: 8-Bit Dual Color Passive LCD Panel A.C. Timing

Table 7-30: 8-Bit Dual Color Passive LCD Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE pulse trailing edge	note 2			
t2	FPFRAME hold from FPLINE pulse trailing edge	14			Ts (note 1)
t3	FPLINE period	note 3			
t4	FPLINE pulse width	9			Ts
t5	MOD transition to FPLINE pulse trailing edge	1		note 4	Ts
t6	FPSHIFT falling edge to FPLINE pulse leading edge	note 5			
t7	FPSHIFT falling edge to FPLINE pulse trailing edge	note 6			
t8	FPLINE pulse trailing edge to FPSHIFT falling edge	t14 + t11			Ts
t9	FPSHIFT period	1			Ts
t10	FPSHIFT pulse width low	0.45			Ts
t11	FPSHIFT pulse width high	0.45			Ts
t12	UD[3:0], LD[3:0] setup to FPSHIFT falling edge	0.45			Ts
t13	UD[3:0], LD[3:0] hold to FPSHIFT falling edge	0.45			Ts
t14	FPLINE pulse trailing edge to FPSHIFT rising edge	13			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t3_{min}$ - 14Ts
3. $t3_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] + 33 Ts
4. $t5_{min}$ = [(((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8)-1] Ts
5. $t6_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 20] Ts
6. $t7_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 11] Ts

7.5.9 16-Bit Dual Color Passive LCD Panel Timing

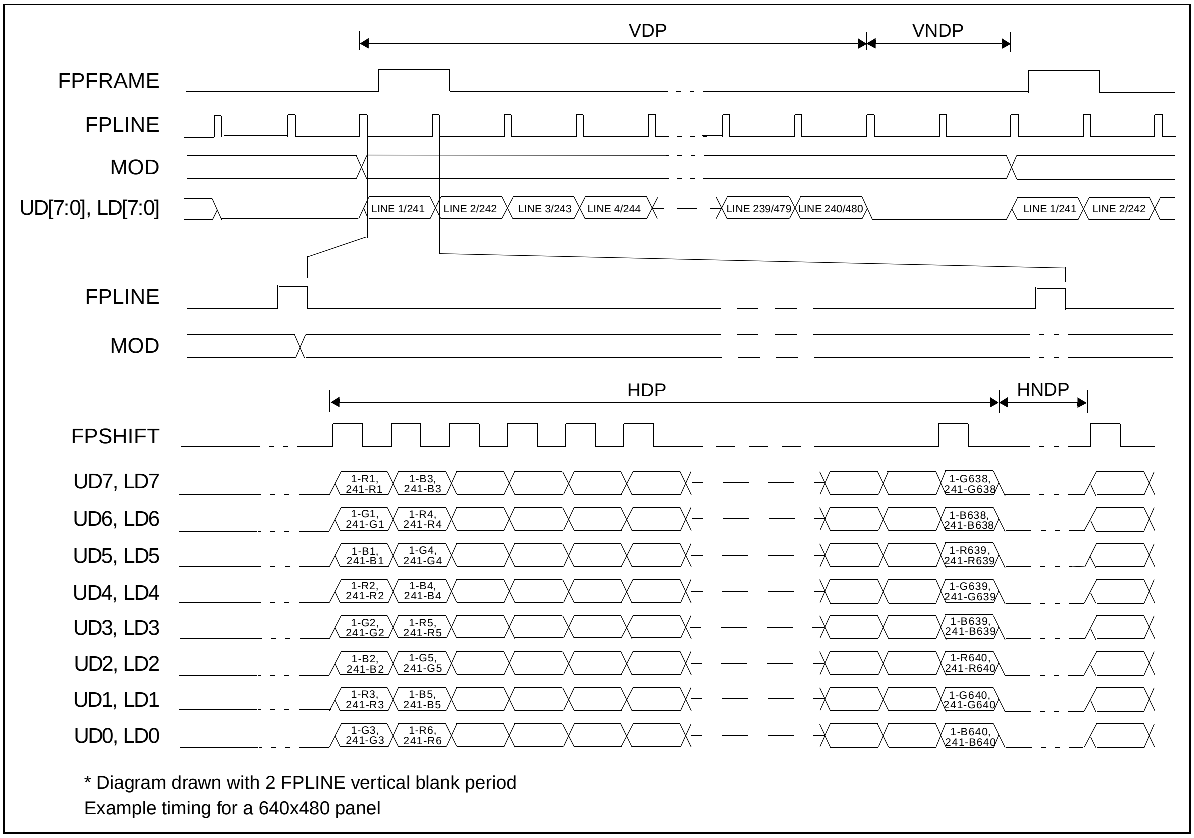


Figure 7-40: 16-Bit Dual Color Passive LCD Panel Timing

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1)*8Ts

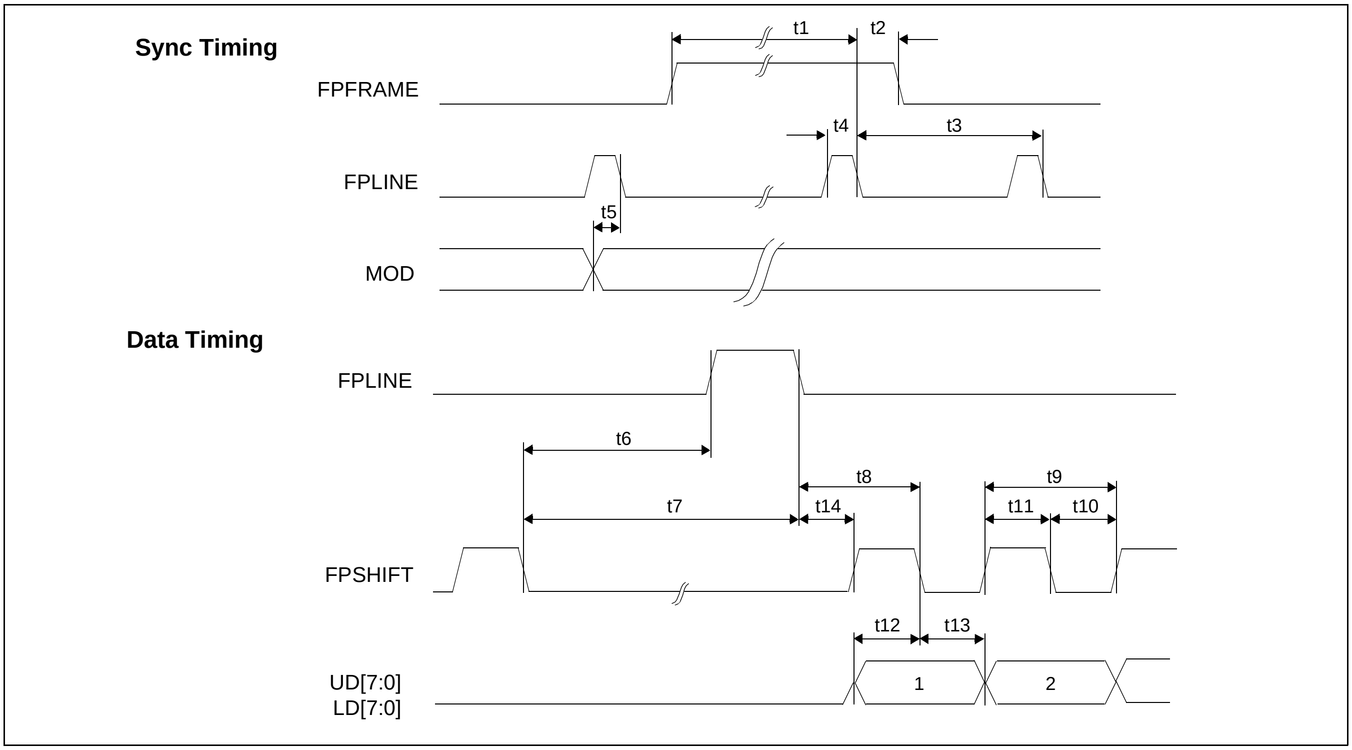


Figure 7-41: 16-Bit Dual Color Passive LCD Panel A.C. Timing

Table 7-31: 16-Bit Dual Color Passive LCD Panel A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME setup to FPLINE pulse trailing edge	note 2			
t2	FPFRAME hold from FPLINE pulse trailing edge	14			Ts (note 1)
t3	FPLINE period	note 3			
t4	FPLINE pulse width	9			Ts
t5	MOD transition to FPLINE pulse trailing edge	1		note 4	Ts
t6	FPSHIFT falling edge to FPLINE pulse leading edge	note 5			
t7	FPSHIFT falling edge to FPLINE pulse trailing edge	note 6			
t8	FPLINE pulse trailing edge to FPSHIFT falling edge	t14 + 2			
t9	FPSHIFT period	2			Ts
t10	FPSHIFT pulse width low	1			Ts
t11	FPSHIFT pulse width high	1			Ts
t12	UD[7:0], LD[7:0] setup to FPSHIFT falling edge	1			Ts
t13	UD[7:0], LD[7:0] hold to FPSHIFT falling edge	1			Ts
t14	FPLINE pulse trailing edge to FPSHIFT rising edge	12			Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t1_{min}$ = $t3_{min}$ - 14Ts
3. $t3_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8] + 33 Ts
4. $t5_{min}$ = [(((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0]) + 1)*8)-1] Ts
5. $t6_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 20] Ts
6. $t7_{min}$ = [((REG[05h] bits [4:0]) + 1)*8 - 11] Ts

7.5.10 16-Bit TFT/D-TFD Panel Timing

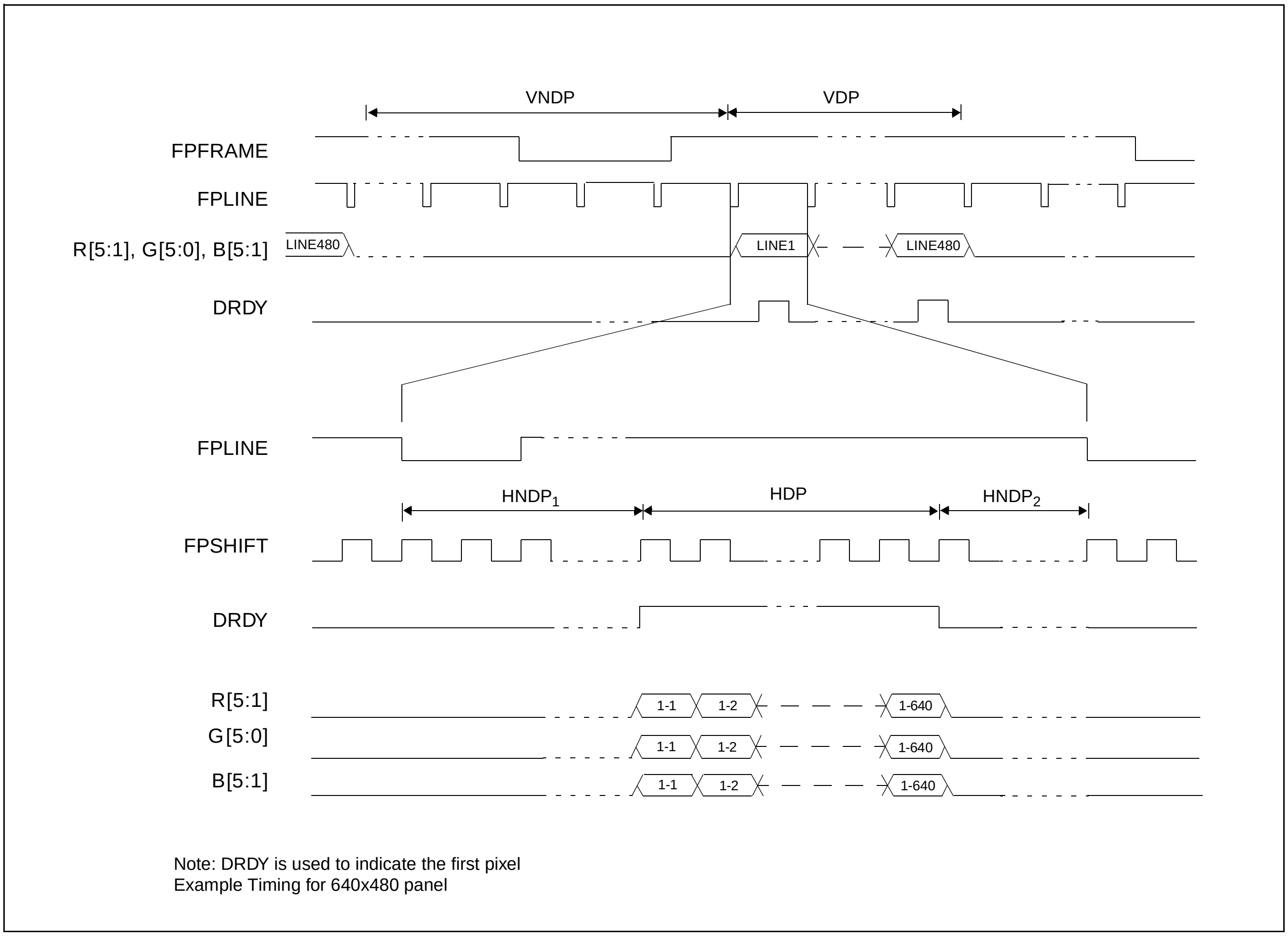


Figure 7-42: 16-Bit TFT/D-TFD Panel Timing

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= $HNDP_1$ + $HNDP_2$ = ((REG[05h] bits [4:0]) + 1)*8Ts

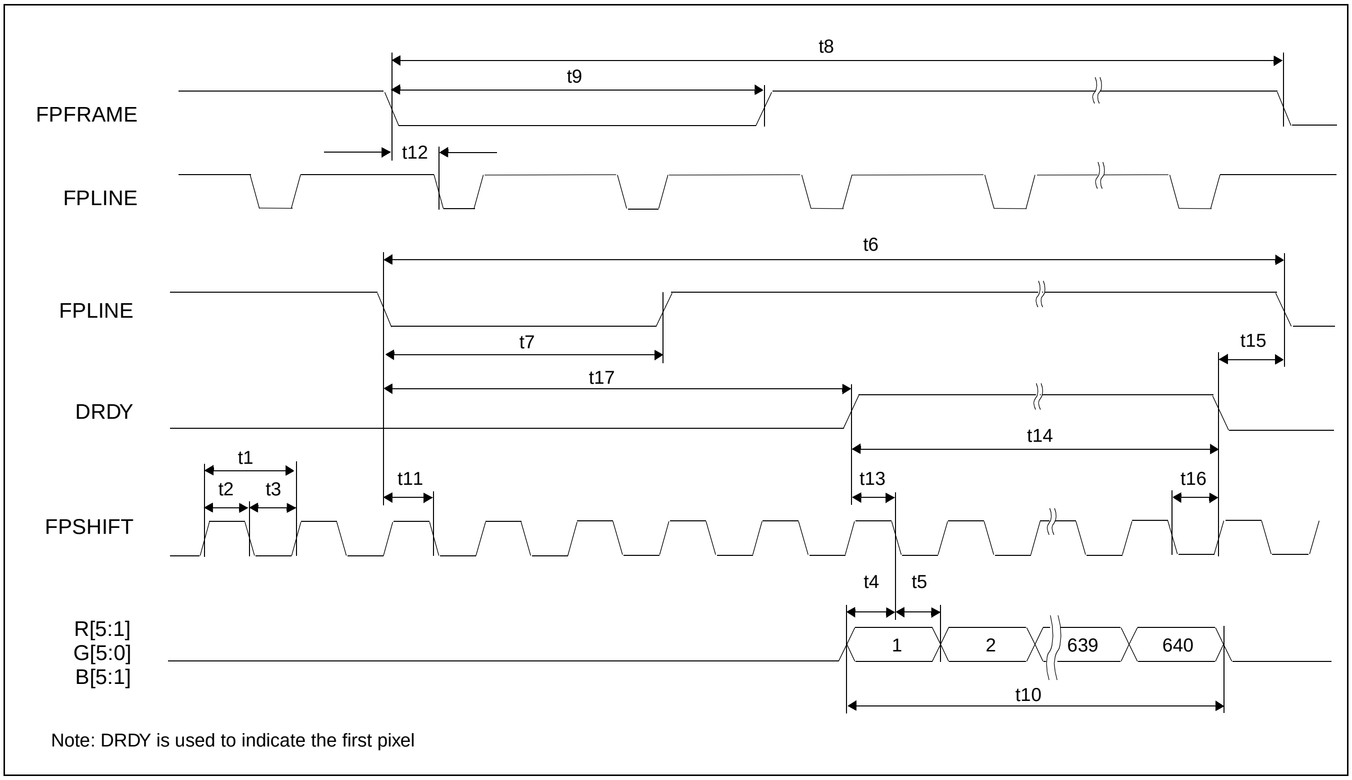


Figure 7-43: TFT/D-TFD A.C. Timing

Table 7-32: TFT/D-TFD A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPSHIFT period	1			Ts (note 1)
t2	FPSHIFT pulse width high	0.45			Ts
t3	FPSHIFT pulse width low	0.45			Ts
t4	data setup to FPSHIFT falling edge	0.45			Ts
t5	data hold from FPSHIFT falling edge	0.45			Ts
t6	FPLINE cycle time	note 2			
t7	FPLINE pulse width low	note 3			
t8	FPFRAME cycle time	note 4			
t9	FPFRAME pulse width low	note 5			
t10	horizontal display period	note 6			
t11	FPLINE setup to FPSHIFT falling edge	0.45			Ts
t12	FPFRAME pulse leading edge to FPLINE pulse leading edge phase difference	note 7			
t13	DRDY to FPSHIFT falling edge setup time	0.45			Ts
t14	DRDY pulse width	note 8			
t15	DRDY falling edge to FPLINE pulse leading edge	note 9			
t16	DRDY hold from FPSHIFT falling edge	0.45			Ts
t17	FPLINE pulse leading edge to DRDY active	note 10		250	Ts

1. Ts = pixel clock period = memory clock, [memory clock]/2, [memory clock]/3, [memory clock]/4 (see REG[19h] bits [1:0])
2. $t6_{min}$ = [((REG[04h] bits [6:0])+1)*8 + ((REG[05h] bits [4:0])+1)*8] Ts
3. $t7_{min}$ = [((REG[07h] bits [3:0])+1)*8] Ts
4. $t8_{min}$ = [((REG[09h] bits [1:0], REG[08h] bits [7:0])+1) + ((REG[0Ah] bits [5:0])+1)] lines
5. $t9_{min}$ = [((REG[0Ch] bits [2:0])+1)] lines
6. $t10_{min}$ = [((REG[04h] bits [6:0])+1)*8] Ts
7. $t12_{min}$ = [((REG[06h] bits [4:0])*8)+1] Ts
8. $t14_{min}$ = [((REG[04h] bits [6:0])+1)*8] Ts
9. $t15_{min}$ = [((REG[06h] bits [4:0])+1)*8 - 2] Ts
10. $t17_{min}$ = [((REG[05h] bits [4:0])+1)*8 - ((REG[06h] bits [4:0])+1)*8 + 2]

7.5.11 CRT Timing

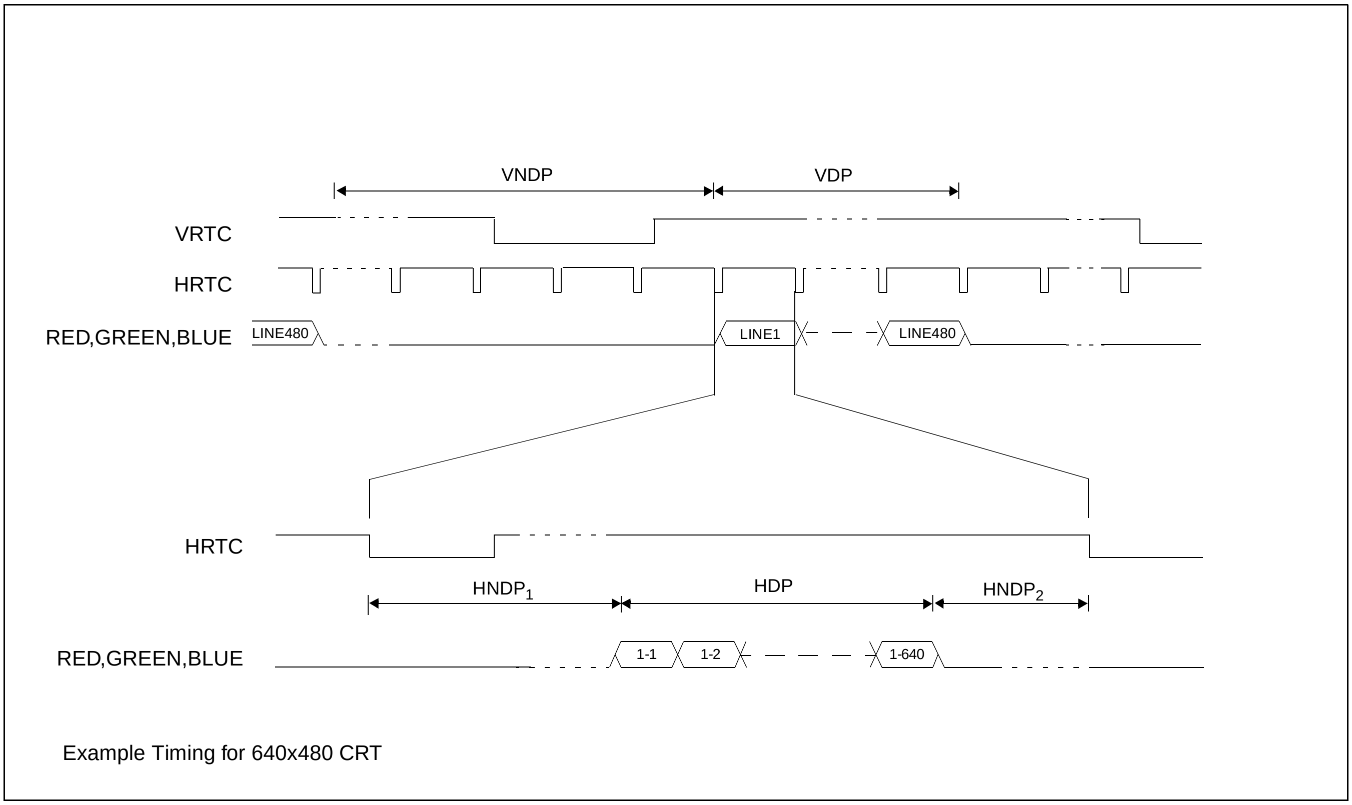


Figure 7-44: CRT Timing

VDP	= Vertical Display Period	= (REG[09h] bits [1:0], REG[08h] bits [7:0]) + 1
VNDP	= Vertical Non-Display Period	= (REG[0Ah] bits [5:0]) + 1
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1)*8Ts
HNDP	= Horizontal Non-Display Period	= $HNDP_1 + HNDP_2$ = ((REG[05h] bits [4:0]) + 1)*8Ts

Note

The signals RED, GREEN and BLUE are analog signals from the embedded DAC and represent the color components which make up each pixel.

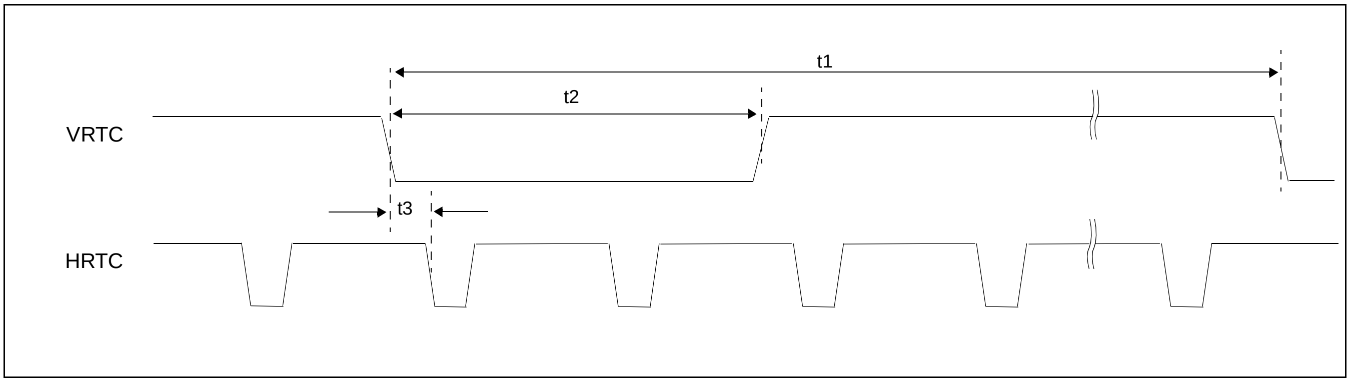


Figure 7-45: CRT A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	VRTC cycle time		note 1		
t2	VRTC pulse width low		note 2		
t3	VRTC falling edge to FPLINE falling edge phase difference		note 3		

1. $t8_{min}$ = [((REG[09h] bits 1:0, REG[08h] bits 7:0)+1) + ((REG[0Ah] bits 6:0)+1)] lines
2. $t9_{min}$ = [((REG[0Ch] bits 2:0)+1)] lines
3. $t12_{min}$ = [((REG[06h] bits 4:0)+1)*8] Ts

8 Registers

8.1 Register Mapping

The S1D13505 registers are memory mapped. The system addresses the registers through the CS#, M/R#, and AB[5:0] input pins. When CS# = 0 and M/R# = 0, the registers are mapped by address bits AB[5:0], e.g. REG[00h] is mapped to AB[5:0] = 000000, REG[01h] is mapped to AB[5:0] = 000001. See the table below:

Table 8-1: S1D13505 Addressing

CS#	M/R#	Access
0	0	Register access: • REG[00h] is addressed when AB[5:0] = 0 • REG[01h] is addressed when AB[5:0] = 1 • REG[n] is addressed when AB[5:0] = n
0	1	Memory access: the 2M byte Display Buffer is addressed by AB[20:0]
1	X	S1D13505 not selected

8.2 Register Descriptions

Unless specified otherwise, all register bits are reset to 0 during power-on. Reserved bits should be written 0 when programming unless otherwise noted.

8.2.1 Revision Code Register

Revision Code Register REG[00h]							RO
Product Code Bit 5	Product Code Bit 4	Product Code Bit 3	Product Code Bit 2	Product Code Bit 1	Product Code Bit 0	Revision Code Bit 1	Revision Code Bit 0

bits 7-2 Product Code Bits [5:0]
This is a read-only register that indicates the product code of the chip. The product code for the S1D13505 is 000011.

bits 1-0 Revision Code Bits [1:0]
This is a read-only register that indicates the revision code of the chip. The revision code for the S1D13505F00A is 00.

8.2.2 Memory Configuration Registers

Memory Configuration Register REG[01h]							RW
n/a	Refresh Rate Bit 2	Refresh Rate Bit 1	Refresh Rate Bit 0	n/a	WE# Control	n/a	Memory Type

bits 6-4 DRAM Refresh Rate Select Bits [2:0]
These bits specify the divisor used to generate the DRAM refresh rate from the input clock (CLKI).

Table 8-2: DRAM Refresh Rate Selection

DRAM Refresh Rate Select Bits [2:0]	CLKI Frequency Divisor	Example Refresh Rate for CLKI = 33MHz	Example period for 256 refresh cycles at CLKI = 33MHz
000	64	520 kHz	0.5 ms
001	128	260 kHz	1 ms
010	256	130 kHz	2 ms
011	512	65 kHz	4 ms
100	1024	33 kHz	8 ms
101	2048	16 kHz	16 ms
110	4096	8 kHz	32 ms
111	8192	4 kHz	64 ms

bit 2 WE# Control
When this bit = 1, 2-WE# DRAM is selected.
When this bit = 0, 2-CAS# DRAM is selected.

bit 0 Memory Type
When this bit = 1, FPM-DRAM is selected.
When this bit = 0, EDO-DRAM is selected.
This bit should be changed only when there are no read/write DRAM cycles. This condition occurs when all of the following are true: the Display FIFO is disabled (REG[23h] bit 7 = 1), and the Half Frame Buffer is disabled (REG[1Bh] bit 0 = 1), and the Ink/Cursor is inactive (Reg[27h] bits 7-6 = 00). This condition also occurs when the CRT and LCD enable bits (Reg[0Dh] bits 1-0) have remained 0 since chip reset. For further programming information, see *S1D13505 Programming Notes and Examples*, document number X23A-G-003-xx.

8.2.3 Panel/Monitor Configuration Registers

Panel Type Register REG[02h]							RW
EL Panel Enable	n/a	Panel Data Width Bit 1	Panel Data Width Bit 0	Panel Data Format Select	Color/Mono. Panel Select	Dual/Single Panel Select	TFT/ Passive LCD Panel Select

bit 7 — EL Panel Mode Enable
When this bit = 1, EL Panel support mode is enabled. Every 262143 frames (approximately 1 hour at 60Hz frame rate) the identical panel data is sent to two consecutive frames, i.e. the frame rate modulation circuitry is frozen for one frame.

bits 5-4 — Panel Data Width Bits [1:0]
These bits select the LCD interface data width as shown in the following table.

Table 8-3: Panel Data Width Selection

Panel Data Width Bits [1:0]	Passive LCD Panel Data Width Size	TFT/D-TFD Panel Data Width Size
00	4-bit	9-bit
01	8-bit	12-bit
10	16-bit	16-bit
11	Reserved	Reserved

bit 3 — Panel Data Format Select
When this bit = 1, color passive LCD panel data format 2 is selected.
When this bit = 0, passive LCD panel data format 1 is selected.

bit 2 — Color/Mono Panel Select
When this bit = 1, color passive LCD panel is selected.
When this bit = 0, monochrome passive LCD panel is selected.

bit 1 — Dual/Single Panel Select
When this bit = 1, dual passive LCD panel is selected.
When this bit = 0, single passive LCD panel is selected.

bit 0 — TFT/Passive LCD Panel Select
When this bit = 1, TFT/D-TFD panel is selected.
When this bit = 0, passive LCD panel is selected.

MOD Rate Register REG[03h]							RW
n/a	n/a	MOD Rate Bit 5	MOD Rate Bit 4	MOD Rate Bit 3	MOD Rate Bit 2	MOD Rate Bit 1	MOD Rate Bit 0

bits 5-0 — MOD Rate Bits [5:0]
When the DRDY pin is configured as MOD, this register controls the toggle rate of the MOD output. When this register is zero, the MOD output signal toggles every FPFRAME. When this register is non-zero, its value represents the number of FPLINE pulses between toggles of the MOD output signal.

Horizontal Display Width Register REG[04h]							RW
n/a	Horizontal Display Width Bit 6	Horizontal Display Width Bit 5	Horizontal Display Width Bit 4	Horizontal Display Width Bit 3	Horizontal Display Width Bit 2	Horizontal Display Width Bit 1	Horizontal Display Width Bit 0

bits 6-0 Horizontal Display Width Bits [6:0]
These bits specify the LCD panel and/or the CRT horizontal display width as follows.

Contents of this Register = (Horizontal Display Width ÷ 8) - 1

For passive LCD panels the Horizontal Display Width must be divisible by 16, and for TFT LCD panels/CRTs the Horizontal Display Width must be divisible by 8. The maximum horizontal display width is 1024 pixels.

Note
This register must be programmed such that REG[04h] ≥ 3 (32 pixels)

Note
When setting a horizontal resolution greater than 767 pixels, with a color depth of 15/16 bpp, the Memory Offset Registers (REG[16h], REG[17h]) must be set to a virtual horizontal pixel resolution of 1024.

Horizontal Non-Display Period Register REG[05h]							RW
n/a	n/a	n/a	Horizontal Non-Display Period Bit 4	Horizontal Non-Display Period Bit 3	Horizontal Non-Display Period Bit 2	Horizontal Non-Display Period Bit 1	Horizontal Non-Display Period Bit 0

bits 4-0 Horizontal Non-Display Period Bits [4:0]
These bits specify the horizontal non-display period.

Horizontal non-display period (pixels) = (Horizontal Non-Display Period Bits [4:0] + 1) × 8

The recommended minimum value which should be programmed into this register is 3 (32 pixels). The maximum value which can be programmed into this register is 1Fh, which gives a horizontal non-display period of 256 pixels.

Note
This register must be programmed such that
REG[05h] ≥ 3 and (REG[05h] + 1) ≥ (REG[06h] + 1) + (REG[07h] bits [3:0] +1)

HRTC/FPLINE Start Position Register REG[06h]							RW
n/a	n/a	n/a	HRTC/ FPLINE Start Position Bit 4	HRTC/ FPLINE Start Position Bit 3	HRTC/ FPLINE Start Position Bit 2	HRTC/ FPLINE Start Position Bit 1	HRTC/ FPLINE Start Position Bit 0

bits 4-0 HRTC/FPLINE Start Position Bits [4:0]
For CRT and TFT/D-TFD, these bits specify the delay from the start of the horizontal non-display period to the leading edge of the HRTC pulse and FPLINE pulse respectively.

HRTC/FPLINE start position (pixels) = (HRTC/FPLINE Start Position Bits [4:0] + 1) × 8 - 2

Note
This register must be programmed such that
(REG[05h] + 1) ≥ (REG[06h] + 1) + (REG[07h] bits [3:0] +1)

HRTC/FPLINE Pulse Width Register REG[07h]							RW
HRTC Polarity Select	FPLINE Polarity Select	n/a	n/a	HRTC/ FPLINE Pulse Width Bit 3	HRTC/ FPLINE Pulse Width Bit 2	HRTC/ FPLINE Pulse Width Bit 1	HRTC/ FPLINE Pulse Width Bit 0

bit 7 HRTC Polarity Select
This bit selects the polarity of the HRTC pulse to the CRT.
When this bit = 1, the HRTC pulse is active high.
When this bit = 0, the HRTC pulse is active low.

bit 6 FPLINE Polarity Select
This bit selects the polarity of the FPLINE pulse to TFT/D-TFD or passive LCD.
When this bit = 1, the FPLINE pulse is active high for TFT/D-TFD and active low for passive LCD.
When this bit = 0, the FPLINE pulse is active low for TFT/D-TFD and active high for passive LCD.

Table 8-4: FPLINE Polarity Selection

FPLINE Polarity Select	Passive LCD FPLINE Polarity	TFT/D-TFD FPLINE Polarity
0	active high	active low
1	active low	active high

bits 3-0 HRTC/FPLINE Pulse Width Bits [3:0]
For CRT and TFT/D-TFD, these bits specify the pulse width of HRTC and FPLINE respectively.
For passive LCD, FPLINE is automatically created and these bits have no effect.

HRTC/FPLINE pulse width (pixels) = (HRTC/FPLINE Pulse Width Bits [3:0] + 1) × 8

The maximum HRTC pulse width is 128 pixels.

Note
This register must be programmed such that
(REG[05h] + 1) ≥ (REG[06h] + 1) + (REG[07h] bits [3:0] +1)

Vertical Display Height Register 0 REG[08h]							RW
Vertical Display Height Bit 7	Vertical Display Height Bit 6	Vertical Display Height Bit 5	Vertical Display Height Bit 4	Vertical Display Height Bit 3	Vertical Display Height Bit 2	Vertical Display Height Bit 1	Vertical Display Height Bit 0

Vertical Display Height Register 1 REG[09h]							RW
n/a	n/a	n/a	n/a	n/a	n/a	Vertical Display Height Bit 9	Vertical Display Height Bit 8

REG[08h] bits 7-0
REG[09h] bits 1-0

Vertical Display Height Bits [9:0]
These bits specify the vertical display height.

Vertical display height (lines) = Vertical Display Height Bits [9:0] + 1

- For CRT, TFT/D-TFD, and single passive LCD panel this register is programmed to: *(vertical resolution of the display) - 1*, e.g. EFh for a 240-line display.
- For dual-panel passive LCD not in simultaneous display mode, this register is programmed to: *((vertical resolution of the display)/2) - 1*, e.g. EFh for a 480-line display.
- For all simultaneous display modes, this register is programmed to: *(vertical resolution of the CRT) - 1*, e.g. 1DFh for a 480-line CRT.

Vertical Non-Display Period Register REG[0Ah]							RW
Vertical Non-Display Period Status (RO)	n/a	Vertical Non-Display Period Bit 5	Vertical Non-Display Period Bit 4	Vertical Non-Display Period Bit 3	Vertical Non-Display Period Bit 2	Vertical Non-Display Period Bit 1	Vertical Non-Display Period Bit 0

bit 7

Vertical Non-Display Period Status
This is a read-only status bit.
When this bit = 1, a vertical non-display period is indicated.
When this bit = 0, a vertical display period is indicated.

bits 5-0

Vertical Non-Display Period Bits [5:0]
These bits specify the vertical non-display period.

Vertical non-display period (lines) = Vertical Non-Display Period Bits [5:0] + 1

Note

This register must be programmed such that
REG[0Ah] ≥ 1 and (REG[0Ah] bits [5:0] + 1) ≥ (REG[0Bh] + 1) + (REG[0Ch] bits [2:0] + 1)

VRTC/FPFRAME Start Position Register REG[0Bh]							RW
n/a	n/a	VRTC/ FPFRAME Start Position Bit 5	VRTC/ FPFRAME Start Position Bit 4	VRTC/ FPFRAME Start Position Bit 3	VRTC/ FPFRAME Start Position Bit 2	VRTC/ FPFRAME Start Position Bit 1	VRTC/ FPFRAME Start Position Bit 0

bits 5-0 VRTC/FPFRAME Start Position Bits [5:0]
For CRT and TFT/D-TFD, these bits specify the delay in lines from the start of the vertical non-display period to the leading edge of the VRTC pulse and FPFRAME pulse respectively. For passive LCD, FPFRAME is automatically created and these bits have no effect.

VRTC/FPFRAME start position (lines) = VRTC/FPFRAME Start Position Bits [5:0] + 1

The maximum start delay is 64 lines.

Note
This register must be programmed such that
(REG[0Ah] bits [5:0] + 1) ≥ (REG[0Bh] + 1) + (REG[0Ch] bits [2:0] + 1)
For exact timing please use the timing diagrams in section 7.5

VRTC/FPFRAME Pulse Width Register REG[0Ch]							RW
VRTC Polarity Select	FPFRAME Polarity Select	n/a	n/a	n/a	VRTC/ FPFRAME Pulse Width Bit 2	VRTC/ FPFRAME Pulse Width Bit 1	VRTC/ FPFRAME Pulse Width Bit 0

bit 7 VRTC Polarity Select
This bit selects the polarity of the VRTC pulse to the CRT.
When this bit = 1, the VRTC pulse is active high.
When this bit = 0, the VRTC pulse is active low.

bit 6 FPFRAME Polarity Select
This bit selects the polarity of the FPFRAME pulse to the TFT/D-TFD or passive LCD.
When this bit = 1, the FPFRAME pulse is active high for TFT/D-TFD and active low for passive.
When this bit = 0, the FPFRAME pulse is active low for TFT/D-TFD and active high for passive.

Table 8-5: FPFRAME Polarity Selection

FPFRAME Polarity Select	Passive LCD FPFRAME Polarity	TFT/D-TFD FPFRAME Polarity
0	active high	active low
1	active low	active high

bits 2-0 VRTC/FPFRAME Pulse Width Bits [2:0]
For CRT and TFT/D-TFD, these bits specify the pulse width of VRTC and FPFRAME respectively. For passive LCD, FPFRAME is automatically created and these bits have no effect.

VRTC/FPFRAME pulse width (lines) = VRTC/FPFRAME Pulse Width Bits [2:0] + 1

Note
This register must be programmed such that
(REG[0Ah] bits [5:0] + 1) ≥ (REG[0Bh] + 1) + (REG[0Ch] bits [2:0] + 1)

8.2.4 Display Configuration Registers

Display Mode Register REG[0Dh]							RW
SwivelView Enable	Simultaneous Display Option Select Bit 1	Simultaneous Display Option Select Bit 0	Bit-per-pixel Select Bit 2	Bit-per-pixel Select Bit 1	Bit-per-pixel Select Bit 0	CRT Enable	LCD Enable

bit 7 SwivelView Enable
When this bit = 1, all CPU accesses to the display buffer are translated to provide clockwise 90° hardware rotation of the display image. Refer to *“Section 13 SwivelView”* for application and limitations.

bits 6-5 Simultaneous Display Option Select Bits [1:0]
These bits are used to select one of four different simultaneous display mode options: Normal, Line Doubling, Interlace, or Even Scan Only. The purpose of these modes is to manipulate the vertical resolution of the image so that it fits on both the CRT, typically 640x480, and LCD. The following table describes the four modes using a 640x480 CRT as an example:

Table 8-6: Simultaneous Display Option Selection

Simultaneous Display Option Select Bits [1:0]	Simultaneous Display Mode	Mode Description
00	Normal	The image is not manipulated. This mode is used when the CRT and LCD have the same resolution, e.g. 480 lines. It is necessary to suit the vertical retrace period to the CRT. This results in a lower LCD duty cycle (1/525 compared to the usual 1/481). This reduced duty cycle may result in lower contrast on the LCD.
01	Line Doubling	Each line is replicated on the CRT. This mode is used to display a 240-line image on a 240-line LCD and stretch it to a 480-line image on the CRT. The CRT has a heightened aspect ratio. It is necessary to suit the vertical retrace period to the CRT. This results in a lower LCD duty cycle (2/525 compared to the usual 1/241). This reduced duty cycle is not extreme and the contrast of the LCD image should not be greatly reduced.
10	Interlace	The odd and even fields of a 480-line image are interlaced on the LCD. This mode is used to display a 480-line image on the CRT and squash it onto a 240-line LCD. The full image is viewed on the LCD but the interlacing may create flicker. The LCD has a shortened aspect ratio. It is necessary to suit the vertical retrace period to the CRT. This results in a lower LCD duty cycle (2/525 compared to the usual 1/241). This reduced duty cycle is not extreme and the contrast of the LCD image should not be greatly reduced.
11	Even Scan Only	Only the even field of a 480-line image is displayed on the LCD. This is an alternate method to display a 480-line image on the CRT and squash it onto a 240-line LCD. Only the even scans are viewed on the LCD. The LCD has a shortened aspect ratio. It is necessary to suit the vertical retrace period to the CRT. This results in a lower LCD duty cycle (2/525 compared to the usual 1/241). This reduced duty cycle is not extreme and the contrast of the LCD image should not be greatly reduced.

Note

1. Dual Panel Considerations: When configured for a dual LCD panel and using Simultaneous Display, the Half Frame Buffer Disable, REG[1Bh] bit 0, must be set to 1. This results in a lower contrast on the LCD panel, which may require adjustment.
2. The Line doubling option is not supported with dual panel.

bits 4-2 — Bit-per-pixel Select Bits [2:0]
These bits select the color depth (bpp) for the displayed data. See *"Section 10.1 Display Mode Formats"* for details of how the pixels are mapped into the image buffer.

Table 8-7: Bit-per-pixel Selection

Bit-per-pixel Select Bits [2:0]	Color Depth (bpp)
000	1 bpp
001	2 bpp
010	4 bpp
011	8 bpp
100	15 bpp
101	16 bpp
110 – 111	Reserved

bit 1 — CRT Enable
This bit enables the CRT monitor.
When this bit = 1, the CRT is enabled.
When this bit = 0, the CRT is disabled.

bit 0 — LCD Enable
This bit enables the LCD panel.
Programming this bit from a 0 to a 1 starts the LCD power-on sequence.
Programming this bit from a 1 to a 0 starts the LCD power-off sequence.

Screen 1 Line Compare Register 0 REG[0Eh]							RW
Screen 1 Line Compare Bit 7	Screen 1 Line Compare Bit 6	Screen 1 Line Compare Bit 5	Screen 1 Line Compare Bit 4	Screen 1 Line Compare Bit 3	Screen 1 Line Compare Bit 2	Screen 1 Line Compare Bit 1	Screen 1 Line Compare Bit 0

Screen 1 Line Compare Register 1 REG[0Fh]							RW
n/a	n/a	n/a	n/a	n/a	n/a	Screen 1 Line Compare Bit 9	Screen 1 Line Compare Bit 8

REG[0Eh] bits 7-0
REG[0Fh] bits 1-0 — Screen 1 Line Compare Bits [9:0]
These bits are set to 1 during power-on.
The display can be split into two images: Screen 1 and Screen 2, with Screen 1 above Screen 2. This 10-bit value specifies the height of Screen 1.

Height of Screen 1 (lines) = Screen 1 Line Compare Bits [9:0] + 1

If the height of Screen 1 is less than the display height then the remainder of the display is taken up by Screen 2. For normal operation (no split screen) this register must be set greater than the Vertical Display Height register (e.g. set to the reset value of 3FFh).

See *"Display Configuration"* for details.

Screen 1 Display Start Address Register 0 REG[10h]							RW
Start Address Bit 7	Start Address Bit 6	Start Address Bit 5	Start Address Bit 4	Start Address Bit 3	Start Address Bit 2	Start Address Bit 1	Start Address Bit 0

Screen 1 Display Start Address Register 1 REG[11h]							RW
Start Address Bit 15	Start Address Bit 14	Start Address Bit 13	Start Address Bit 12	Start Address Bit 11	Start Address Bit 10	Start Address Bit 9	Start Address Bit 8

Screen 1 Display Start Address Register 2 REG[12h]							RW
n/a	n/a	n/a	n/a	Start Address Bit 19	Start Address Bit 18	Start Address Bit 17	Start Address Bit 16

REG[10h] bits 7-0
REG[11h] bits 7-0
REG[12h] bits 3-0

Screen 1 Start Address Bits [19:0]
These registers form the 20-bit address for the starting word of the Screen 1 image in the display buffer.
Note that this is a word address.
A combination of this register and the Pixel Panning register (REG[18h]) can be used to uniquely identify the start (top left) pixel within the Screen 1 image stored in the display buffer.

See “*Display Configuration*” for details.

Screen 2 Display Start Address Register 0 REG[13h]							RW
Start Address Bit 7	Start Address Bit 6	Start Address Bit 5	Start Address Bit 4	Start Address Bit 3	Start Address Bit 2	Start Address Bit 1	Start Address Bit 0

Screen 2 Display Start Address Register 1 REG[14h]							RW
Start Address Bit 15	Start Address Bit 14	Start Address Bit 13	Start Address Bit 12	Start Address Bit 11	Start Address Bit 10	Start Address Bit 9	Start Address Bit 8

Screen 2 Display Start Address Register 2 REG[15h]							RW
n/a	n/a	n/a	n/a	Start Address Bit 19	Start Address Bit 18	Start Address Bit 17	Start Address Bit 16

REG[13h] bits 7-0
REG[14h] bits 7-0
REG[15h] bits 3-0

Screen 2 Start Address Bits [19:0]
These registers form the 20-bit address for the starting word of the Screen 2 image in the display buffer.
Note that this is a word address.
A combination of this register and the Pixel Panning register (REG[18h]) can be used to uniquely identify the start (top left) pixel within the Screen 2 image stored in the display buffer.

See “*Display Configuration*” for details.

Memory Address Offset Register 0 REG[16h]							RW
Memory Address Offset Bit 7	Memory Address Offset Bit 6	Memory Address Offset Bit 5	Memory Address Offset Bit 4	Memory Address Offset Bit 3	Memory Address Offset Bit 2	Memory Address Offset Bit 1	Memory Address Offset Bit 0

Memory Address Offset Register 1 REG[17h]							RW
n/a	n/a	n/a	n/a	n/a	Memory Address Offset Bit 10	Memory Address Offset Bit 9	Memory Address Offset Bit 8

REG[16h] bits 7-0
REG[17h] bits 2-0

Memory Address Offset Bits [10:0]
These bits form the 11-bit address offset from the starting word of line n to the starting word of line n+1. This value is applied to both Screen 1 and Screen 2.
Note that this value is in words.
A virtual image can be formed by setting this register to a value greater than the width of the display. The displayed image is a window into the larger virtual image.

See "Section 10 *Display Configuration*" for details.

Pixel Panning Register REG[18h]							RW
Screen 2 Pixel Panning Bit 3	Screen 2 Pixel Panning Bit 2	Screen 2 Pixel Panning Bit 1	Screen 2 Pixel Panning Bit 0	Screen 1 Pixel Panning Bit 3	Screen 1 Pixel Panning Bit 2	Screen 1 Pixel Panning Bit 1	Screen 1 Pixel Panning Bit 0

This register is used to control the horizontal pixel panning of Screen 1 and Screen 2. Each screen can be independently panned to the left by programming its respective Pixel Panning Bits to a non-zero value. The value represents the number of pixels panned. The maximum pan value is dependent on the display mode.

Table 8-8: Pixel Panning Selection

Display Mode	Maximum Pan Value	Pixel Panning Bits active
1 bpp	16	Bits [3:0]
2 bpp	8	Bits [2:0]
4 bpp	4	Bits [1:0]
8 bpp	1	Bit 0
15/16 bpp	0	none

Smooth horizontal panning can be achieved by a combination of this register and the Display Start Address registers.

See "Section 10 *Display Configuration*" for details.

bits 7-4
Screen 2 Pixel Panning Bits [3:0]
Pixel panning bits for screen 2.

bits 3-0
Screen 1 Pixel Panning Bits [3:0]
Pixel panning bits for screen 1.

8.2.5 Clock Configuration Register

Clock Configuration Register REG[19h]							RW
Reserved	n/a	n/a	n/a	n/a	MCLK Divide Select	PCLK Divide Select Bit 1	PCLK Divide Select Bit 0

bit 7 Reserved
This bit must be set to 0.

Note
There must always be a source clock at CLKI.

bit 2 MCLK Divide Select
When this bit = 1 the MCLK frequency is half of its source frequency.
When this bit = 0 the MCLK frequency is equal to its source frequency.
The MCLK frequency should always be set to the maximum frequency allowed by the DRAM; this provides maximum performance and minimum overall system power consumption.

bits 1-0 PCLK Divide Select Bits [1:0]
These bits select the MCLK: PCLK frequency ratio

Table 8-9: PCLK Divide Selection

PCLK Divide Select Bits [1:0]	MCLK: PCLK Frequency Ratio
00	1: 1
01	2: 1
10	3: 1
11	4: 1

See section on "*Maximum MCLK:PCLK Frequency Ratios*" for selection of clock ratios.

8.2.6 Power Save Configuration Registers

Power Save Configuration Register REG[1Ah]							RW
Power Save Status RO	n/a	n/a	n/a	LCD Power Disable	Suspend Refresh Select Bit 1	Suspend Refresh Select Bit 0	Software Suspend Mode Enable

bit 7 Power Save Status
This is a read-only status bit.
This bit indicates the power-save state of the chip.
When this bit = 1, the panel has been powered down and the memory controller is either in self refresh mode or is performing only CAS-before-RAS refresh cycles.
When this bit = 0, the chip is either powered up, in transition of powering up, or in transition of powering down. See Section 15 *Power Save Modes* for details.

bit 3 LCD Power Disable
This bit is used to override the panel on/off sequencing logic.
When this bit = 0 the LCDPWR output is controlled by the panel on/off sequencing logic.
When this bit = 1 the LCDPWR output is directly forced to the off state.

The LCDPWR "On/Off" polarity is configured by MD10 at the rising edge of RESET# (MD10 = 0 configures LCDPWR = 0 as the Off state; MD10 = 1 configures LCDPWR = 1 as the Off state).

bits 2-1 Suspend Refresh Select Bits [1:0]
These bits specify the type of DRAM refresh to use in Suspend mode.

Table 8-10: Suspend Refresh Selection

Suspend Refresh Select Bits [1:0]	DRAM Refresh Type
00	CAS-before-RAS (CBR) refresh
01	Self-Refresh
1X	No Refresh

Note
These bits should not be changed while suspend mode is active.

bit 0 Software Suspend Mode Enable
When this bit = 1 software Suspend mode is enabled.
When this bit = 0 software Suspend mode is disabled.
See *Section 15 Power Save Modes* for details.

8.2.7 Miscellaneous Registers

Miscellaneous Register REG[1Bh]							RW
Host Interface Disable	n/a	n/a	n/a	n/a	n/a	n/a	Half Frame Buffer Disable

bit 7 Host Interface Disable
This bit is set to 1 during power-on/reset.
This bit must be programmed to 0 to enable the Host Interface. When this bit is high, all memory and all registers except REG[1Ah] (read-only) and REG[1Bh] are inaccessible.

bit 0 Half Frame Buffer Disable
This bit is used to disable the Half Frame Buffer.
When this bit = 1, the Half Frame Buffer is disabled.
When this bit = 0, the Half Frame Buffer is enabled.
When a single panel is selected, the Half Frame Buffer is automatically disabled and this bit has no effect.

The half frame buffer is needed to fully support dual panels. Disabling the Half Frame Buffer reduces memory bandwidth requirements and increases the supportable pixel clock frequency, but results in reduced contrast on the LCD panel (the duty cycle of the LCD is halved). This mode is not normally used except under special circumstances such as simultaneous display on a CRT and dual panel LCD. When this mode is used the Alternate Frame Rate Modulation scheme should be used (see REG[31h]). For details on Frame Rate calculation see Section 14.2, "Frame Rate Calculation" on page 141.

MD Configuration Readback Register 0 REG[1Ch]							RO
MD[7] Status	MD[6] Status	MD[5] Status	MD[4] Status	MD[3] Status	MD[2] Status	MD[1] Status	MD[0] Status

MD Configuration Readback Register 1 REG[1Dh]							RO
MD[15] Status	MD[14] Status	MD[13] Status	MD[12] Status	MD[11] Status	MD[10] Status	MD[9] Status	MD[8] Status

REG[1Ch] bits 7-0
REG[1Dh] bits 7-0

MD[15:0] Configuration Status
These are read-only status bits for the MD[15:0] pins configuration status at the rising edge of RESET#. MD[15:0] are used to configure the chip at the rising edge of RESET# – see *Pin Descriptions* and *Summary of Configuration Options* for details.

General IO Pins Configuration Register 0 REG[1Eh]							RW
n/a	n/a	n/a	n/a	GPIO3 Pin IO Config.	GPIO2 Pin IO Config.	GPIO1 Pin IO Config.	n/a

Pins MA9, MA10, MA11 are multi-functional – they can be DRAM address outputs or general purpose IO dependent on the DRAM type. MD[7:6] are used to identify the DRAM type and configure these pins as follows:

Table 8-11: MA/GPIO Pin Functionality

MD[7:6] at rising edge of RESET#	**Pin Function**		
	MA9	**MA10**	**MA11**
00	GPIO3	GPIO1	GPIO2
01	MA9	GPIO1	GPIO2
10	MA9	GPIO1	GPIO2
11	MA9	MA10	MA11

These bits are used to control the direction of these pins when they are used as general purpose IO. These bits have no effect when the pins are used as DRAM address outputs.

bit 3 GPIO3 Pin IO Configuration
When this bit = 1, the GPIO3 pin is configured as an output pin.
When this bit = 0 (default), the GPIO3 pin is configured as an input pin.

bit 2 GPIO2 Pin IO Configuration
When this bit = 1, the GPIO2 pin is configured as an output pin.
When this bit = 0 (default), the GPIO2 pin is configured as an input pin.

bit 1 GPIO1 Pin IO Configuration
When this bit = 1, the GPIO1 pin is configured as an output pin.
When this bit = 0 (default), the GPIO1 pin is configured as an input pin.

General IO Pins Configuration Register 1 REG[1Fh] RW							
n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a

This register position is reserved for future use.

General IO Pins Control Register 0 REG[20h] RW							
n/a	n/a	n/a	n/a	GPIO3 Pin IO Status	GPIO2 Pin IO Status	GPIO1 Pin IO Status	n/a

bit 3 GPIO3 Pin IO Status
When GPIO3 is configured as an output (see REG[1Eh]), a “1” in this bit drives GPIO3 high and a “0” in this bit drives GPIO3 low.
When GPIO3 is configured as an input, a read from this bit returns the status of GPIO3.

bit 2 GPIO2 Pin IO Status
When GPIO2 is configured as an output (see REG[1Eh]), a “1” in this bit drives GPIO2 high and a “0” in this bit drives GPIO2 low.
When GPIO2 is configured as an input, a read from this bit returns the status of GPIO2.

bit 1 GPIO1 Pin IO Status
When GPIO1 is configured as an output (see REG[1Eh]), a “1” in this bit drives GPIO1 high and a “0” in this bit drives GPIO1 low.
When GPIO1 is configured as an input, a read from this bit returns the status of GPIO1.

General IO Pins Control Register 1 REG[21h] RW							
GPO Control	n/a	n/a	n/a	n/a	n/a	n/a	n/a

bit 7 GPO Control
This bit is used to control the state of the SUSPEND# pin when it is configured as General Purpose Output (GPO). When this bit = 0, the GPO output is set to the reset state. When this bit = 1, the GPO output is set to the inverse of the reset state. For information on the reset state of this pin see “Miscellaneous Interface Pin Descriptions“ on page 32 and “Summary of Power On/Reset Options“ on page 33.

Performance Enhancement Register 0 REG[22h] RW							
Reserved	RC Timing Value Bit 1	RC Timing Value Bit 0	RAS#-to-CAS# Delay Value	RAS# Precharge Timing Value Bit 1	RAS# Precharge Timing Value Bit 0	Reserved	Reserved

Note

Changing this register to non-zero value, or to a different non-zero value, should be done only when there are no read/write DRAM cycles. This condition occurs when all of the following are true: the Display FIFO is disabled (REG[23h] bit 7 = 1), and the Half Frame Buffer is disabled (REG[1Bh] bit 0 = 1), and the Ink/Cursor is inactive (Reg[27h] bits 7-6 = 00). This condition also occurs when the CRT and LCD enable bits (Reg[0Dh] bits 1-0) have remained 0 since chip reset. For further programming information, see *S1D13505 Programming Notes and Examples*, document number X23A-G-003-xx.

bit 7 Reserved

bits 6-5 RC Timing Value (N_{RC}) Bits [1:0]

These bits select the DRAM random-cycle timing parameter, t_{RC}. These bits specify the number (N_{RC}) of MCLK periods (T_M) used to create t_{RC}. N_{RC} should be chosen to meet t_{RC} as well as t_{RAS}, the RAS pulse width. Use the following two formulae to calculate N_{RC} then choose the larger value. Note, these formulae assume an MCLK duty cycle of 50 +/- 5%.

N_{RC} = Round-Up (t_{RC}/T_M)

N_{RC} = Round-Up ($t_{RAS}/T_M + N_{RP}$) if N_{RP} = 1 or 2
= Round-Up (t_{RAS}/T_M + 1.55) if N_{RP} = 1.5

The resulting t_{RC} is related to N_{RC} as follows:

t_{RC} = (N_{RC}) T_M

Table 8-12: Minimum Memory Timing Selection

REG[22h] bits [6:5]	N_{RC}	Minimum Random Cycle Width (t_{RC})
00	5	5
01	4	4
10	3	3
11	Reserved	Reserved

bit 4 RAS#-to-CAS# Delay Value (N_{RCD})
This bit selects the DRAM RAS#-to-CAS# delay parameter, t_{RCD}. This bit specifies the number (N_{RCD}) of MCLK periods (T_M) used to create t_{RCD}. N_{RCD} must be chosen to satisfy the RAS# access time, t_{RAC}. Note, these formulae assume an MCLK duty cycle of 50 +/- 5%.

N_{RCD}	= Round-Up((t_{RAC} + 5)/T_M - 1)	if EDO and N_{RP} = 1 or 2
	= 2	if EDO and N_{RP} = 1.5
	= Round-Up(t_{RAC}/T_M - 1)	if FPM and N_{RP} = 1 or 2
	= Round-Up(t_{RAC}/T_M - 0.45)	if FPM and N_{RP} = 1.5

Note that for EDO-DRAM and N_{RP} = 1.5, this bit is automatically forced to 0 to select 2 MCLK for N_{RCD}. This is done to satisfy the CAS# address setup time, t_{ASC}.

The resulting t_{RC} is related to N_{RCD} as follows:

t_{RCD}	= (N_{RCD}) T_M	if EDO and N_{RP} = 1 or 2
t_{RCD}	= (1.5) T_M	if EDO and N_{RP} = 1.5
t_{RCD}	= (N_{RCD} + 0.5) T_M	if FPM and N_{RP} = 1 or 2
t_{RCD}	= (N_{RCD}) T_M	if FPM and N_{RP} = 1.5

Table 8-13: RAS#-to-CAS# Delay Timing Select

REG[22h] bit 4	N_{RCD}	RAS#-to-CAS# Delay (t_{RCD})
0	2	2
1	1	1

bits 3-2 RAS# Precharge Timing Value (N_{RP}) Bits [1:0]
Minimum Memory Timing for RAS# precharge
These bits select the DRAM RAS# Precharge timing parameter, t_{RP}. These bits specify the number (N_{RP}) of MCLK periods (T_M) used to create t_{RP} – see the following formulae. Note, these formulae assume an MCLK duty cycle of 50 +/- 5%.

N_{RP}	= 1	if (t_{RP}/T_M) < 1
	= 1.5	if 1 ≤ (t_{RP}/T_M) < 1.45
	= 2	if (t_{RP}/T_M) ≥ 1.45

The resulting t_{RC} is related to N_{RP} as follows:

t_{RP}	= (N_{RP} + 0.5) T_M	if FPM refresh cycle and N_{RP} = 1 or 2
t_{RP}	= (N_{RP}) T_M	for all other

bits 1-0 Reserved
These bits must be set to 0.

Table 8-14: RAS Precharge Timing Select

REG[22h] bits [3:2]	N_{RP}	RAS# Precharge Width (t_{RP})
00	2	2
01	1.5	1.5
10	1	1
11	Reserved	Reserved

Optimal DRAM Timing

The following table contains the optimally programmed values of N_{RC}, N_{RP}, and N_{RCD} for different DRAM types, at maximum MCLK frequencies.

Table 8-15: Optimal N_{RC}, N_{RP}, and N_{RCD} values at maximum MCLK frequency

DRAM Type	DRAM Speed (ns)	T_M (ns)	N_{RC} (#MCLK)	N_{RP} (#MCLK)	N_{RCD} (#MCLK)
EDO	50	25	4	1.5	2
	60	30	4	1.5	2
	70	33	5	2	2
FPM	60	40	4	1.5	2
	70	50	3	1.5	1

bit 0 Reserved
This reserved bit must be set to 0.

Performance Enhancement Register 1 REG[23h] RW							
Display FIFO Disable	CPU to Memory Wait State Bit 1	CPU to Memory Wait State Bit 0	Display FIFO Threshold Bit 4	Display FIFO Threshold Bit 3	Display FIFO Threshold Bit 2	Display FIFO Threshold Bit 1	Display FIFO Threshold Bit 0

bit 7 Display FIFO Disable
When this bit = 1 the display FIFO is disabled and all data outputs are forced to zero (i.e., the screen is blanked). This accelerates screen updates by allocating more memory bandwidth to CPU accesses.
When this bit = 0 the display FIFO is enabled.

Note

For further performance increase in dual panel mode disable the half frame buffer (see section 8.2.7) and disable the cursor (see section 8.2.9).

bit 6-5 CPU to Memory Wait State Bits [1:0]
These bits are used to optimize the handshaking between the host interface and the memory controller. The bits should be set according to the relationship between BCLK and MCLK – see the table below where T_B and T_M are the BCLK and MCLK periods respectively.

Table 8-16: Minimum Memory Timing Selection

Wait State Bits [1:0]	Condition
00	no restrictions (default)
01	$2T_M$ - 4ns > T_B
10	undefined
11	undefined

bits 4-0 Display FIFO Threshold Bits [4:0]
These bits specify the display FIFO depth required to sustain uninterrupted display fetches. When these bits are all “0”, the display FIFO depth is calculated automatically.
These bits should always be set to 0, except in the following configurations:
Landscape mode at 15/16 bpp (with MCLK=PCLK),
Portrait mode at 8/16 bpp (with MCLK=PCLK).
When in the above configurations, a value of 1Bh should be used.

Note
The utility 13505CFG will, given the correct configuration values, automatically generate the correct values for the Performance Enhancement Registers.

8.2.8 Look-Up Table Registers

Look-Up Table Address Register REG[24h]							RW
LUT Address Bit 7	LUT Address Bit 6	LUT Address Bit 5	LUT Address Bit 4	LUT Address Bit 3	LUT Address Bit 2	LUT Address Bit 1	LUT Address Bit 0

bits 7-0 LUT Address Bits [7:0]
These 8 bits control a pointer into the Look-Up Tables (LUT). The S1D13505 has three 256-position, 4-bit wide LUTs, one for each of red, green, and blue – refer to *“Look-Up Table Architecture”* for details.

This register selects which LUT entry is read/write accessible through the LUT Data Register (REG[26h]). Writing the LUT Address Register automatically sets the pointer to the Red LUT. Accesses to the LUT Data Register automatically increment the pointer.

For example, writing a value 03h into the LUT Address Register sets the pointer to R[3]. A subsequent access to the LUT Data Register accesses R[3] and moves the pointer onto G[3]. Subsequent accesses to the LUT Data Register move the pointer onto B[3], R[4], G[4], B[4], R[5], etc. Note that the RGB data is inserted into the LUT after the Blue data is written, i.e. all three colors must be written before the LUT is updated.

Look-Up Table Data Register REG[26h]							RW
LUT Data Bit 3	LUT Data Bit 2	LUT Data Bit 1	LUT Data Bit 0	n/a	n/a	n/a	n/a

bits 7-4 LUT Data
This register is used to read/write the RGB Look-Up Tables. This register accesses the entry at the pointer controlled by the Look-Up Table Address Register (REG[24h]) – see above.

Accesses to the Look-Up Table Data Register automatically increment the pointer.Note that the RGB data is inserted into the LUT after the Blue data is written, i.e. all three colors must be written before the LUT is updated.

8.2.9 Ink/Cursor Registers

Ink/Cursor Control Register REG[27h]							RW
Ink/Cursor Mode Bit 1	Ink/Cursor Mode Bit 0	n/a	n/a	Cursor High Threshold Bit 3	Cursor High Threshold Bit 2	Cursor High Threshold Bit 1	Cursor High Threshold Bit 0

bit 7-6 Ink/Cursor Control Bits [1:0]
These bits select the operating mode of the Ink/Cursor circuitry. See table below

Table 8-17: Ink/Cursor Selection

REG[27h]		Operating Mode
Bit 7	**Bit 6**	
0	0	inactive
0	1	Cursor
1	0	Ink
1	1	reserved

bit 3-0 Ink/Cursor FIFO Threshold Bits [3:0]
These bits specify the Ink/Cursor FIFO depth required to sustain uninterrupted display fetches. When these bits are all 0, the Ink/Cursor FIFO depth is calculated automatically.

Cursor X Position Register 0 REG[28h]							RW
Cursor X Position Bit 7	Cursor X Position Bit 6	Cursor X Position Bit 5	Cursor X Position Bit 4	Cursor X Position Bit 3	Cursor X Position Bit 2	Cursor X Position Bit 1	Cursor X Position Bit 0

Cursor X Position Register 1 REG[29h]							RW
Reserved	n/a	n/a	n/a	n/a	n/a	Cursor X Position Bit 9	Cursor X Position Bit 8

REG[29] bit 7 Reserved
This bit must be set to 0.

REG[28] bits 7-0 Cursor X Position Bits [9:0]
REG[29] bits 1-0 In Cursor mode, this 10-bit register is used to program the horizontal pixel position of the Cursor's top left pixel.
This register must be set to 0 in Ink mode.

Note
The Cursor X Position register must be set during VNDP (vertical non-display period). Check the VNDP status bit (REG[0Ah] bit 7) to determine if you are in VNDP, then update the register.

Cursor Y Position Register 0 REG[2Ah]							RW
Cursor Y Position Bit 7	Cursor Y Position Bit 6	Cursor Y Position Bit 5	Cursor Y Position Bit 4	Cursor Y Position Bit 3	Cursor Y Position Bit 2	Cursor Y Position Bit 1	Cursor Y Position Bit 0

Cursor Y Position Register 1 REG[2Bh]							RW
Reserved	n/a	n/a	n/a	n/a	n/a	Cursor Y Position Bit 9	Cursor Y Position Bit 8

REG[2Bh] bit 7 Reserved
This bit must be set to 0.

REG[2Ah] bits 7-0 Cursor Y Position Bits [9:0]
REG[2Bh] bits 1-0 In Cursor mode, this 10-bit register is used to program the vertical pixel position of the Cursor's top left pixel.
This register must be set to 0 in Ink mode.

Note
The Cursor Y Position register must be set during VNDP (vertical non-display period). Check the VNDP status bit (REG[0Ah] bit 7) to determine if you are in VNDP, then update the register.

Ink/Cursor Color 0 Register 0 REG[2Ch]							RW
Cursor Color 0 Bit 7	Cursor Color 0 Bit 6	Cursor Color 0 Bit 5	Cursor Color 0 Bit 4	Cursor Color 0 Bit 3	Cursor Color 0 Bit 2	Cursor Color 0 Bit 1	Cursor Color 0 Bit 0

Ink/Cursor Color 0 Register 1 REG[2Dh]							RW
Cursor Color 0 Bit 15	Cursor Color 0 Bit 14	Cursor Color 0 Bit 13	Cursor Color 0 Bit 12	Cursor Color 0 Bit 11	Cursor Color 0 Bit 10	Cursor Color 0 Bit 9	Cursor Color 0 Bit 8

REG[2C] bits 7:0 Ink/Cursor Color 0 Bits [15:0]
REG[2D] bits 7:0 These bits define the 5-6-5 RGB Ink/Cursor color 0.

Ink/Cursor Color 1 Register 0 REG[2Eh]							RW
Cursor Color 1 Bit 7	Cursor Color 1 Bit 6	Cursor Color 1 Bit 5	Cursor Color 1 Bit 4	Cursor Color 1 Bit 3	Cursor Color 1 Bit 2	Cursor Color 1 Bit 1	Cursor Color 1 Bit 0

Ink/Cursor Color 1 Register 1 REG[2Fh]							RW
Cursor Color 1 Bit 15	Cursor Color 1 Bit 14	Cursor Color 1 Bit 13	Cursor Color 1 Bit 12	Cursor Color 1 Bit 11	Cursor Color 1 Bit 10	Cursor Color 1 Bit 9	Cursor Color 1 Bit 8

REG[2E] bits 7:0 Ink/Cursor Color 1 Bits [15:0]
REG[2F] bits 7:0 These bits define the 5-6-5 RGB Ink/Cursor color 1

Ink/Cursor Start Address Select Register REG[30h]							RW
Ink/Cursor Start Address Select Bit 7	Ink/Cursor Start Address Select Bit 6	Ink/Cursor Start Address Select Bit 5	Ink/Cursor Start Address Select Bit 4	Ink/Cursor Start Address Select Bit 3	Ink/Cursor Start Address Select Bit 2	Ink/Cursor Start Address Select Bit 1	Ink/Cursor Start Address Select Bit 0

bits 7-0 Ink/Cursor Start Address Select Bits [7:0]
These bits define the start address for the Ink/Cursor buffer. The Ink/Cursor buffer must be positioned where it does not conflict with the image buffer and half-frame buffer – see Memory Mapping for details.

The start address for the Ink/Cursor buffer is programmed as shown in the following table where Display Buffer Size represents the size in bytes of the attached DRAM device (see MD[7:6] in *Summary of Configuration Options*):

Table 8-18: Ink/Cursor Start Address Encoding

Ink/Cursor Start Address Bits [7:0]	**Start Address (Bytes)**
0	Display Buffer Size - 1024
n = 255...1	Display Buffer Size - (n $\times$ 8192)

The Ink/Cursor image is stored contiguously. The address offset from the starting word of line n to the starting word of line n+1 is calculated as follows:
Ink Address Offset (words) = REG[04h] + 1
Cursor Address Offset (words) = 8

Alternate FRM Register							
REG[31h]							RW
Alternate FRM Bit 7	Alternate FRM Bit 6	Alternate FRM Bit 5	Alternate FRM Bit 4	Alternate FRM Bit 3	Alternate FRM Bit 2	Alternate FRM Bit 1	Alternate FRM Bit 0

bits 7-0 Alternate Frame Rate Modulation Select
Register that controls the alternate FRM scheme. When all bits are set to zero, the default FRM is selected. For single passive, or dual passive with the half frame buffer enabled, either the original or the alternate FRM scheme may be used. The alternate FRM scheme may produce more visually appealing output. The following table shows the recommended alternate FRM scheme values.

Table 8-19: Recommended Alternate FRM Scheme

Panel Mode	**Register Value**
Single Passive	0000 0000 or 1111 1111
Dual Passive w/Half Frame Buffer Enabled	0000 0000 or 1111 1010
Dual Passive w/Half Frame Buffer Disabled	1111 1111

9 Display Buffer

The system addresses the display buffer through the CS#, M/R#, and AB[20:0] input pins. When CS# = 0 and M/R# = 1, the display buffer is addressed by bits AB[20:0]. See the table below:

Table 9-1: S1D13505 Addressing

CS#	M/R#	Access
0	0	Register access: • REG[00h] is addressed when AB[5:0] = 0 • REG[01h] is addressed when AB[5:0] = 1 • REG[n] is addressed when AB[5:0] = n
0	1	Memory access: the 2M byte display buffer is addressed by AB[20:0]
1	X	S1D13505 not selected

The display buffer address space is always 2M bytes. However, the physical display buffer may be either 512K bytes or 2M bytes – see *"Summary of Configuration Options"*.

The display buffer can contain an image buffer, one or more Ink/Cursor buffers, and a half-frame buffer.

A 512K byte display buffer is replicated in the 2M byte address space – see the figure below.

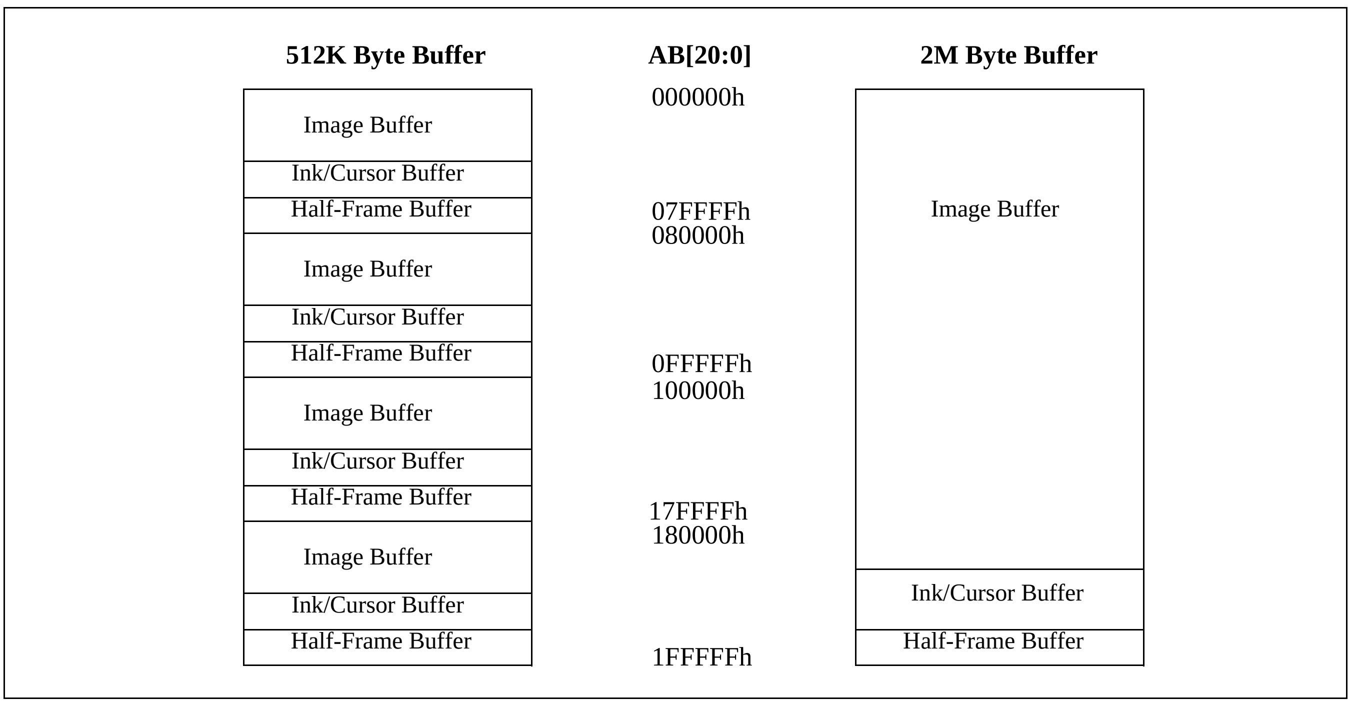


Figure 9-1: Display Buffer Addressing

9.1 Image Buffer

The image buffer contains the formatted display mode data – see *"Display Mode Data Formats"*.

The displayed image(s) could take up only a portion of this space; the remaining area may be used for multiple images – possibly for animation or general storage. See "Display Configuration" on page 124 for the relationship between the image buffer and the display.

9.2 Ink/Cursor Buffers

The Ink/Cursor buffers contain formatted image data for the Ink or Cursor. There may be several Ink/Cursor images stored in the display buffer but only one may be active at any given time. See "Ink/Cursor Architecture" on page 133 for details.

9.3 Half Frame Buffer

In dual panel mode, with the half frame buffer enabled, the top of the display buffer is allocated to the half-frame buffer. The size of the half frame buffer is a function of the panel resolution and whether the panel is color or monochrome type:

Half Frame Buffer Size (in bytes) = (panel width x panel length) * factor / 16

where factor = 4 for color panel
= 1 for monochrome panel

For example, for a 640x480 8 bpp color panel the half frame buffer size is 75K bytes. In a 512K byte display buffer, the half-frame buffer resides from 6D400h to 7FFFFh. In a 2M byte display buffer, the half-frame buffer resides from 1ED400h to 1FFFFFh.

10 Display Configuration

10.1 Display Mode Data Format

The following diagrams show the display mode data formats for a little-endian system.

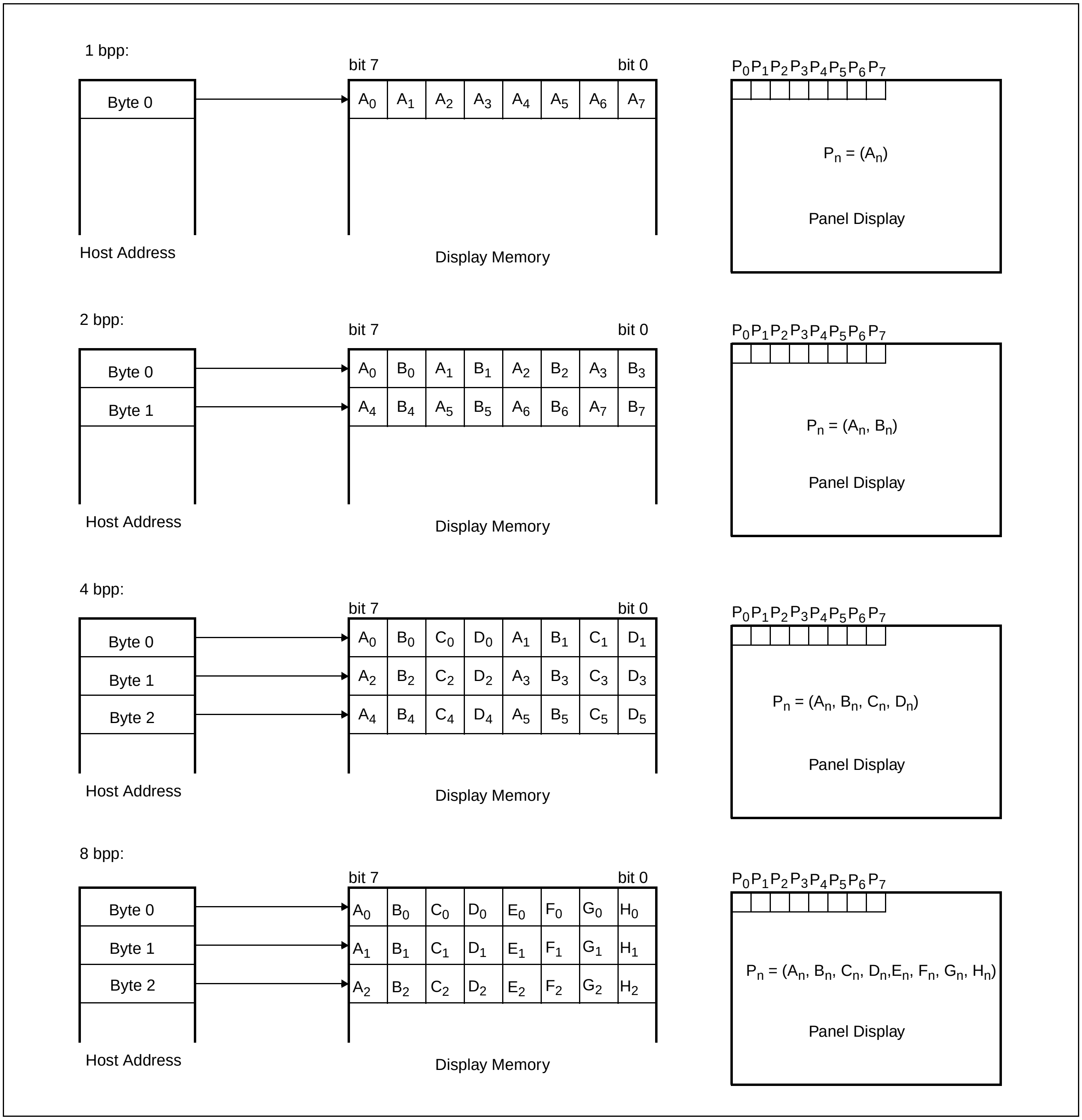


Figure 10-1: 1/2/4/8 Bit-per-pixel Format Memory Organization

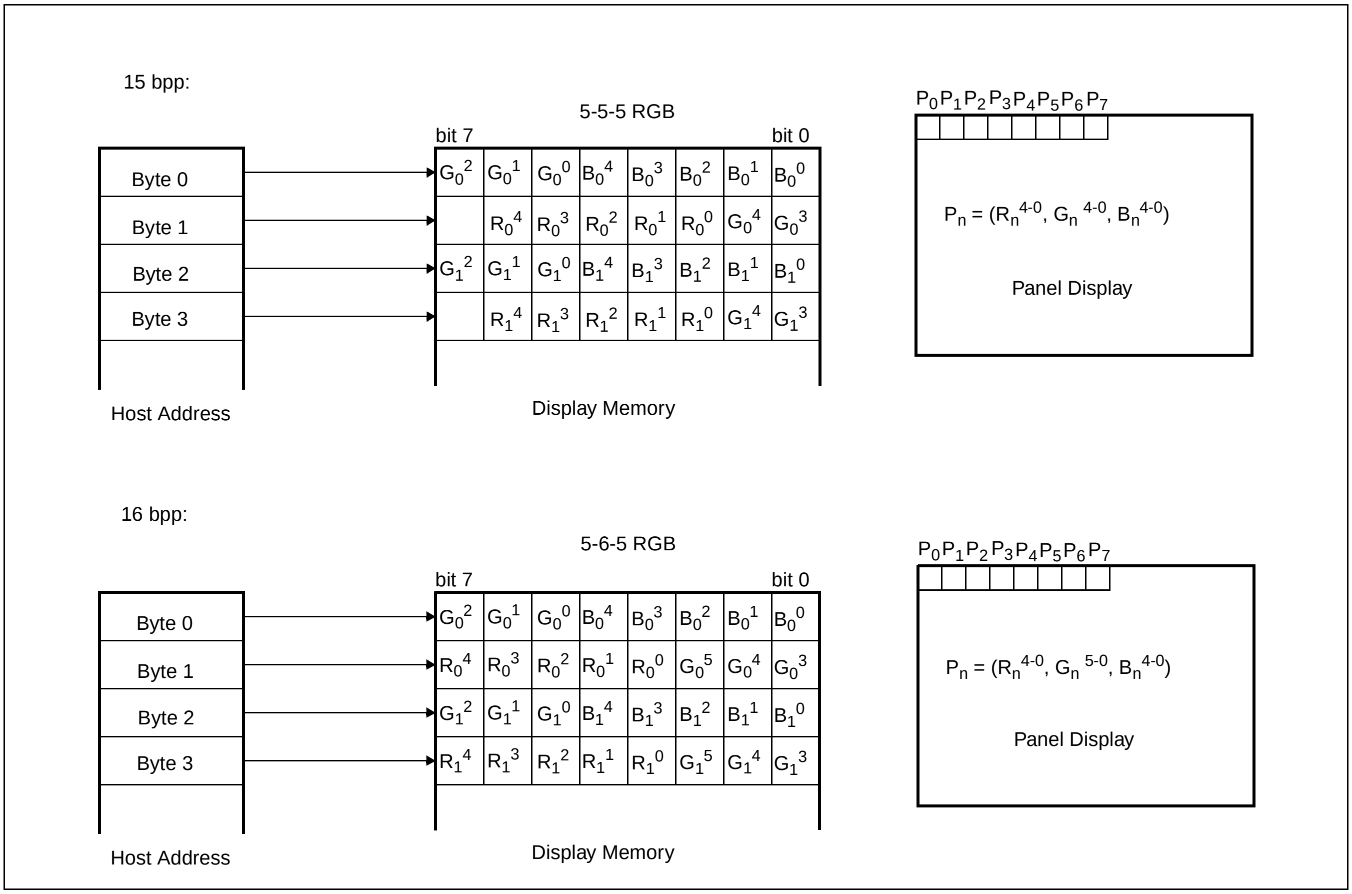


Figure 10-2: 15/16 Bit-per-pixel Format Memory Organization

Note

1. The Host-to-Display mapping shown here is for a little-endian system.
2. For 15/16 bpp formats, R_n, G_n, B_n represent the red, green, and blue color components.

10.2 Image Manipulation

The figure below shows how Screen 1 and 2 images are stored in the image buffer and positioned on the display. Screen 1 and Screen 2 can be parts of a larger virtual image or images.

- (REG[17h],REG[16h]) defines the width of the virtual image(s)
- (REG[12h],REG[11h],REG[10]) defines the starting word of the Screen 1, (REG[15h],REG[14h],REG[13]) defines the starting word of the Screen 2
- REG[18h] bits [3:0] define the starting pixel within the starting word for Screen 1, REG[18h] bits [7:4] define the starting pixel within the starting word for Screen 2
- (REG[0Fh],REG[0Eh]) define the last line of Screen 1, the remainder of the display is taken up by Screen 2

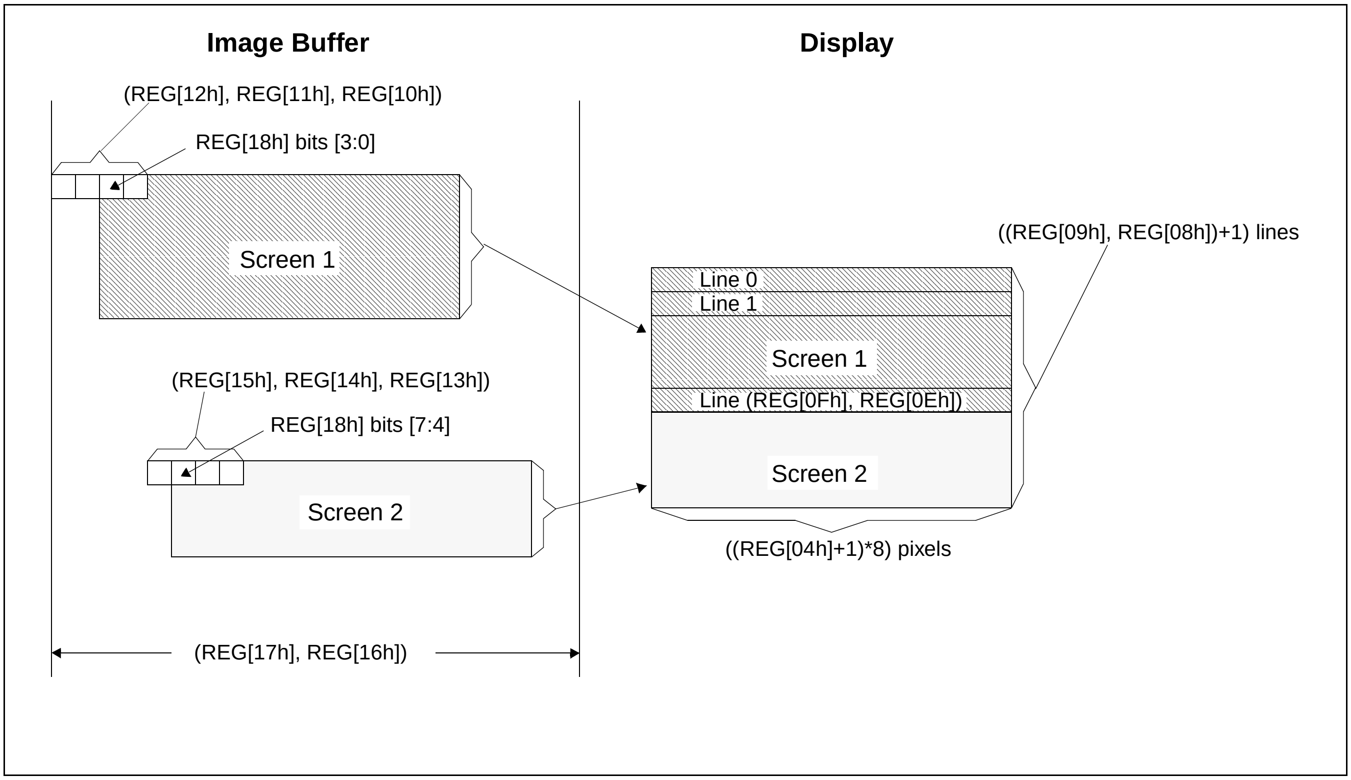


Figure 10-3: Image Manipulation

11 Look-Up Table Architecture

The following figures are intended to show the display data output path only.

11.1 Monochrome Modes

The green Look-Up Table (LUT) is used for all monochrome modes.

1 Bit-per-pixel Monochrome mode

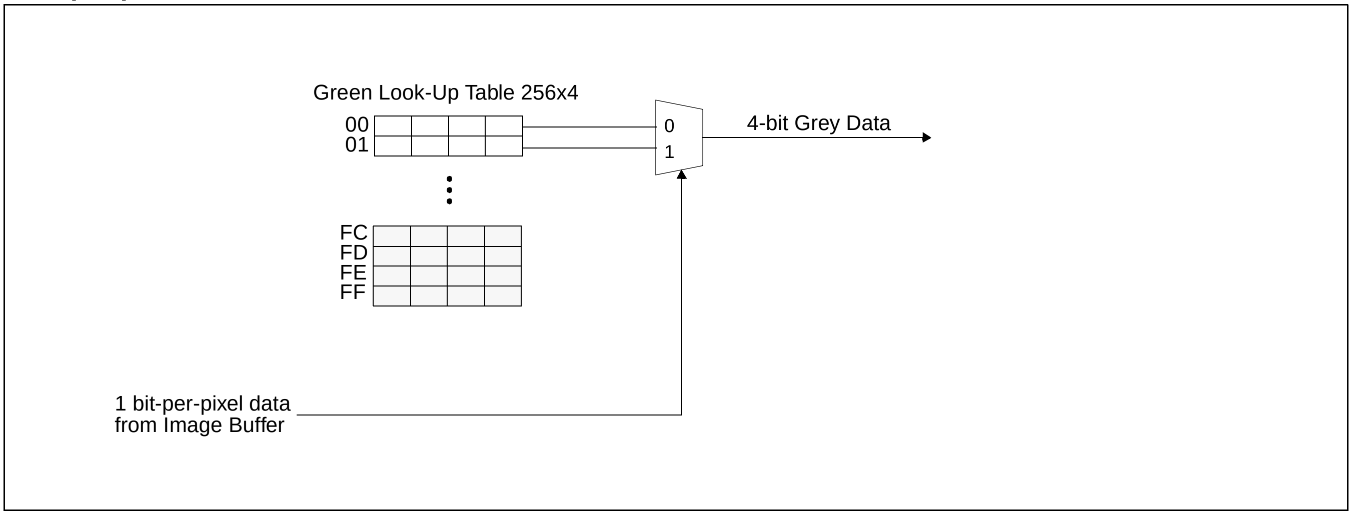


Figure 11-1: 1 Bit-per-pixel Monochrome Mode Data Output Path

2 Bit-per-pixel Monochrome Mode

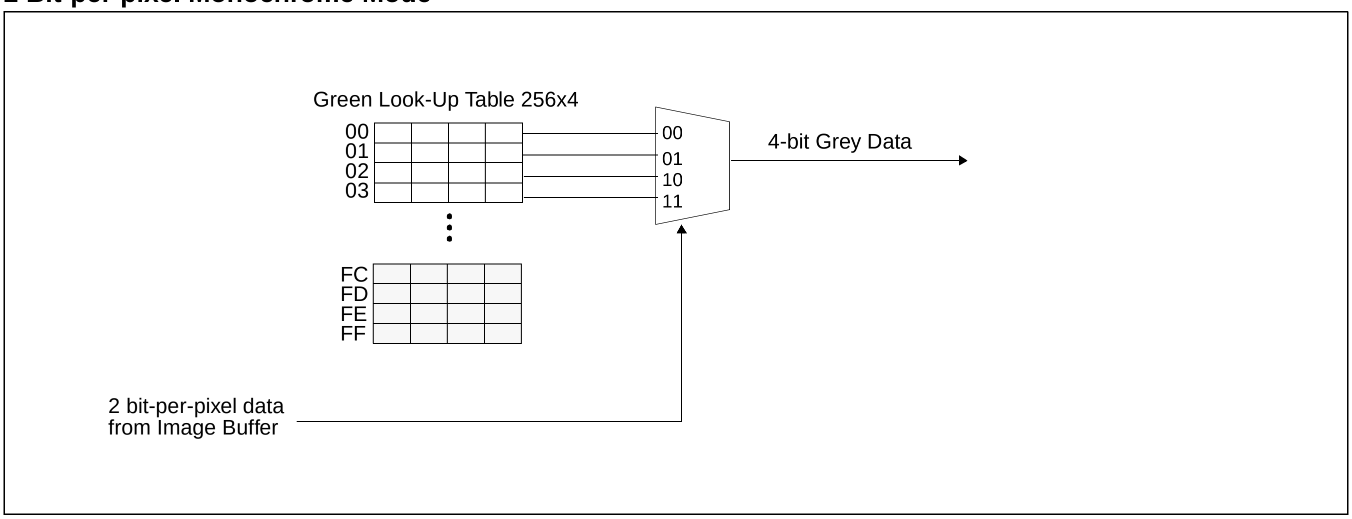


Figure 11-2: 2 Bit-per-pixel Monochrome Mode Data Output Path

4 Bit-per-pixel Monochrome Mode

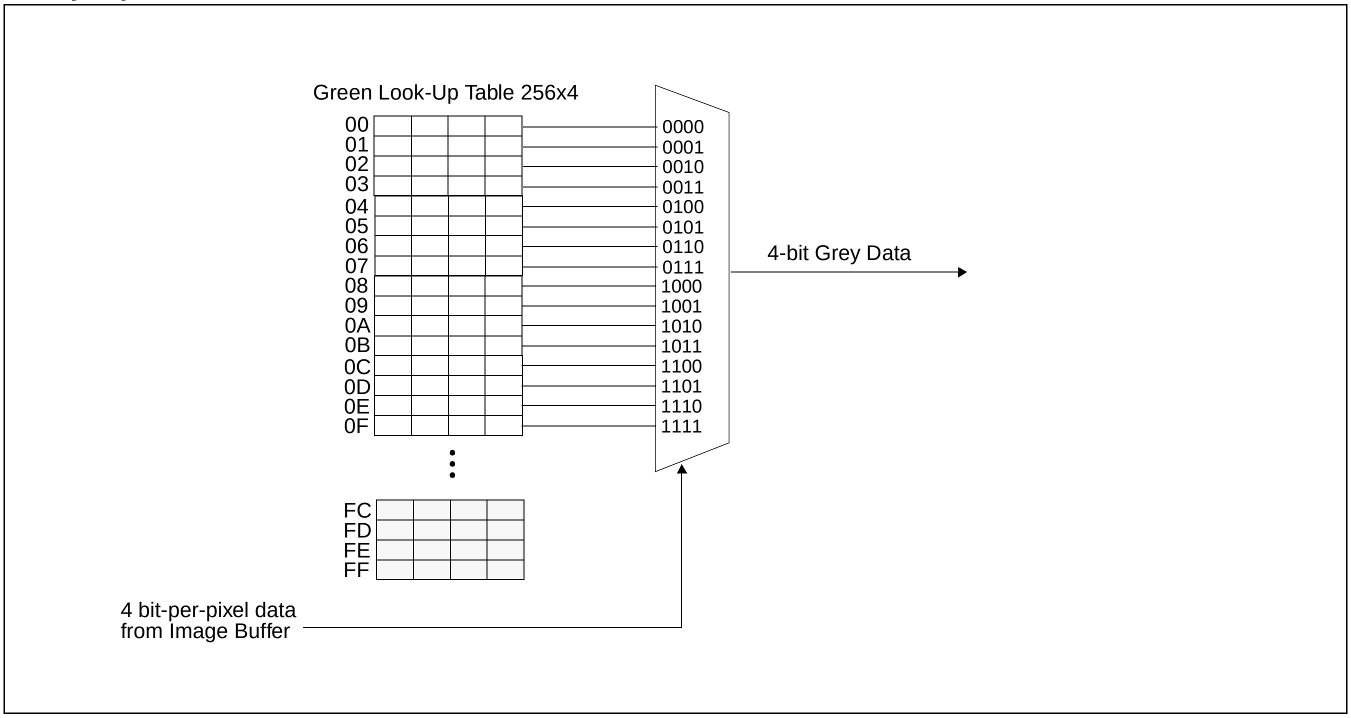


Figure 11-3: 4 Bit-per-pixel Monochrome Mode Data Output Path

11.2 Color Modes

1 Bit-per-pixel Color Mode

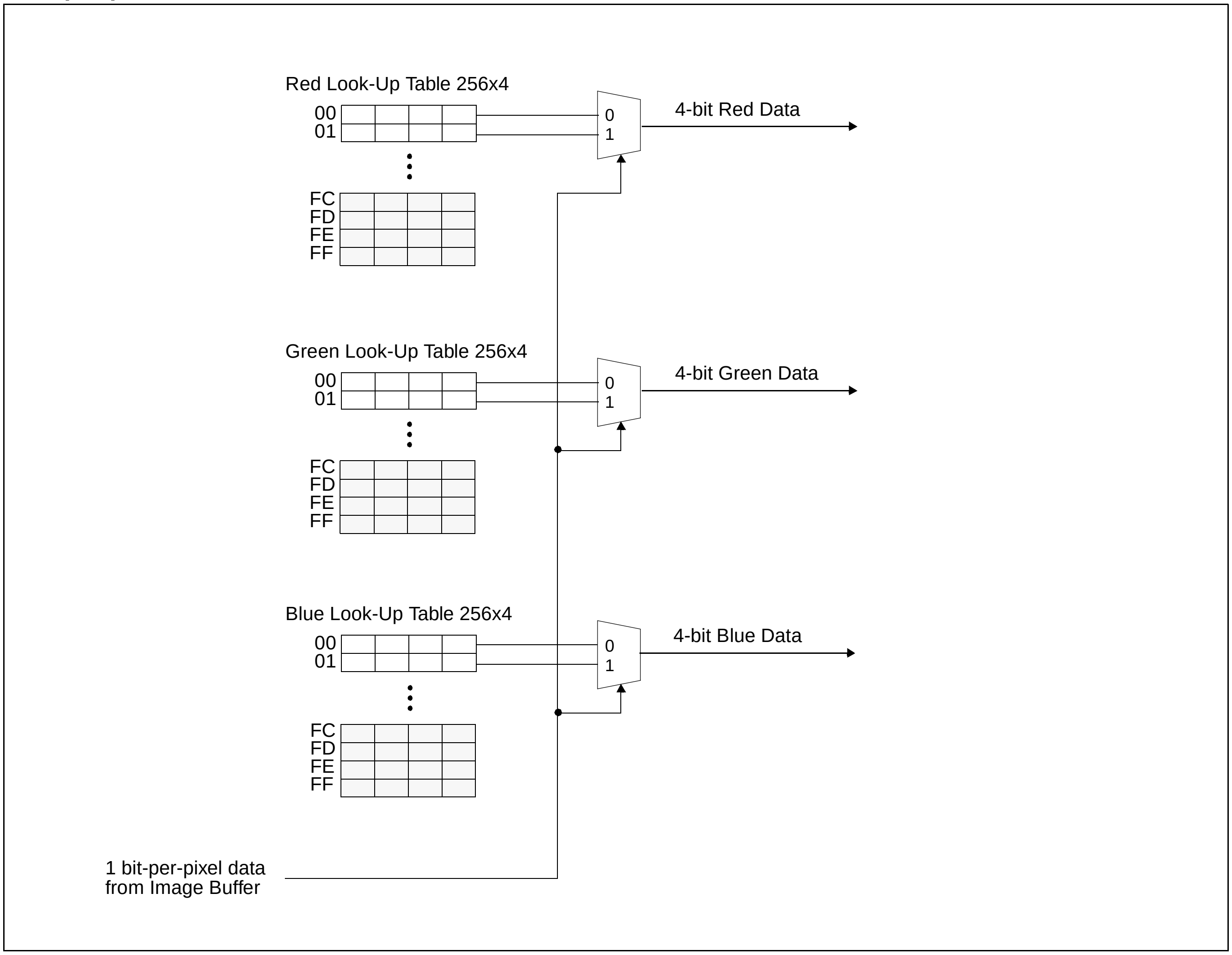


Figure 11-4: 1 Bit-per-pixel Color Mode Data Output Path

2 Bit-per-pixel Color Mode

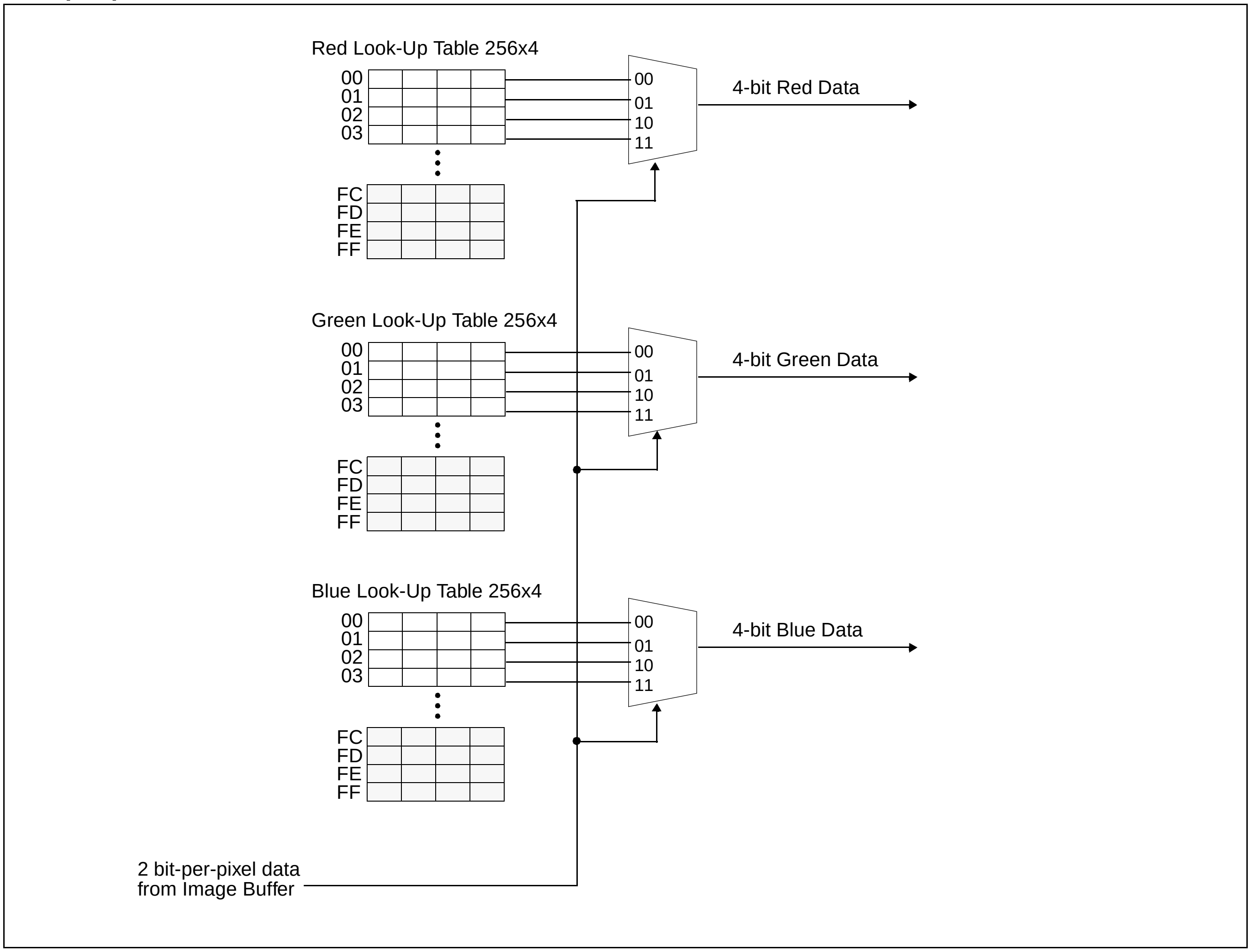


Figure 11-5: 2 Bit-per-pixel Color Mode Data Output Path

4 Bit-per-pixel Color Mode

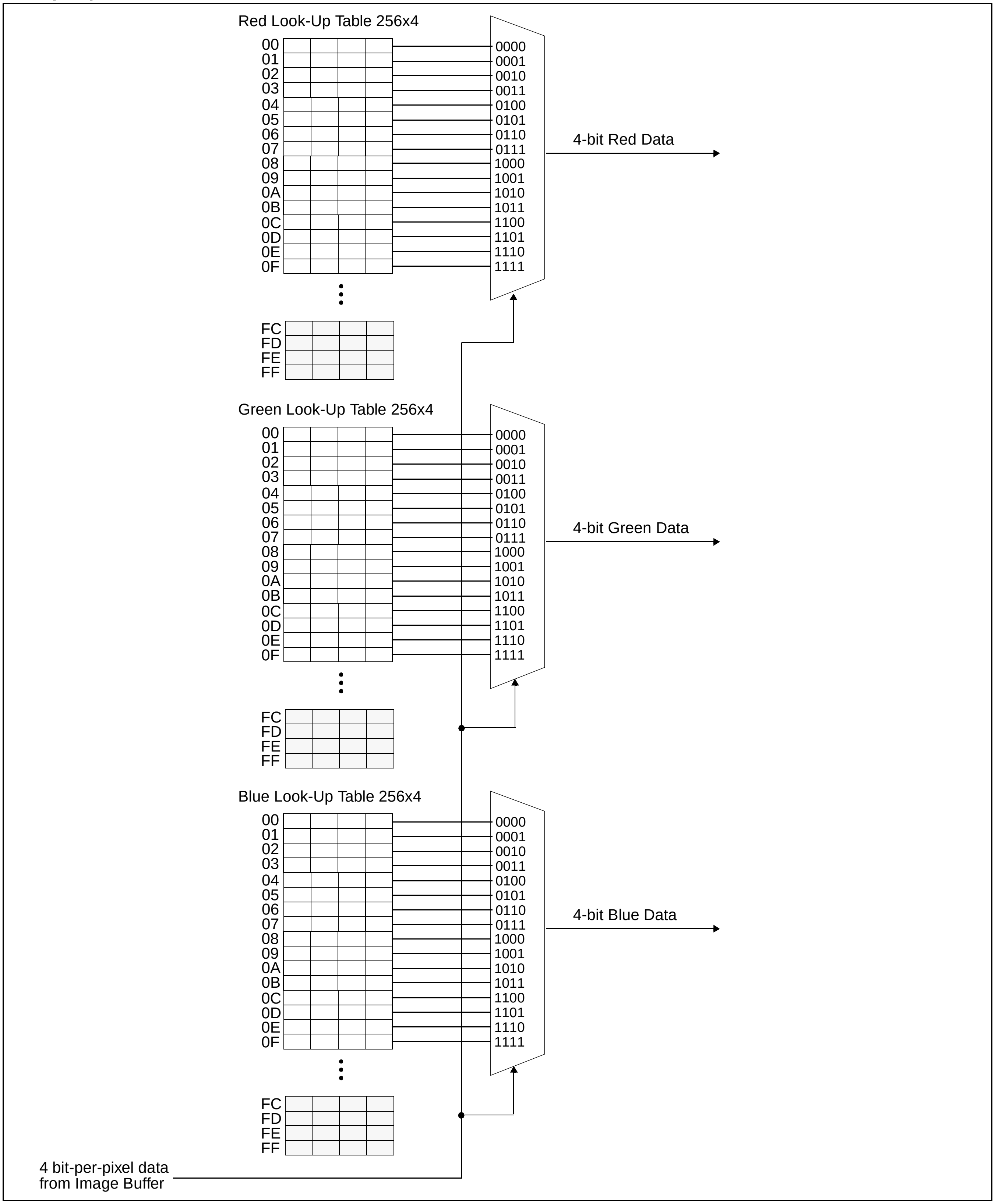


Figure 11-6: 4 Bit-per-pixel Color Mode Data Output Path

8 Bit-per-pixel Color Mode

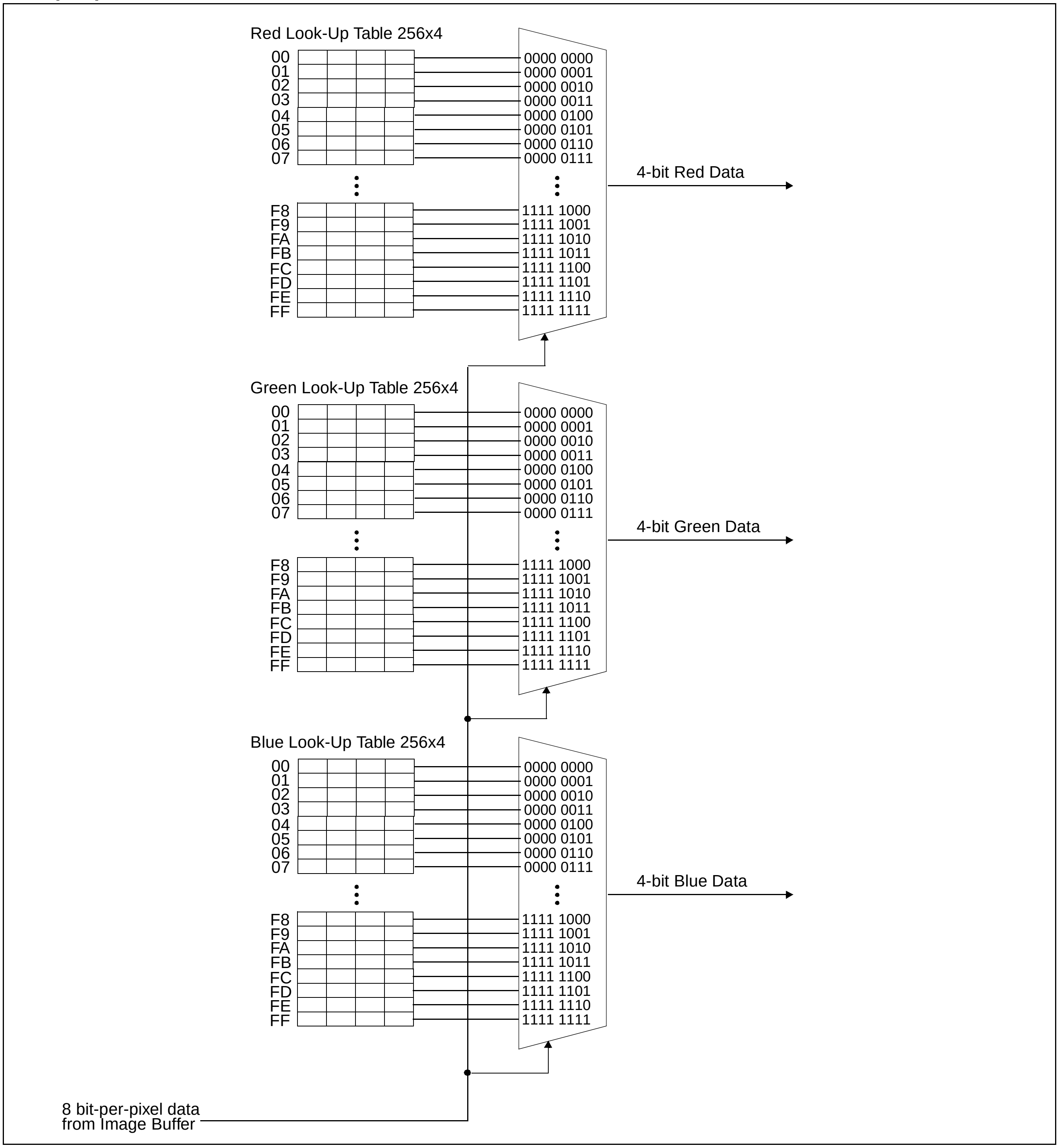


Figure 11-7: 8 Bit-per-pixel Color Mode Data Output Path

15/16 Bit-per-pixel Color Modes

The LUT is bypassed and the color data is directly mapped for this color mode – See “Display Configuration” on page 124.

12 Ink/Cursor Architecture

12.1 Ink/Cursor Buffers

The Ink/Cursor buffers contain formatted image data for the Ink Layer or Hardware Cursor. There may be several Ink/Cursor images stored in the display buffer but only one may be active at any given time.

The active Ink/Cursor buffer is selected by the Ink/Cursor Start Address register (REG[30h]). This register defines the start address for the active Ink/Cursor buffer. The Ink/Cursor buffer must be positioned where it does not conflict with the image buffer and half-frame buffer. The start address for the Ink/Cursor buffer is programmed as shown in the following table:

Table 12-1: Ink/Cursor Start Address Encoding

Ink/Cursor Start Address Bits [7:0]	Start Address (Bytes)	Comments
0	Display Buffer Size - 1024	This default value is suitable for a cursor when there is no half-frame buffer.
n = 255...1	Display Buffer Size - $(n \times 8192)$	These positions can be used to: • position an Ink buffer at the top of the display buffer; • position an Ink buffer between the image and half-frame buffers; • position a Cursor buffer between the image and half-frame buffers; • select from a multiple of Cursor buffers.

The Ink/Cursor image is stored contiguously. The address offset from the starting word of line *n* to the starting word of line *n+1* is calculated as follows:

Ink Address Offset (words) = REG[04h] + 1
Cursor Address Offset (words) = 8

12.2 Ink/Cursor Data Format

The Ink/Cursor image is always 2 bit-per-pixel. The following diagram shows the Ink/Cursor data format for a little-endian system.

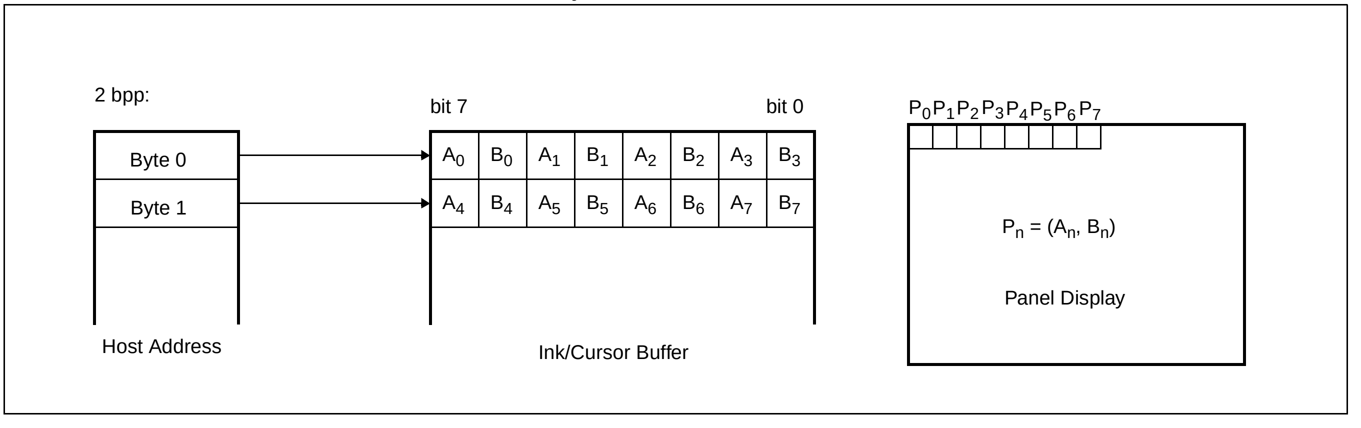


Figure 12-1: Ink/Cursor Data Format

The image data for pixel n, (A_n,B_n), selects the color for pixel n as follows:

Table 12-2: Ink/Cursor Color Select

(A_n,B_n)	**Color**	**Comments**
00	Color 0	Ink/Cursor Color 0 Register, (REG[2Dh],REG[2Ch])
01	Color 1	Ink/Cursor Color 1 Register, (REG[2Fh],REG[2Eh])
10	Background	Ink/Cursor is transparent – show background
11	Inverted Background	Ink/Cursor is transparent – show inverted background

12.3 Ink/Cursor Image Manipulation

12.3.1 Ink Image

The Ink image should always start at the top left pixel, i.e. Cursor X Position and Cursor Y Position registers should always be set to zero. The width and height of the ink image are automatically calculated to completely cover the display.

12.3.2 Cursor Image

The Cursor image size is always 64x64 pixels. The Cursor X Position and Cursor Y Position registers specify the position of the top left pixel. The following diagram shows how to position a cursor.

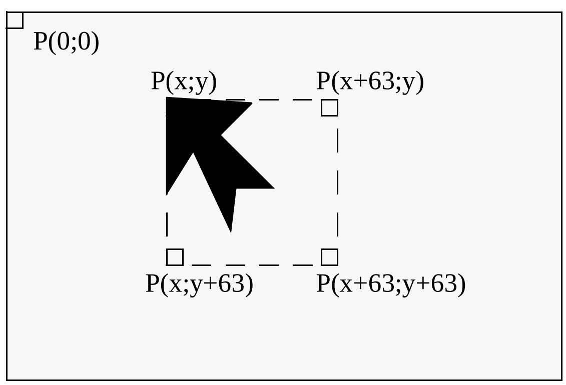


Figure 12-2: Cursor Positioning

where x = (REG[29h] bits [1:0], REG[28h]) REG[29h] bit 7 = 0
y = (REG[2Bh] bits [1:0], REG[2Ah]) REG[2Bh] bit 7 = 0

Note
There is no means to set a negative cursor position. If a cursor must be set to a negative position, this must be dealt with through software.

13 SwivelView™

13.1 Concept

Computer displays are refreshed in landscape – from left to right and top to bottom; computer images are stored in the same manner. When a display is used in SwivelView it becomes necessary to rotate the display buffer image by 90°. SwivelView rotates the image 90° clockwise as it is written to the display buffer. This rotation is done in hardware and is transparent to the programmer for all display buffer reads and writes.

SwivelView uses a 1024 × 1024 pixel virtual image. The following figures show how the programmer sees the image and how the image is actually stored in the display buffer. The display is refreshed in the following sense: C–A–D–B. The application image is written to the S1D13505 in the following sense: A–B–C–D. The S1D13505 rotates and stores the application image in the following sense: C–A–D–B, the same sense as display refresh.

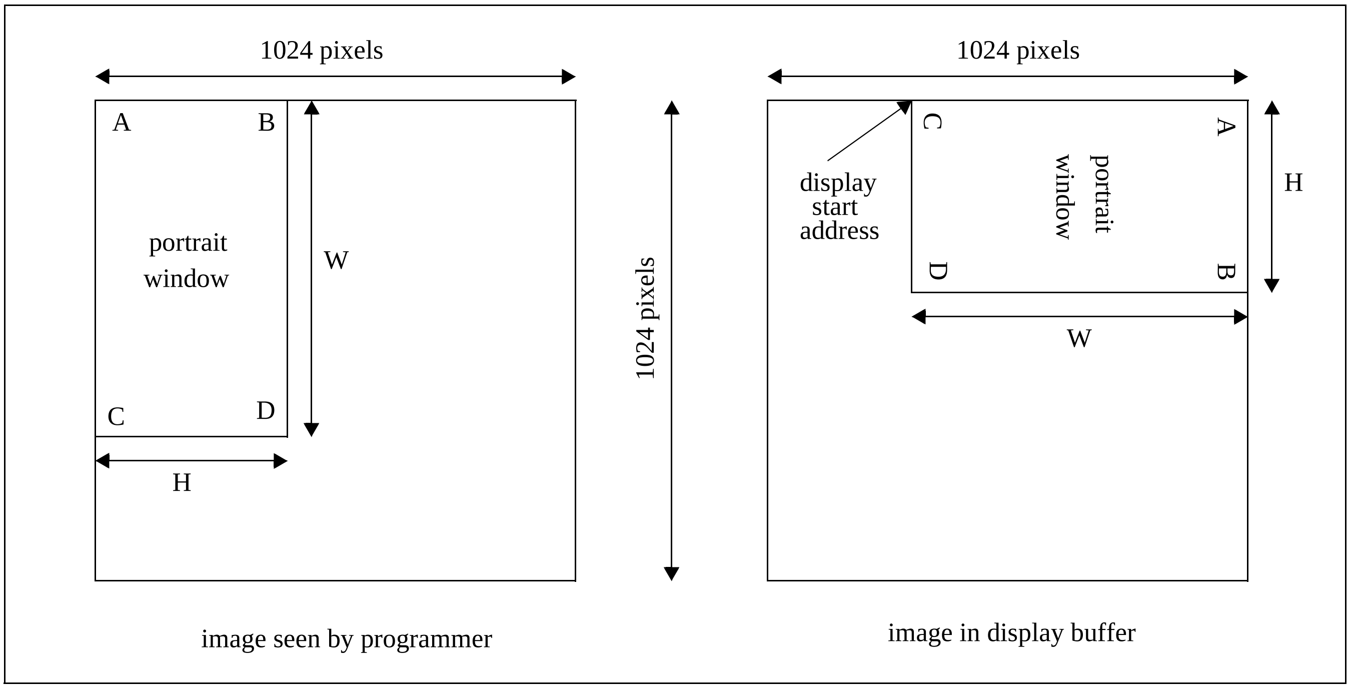


Figure 13-1: Relationship Between The Screen Image and the Image Residing in the Display Buffer

Note
The image must be written with a 1024 pixel offset between adjacent lines (e.g. 1024 bytes for 8 bpp mode or 2048 bytes for 16 bpp mode) and a display start address that is non-zero.

13.2 Image Manipulation in SwivelView

Display Start Address

It can be seen from Figure 13-1 that the top left pixel of the display is not at the top left corner of the virtual image, i.e. it is non-zero. The Display Start Address register must be set accordingly:

Display Start Address (words)	=(1024 - W)	for 16 bpp mode
	=(1024 - W) / 2	for 8 bpp mode

Memory Address Offset

The Memory Address Offset register must be set for a 1024 pixel offset:

Memory Address Offset (words)	=1024	for 16 bpp mode
	=512	for 8 bpp mode

Horizontal Panning

Horizontal panning is achieved by changing the start address. Panning of the portrait window to the right by 1 pixel is achieved by adding 1024 pixels to the Display Start Address register (or subtracting if panning to the left).

- Panning to right by 1 pixel: add current start address by 1024 (16 bpp mode) or 512 (8 bpp mode).
- Panning to left by 1 pixel: subtract current start address by 1024 (16 bpp mode) or 512 (8 bpp mode).

How far the portrait window can be panned to the right is limited not only by 1024 pixels but also by the amount of physical memory installed.

Vertical Scrolling

Vertical scrolling is achieved by changing the Display Start Address register and/or changing the Pixel Panning register.

- Increment/decrement Display Start Address register in 8 bpp mode: scroll down/up by 2 lines.
- Increment/decrement Display Start Address register in 16 bpp mode: scroll down/up by 1 line.
- Increment/decrement Pixel Panning register in 8 bpp or 16 bpp mode: scroll down/up by 1 line.

13.3 Physical Memory Requirement

Because the programmer must now deal with a virtual display, the amount of image buffer required for a particular display mode has increased. The minimum amount of image buffer required is:

Minimum Required Image Buffer (bytes)

$=(1024 \times H) \times 2$ for 16 bpp mode

$=(1024 \times H)$ for 8 bpp mode

For single panel, the required display buffer size is the same as the image buffer required. For dual panel, the display buffer required is the sum of the image buffer required and the half-frame buffer memory required. The half-frame buffer memory requirement is:

Half-Frame Buffer Memory (bytes)

$=(W \times H) / 4$ for color mode

$=(W \times H) / 16$ for monochrome mode

The half-frame buffer memory is always located at the top of the physical memory.

For simplicity the hardware cursor and ink layer memory requirement is ignored. The hardware cursor and ink layer memory must be located at 16K byte boundaries and it must not overlap the image buffer and half-frame buffer memory areas.

Even though the virtual display is 1024×1024 pixels, the actual panel window is always smaller. Thus it is possible for the display buffer size to be smaller than the virtual display but large enough to fit both the required image buffer and the half-frame buffer memory. This poses a maximum "accessible" horizontal virtual size limit.

Maximum Accessible Horizontal Virtual Size (pixels)

= (Physical Memory – Half-Frame Buffer Memory) / 2048 for 16 bpp mode

= (Physical Memory – Half-Frame Buffer Memory) / 1024 for 8 bpp mode

For example, a 640×480 single panel running 8 bpp mode requires 480K byte of image buffer and 0K byte of half-frame buffer memory. The virtual display size is 1024×1024 = 1M byte. The programmer may use a 512K byte DRAM which is smaller than the 1M byte virtual display but greater than the 480K byte minimum required image buffer. The maximum accessible horizontal virtual size is = (512K byte - 0K byte) / 1024 = 512. The programmer therefore has room to pan the portrait window to the right by 512 - 480 = 32 pixels. The programmer also should not read/write to the memory beyond the maximum accessible horizontal virtual size because that memory is either reserved for the half-frame buffer or not associated with any real memory at all.

The following table summarizes the DRAM size requirement for SwivelView using different panel sizes and display modes. Note that DRAM size for the S1D13505 is limited to either 512K byte or 2M byte. The calculation is based on the minimum required image buffer size. The calculated minimum display buffer size is based on the image buffer and the half-frame buffer only; it does not take into account the hardware cursor/ink layer and so it may or may not be sufficient to support it – this is noted in the table. The hardware cursor requires 1K byte of memory and the 2-bit ink layer requires $(W \times H) / 4$ bytes of memory; both must reside at 16K byte boundaries but only one is supported at a time. The table shows only one possible sprite/ink layer location – at the highest possible 16K byte boundary below the half-frame buffer which is always at the top.

Table 13-2 Minimum DRAM Size Required for SwivelView

<table>
<tr><th>Panel Size</th><th colspan="2">Panel Type</th><th>Display Mode</th><th>Display Buffer Size</th><th>Half-Frame Buffer Size</th><th>Minimum DRAM Size</th><th>Sprite/Ink Layer Buffer Size</th><th>Ink/Cursor Layer Location</th></tr>
<tr><td rowspan="8">320 × 240</td><td rowspan="4">Single</td><td rowspan="2">Color</td><td>8 bpp</td><td>240KB</td><td rowspan="4">0KB</td><td rowspan="9">512KB</td><td rowspan="8">1KB/18.75KB</td><td rowspan="4">496KB/ 480KB</td></tr>
<tr><td>16 bpp</td><td>480KB</td></tr>
<tr><td rowspan="2">Mono</td><td>8 bpp</td><td>240KB</td></tr>
<tr><td>16 bpp</td><td>480KB</td></tr>
<tr><td rowspan="4">Dual</td><td rowspan="2">Color</td><td>8 bpp</td><td>240KB</td><td rowspan="2">18.75KB</td><td>480KB/464KB</td></tr>
<tr><td>16 bpp</td><td>480KB</td><td>480KB/--</td></tr>
<tr><td rowspan="2">Mono</td><td>8 bpp</td><td>240KB</td><td rowspan="2">4.69KB</td><td rowspan="2">496KB/480KB</td></tr>
<tr><td>16 bpp</td><td>480KB</td></tr>
<tr><td rowspan="8">640 × 480</td><td rowspan="4">Single</td><td rowspan="2">Color</td><td>8 bpp</td><td>480KB</td><td rowspan="4">0KB</td><td rowspan="8">1KB/75KB</td><td>496KB/--</td></tr>
<tr><td>16 bpp</td><td>960KB</td><td>2MB</td><td>2032KB/1968KB</td></tr>
<tr><td rowspan="2">Mono</td><td>8 bpp</td><td>480KB</td><td>512KB</td><td>496KB/--</td></tr>
<tr><td>16 bpp</td><td>960KB</td><td rowspan="3">2MB</td><td rowspan="3">2032K/1968K</td></tr>
<tr><td rowspan="4">Dual</td><td rowspan="2">Color</td><td>8 bpp</td><td>480KB</td><td rowspan="2">75KB</td></tr>
<tr><td>16 bpp</td><td>960KB</td></tr>
<tr><td rowspan="2">Mono</td><td>8 bpp</td><td>480KB</td><td rowspan="2">18.75KB</td><td>512KB</td><td>496KB/--</td></tr>
<tr><td>16 bpp</td><td>960KB</td><td rowspan="9">2MB</td><td>2032KB/1968KB</td></tr>
<tr><td rowspan="8">800 × 600</td><td rowspan="4">Single</td><td rowspan="2">Color</td><td>8 bpp</td><td>600KB</td><td rowspan="4">0KB</td><td rowspan="8">1KB/
117.19KB</td><td rowspan="8">2032KB/1920KB</td></tr>
<tr><td>16 bpp</td><td>1.2MB</td></tr>
<tr><td rowspan="2">Mono</td><td>8 bpp</td><td>600KB</td></tr>
<tr><td>16 bpp</td><td>1.2MB</td></tr>
<tr><td rowspan="4">Dual</td><td rowspan="2">Color</td><td>8 bpp</td><td>600KB</td><td rowspan="2">117.19KB</td></tr>
<tr><td>16 bpp</td><td>1.2MB</td></tr>
<tr><td rowspan="2">Mono</td><td>8 bpp</td><td>600KB</td><td rowspan="2">29.30KB</td></tr>
<tr><td>16 bpp</td><td>1.2MB</td></tr>
</table>

Where KB = K bytes and MB = 1024K bytes

13.4 Limitations

The following limitations apply to SwivelView:

- Only 8 bpp and 16 bpp modes are supported – 1/2/4 bpp modes are not supported.
- Hardware cursor and ink layer images are not rotated – software rotation must be used. SwivelView must be turned off when the programmer is accessing the sprite or the ink layer.
- Split screen images appear side-by-side, i.e. the portrait display is split vertically.
- Pixel panning works vertically.

14 Clocking

14.1 Maximum MCLK: PCLK Ratios

Table 14-1: Maximum PCLK Frequency with EDO-DRAM

Ink	Display type	N_{RC}	Maximum PCLK Allowed				
			1 bpp	**2 bpp**	**4 bpp**	**8 bpp**	**16 bpp**
off	• Single Panel. • CRT. • Dual Monochrome/Color Panel with Half Frame Buffer Disabled. • Simultaneous CRT + Single Panel. • Simultaneous CRT + Dual Monochrome/Color Panel with Half Frame Buffer Disabled.	5, 4, 3	MCLK				
	• Dual Monochrome Panel with Half Frame Buffer Enabled. • Simultaneous CRT + Dual Monochrome Panel with Half Frame Buffer Enable.	5	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
		4	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
		3	MCLK	MCLK	MCLK/2	MCLK/2	MCLK/2
	• Dual Color Panel with Half Frame Buffer Enabled. • Simultaneous CRT + Dual Color Panel with Half Frame Buffer Enable.	5	MCLK/2	MCLK/2	MCLK/2	MCLK/3	MCLK/3
		4	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
		3	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
on	• Single Panel. • CRT. • Dual Monochrome/Color Panel with Half Frame Buffer Disabled. • Simultaneous CRT + Single Panel. • Simultaneous CRT + Dual Monochrome/Color Panel with Half Frame Buffer Disabled.	5	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
		4	MCLK	MCLK	MCLK/2	MCLK/2	MCLK/2
		3	MCLK	MCLK	MCLK	MCLK/2	MCLK/2
	• Dual Monochrome Panel with Half Frame Buffer Enabled. • Simultaneous CRT + Dual Monochrome Panel with Half Frame Buffer Enable.	5	MCLK/2	MCLK/3	MCLK/3	MCLK/3	MCLK/3
		4	MCLK/2	MCLK/2	MCLK/2	MCLK/3	MCLK/3
		3	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
	• Dual Color Panel with Half Frame Buffer Enabled. • Simultaneous CRT + Dual Color Panel with Half Frame Buffer Enable.	5	MCLK/3	MCLK/3	MCLK/3	MCLK/3	MCLK/4
		4	MCLK/2	MCLK/2	MCLK/3	MCLK/3	MCLK/3
		3	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3

Table 14-2: Maximum PCLK Frequency with FPM-DRAM

Ink	Display type	N_{RC}	Maximum PCLK allowed				
			1 bpp	**2 bpp**	**4 bpp**	**8 bpp**	**16 bpp**
off	• Single Panel. • CRT. • Dual Monochrome/Color Panel with Half Frame Buffer Disabled. • Simultaneous CRT + Single Panel. • Simultaneous CRT + Dual Monochrome/Color Panel with Half Frame Buffer Disabled.	5, 4, 3	MCLK				
	• Dual Monochrome with Half Frame Buffer Enabled. • Simultaneous CRT + Dual Monochrome Panel with Half Frame Buffer Enable.	5	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
		4	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/2
		3	MCLK	MCLK	MCLK	MCLK/2	MCLK/2
	• Dual Color with Half Frame Buffer Enabled. • Simultaneous CRT + Dual Color Panel with Half Frame Buffer Enable.	5	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
		4	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
		3	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/2
on	• Single Panel. • CRT. • Dual Monochrome/Color Panel with Half Frame Buffer Disabled. • Simultaneous CRT + Single Panel. • Simultaneous CRT + Dual Monochrome/Color Panel with Half Frame Buffer Disabled.	5	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
		4	MCLK	MCLK	MCLK/2	MCLK/2	MCLK/2
		3	MCLK	MCLK	MCLK	MCLK/2	MCLK/2
	• Dual Monochrome with Half Frame Buffer Enabled. • Simultaneous CRT + Dual Monochrome Panel with Half Frame Buffer Enable.	5	MCLK/2	MCLK/2	MCLK/3	MCLK/3	MCLK/3
		4	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
		3	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3
	• Dual Color with Half Frame Buffer Enabled. • Simultaneous CRT + Dual Color Panel with Half Frame Buffer Enable.	5	MCLK/3	MCLK/3	MCLK/3	MCLK/3	MCLK/4
		4	MCLK/2	MCLK/2	MCLK/2	MCLK/3	MCLK/3
		3	MCLK/2	MCLK/2	MCLK/2	MCLK/2	MCLK/3

14.2 Frame Rate Calculation

The frame rate is calculated using the following formula:

$$\text{FrameRate} = \frac{PCLK_{max}}{(HDP + HNDP) \times (VDP + VNDP)}$$

Where:

VDP	= Vertical Display Period	= REG[09h] bits [1:0], REG[08h] bits [7:0] + 1
VNDP	= Vertical Non-Display Period	= REG[0Ah] bits [5:0] + 1 = in table below
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1) * 8Ts
HNDP	= Horizontal Non-Display Period	= ((REG[05h] bits [4:0]) + 1) * 8Ts = given in table below
Ts	= Pixel Clock	= PCLK

Table 14-3: Example Frame Rates with Ink Disabled

DRAM Type[1] (Speed Grade)	Display	Resolution	Color Depth (bpp)	Maximum Pixel Clock (MHz)	Minimum Panel HNDP(T_s)	Maximum Frame Rate (Hz)	
						Panel[4]	CRT
50ns EDO-DRAM MClk = 40MHz N_{RC} = 4 N_{RP} = 1.5 N_{RCD} = 2	• Single Panel. • CRT. • Dual Monochrome/Color Panel with Half Frame Buffer Disabled.[5] • Simultaneous CRT + Single Panel. • Simultaneous CRT + Dual Monochrome/Color Panel with Half Frame Buffer Disabled.[5]	800x600[2]	1/2/4/8	40	32	80	60
			15/16[6]		56	78	60
		640x480	1/2/4/8		32	123	85
			15/16		56	119	85
		640x240	1/2/4/8		32	247	-
			15/16		56	242	-
		480x320	1/2/4/8		32	243	-
			15/16		56	232	-
		320x240	1/2/4/8		32	471	-
			15/16		56	441	-
	• Dual Color with Half Frame Buffer Enabled. • Dual Mono with Half Frame Buffer Enabled.	800x600[2,3]	1/2/4/8	20	32	80	-
			15/16[6]	13.3	32	53	-
		640x480	1/2/4/8	20	32	123	-
			15/16	13.3	32	82	-

Table 14-3: Example Frame Rates with Ink Disabled (Continued)

DRAM Type[1] (Speed Grade)	Display	Resolution	Color Depth (bpp)	Maximum Pixel Clock (MHz)	Minimum Panel HNDP(T_S)	Maximum Frame Rate (Hz)	
						Panel[4]	CRT
60ns EDO-DRAM MClk = 33MHz N_{RC} = 4 N_{RP} = 1.5 N_{RCD} = 2	• Single Panel. • CRT. • Dual Mono/Color Panel with Half Frame Buffer Disabled.[5] • Simultaneous CRT + Single Panel. • Simultaneous CRT + Dual Mono/Color Panel with Half Frame Buffer Disabled.[5]	800x600[2]	1/2/4/8	33	32	66	55
			15/16[6]		56	65	55
		640x480	1/2/4/8		32	101	78
			15/16		56	98	78
		640x240	1/2/4/8		32	203	-
			15/16		56	200	-
		480x320	1/2/4/8		32	200	-
			15/16		56	196	-
		320x240	1/2/4/8		32	388	-
			15/16		56	380	-
	• Dual Color with Half Frame Buffer Enabled. • Dual Mono with Half Frame Buffer Enabled.	800x600[2,3]	1/2/4/8	16.5	32	66	-
			15/16[6]	11	32	43	-
		640x480	1/2/4/8	16.5	32	103	-
			15/16	11	32	68	-
60ns FPM-DRAM MClk = 25MHz N_{RC} = 4 N_{RP} = 1.5 N_{RCD} = 2	• Single Panel. • CRT. • Dual Mono/Color Panel with Half Frame Buffer Disabled.[5] • Simultaneous CRT + Single Panel. • Simultaneous CRT + Dual Mono/Color Panel with Half Frame Buffer Disabled.[5]	800x600[2]	1/2/4/8	25	32	50	-
			15/16[6]		56	48	-
		640x480	1/2/4/8		32	77	60
			15/16		56	75	60
		640x240	1/2/4/8		32	142	-
			15/16		56	136	-
		480x320	1/2/4/8		32	152	-
			15/16		56	145	-
		320x240	1/2/4/8		32	294	-
			15/16		56	280	-
	• Dual Mono with Half Frame Buffer Enabled.	800x600[2]	1/2/4/8/15/16[6]	12.5	32	50	-
		640x480	1/2/4/8/15/16	12.5	32	77	-
		640x400	1/2/4/8/15/16	12.5	32	92	-
	• Dual Color with Half Frame Buffer Enabled.	800x600[2,3]	1/2/4/8	12.5	32	50	-
			15/16[6]	8.33	32	33	-
		640x480	1/2/4/8	12.5	32	77	-
			15/16	8.33	32	51	-

1. Must set N_{RC} = 4MCLK. See REG[22h], Performance Enhancement Register.
2. 800x600 @ 16 bpp requires 2M bytes of display buffer for all display types.
3. 800x600 @ 8 bpp on a dual color panel requires 2M bytes of display buffer if the half frame buffer is enabled.

4. Optimum frame rates for panels range from 60Hz to 150Hz. If the maximum refresh rate is too high for a panel, MCLK should be reduced or PCLK should be divided down.

5. Half Frame Buffer disabled by REG[1Bh] bit 0.

6. When setting a horizontal resolution greater than 767 pixels, with a color depth of 15/16 bpp, the Memory Offset Registers (REG[16h], REG[17h]) must be set to a virtual horizontal pixel resolution of 1024.

14.3 Bandwidth Calculation

When calculating the average bandwidth, there are two periods that must be calculated separately.

The first period is the time when the CPU is in competition with the display refresh fetches. The CPU can only access the memory when the display refresh releases the memory controller. The CPU bandwidth during this period is called the “bandwidth during display period”.

The second period is the time when the CPU has full access to the memory, with no competition from the display refresh. The CPU bandwidth during this period is called the “bandwidth during non display period.”

To calculate the average bandwidth, calculate the percentage of time between display period and non display period. The percentage of display period is multiplied with the bandwidth during display period. The percentage of non display period is multiplied with the bandwidth during non display period. The two products are summed to provide the average bandwidth.

Bandwidth during non display period

Based on simulation, it requires a minimum of 12 MCLKs to service one, two byte, CPU access to memory. This includes all the internal handshaking and assumes that N_{RC} is set to 4MCLKs and the wait state bits are set to 10b.

Bandwidth during non display period = f(MCLK) / 6 Mb/s

Bandwidth during display period

The amount of time taken up by display refresh fetches is a function of the color depth, and the display type. Below is a table of the number of MCLKs required for various memory fetches to display 16 pixels. Assuming N_{RC} = 4MCLKs.

Table 14-4: Number of MCLKs required for various memory access

Memory access	Number of MCLKs
Half Frame Buffer, monochrome	7
Half Frame Buffer, color	11
Display @ 1 bpp	4
Display @ 2 bpp	5
Display @ 4 bpp	7
Display @ 8 bpp	11
Display @ 16 bpp	19
CPU	4

Table 14-5: Total # MCLKs taken for Display refresh

Display	MCLKs for Display Refresh				
	1 bpp	2 bpp	4 bpp	8 bpp	16 bpp
• Single Panel. • CRT. • Dual Monochrome/Color Panel with Half Frame Buffer Disabled. • Simultaneous CRT + Single Panel. • Simultaneous CRT + Dual Monochrome/Color Panel with Half Frame Buffer Disabled.	4	5	7	11	19
• Dual Monochrome Panel with Half Frame Buffer Enabled. • Simultaneous CRT + Dual Monochrome Panel with Half Frame Buffer Enable.	11	12	14	18	26
• Dual Color Panel with Half Frame Buffer Enabled.	15	16	18	22	30

Bandwidth during display period = MIN (bandwidth during non display period, B/C/D)
where B = number of MCLKs left available for CPU access after every 16 pixels drawn
= (f(MCLK)/f(PCLK) * 16 - Total MCLK for Display refresh), units in MCLKs 16 pixels
where C = number of MCLKs required to service 1 CPU access (2 bytes of data)
= 4, units in MCLKs/2 bytes
where D = time to draw 16 pixels
= 16 / f(PCLK), units in 16 pixels

The minimum function limits the bandwidth to the bandwidth available during non display period should the display fetches constitute a small percentage of the overall memory activity.

For 16 bpp single panel/CRT/dual panel with half frame buffer disable, the number of MCLKs required to fetch 16 pixels when PCLK = MCLK exceeds 16. In this case, the display fetch does not allow any CPU access during the display period. CPU access can only be achieved during non display periods.

Average Bandwidth

All displays have a horizontal non display period, and a vertical non display period. The formula for calculating the percentage of non display period is as follows

Percentage of non display period = (HTOT * VTOT - WIDTH * HEIGHT)/(HTOT * VTOT)

Percentage of non display period for CRT = (800*525 - 640*480)/(800*525) = 26.6%

Percentage of non display period for single panel = (680*482 - 640*480)/680*482) = 6.2%

Percentage of non display period for dual panel = (680*242 - 640*240)/680*242) = 6.6%

Average Bandwidth =
Percentage of non display period * Bandwidth during non display period +
(1- Percentage of non display period) * Bandwidth during display period

Table 14-6: Theoretical Maximum Bandwidth M byte/sec, Cursor/Ink disabled

DRAM Type[1] (Speed Grade)	640x480 Display	Max. Pixel Clock (MHz)	Maximum Bandwidth (M byte/sec)				
			1 bpp	2 bpp	4 bpp	8 bpp	16 bpp
50ns EDO-DRAM MCLK = 40MHz	• CRT. • Simultaneous CRT + Single Panel. • Simultaneous CRT + Dual Monochrome/Color Panel with Half Frame Buffer Disabled.	40	6.67	6.67	6.67	6.36	1.79
	• Single Panel.	40	6.67	6.67	6.60	6.27	0.41
	• Dual Monochrome/Color Panel with Half Frame Buffer Disabled.	20	6.67	6.67	6.67	6.67	6.67
	• Dual Monochrome Panel with Half Frame Buffer Enabled.	40	6.27	5.11	-	-	-
		20	6.67	6.67	6.67	6.67	3.94
		13.3	6.67	6.67	6.67	6.67	6.67
	• Simultaneous CRT + Dual Mono Panel with Half Frame Buffer Enable.	40	6.36	5.44	-	-	-
	• Dual Color Panel with Half Frame Buffer Enabled.	20	6.67	6.67	6.27	6.27	-
		13.3	6.67	6.67	6.67	6.67	6.67
60ns EDO-DRAM MCLK = 33MHz	• CRT. • Simultaneous CRT + Single Panel. • Simultaneous CRT + Dual Monochrome/Color Panel with Half Frame Buffer Disabled.	33	5.5	5.5	5.5	5.24	1.47
	• Single Panel.	33	5.5	5.5	5.5	5.17	0.34
	• Dual Monochrome/Color Panel with Half Frame Buffer Disabled.	16.5	5.5	5.5	5.5	5.5	5.5
	• Dual Monochrome Panel with Half Frame Buffer Enabled.	33	5.17	4.21	-	-	-
		16.5	5.5	5.5	5.5	5.5	3.25
		11	5.5	5.5	5.5	5.5	5.5
	• Simultaneous CRT + Dual Monochrome Panel with Half Frame Buffer Enable.	33	5.24	4.49	-	-	-
	• Dual Color Panel with Half Frame Buffer Enabled.	16.5	5.5	5.5	5.5	5.17	-
		11	5.5	5.5	5.5	5.5	5.5

Table 14-6: Theoretical Maximum Bandwidth M byte/sec, Cursor/Ink disabled (Continued)

DRAM Type[1] (Speed Grade)	640x480 Display	Max. Pixel Clock (MHz)	Maximum Bandwidth (M byte/sec)				
			1 bpp	2 bpp	4 bpp	8 bpp	16 bpp
60ns FPM-DRAM MCLK = 25MHz	• CRT. • Simultaneous CRT + Single Panel. • Simultaneous CRT + Dual Monochrome/Color Panel with Half Frame Buffer Disabled.	25	4.16	4.16	4.16	3.97	1.11
	• Single Panel. • Dual Monochrome/Color Panel with Half Frame Buffer Disabled.	25	4.16	4.16	4.16	3.92	0.26
		12.5	4.16	4.16	4.16	4.16	4.16
	• Dual Monochrome with Half Frame Buffer Enabled.	25	3.92	3.19	-	-	-
		12.5	4.16	4.16	4.16	4.16	2.46
		8.3	4.16	4.16	4.16	4.16	4.16
	• Simultaneous CRT + Dual Monochrome Panel with Half Frame Buffer Enable.	25	3.97	3.40	-	-	-
	• Dual Color Panel with Half Frame Buffer Enabled.	12.5	4.16	4.16	4.16	3.92	-
		8.33	4.16	4.16	4.16	4.16	4.16

15 Power Save Modes

Three power save modes are incorporated into the S1D13505 to meet the important need for power reduction in the hand-held device market.

Table 15-1: Power Save Mode Function Summary

Function	Power Save Mode (PSM)			
	Normal (Active)	**No Display LCDEnable = 0 CRTEnable = 0**	**Software Suspend**	**Hardware Suspend**
Display Active?	Yes	No	No	No
Register Access Possible?	Yes	Yes	Yes	No
Memory Access Possible?	Yes	Yes	No	No
LUT Access Possible?	Yes	Yes	Yes	No

Table 15-2: Pin States in Power-save Modes

Pins	Pin State			
	Normal (Active)	**No Display LCDEnable = 0 CRTEnable = 0**	**Software Suspend**	**Hardware Suspend**
LCD outputs	Active (LCDEnable = 1)	Forced Low[2]	Forced Low[2]	Forced Low[2]
LCDPWR	On (LCDEnable = 1)	Off	Off	Off
DRAM outputs	Active	CBR Refresh only	Refresh Only[1]	Refresh Only[1]
CRT/DAC outputs	Active (CRTEnable = 1)	Disabled	Disabled	Disabled
Host Interface outputs	Active	Active	Active	Disabled

1. Refresh method is selectable by REG[1Ah]. Supported methods are CBR refresh, self-refresh or no refresh at all.

2. The FPFRAME and FPLINE signals are set to their inactive states during power-down. The inactive states are determined by REG[07h] bit 6 and REG[0Ch] bit 6. A problem may occur if the inactive state is high (typical TFT/D-TFD configuration) and power is removed from the LCD panel.

   For software suspend the problem can be solved in the following manner. At power-down, first enable software suspend, then wait ~120 VNDP, and lastly reverse the polarity bits. At power-up, first disable software suspend, then revert the polarity bits back to the configuration state.

   For hardware suspend an external hardware solution would be to use an AND gate on the sync signal. One input of the AND gate is connected to a sync signal, the other input would be tied to the panel's logic power supply. When the panel's logic power supply is removed, the sync signal is forced low.

16 Mechanical Data

128-pin QFP15 surface mount package

Unit: mm

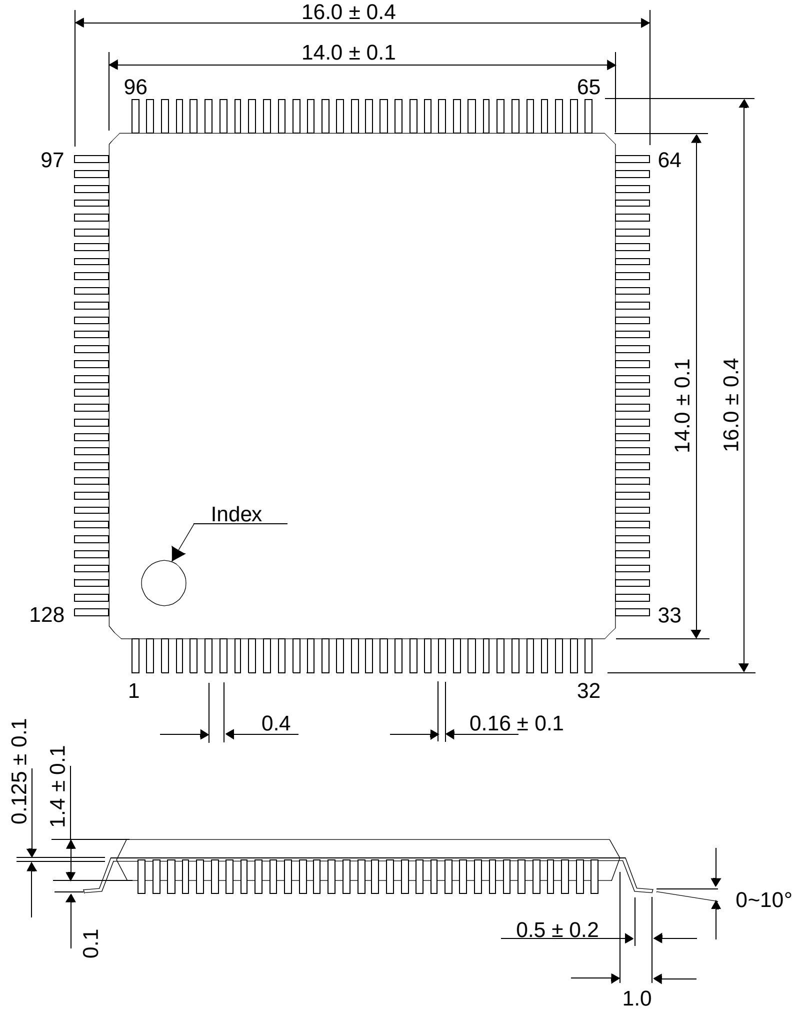


Figure 16-1: Mechanical Drawing QFP15