



LCD Module Technical Specification

First Edition
Jan 1, 2001
Final Revision

T-51381L064J-FW-P-AA

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Revision History

Rev.	Date	Page	Comment

1. Application

This technical specification applies to 6.4" color TFT-LCD module. The applications of the panel are car TV, portable TV, multimedia applications and others AV system.

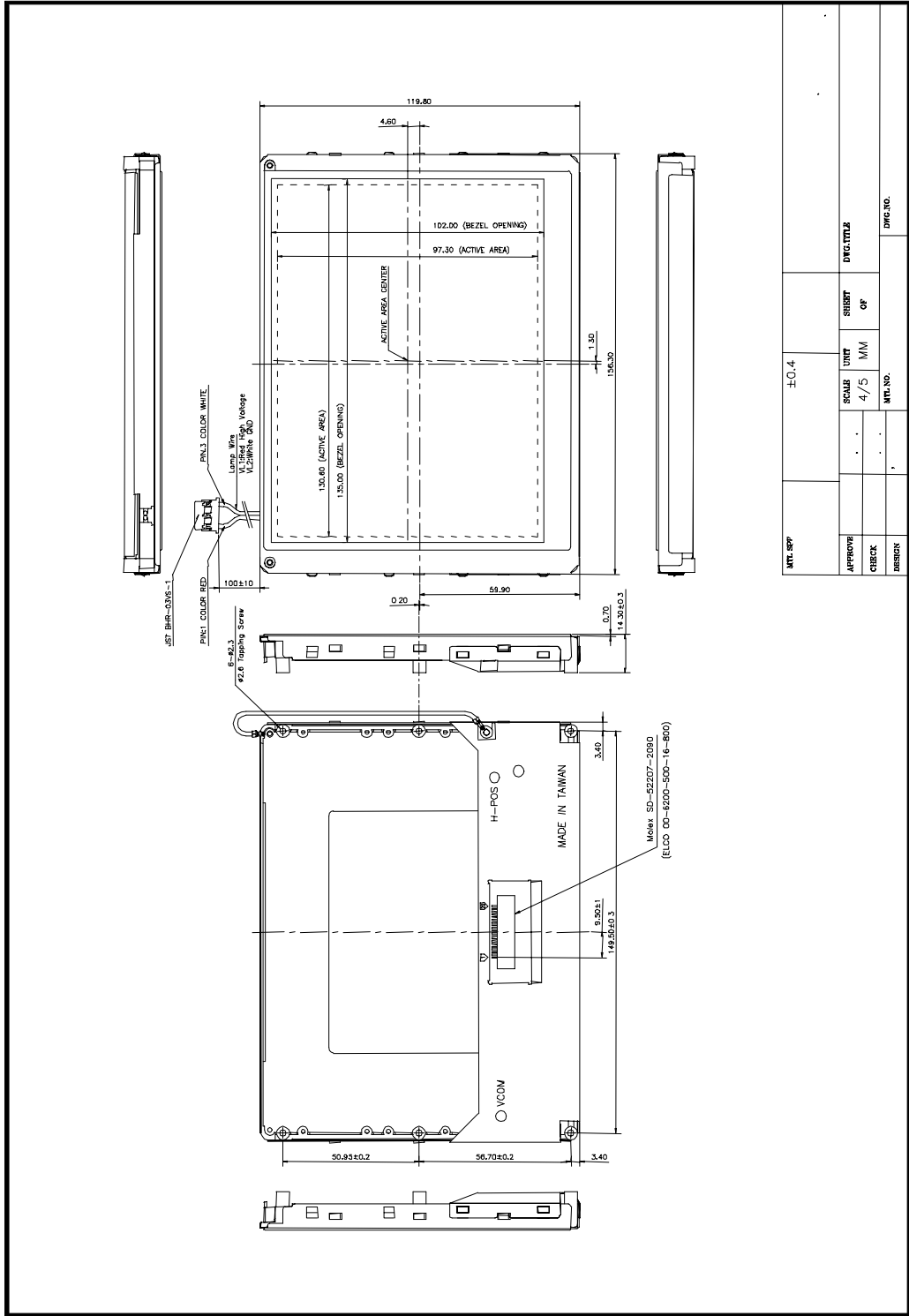
2. Features

- . Compatible with NTSC and PAL system
- . Pixel in stripe configuration
- . Slim and compact
- . High Brightness
- . Optimum Viewing Direction : 6 o'clock
- . Image Reversion : Up/Down and Left/Right

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	6.4 (diagonal)	inch
Display Format	960 x 234	dot
Active Area	130.6 (H) x 97.3 (V)	mm
Dot Pitch	0.136 (H) x 0.416 (V)	mm
Pixel Configuration	Stripe	
Outline Dimension	156.3 (W) x 119.8 (H) x 14.3 (D)	mm
Weight	280±5	g

4. Mechanical Drawing of TFT-LCD Module



MTL:SPF	±0.4						
APPROVE	SCALE	UNIT	SHEET	DWG. TITLE			
CHECK	4/5	MM	OF				
DESIGN					MTL NO.	DWG. NO.	

5. Input / Output Terminals

5-1) TFT-LCD Panel Driving

Pin No	Symbol	I/O	Description	Remark
1	$\overline{\text{HSY}}$	I/O	Horizontal Sync. Input / Output	Note 5-1
2	FRP	O	Video Polarity Alternating Signal	
3	CSY	I	Composite Sync. Signal	Note 5-1
4	V _{GH}	I	Supply Voltage for Gate Driver (Hi level)	Note 5-3
5	V _{GL}	I	Supply Voltage for Gate Driver (Low level)	Note 5-4
6	V _B	I	Video Signal (Blue)	
7	V _R	I	Video Signal (Red)	
8	V _G	I	Video Signal (Green)	
9	GND	I	Ground	
10	V _{DD}	I	Supply voltage for Controller	Note 5-5
11	V _{SH}	I	Supply voltage for source driver	Note 5-6
12	GND	I	Ground	
13	CKC	I	Control pin for select I/O signal	Note 5-1, 5-2
14	$\overline{\text{VSY}}$	I/O	Vertical Sync. Input/ Output	Note 5-1
15	PSI	O	Synchronize Pulse for Decoder	Note 5-7
16	PSC	O	Synchronize Pulse for DC-DC Converter	Note 5-8
17	VIY	I	Vertical Sync. Input Pin for reset Vertical Counter	
18	UD	I	UP/DOWN Control	Note 5-10
19	RL	I	Right/Left Shift Control	Note 5-9
20	NP	I	NTSC/PAL Input	Note 5-11

Note 5-1 : Pin 13 (CKC) can select the function for Pin 1 ($\overline{\text{HSY}}$), Pin 3 (CSY), and Pin 14 ($\overline{\text{VSY}}$).

Pin 13 (CKC)	Pin 1 ($\overline{\text{HSY}}$)	Pin 3 (CSY)	Pin 14 ($\overline{\text{VSY}}$)
Hi	$\overline{\text{HSY}}$ Output	CSY Input	$\overline{\text{VSY}}$ Output
Low	External Horizontal Sync. Input	External Clock Input	External Vertical Sync. Input

Note 5-1-1: CKC= High:

- If CKC=1, the phase lock loop (PLL) is adopted in the LCD module.
- Inputs CSY, the controller of LCD module will separate the Vertical Sync and Horizontal Sync from CSY.

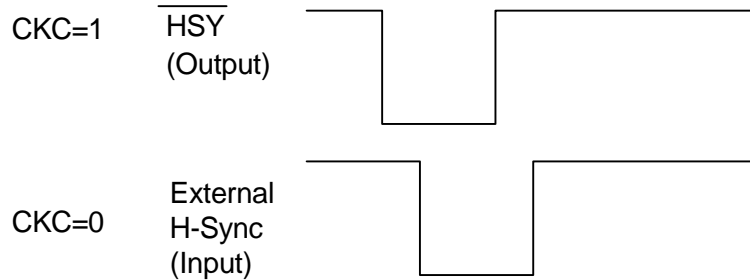
C. Output Horizontal Sync ($\overline{\text{HSY}}$, Pin 1) and Vertical Sync ($\overline{\text{VSY}}$, Pin 14)..

d. The internal detect will detect Vertical Sync to reset the vertical counter.

Note 5-1-2: CKC= Low

- a. If CKC=0, the phase lock loop (PLL) is not adopted in the LCD module.
- b. If CKC=0, the external clock input frequency of Pin 3 is 18.9 MHz.
- c. Input external Vertical Sync (VIY, Pin 17) and Horizontal Sync (Pin 1) to synchronize the LCD module. External Horizontal Sync and External Vertical Sync input pulse can be high going or low going.
- d. The pulse width of external Horizontal Sync input is $4.7\mu\text{s} \pm 2\mu\text{s}$. The pulse width of external Vertical Sync input is $2\text{H} \sim 4\text{H}$.
- e. The pulse length of external input Vertical Sync of NTSC system is $262\text{H} \pm 4\text{H}$ and PAL system is $312\text{H} \pm 4\text{H}$.

Note 5-1-3: The timing chart of $\overline{\text{HSY}}$ and external Horizontal input:



Note 5-1-4: If there is any question about CKC=0, please contact PVI.

Note 5-2: If CKC=1, the phase lock loop (PLL) is adopted in the LCD module.
 If CKC=0, the phase lock loop (PLL) is not adopted in the LCD module.
 If CKC=0, the external clock input frequency of Pin 3 is 18.9 MHz.

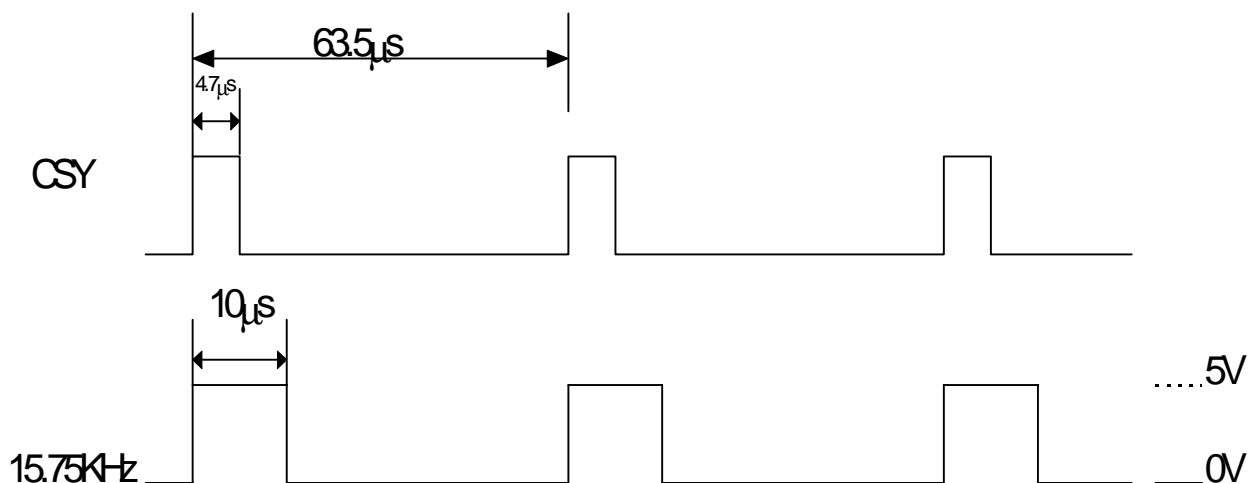
Note 5-3: $V_{\text{GH TYP.}} = +20\text{V}$

Note 5-4: $V_{\text{GL TYP.}} = -5\text{V}$

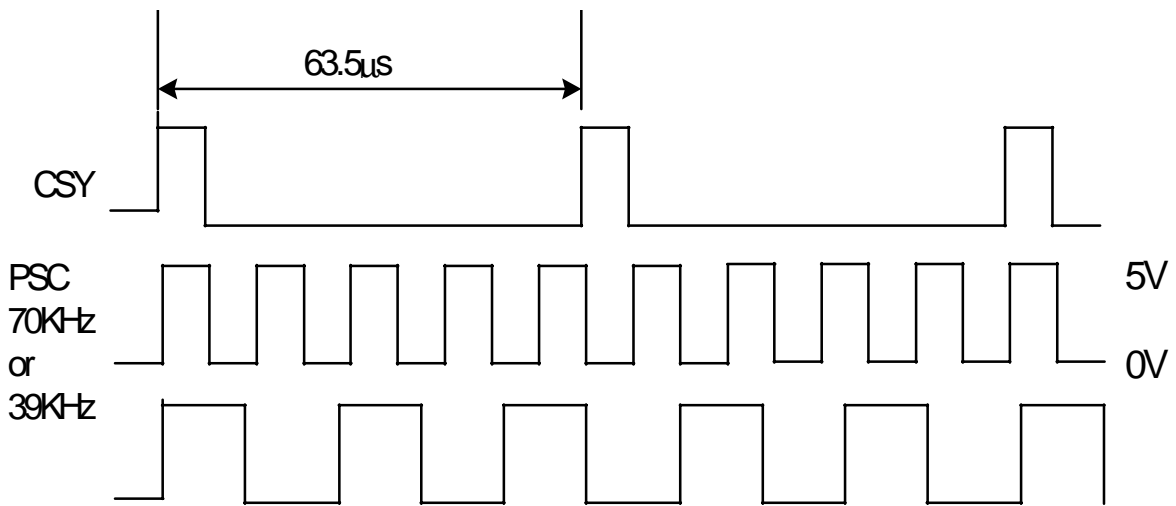
Note 5-5: $V_{\text{DD TYP.}} = +5\text{V}$

Note 5-6: $V_{\text{SH TYP.}} = +14\text{V}$

Note 5-7: The frequency of PSI is 15.75KHz.



Note 5-8 The frequency of PSC is 70KHz or 39KHz(Default is 70KHz).



Note 5-9 : Default Hi (+5V) for shift Right; Input Low (0V) for inverse (shift Left).

Note 5-10: Default Hi (+5V) for DOWN; Low (0V) for UP.

Note 5-11 : NTSC=Hi(+5V),PAL=LOW(0V)

5-2) Backlight driving

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	
2	VL2	Input terminal (Low voltage side)	Note 5-12

Note 5-12 : Low voltage side of backlight inverter connects with Ground of inverter circuits.

5-3) Input / Output Connector

A) LCD Module Connector

FFC Up Connector

16 Pins or 20 Pins

Pitch : 1.0 mm

B) Backlight Connector

JST BHR-03VS-1

Pin No. : 3

Pitch : 4 mm

6. Absolute Maximum Ratings:

GND = 0 V_o A Ta = 25

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage for Source Driver	V _{SH}	-0.5	+16	V	
Supply Voltage for Gate Driver	H Level	V _{GH}	-0.3	+26.5	V
	L Level	V _{GL}	-7	20	V
Supply voltage for controller	V _{DD}	-0.3	+6.5	V	
Analog input signals	V _B , V _R , V _G	0	12	V	
Digital input signals		-0.5	5.5	V	Note 6-1
Digital output signals		-0.5	5.5	V	Note 6-2
Storage Temperature		-30	+80		
Operation Temperature		-10	+60		

Note 6-1 : \overline{HSY} , CSY, \overline{VSY} , CKC,

Note 6-2 : \overline{HSY} , \overline{VSY} , PSI, PSC

7. Electrical Characteristics

7-1) Recommended Operating Conditions:

A) Driving for TFT-LCD Panel

GND = 0V_o A Ta = 25

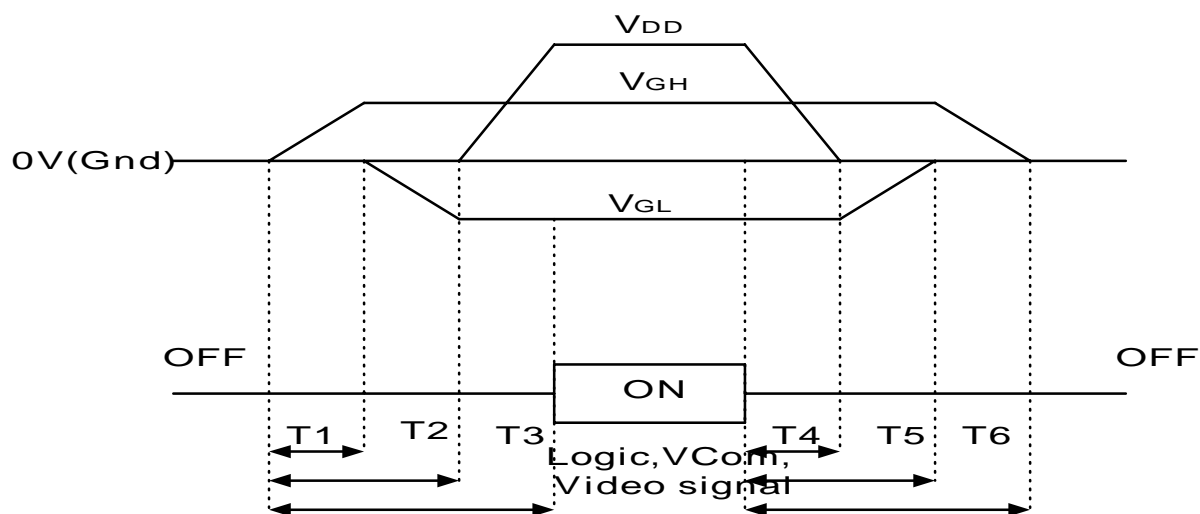
Parameter	Symbol	MIN.	TYP	MAX.	Unit	Remark
Supply voltage for source driver	V _{SH}	+13.5	+14	+14.5	V	
Supply voltage for gate driver	H Level	V _{GH}	+19	+20	+24	V
	L level	V _{GL}	-5.5	-5	-4	V
Supply voltage for controller	V _{DD}	+4.7	+5	+5.3	V	
Analog input Voltage	Amplitude	V _B , V _R , V _G	+2	-	+12	V
	DC component		+4	+6	+8	V
Digital input Voltage	H level		+2.4	-	+5	V
	L level		-0.3	-	+0.8	V
Digital output Voltage	H level		+2.4	+4	+5	V
	L level		0	-	+0.5	V

Note 7-1 : \overline{HSY} , CSY, \overline{VSY} , CKC

Note 7-2 : \overline{HSY} , \overline{VSY} , PSI, PSC

B) Power on sequence(Voltage source)

The Power on sequence only effect by V_{DD} , V_{GH} and V_{GL} , the others do not care.



- 1) $10ms \cdot T1 \cdot T2 \cdot T3 \cdot T4 \cdot T5$
- 2) $10ms \cdot T6 \cdot T7 \cdot T8 \cdot T9 \cdot T10$

C) Driving for backlight

$T_a = 25$

Parameter	Symbol	Min.	Typ.	Max	Unit	Remark
Lamp voltage	V_L	480	520	560	Vrms	$I_L = 6mA$
Lamp current	I_L	4	6	8	mA	
Lamp frequency	P_L	20		60	KHz	Note 7-3
Kick-off voltage	V_s			150 0	Vrms	

Note 7-3 : The wave form of lamp driving voltage should be as closed to a perfect SIN wave as possible.

7-2) Power Consumption

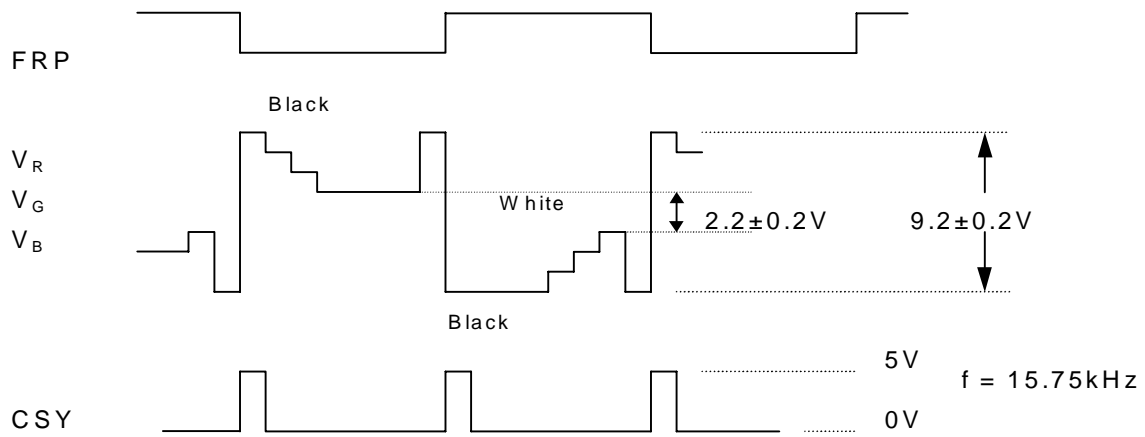
$T_a = 25$

Parameter	Symbol	Conditions	TYP.	MAX	Unit	Remark
Supply current for Gate Driver (Hi level)	I_{GH}	$V_{GH} = +20V$	6	9	mA	
Supply current for Gate Driver (Low level)	I_{GL}	$V_{GL} = -5V$	5	10	mA	
Supply current for Source Driver	I_{SH}	$V_{EE} = +14V$	12	15	mA	
Supply current for controller	I_{DD}	$V_{DD} = +5V$	22	30	mA	
LCD Panel Power Consumption			0.45		W	Note 7-4
Backlight Lamp Power Consumption			3.12		W	Note 7-5

Note 7-4 The power consumption for backlight is not included.

Note 7-5 Backlight lamp power consumption is calculated by $I_L \times V_L$.

7-3) Input / Output signal timing chart

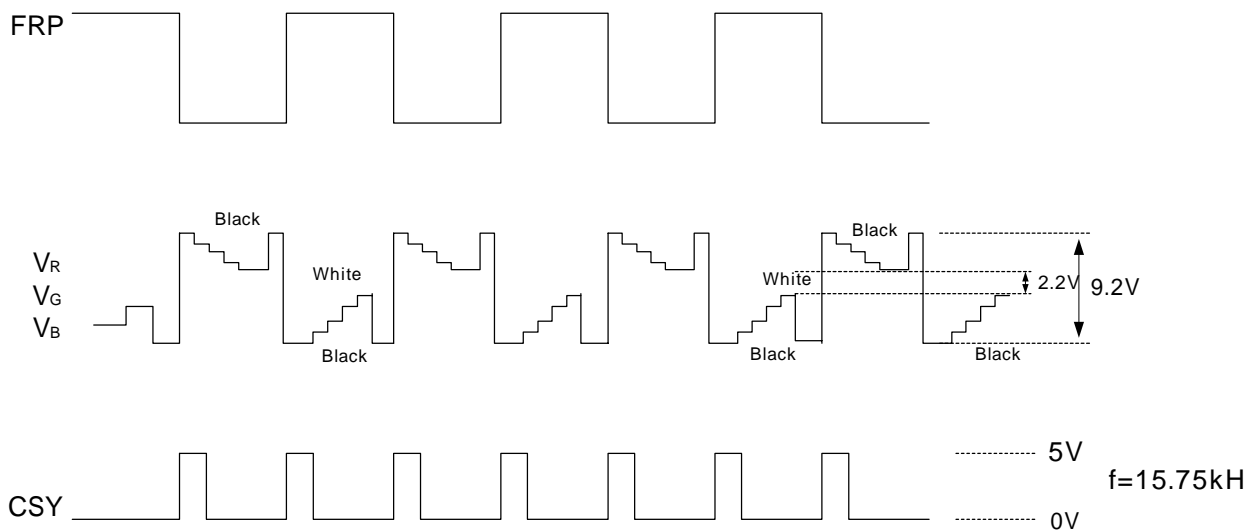


Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remarks	
Horizontal Sync. Output Pulse	Width	T_{HO}	4.2	4.7	5.2	μs	
	Phase Difference	T_{HP}	0	2		μs	
	Rising Time	T_{HR}	-	-	0.5	μs	
	Falling Time	T_{HF}	-	-	0.5	μs	
Vertical Sync. Output Pulse	Width	T_{VO}	-	4H	-	μs	$H=1/15.75\text{KHZ}$
	Phase Difference	T_{VPO}	-	1H	-	μs	odd field
	Phase Difference	T_{VPE}	-	1.5H	-	μs	even field
	Rising Time	T_{VR}	-	-	2	μs	
	Frequency	f_{FRP}	7.67	7.87	8.07	KHz	
Polarity Alternating Signal	Delay time	T_{FD}	-	-	4	μs	
	Falling Time	T_{VF}	-	-	2	μs	

7-4) Display Time Range

A) When sync. signal of NTSC system is applied.

- a) Horizontally
12.6 ~ 63.39 μs .
- b) Vertical
19 ~ 253 H



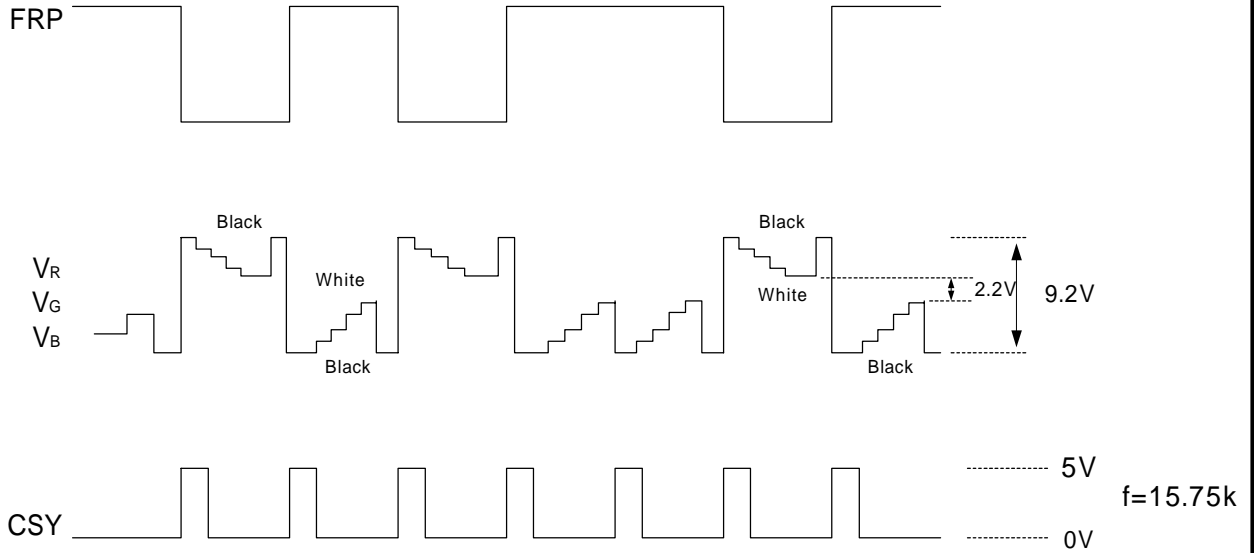
B) When sync. signal of PAL system is applied.

a) Horizontally
13.0 ~ 63.8 μ s.

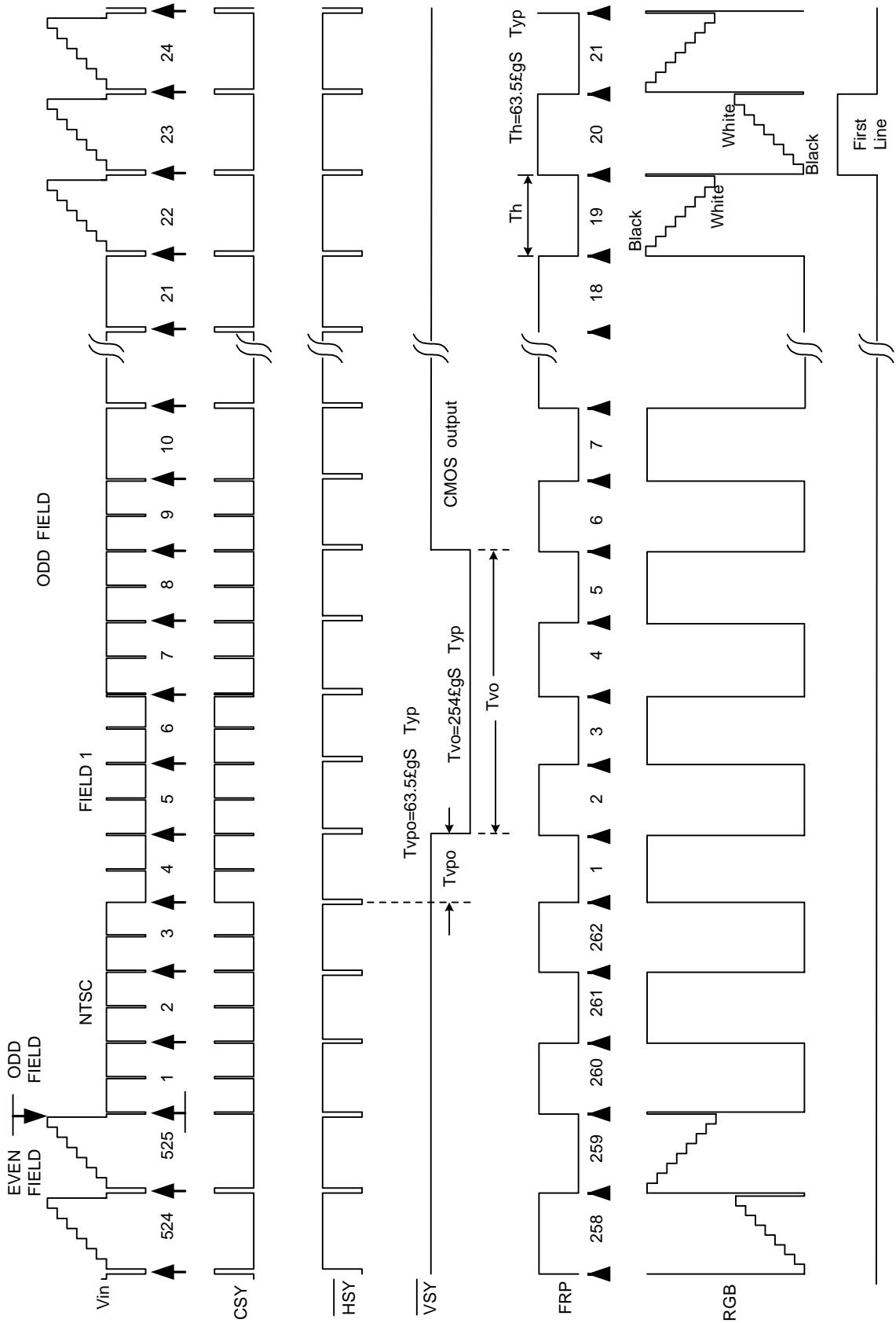
b) Vertical
26 ~ 298 H

c) odd field : Scan lines $14n+17$ $14n+23$ ($n = 1, 2, 3..$) are not displayed.

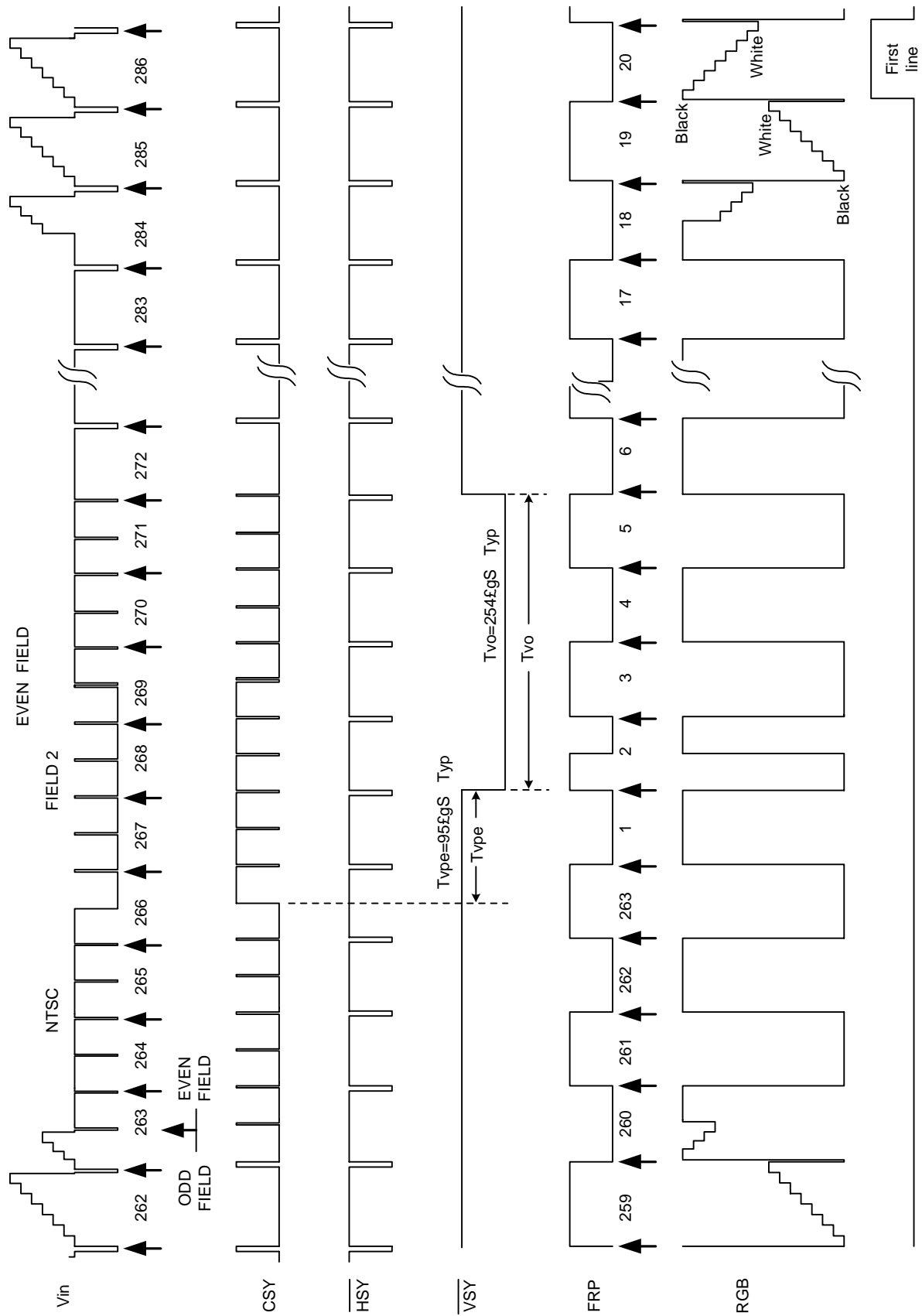
even field : Scan lines $14n+12$ $14n+20$ ($n = 1, 2, 3..$) are not displayed.



C) NTSC System

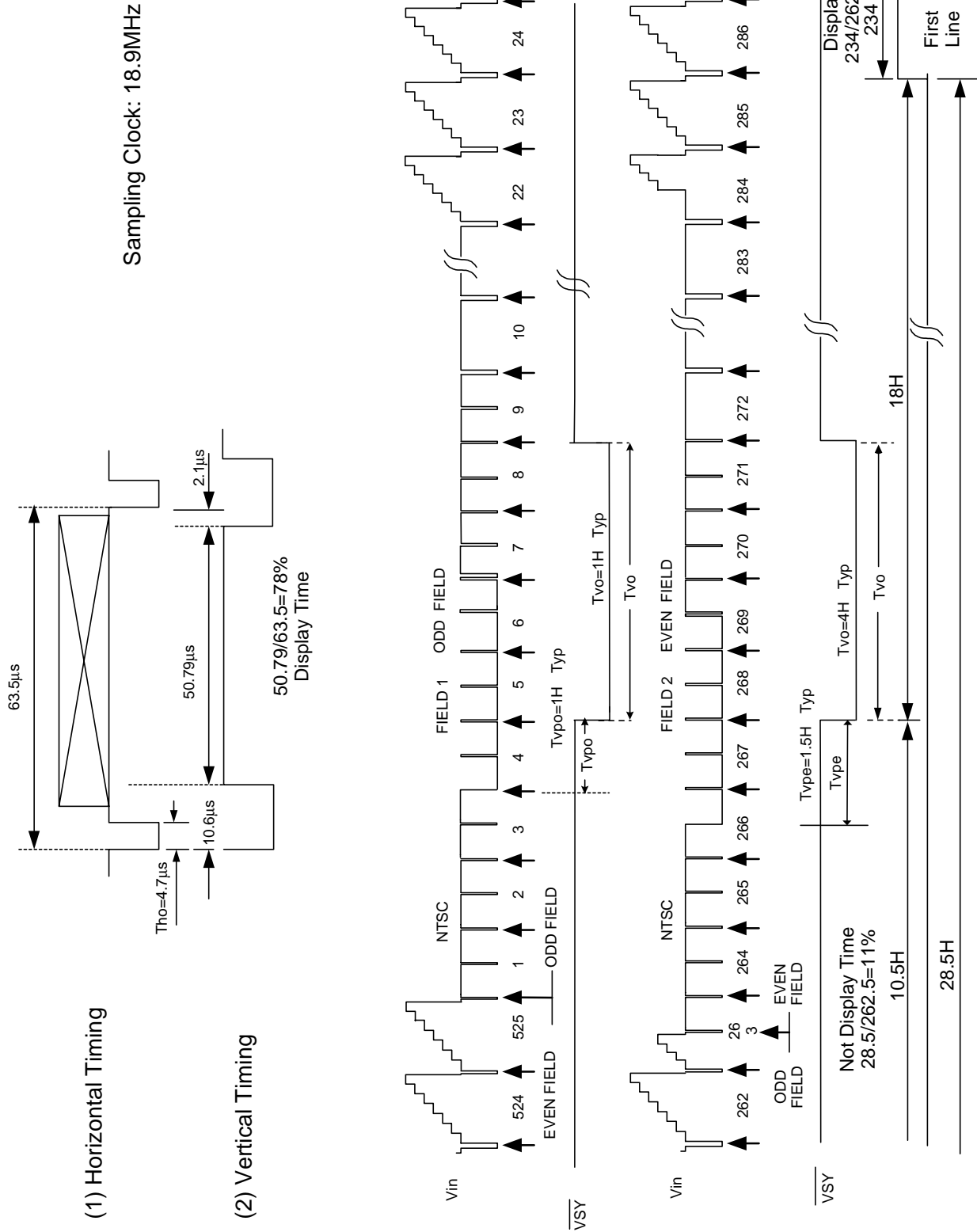


Timing chart of I/O and RGB signal

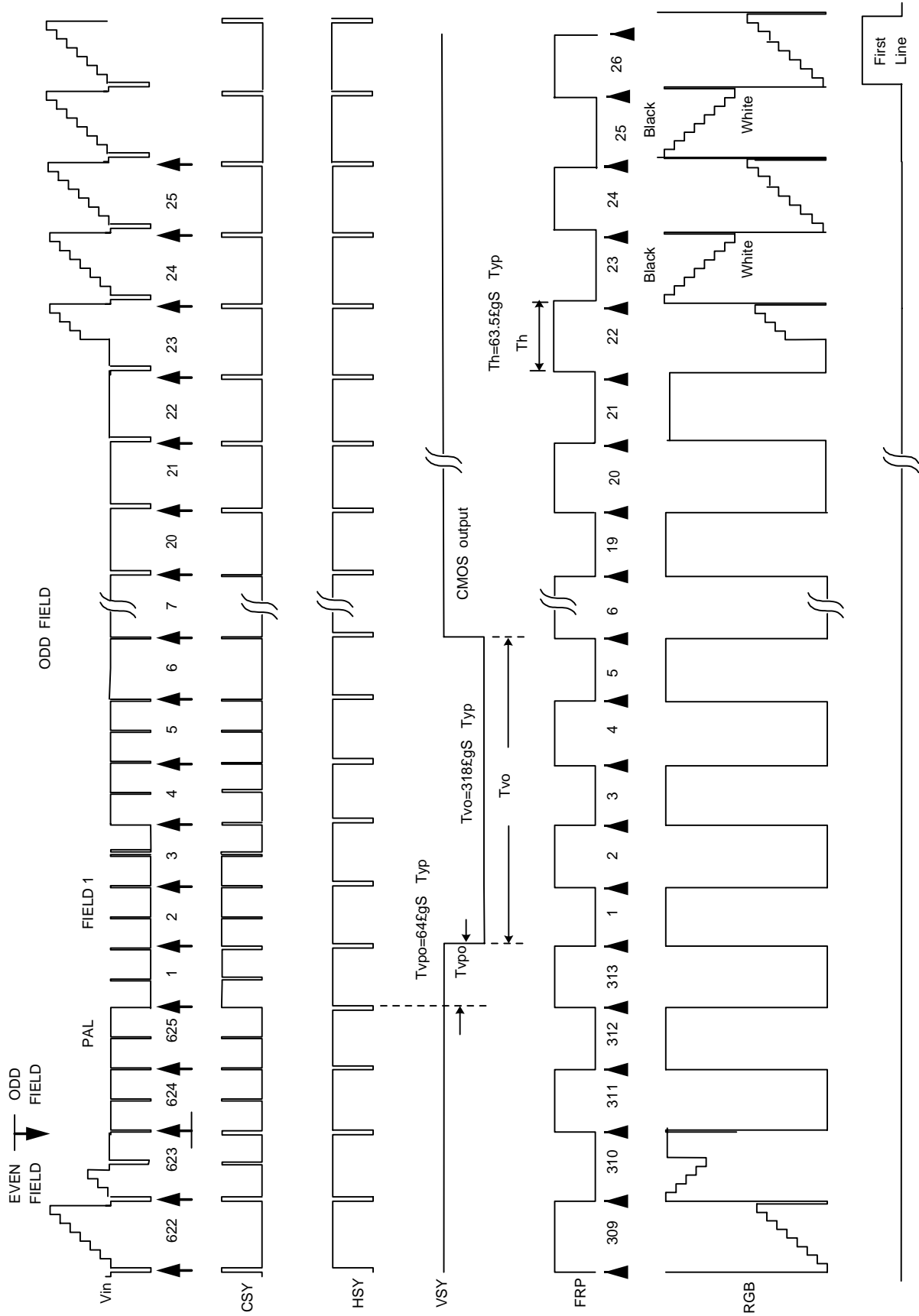


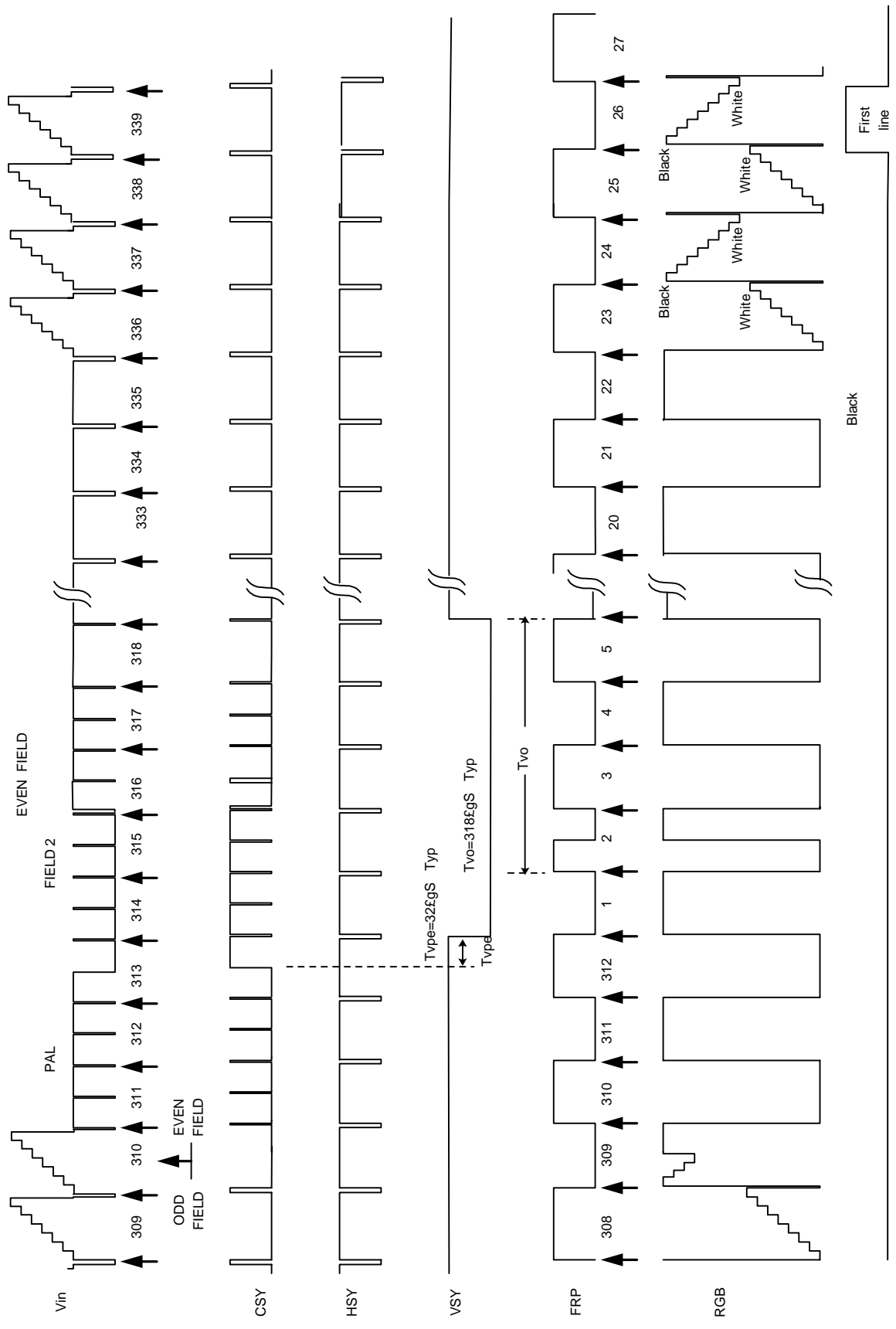
Timing chart of I/O and RGB signal

D) NTSC Display Timing



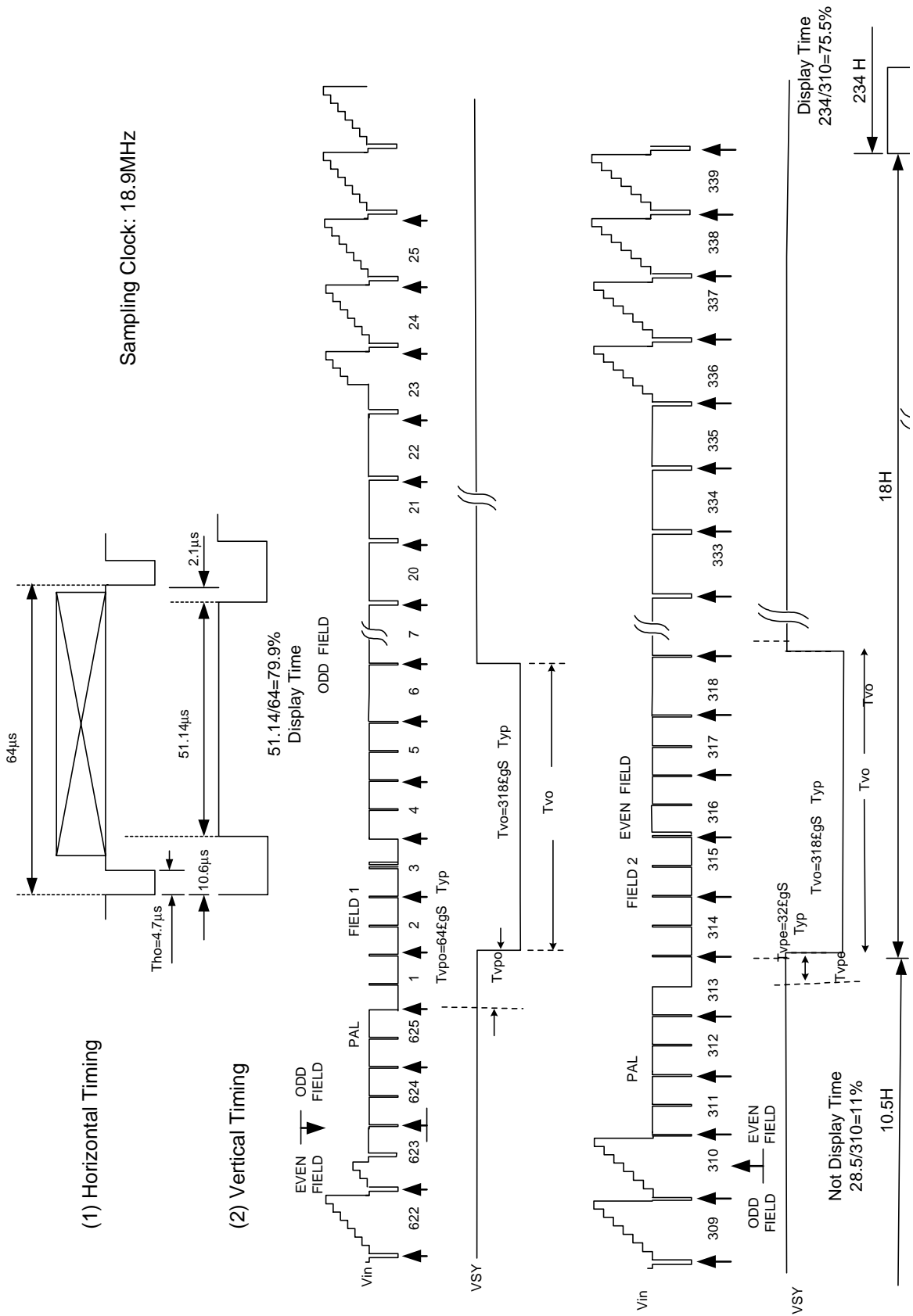
E) PAL System





Timing chart of I/O and RGB signal

F) PAL Display Timing



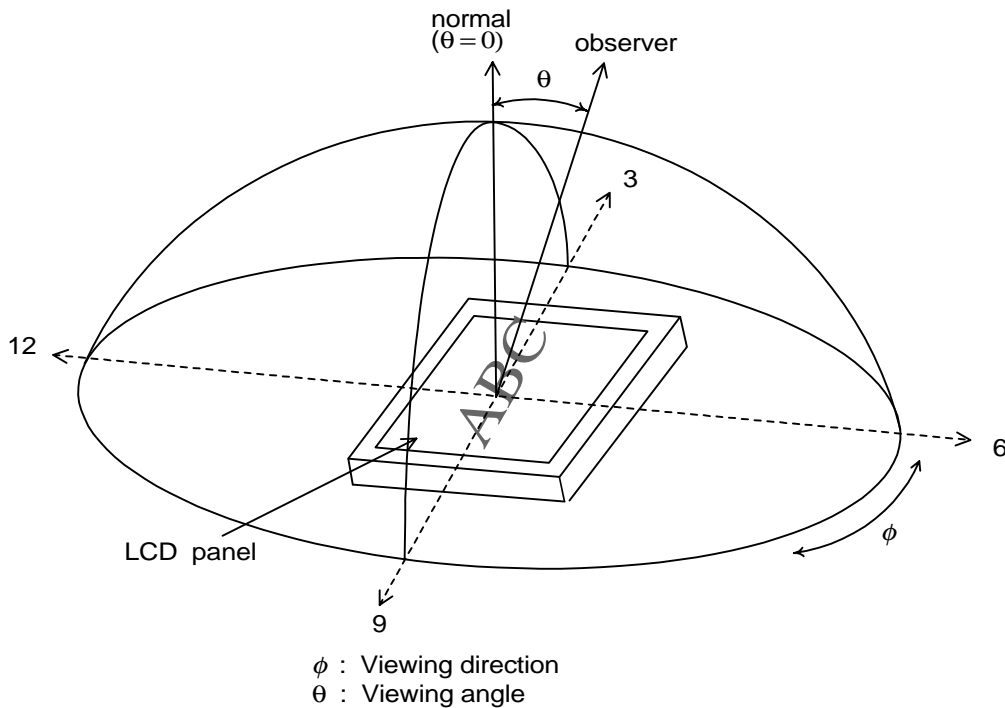
8. Optical Characteristics

8-1) Specification:

Ta = 25

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal		CR 10	45	55		deg	Note 8-1
	Vertical	(to 12 o'clock)		10	15		deg	Note 8-1
		(to 6 o'clock)		30	35		deg	Note 8-1
Contrast Ratio		CR		80	120			Note 8-2
Response time	Rise	Tr	=0° Φ=0°			30	ms	Note 8-4
	Fall	Tf				50	ms	
Brightness				250	300		cd/m ²	Note 8-3
White Chromaticity		x		0.250	0.300	0.350		Note 8-3
		y		0.265	0.315	0.365		
Lamp Life Time +25				10,000			hr	

Note 8-1: The definitions of viewing angles



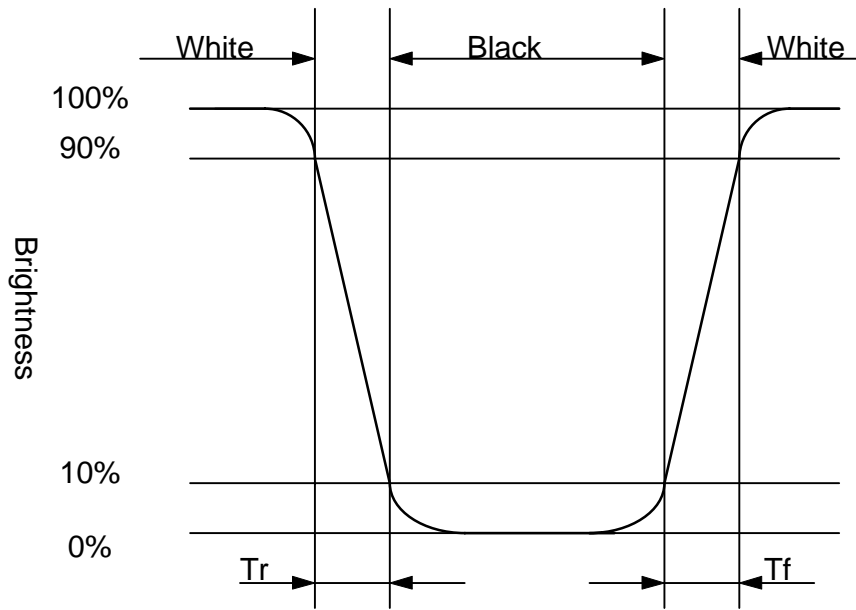
Note 8-2 : CR = $\frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

(Testing configuration see 8-2)

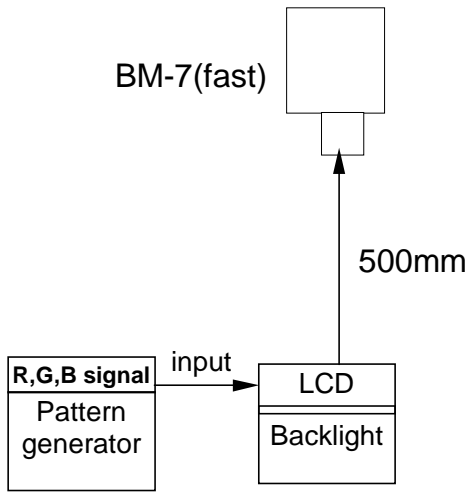
Contrast Ratio is measured in optimum common electrode voltage.

Note 8-3 : Topcon BM-7(fast) luminance meter 2°Xfield of view is used in the testing (after 20~30 minutes operation). Lamp Current 6mA

Note 8-4: The definition of response time:

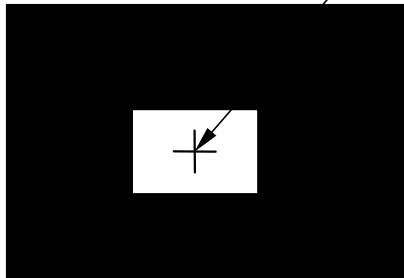


8-2) Testing configuration

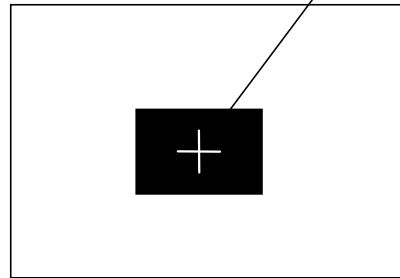


Caution: 1. Environmental illumination 1 lux
 2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

- LCD Display Testing Point Testing Point

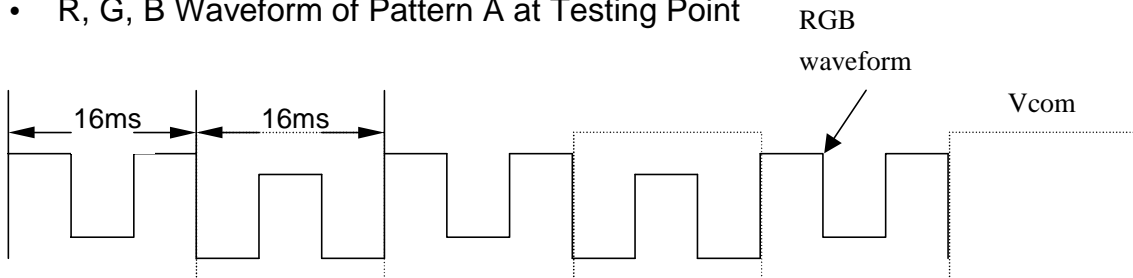


Pattern A



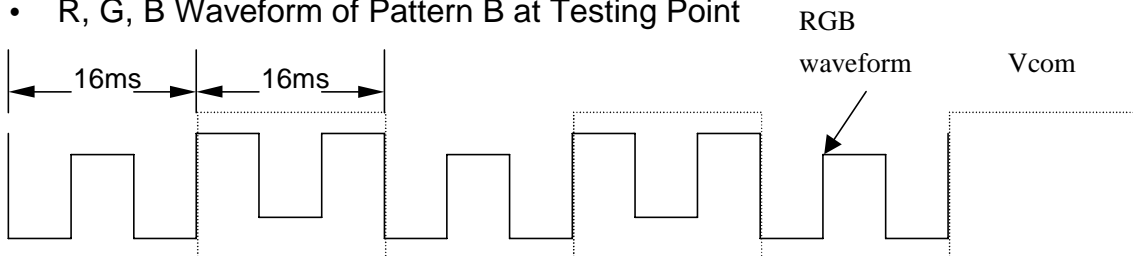
Pattern B

- R, G, B Waveform of Pattern A at Testing Point



$$V_w = 2.2 \pm 0.2V$$

- R, G, B Waveform of Pattern B at Testing Point



$$V_b = 9.2 \pm 0.2V$$

9. Handling Cautions

9-1) Mounting of module

- a) Please power off the module when you connect the input/output connector.
- b) Please connect the ground pattern of the inverter circute surely. If the connection is not perfect, some following problems may happen possibly.
 - 1.The noise from the backlight unit will increase.
 - 2.The output from inverter circuit will be unstable.
 - 3.In some cases a part of module will heat.
- c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

9-2) Precautions in mounting

- a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

9-3) Adjusting module

- a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
- b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

9-4) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many Hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.
- f) Please adjust the voltage of common electrode as material of attachment by 1 module.

10. Reliability Test

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +80 , 240 hrs
2	Low Temperature Storage Test	Ta = -30 , 240 hrs
3	High Temperature Operation Test	Ta = +60 , 240 hrs
4	Low Temperature Operation Test	Ta = -10 , 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +60 , 95%RH, 240 hrs
6	Thermal Cycling Test (non-operating)	-25 → +25 → +70 , 200 Cycles 30 min 5min 30 min
7	Vibration Test (non-operating)	Frequency: 10 ~ 55 Hz Amplitude: 1.5 mm Sweep time: 11 mins Test Period: 6 Cycles for each direction of X, Y, Z
8	Shock Test (non-operating)	100G, 6ms Direction: ±X, ±Y, ±Z Cycle: 3 times
9	Electrostatic Discharge Test	150pF, 330 Air: ±15KV; Contact: ±8KV 10 times/point, 9 points/panel face

Ta: ambient temperature

[Criteria]

Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

11. Block Diagram

