Single Phase PWM Controller with Light-Load Efficiency Optimization

General Description

The uP1539 is a single phase PWM controller with integrated high-current MOSFET driver. It can work with either 5V or 12V supplies and converts 1.5V to 19V power input. The bootstrap diode is built-in to simplify the circuit design and minimize external part count.

The uP1539 implements voltage mode control loop with fast transient response. High light-load efficiency is achieved by the single control loop. The operation frequency is programmable up to 1000kHz.

The uP1539 provides a programmable dual level overcurrent protection. The current information is monitored across the inductor DCR. Other features include pre-bias internal soft-start, power OK indication, UVP, OVP and OTP. With aforementioned functions, this part provides a compact, high efficiency, well-protected and cost-effective solutions. This part is available in WQFN3x3 - 16L package.

Ordering Information

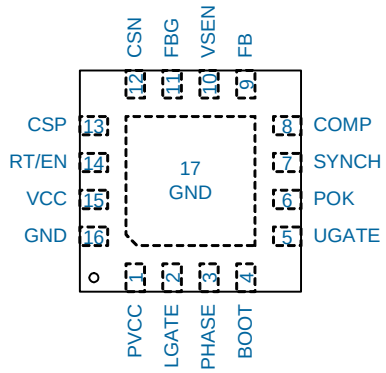
Order Number	Package	Remark
uP1539QQDD	WQFN3x3 - 16L	

Note:

(1) Please check the sample/production availability with uPI representatives.

(2) uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



Features

- VCC Supply Input from 5V to 12V
- Power Converter Input from 1.5V to 19V
- Integrated MOSFET Gate Driver
- Integrated Bootstrap Diode
- V_{IN} Detection Function
- Voltage Mode Control Loop
- Light-Load Efficiency Optimization
- 0.8V Reference Voltage with 0.5% Accuracy
- Programmable Operating Frequency from 100kHz to 1000kHz
- Pre-Bias Start-Up
- Synchronization Function
- Precise Lossless Inductor DCR Current Sense
- Programmable Dual Level OCP
- OVP, UVP, OTP
- RoHS Compliant and Halogen Free
- WQFN3x3 - 16L Package

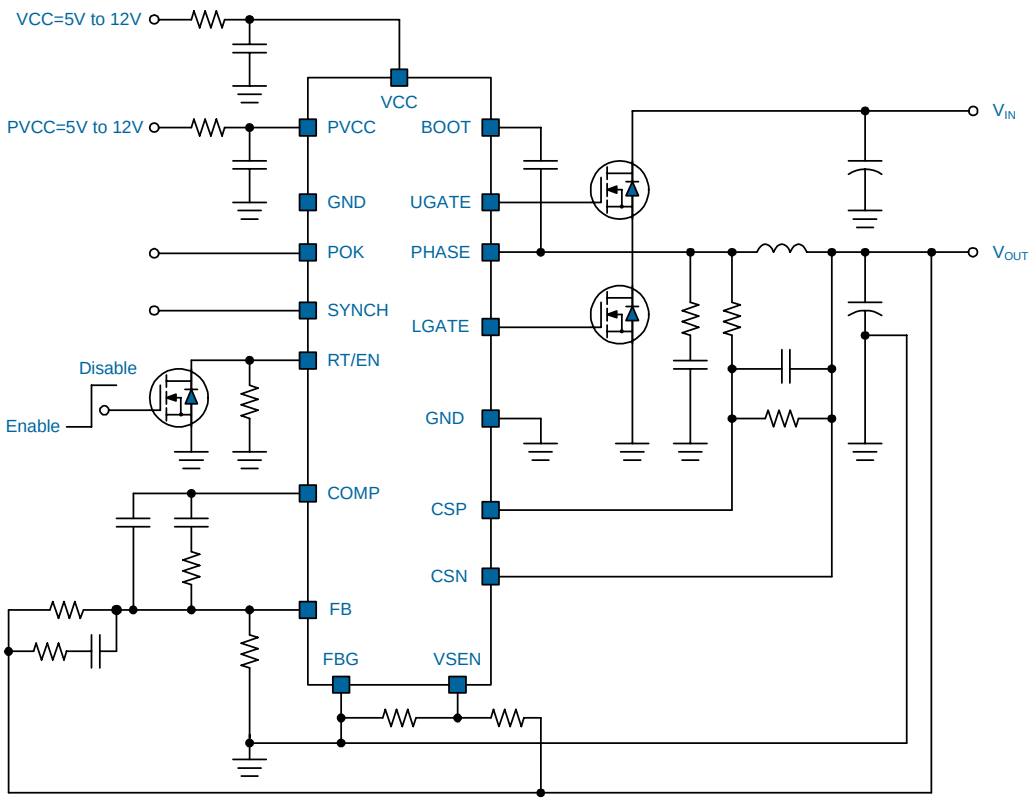
Applications

- Power Supplies for Microprocessors or Subsystem Power Supplies
- Cable Modems, Set Top Boxes, and DSL Modems
- Industrial Power Supplies; General Purpose Supplies
- Low-Voltage Distributed Power Supplies
- 5V or 12V General DC-DC Controller

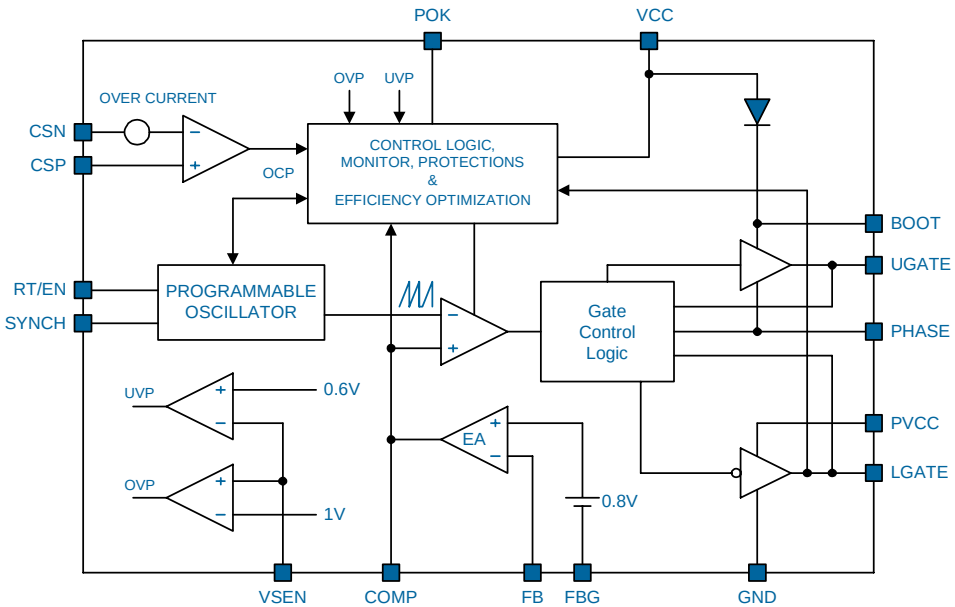
Functional Pin Description

No.	Pin Name	Pin Function
1	PVCC	**Supply Voltage for Lower Gate Drivers.** This pin provides current for lower gate drivers. Connect this pin to 12V (or 5V) voltage source and bypass it with a RC filter.
2	LGATE	**Lower MOSFET Gate Driver Output.** This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off. Connect this pin to the gate of lower MOSFET.
3	PHASE	**Switch Node.** This pin is used as the sink for the upper MOSFET gate driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET.
4	BOOT	**Bootstrap Supply for the Floating Upper MOSFET Gate Driver.** The bootstrap capacitor provides the charge to turn on the upper MOSFET. Connect this bootstrap capacitor between BOOT pin and the PHASE pin to form a bootstrap circuit.
5	UGATE	**Upper MOSFET Gate Driver Output.** This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. Connect this pin to the gate of upper MOSFET.
6	POK	**Power OK Indication.** POK is the open-drain architecture that indicates the output voltage is ready or not. This pin is set to high impedance when the output voltage is within regulation and the soft-start circuit has terminated. POK is pulled low immediately when either output is in soft-start, shutdown or protection.
7	SYNCH	**Synchronization Pin.** The controller synchronizes on the falling edge of a square wave provided to this pin. Short to GND if not used.
8	COMP	**Error Amplifier Output.** This is the output of the error amplifier (EA) and the non-inverting input of the PWM comparator. Use this pin in combination with the FB pin to compensate the voltage-control feedback loop of the buck converter. Connect with an R-C to FB.
9	FB	**Feedback Voltage.** This pin is the inverting input to the error amplifier. A resistor divider from the output to GND is used to set the regulation voltage. Connect this pin to V_{OUT} with a resistor R_{FB}, and with an R-C to COMP.
10	VSEN	**Output Voltage Monitor.** It manages OVP and UVP protections and POK. Connect to the positive side of the load for remote sensing.
11	FBG	**Remote Ground Sense.** Connect to the negative side of the load for remote sensing.
12	CSN	**Current Sense Negative Input.** Connect to the output-side of the main inductor. The maximum operation range of CSN is 3.3V.
13	CSP	**Current Sense Positive Input.** Connect through an R-C filter to the phase-side of the main inductor.
14	RT/ EN	**Frequency Setting and Chip Disable.** Internally set to 1.2V, a resistor to GND sets the operation frequency of the buck controller. According to the resistor R_{RT} connected to GND with a gain of 10kHz/uA. If floating, the switching frequency is 200kHz. Pulling this pin to GND disables the controller.
15	VCC	**Device Power Supply.** Operative voltage is 5V to 12V bus. A minimum 1uF ceramic capacitor to GND is required for locally bypassing the input voltage. VCC is also as the high side MOSFET driver power supply.
16	GND	**Ground.** All internal references, logic and driver return path are referenced to this pin. Connect to the PCB GND ground plane and filter to VCC and PVCC.
Exposed Pad		The exposed pad should be well soldered to PCB for effective heat conduction. Connect the exposed pad to the ground.

Typical Application Circuit



Functional Block Diagram



Functional Description

The uP1539 is a single buck PWM controller with integrated driver. It is designed to operate from a 5V or 12V supply. The voltage mode control loop with automatically CCM/DCM operation provides fast transient response and high efficiency over wide load range.

The internal precise 0.8V reference and remote voltage sensing provide high output voltage accuracy. Frequency, OCP level are programmable. The synchronization function allows the reduction of the input capacitors RMS current resulting in a cheap and cost-effective system design.

Supply Voltage and Power On Reset (POR)

The uP1539 requires two supply input for PVCC and VCC. PVCC is the power supply for low side MOSFET driver. VCC is the power supply for high side MOSFET driver and control circuit. The supply voltage range of PVCC and VCC is from 4.5V to 13.2V with respect to GND. For 19V power conversion, please use 5V for VCC and PVCC.

The power on reset (POR) circuit monitors the supply voltage at the VCC and PVCC pin. If VCC and PVCC exceeds the POR rising threshold voltage, the controller is reset and prepares the PWM for operation. If VCC and PVCC falls below the POR falling threshold during normal operations, all MOSFETs will stop switching. The POR rising and falling threshold has a hysteresis to prevent noise caused reset.

Chip Enable and Frequency Setting

The RT/EN pin of uP1539 is a multi-functional pin. The IC can be disabled by directly pulling this pin to GND. By connecting a resistor (R_{RT}) from RT/EN pin to GND sets the operation frequency of CCM. In DCM, the operation frequency depends on output loading.

The switching frequency is internally fixed at 200kHz when RT/EN pin is floating. The RT/EN pin is fixed at 1.2V, the frequency is varied proportionally to the current sink from the pin considering the internal gain of 10kHz/uA.

Connecting R_{RT} to GND, the frequency is increased, according to the following relationships

$$f_{SW} = 200kHz + \frac{1.2}{R_{RT}} \times 10 \left(\frac{kHz}{\mu A} \right)$$

Connecting R_{RT} to positive voltage V, the frequency is decreased, according to the following relationships

$$f_{SW} = 200kHz - \frac{V - 1.2}{R_{RT}} \times 10 \left(\frac{kHz}{\mu A} \right)$$

Internal Soft-start

The uP1539 provides soft-start function internally. The soft-start function prevents large inrush current and output voltage overshoot while the converter is being powered up. After the chip is enabled (with around 100us delay), the soft-start function automatically begins. The reference ramps up and lasts for 1024 clock cycles. At the end of the soft-start, the POK signal is set free with 3 clock cycles delay.

The soft-start time can be determined as follow:

$$T_{SS} = \left(\frac{1024}{f_{SW}(kHz)} \right) \quad (ms)$$

The UVP is blanked until soft-start is finished.

Discontinuous Conduction Mode

At light load condition, the uP1539 automatically operates in ultrasonic mode to improve the light load efficiency and avoid acoustic noise issue. As the output current decreases from heavy load condition, the inductor current decreases. The inductor valley current eventually decreases to zero, which is the boundary between continuous conduction mode and discontinuous conduction mode. By emulating the behavior of diodes, the low side MOSFET allows only partial of negative current to flow when the inductor freewheeling current reaches negative.The ultrasonic mode operation keeps the switching frequency higher than 30kHz to avoid the acoustic noise.

Synchronization

uP1539 provides the user the possibility to synchronize to an external signal when properly connected to the SYNCH pin. Synchronization allows different converters to share the same input filter reducing the resulting Irms and so reducing the total capacitor count required to sustain the load. Furthemore, synchronized systems generally exhibits higher noise immunity and better regulation.

The device synchronize the high-side MOSFET turn-on with the falling-edge of the SYNCH pin input signal locking the internal saw-tooth generator to the external signal. When setting uP1539 internal frequency (OSC) to the same value of the frequency to which it has to be synchronized (SYNCH), the device is then able to recover up to +40% variations between the internal frequency set by OSC and the external frequency present at SYNCH pin.

In case the IC is not able to recover the frequency difference (i.e. the external frequency falls outside the +40% acceptance window), the internal oscillator is used and external signal is ignored. When the IC works in light-load conditions the SYNCH input is ignored.

SYNCH pin can then be connected to other regulator's PWM and/or PHASE and/or GATE signals according to the desired phase-shift with proper voltage scaling.

Functional Description

Over Current Protection

The uP1539 senses the output current information across the inductor DCR. The inductor DCR current sense is implemented by comparing and monitoring the difference between the CSP and CSN pins. If the monitored voltage is higher than the internal thresholds, an overcurrent event is detected.

DCR current sensing requires time constant matching between the inductor and the reading network. For the maximum safety and load protection, the uP1539 implements dual level OCP. The first OCP threshold is 20mV (typ.). If the monitored voltage between CSP and CSN exceeds this threshold, a 1st level over current is detected. After four consecutive OC events, over current protection will be triggered and the IC latches.

The second OCP threshold is 30mV (typ.). If the monitored voltage between CSP and CSN exceeds this threshold, a 2nd level over current is detected. After immediately OC events, over current protection will be triggered and the IC latches.

By properly designing the current reading network, it is possible to program the OC threshold as shown in Figure 1.

$$I_{OCP} = \frac{20mV}{DCR} \times \frac{R3+R4}{R4}$$

Time constant matching is in this case designed considering:

$$\frac{L}{DCR} = (R3 // R4) \times C$$

This means that once inductor has been chosen, the two conditions above define the proper values for R3 and R4.

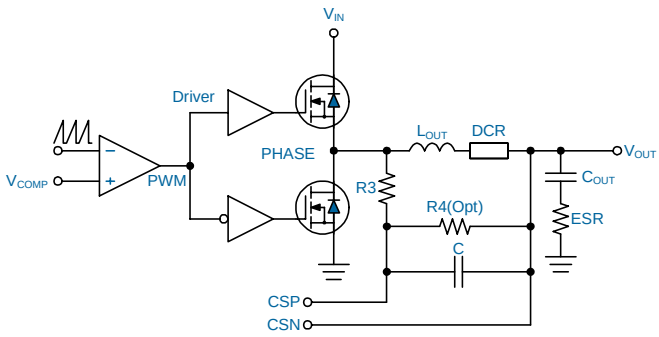


Figure 1. Current Reading Network

Output Voltage Setting

uP1539 is capable to precisely regulate an output voltage as low as 0.8V. In fact, the device comes with a fixed 0.8V internal reference that guarantee the output regulated voltage to be within ±0.5% tolerance. Output voltage higher than 0.8V can be easily achieved by adding a resistor between FB pin and ground. The steady state DC output voltage will be:

$$V_{OUT} = V_{REF} \times \frac{R1+R2}{R2}$$

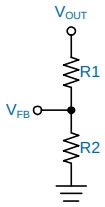


Figure 2. Feedback Circuit

POK Indication and Protection

uP1539 monitors the voltage at VSEN pin and compares it to internal reference voltage in order to provide under voltage and over voltage protections as well as POK indication.

- POK Indication

The POK is an open-drain type output. It is asserted at the end of the soft-start phase with 3 clock cycles delay and no protection is occurred.

- Under Voltage Protection

If the voltage at VSEN pin drops below the UVP threshold, the device turns off both high-side and low-side MOSFETs, latching the condition. Cycle the VCC or EN to release the UVP.

- Over Voltage Protection

If the voltage at the VSEN pin rises over the OVP threshold, overvoltage protection turns off the high-side MOSFET and turns on the low-side MOSFET. The low-side MOSFET is turned off as soon as VSEN goes below V_{REF}/2. The condition is latched, cycle VCC/EN to recover. Note that, even if the device is latched, the device still controls the low-side MOSFET and can switch it on whenever VSEN rises above the OVP threshold.

- PreOVP Protection

The uP1539 monitors VSEN when IC is disabled. If VSEN surpasses the OVP threshold, IC turns on the low-side MOSFET to protect the load. On the EN rising edge, the protection is disabled and the IC implements the SS procedure.

PreOVP is disabled when EN is high but the OV protection becomes operative.

High Current Embedded Drivers

uP1539 provides high-current driving control. The driver for the high-side MOSFET use BOOT pin for supply and PHASE pin for return. The driver for the low-side MOSFET use the PVCC pin for supply and GND pin for return.

The embedded driver embodies an anti-shoot-through and adaptive dead-time control to minimize low-side body diode conduction time maintaining good efficiency saving the use of schottky diode.

Power Dissipation

It is important to consider the power that the device is going to dissipate in driving the external MOSFETs in order to avoid overcoming the maximum junction operative temperature.

Two main terms contribute in the device power dissipation: bias power and drivers power.

- Device Power (P_{DC}) depends on the static consumption of the device through the supply pins and it is simply quantifiable ad follow:

$$P_{DC} = V_{CC} \times I_{CC} + V_{PVCC} \times I_{PVCC}$$

- The power of drivers is needed by the driver to continuously switch ON and OFF the external MOSFETs; it is a function of the switching frequency and total gate charge of the selected MOSFETs. It can be quantified considering that the total power P_{SW} dissipated to switch the MOSFETs dissipated by three main factors: external gate resistance (when present), intrinsic MOSFET resistance and intrinsic driver resistance.

This last term is the important one to be determined to calculate the device power dissipation.

The total power dissipated to switch the MOSFETs for each phase featuring embedded driver results:

$$P_{SW} = f_{SW} \times (Q_{GHS} \times PVCC + Q_{GLS} \times PVCC)$$

Where Q_{GHS} is the total gate charge of the high-side MOSFETs and Q_{GLS} is the total gate charge of the low-side MOSFETs.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage (VCC, PVCC) ---------- -0.3V to +15V

PHASE to GND

DC ---------- -0.3V to 30V

< 200ns ---------- -5V to 30V

BOOT to GND

DC ---------- -0.3V to PH + 15V

< 200ns ---------- -5V to 38V

LGATE to GND

DC ---------- -0.3V to + (PVCC + 0.3V)

<200ns ---------- -5V to 18V

UGATE to PHASE

DC ---------- -0.3V to 15V

<200ns ---------- -5V to 18V

CSP to GND

DC ---------- -0.3V to 6V

All Other Pin to GND

DC ---------- -0.3V to +6V

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- 150°C

Lead Temperature (Soldering, 10 sec) ---------- 260°C

ESD Rating (Note 2)

HBM (Human Body Mode) ---------- 2kV

MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)

WQFN3x3 - 16L θ_{JA} ---------- 68°C/W

WQFN3x3 - 16L θ_{JC} ---------- 6°C/W

Power Dissipation, PD @ T_A = 25OC

WQFN3x3 - 16L ---------- 1.47W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C

Operating Ambient Temperature Range ---------- -40°C to +85°C

Power Input Voltage, V_{IN} ---------- +1.5V to 19V

Supply Input Voltage, VCC, PVCC ---------- +4.5V to 13.2V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(VCC = PVCC = 12V, T_A = 25°C, unless otherwise specified)

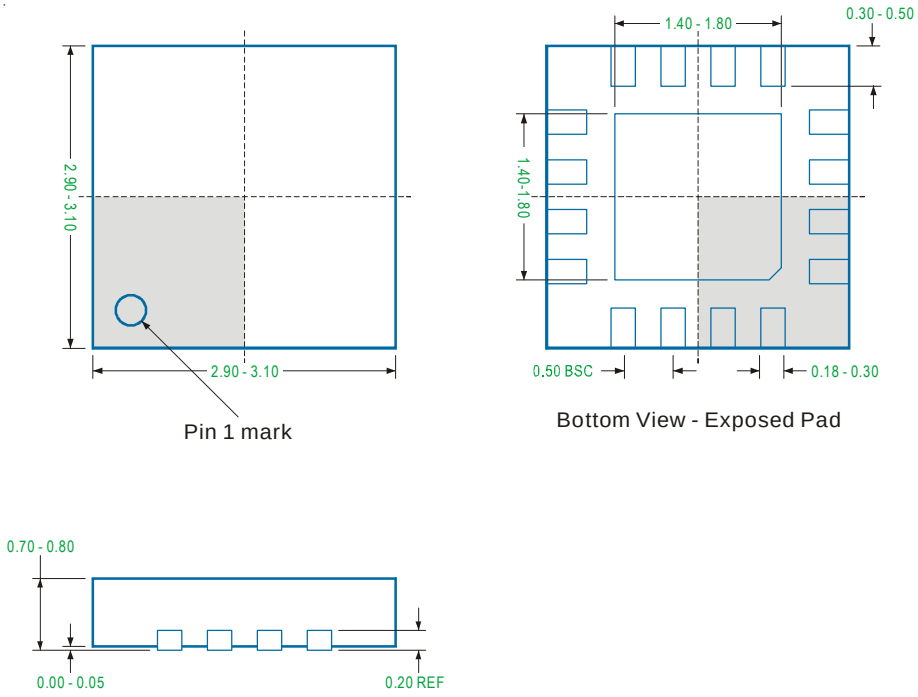
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Current	I_{VCC}	UG and LG Open	--	--	5	mA
		RT/EN = GND	--	--	0.55	
Supply Current	I_{PVCC}	UG and LG Open	--	3.5	5	mA
		RT/EN = GND	--	--	0.2	
VCC POR Threshold	VCC_{POR}	V_{CC} rising	--	--	4.5	V
VCC POR Hysteresis	VCC_{POR_HYS}		--	0.3	--	V
PVCC POR Threshold	$PVCC_{POR}$	PVCC rising	--	--	4.2	V
PVCC POR Hysteresis	$PVCC_{POR\_HYS}$		--	0.2	--	V
Synchronization Input	SYNCH	V_{IL}	--	--	1	V
		V_{IH}	2.5	--	--	V
Oscillator and Soft Start						
Switching Frequency	f_{OSC}	RT/EN = Open	180	200	220	kHz
Oscillator Gain	k_{OSC}	Current sink/source from RT/EN	--	10	--	kHz/uA
Sawtooth Amplitude	ΔV_{OSC}		--	1.0	--	V
Disable Threshold Level	V_{DIS}	$V_{RT/EN}$ falling	--	--	0.75	V
Soft Start Interval	T_{SS}	RT/EN = Open	--	5.12	--	ms
Maximum Duty Cycle		RT/EN = Open	80	--	--	%
Minimum Pulse Width	T_{ON_MIN}	RT/EN = Open	--	90	--	ns
Minimum PSM Frequency	F_{PSM}	In light load	30	--	--	kHz
Zero Current Detection						
Zero Current Crossing Detection	V_{PH}	V_{PH} to GND	-3	--	3	mV
Reference Voltage						
Reference Voltage	V_{REF}		0.796	0.800	0.804	V
Reference Voltage Accuracy		V_{FB} to FBG	-0.5	--	0.5	%

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by Design	--	120	--	dB
Gain-Bandwidth Product	GBW	Guaranteed by Design	15	18	--	MHz
Slew Rate	SR	Guaranteed by Design	--	8	--	V/us
Transconductance	GM		--	11000	--	uA/V
Maximum Output Source Current	$I_{COMP-SR}$	$V_{FB} < V_{REF}$	1000	--	--	uA
Maximum Output Sink Current	$I_{COMP-SK}$	$V_{FB} > V_{REF}$	1000	--	--	uA
Buck Controller Gate Drivers						
UGATE Source Resistance	R_{UG_SRC}	I_{UG} = -100mA	--	2.5	5	Ω
UGATE Sink Resistance	R_{UG_SNK}	I_{UG} = 100mA	--	2	2.5	Ω
LGATE Source Resistance	R_{LG_SRC}	I_{LG} = -100mA	--	2	3	Ω
LGATE Sink Resistance	R_{LG_SNK}	I_{LG} = 100mA	--	1	1.5	Ω
PH Falling to LG Rising Delay	T_{PH-LG}	V_{PH} < 1.2V to V_{LG}>1.2V	--	15	30	ns
LG Falling to UG Rising Delay	T_{PH-UG}	V_{LG} < 1.2V to (V_{UG} - V_{PH}) > 1.2V	10	20	35	ns
Current Sense						
OC Current Threshold	V_{OCTH}	CSP - CSN; 4 clock Masking	17	20	23	mV
		CSP - CSN; Immediate Action	--	30	--	mV
POK and Protection						
OVP Threshold Level	V_{OVP}	VSEN Rising	--	1	--	V
		un-latch, VSEN Falling	--	0.4	--	V
UVP Threshold Level	V_{UVP}	VSEN Falling	--	0.6	--	V
OTP Threshold	V_{OTP}		--	160	--	°C
POK High Delay	T_{PG-H}	3 clock	--	--	50	us
POK Low Delay	T_{PG-L}		--	--	1	us

Package Information

WQFN3x3 - 16L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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