5V/12V Synchronous-Rectified Buck Controller

General Description

The uP1540 is a compact synchronous-rectified buck controller specifically designed to operate from 5V or 12V supply voltage and to deliver high quality output voltage as low as 0.8V.

The uP1540 adopts proprietary RCOT™ technology, providing flexible selection of output LC filter and excellent transient response to load and line change. The uP1540 supports both tracking mode and stand-alone mode operation.

This controller integrates internal MOSFET drivers that support 12V+12V or 5V+19V bootstrapped voltage for high efficiency power conversion. The bootstrap diode is built-in to simplify the circuit design and minimize external part count.

Other features include internal soft start, over/under voltage protection, over current protection and shutdown function. With aforementioned functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solutions. This part is available in WDFN3x3-10L package.

Ordering Information

Order Number	Package	Top Marking
uP1540PDDA	WDFN3x3-10L	uP1540P

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

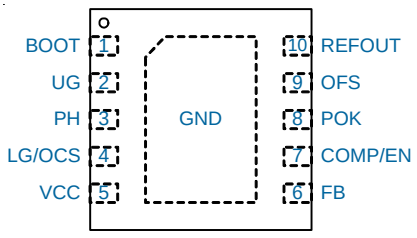
Features

- **Operates from 5V or 12V Supply Voltage**
  - **3.3V to 12V V_{IN} Input Range**
  - **0.8V V_{REF} with 1.0% Accuracy**
  - **Support V_{CC} = 5V, V_{IN} = 19V**
- **Support Stand-Alone and Tracking Mode Operation**
  - **Offset Voltage Tuning**
- **Compensated Constant On Time Operation**
  - **Quasi Constant Frequency Operation**
  - **Fast Transient Response**
  - **Smooth Mode Transition**
- **Lossless, Adjustable Over Current Protection**
  - **Uses Lower MOSFET $R_{DS(ON)}$**
- **Internal Soft Start**
- **Over Voltage and Under Voltage Protection**
- **Integrated Bootstrap Diode**
- **WDFN3x3-10L Package**
- **RoHS Compliant and Halogen Free**

Applications

- **Power Supplies for Microprocessors or Subsystem Power Supplies**
- **Cable Modems, Set Top Boxes, and DSL Modems**
- **Industrial Power Supplies; General Purpose Supplies**
- **5V or 12V Input DC-DC Regulators**
- **Low-Voltage Distributed Power Supplies**

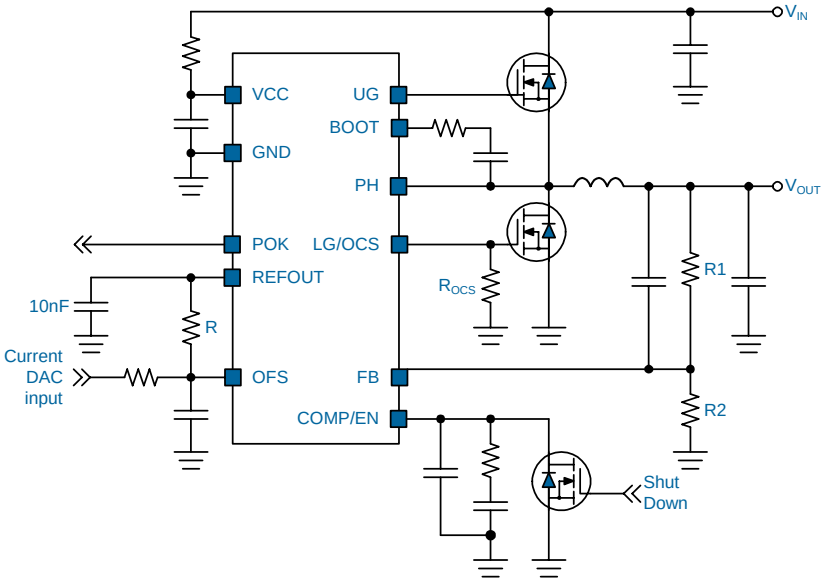
Pin Configuration



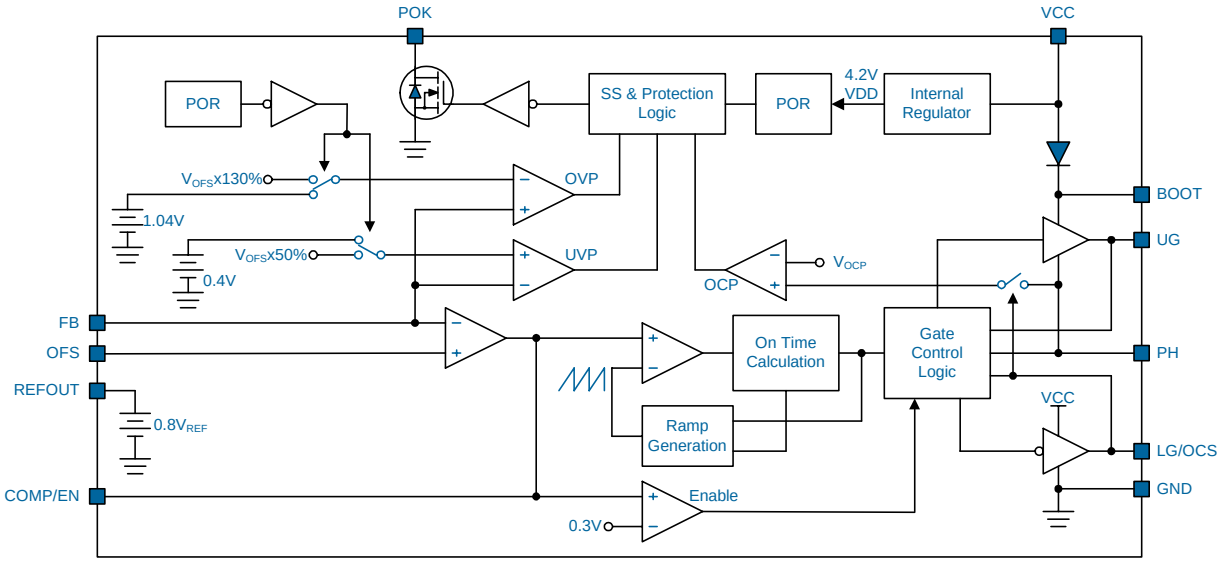
Functional Pin Description

No.	Pin Name	Pin Function
1	BOOT	**Bootstrap Supply** for the floating upper gate driver. Connect the bootstrap capacitor between BOOT pin and the PH pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET.
2	UG	**Upper Gate Driver Output.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
3	PH	**PHASE Switch Node.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UG driver, and to monitor the voltage drop across the lower MOSFET for over current protection. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
4	LG/OCS	**Lower Gate Driver Output.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off. **Over Current Protection Setting.** Connect a resistor from this pin to GND to set the OCP level.
5	VCC	**Supply Input Voltage.** This pin provides the bias supply for the uP1540 and the lower gate driver. Connect a well-decoupled 4.5V to 13.2V supply voltage to this pin. Ensure that a decoupling capacitor is placed near the IC.
6	FB	**Feedback Input Voltage.** This pin is the inverting input to the error amplifier. A resistor divider from the output to GND is used to set the regulation voltage. Use this pin in combination with the COMP/EN pin to compensate the voltage control feedback loop of the converter.
7	COMP/EN	**Error Amplifier Output.** This is the output of the error amplifier and the non-inverting input of the PWM comparator. Use this pin in combination with the FB pin to compensate the voltage-control feedback loop of the converter. Pulling COMP/EN to a level below 0.3V disables the controller and both UG and LG outputs are held low.
8	POK	**Power OK Indication.** This open-drain output is set high impedance when the output voltage is within regulation.
9	OFS	**Offset Voltage.** The FB voltage changed under external sinking or sourcing current on this pin. Short this pin and REFOUT to disable the voltage tuning function.
10	REFOUT	**0.8V Voltage Output.** Connect a resistor from this pin to OFS to set the offset voltage scale. Short this pin and OFS to disable the voltage tuning function.
Exposed Pad		**Ground.** The exposed pad is the dominate heat conducting path and should be well soldered to the PCB with multiple vias for optimal thermal performance.

Typical Application Circuit



Functional Block Diagram



Functional Description

The uP1540 is a compact synchronous-rectified buck controller specifically designed to operate from 5V or 12V supply voltage and to deliver high quality output voltage as low as 0.8V.

Supply Voltage

The VCC pin receives a well-decoupled 4.5V to 13.2V supply voltage to power the control circuit, the lower gate driver and the bootstrap circuit for the higher gate driver. A minimum 1uF ceramic capacitor is recommended to bypass the supply voltage. Place the bypassing capacitor physically near the IC.

An internal linear regulator regulates the supply voltage into a 4.2V voltage VDD for internal control logic circuit. No external bypass capacitor is required for filtering the VDD voltage.

The uP1540 integrates MOSFET gate drives that are powered from the VCC pin and support 12V+12V driving capability. A bootstrap diode is embedded to facilitate PCB design and reduce the total BOM cost. The embedded bootstrap diode is a Schottky diode. Converters that consist of uP1540 feature high efficiency without special consideration on the selection of MOSFETs.

Power On Reset and Chip Enable

A power on reset (POR) circuitry continuously monitors the supply voltage at VCC pin. Once the rising POR threshold is exceeded, the uP1540 sets itself to active state and is ready to accept chip enable command. The rising POR threshold is typically 4.2V at VCC rising.

The COMP/EN is a multifunctional pin: control loop compensation and chip enable as shown in Figure 1. An Enable Comparator monitors the COMP/EN pin voltage for chip enable. A signal level transistor is adequate to pull this pin down to ground and shut down the uP1540. An 80uA current source charges the external compensation network with 0.45V ceiling when this pin is released. If the voltage at COMP/EN pin exceeds 0.3V, the uP1540 initiates its softstart cycle.

The 80uA current source keeps charging the COMP pin to its ceiling until the feedback loop boosts the COMP pin higher than 0.45V according to the feedback signal. The current source is cut off when V_{COMP} is higher than 0.6V during normal operation.

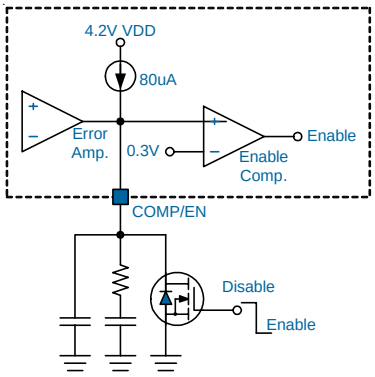


Figure 1. Chip Enable Function

Soft Start

A built-in Soft Start is used to prevent surge current from power supply input during turn on (referring to the Functional Block Diagram). The error amplifier is a three-input device. Reference voltage V_{REF} or the internal soft start voltage SS whichever is smaller dominates the behavior of the non-inverting inputs of the error amplifier. SS internally ramps up to VDD with a slew rate of 0.4V/ms after the softstart cycle is initiated. Accordingly, the output voltage will follow the SS signal and ramp up smoothly to its target level.

The SS signal keeps ramping up after it exceeds the reference voltage V_{REF}. However, the reference voltage V_{REF} takes over the behavior of error amplifier after SS > V_{REF}. When the SS signal climbs to 1.3 x V_{REF}, the uP1540 claims the end of softstart cycle, enables the under voltage protection of the output voltage.

Figure 2 shows a typical start up interval for uP1540 where the COMP/EN pin has been released from a grounded (system shutdown) state.

The internal 80uA current source starts charge the compensation network after the COMP/EN pin is released from grounded at T1. The COMP/EN exceeds 0.3V and enable the uP1540 at T2. The COMP/EN continues ramping up and stays at 0.6V before the SS starts ramping up at T3. The uP1540 initializes itself such as current limit level setting (see the relative section) during the time interval between T2 and T3. The output voltage follows the internal SS and ramps up to its final level during T3 and T4. At T4, the reference voltage V_{REF} takes over the behavior of the error amplifier as the internal SS crosses V_{REF}. The internal SS keeps ramping up and reaches 1.3 x V_{REF} at T5, where the uP1540 asserts the end of softstart cycle.

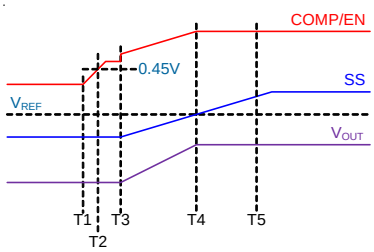


Figure 2. Softstart Behavior of uP1540

Power Input Detection

The uP1540 detects PH voltage for the present of power input when the UG turns on the first time. If the PH voltage does not exceed 2.0V when the UG turns on, the uP1540 asserts that power input in not ready and stops the softstart cycle. Another softstart cycle is initiate after a 4ms time delay.

Output Voltage Selection

An voltage divider sets the output voltage (refer to the Typical Application Circuit on page 3 for detail). In real applications, choose R1 in 1kΩ ~ 10kΩ range and choose appropriate R2 according to the desired output voltage.

$$V_{OUT} = V_{REF} \times \frac{R1+R2}{R2}$$

Over Current Protection (OCP)

The uP1540 monitors the inductor peak current by low side MOSFET $R_{DS(ON)}$ for over current protection when it is turned on. If V_{PHASE} is lower than the user-programmable voltage V_{OCP}, the uP1540 asserts OCP and shuts down the converter by latch-off type. The OCP level can be programmed by OCS pin.

The uP1540 sources a 10uA current source out of OCS pin. Connect resistor R_{OCS} at OCS pin to create voltage level V_{OCS} for OCP setting. The minimum of Vocp is typically 50mV and maximum of Vocp is typically 690mV. The Vocp would be clamped 690mV until V_{OCS} ≥800mV. If V_{OCS} >800mV, the V_{OCP} will be set to 300mV. The OCP level is 5mV per step.

$$V_{OCS} = 10uA \times R_{OCS}$$

$$V_{OCP} = V_{OCS}$$

$$I_{OCP} = \frac{V_{OCP}}{R_{DS(ON)}} \quad (A)$$

For example:

If V_{OCP} = 375mV, and $R_{DS(ON)}$ = 10mΩ, the I_{OCP} will be 37.5A.

If V_{OCP} = 225mV, and $R_{DS(ON)}$ = 10mΩ, the I_{OCP} will be 22.5A.

Over Voltage Protection

The uP1540 continuously monitors FB voltage for over voltage protection. When VCC power on, The OVP level is set 130% of 0.8V, and then it is set 130% of V_{OFS} after VCC reaches to POR threshold over 1ms. When V_{FB} is higher than the OVP level, the uP1540 triggers over voltage protection and the low-side MOSFET is turned on while high-side MOSFET is turned off to discharge the output voltage. OVP is latch-off type and can be reset by POR or toggling the COMP/EN pin.

Under Voltage Protection

After the end of soft-start, the uP1540 continuously monitors FB voltage for under voltage protection. When VCC power on, The UVP level is set 50% of 0.8V, and then it is set 50% of V_{OFS} after VCC reaches to POR threshold over 1ms. When V_{FB} is lower than the UVP level, the uP1540 triggers under voltage protection and turn-off all high-side and low-side MOSFETs. The device will enters hiccup mode until the under-voltage phenomenon is released.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCC ---------- -0.3V to +15V
BOOT to PH ---------- -0.3V to +15V
PH to GND
- DC ---------- -0.5V to 15V
- < 200ns ---------- -10V to 30V

BOOT to GND
- DC ---------- -0.3V to PH + 15V
- < 200ns ---------- -0.3V to 42V

UG to PH
- DC ---------- -0.3V to (BOOT - PH +0.3V)
- <200ns ---------- -5V to (BOOT - PH + 0.3V)

LG to GND
- DC ---------- -0.3V to + (VCC + 0.3V)
- <200ns ---------- -5V to VCC + 0.3V

Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
- WDFN3x3 - 10L θ_{JA} ---------- 68°C/W
- WDFN3x3 - 10L θ_{JC} ---------- 6°C/W

Power Dissipation, P_D @ T_A = 25°C
- WDFN3x3 - 10L ---------- 1.47W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC} ---------- +4.5V to 13.2V
Power Input Voltage, V_{IN} ---------- +3V to 21V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

Guaranteed by Design	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Voltage	V_{CC}		4.5	--	13.2	V
Supply Current	I_{CC}	UG and LG Open, V_{CC} = 12V, Switching	--	2	--	mA
Shut Down Current	I_{CC_SD}	$V_{COMP/EN}$ = 0V	--	--	0.5	mA
Power On Reset						
POR Threshold	V_{CCRTH}	V_{CC} rising	3.9	4.2	4.5	V
POR Hysteresis	V_{CCHYS}		--	0.5	--	V
PWM On-Time						
On-Time	T_{ON}	V_{IN} = 12V, V_{OUT} = 1V, Freq = 300kHz	--	278	--	ns
Minimum Off Time	T_{OFF_MIN}		--	400	--	ns
Reference Voltage						
Internal Reference Voltage	V_{REFOUT}		0.792	0.80	0.808	V
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by Design	55	70	--	dB
Gain-Bandwidth Product	GBW	Guaranteed by Design	--	10	--	MHz
Slew Rate	SR	Guaranteed by Design	3	6	--	V/us
Transconductance			--	2400	--	uA/V
Maximum Output Source Current		$V_{FB} < V_{OFS}$	150	--	--	uA
Maximum Output Sink Current		$V_{FB} > V_{OFS}$	150	--	--	uA
Input Offset Voltage			-1.0	0	1.0	mV
Input Leakage Current		Guaranteed by Design	--	0.1	1.0	nA
MOSFET Gate Drivers						
Upper Gate Source	R_{UG_SRC}	I_{UG} = 100mA Source	--	3	5	Ω
Upper Gate Sink	R_{UG_SNK}	I_{UG} = 100mA Sink	--	1.5	3	Ω
Lower Gate Source	R_{LG_SRC}	I_{LG} = 100mA Source	--	3	5	Ω
Lower Gate Sink	R_{LG_SNK}	I_{LG} = 100mA Sink	--	1	2	Ω
UG Falling to LG Rising Delay		$V_{PH} < 1.2V$ to $V_{LG} > 1.2V$	--	30	--	ns
LG Falling to UG Rising Delay		$V_{LG} < 1.2V$ to $(V_{UG} - V_{PH}) > 1.2V$	--	30	--	ns
REFOUT						
Source Current			--	2.56	--	mA
Sink Current			--	2.56	--	mA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Soft Start						
Soft Start Time			--	2.0	--	ms
Protection						
Under Voltage Protection	V_{FB_UVP}	Percentage of V_{OFS}	--	50	--	%
Under Voltage Protection Delay			--	10	--	us
Over Voltage Protection	V_{FB_OVP}	Percentage of V_{OFS}	--	130	--	%
Over Voltage Protection Delay			--	10	--	us
OCP Programmable Range	V_{OCP}		-690	--	-50	mV
OCS Source Current for OCP Setting	I_{OCS}		--	10	--	uA
OCP Delay Time			--	10	--	us
Over Temperature Protection			--	160	--	°C
ENABLE Control						
Enable Threshold	V_{ENRTH}	$V_{COMP/EN}$ rising	0.45	--	--	V
Disable Threshold	V_{DSFTH}	$V_{COMP/EN}$ falling	--	--	0.15	V

Component Selection Guidelines

The selection of external component is primarily determined by the maximum load current and begins with the selection of power MOSFET switches. The desired amount of ripple current and operating frequency largely determines the inductor value. Finally, C_{IN} is selected for its capability to handle the large RMS current into the converter and C_{OUT} is chosen with low enough ESR to meet the output voltage ripple and transient specification.

Power MOSFET Selection

The uP1540 requires two external N-channel power MOSFETs for upper (controlled) and lower (synchronous) switches. Important parameters for the power MOSFETs are the breakdown voltage $V_{(BR)DSS}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, maximum current $I_{DS(MAX)}$, gate supply requirements, and thermal management requirements.

The gate drive voltage is supplied by VCC pin that receives 4.5V~13.2V supply voltage. When operating with a 7~13.2V power supply for VCC, a wide variety of NMOSFETs can be used. Logic-level threshold MOSFET should be used if the input voltage is expected to drop below 7V. Caution should be exercised with devices exhibiting very low $V_{GS(ON)}$ characteristics. The shoot-through protection present aboard the uP1540 may be circumvented by these MOSFETs if they have large parasitic impedances and/or capacitances that would inhibit the gate of the MOSFET from being discharged below its threshold level before the complementary MOSFET is turned on. Also avoid MOSFETs with excessive switching times; the circuitry is expecting transitions to occur in under 30ns or so.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components: conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty cycle. Since the uP1540 is operating in continuous conduction mode, the duty cycles for the MOSFETs are:

$$D_{UP} = \frac{V_{OUT}}{V_{IN}};\ D_{LOW} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The resulting power dissipation in the MOSFETs at maximum output current are:

$$P_{UP} = I_{OUT}^2 \times R_{DS(ON)} \times D_{UP} + 0.5 \times I_{OUT} \times V_{IN} \times T_{SW} \times f_{OSC}$$

$$P_{LOW} = I_{OUT}^2 \times R_{DS(ON)} \times D_{LOW}$$

where T_{SW} is the combined switch ON and OFF time.

Both MOSFETs have I^2R losses and the upper MOSFET includes an additional term for switching losses, which are largest at high input voltages. The lower MOSFET losses are greatest when the bottom duty cycle is near 100%, during a short-circuit or at high input voltage. These equations assume linear voltage current transitions and do not adequately model power loss due the reverse-recovery of the lower MOSFET's body diode.

Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

The gate-charge losses are mainly dissipated by the uP1540 and don't heat the MOSFETs. However, large gate charge increases the switching interval, T_{SW} that increases the MOSFET switching losses. The gate-charge losses are calculated as:

$$P_{G\_C} = V_{CC} \times \left[V_{CC} \times \left(C_{ISS\_UP} + C_{ISS\_LO}\right) + V_{IN} \times C_{RSS\_UP}\right] \times f_{OCS}$$

where C_{ISS_UP} is the input capacitance of the upper MOSFET, C_{ISS_LOW} is the input capacitance of the lower MOSFET, and C_{RSS_UP} is the reverse transfer capacitance of the upper MOSFET. Make sure that the gate-charge loss will not cause over temperature at uP1540, especially with large gate capacitance and high supply voltage.

Output Inductor Selection

Output inductor selection usually is based on the considerations of inductance, rated current, size requirements and DC resistance (DCR).

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{1}{f_{OSC} \times L_{OUT}} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 20% of $I_{OUT(MAX)}$.

There is another tradeoff between output ripple current/ voltage and response time to a transient load. Increasing the value of inductance reduces the output ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

Application Information

Maximum current ratings of the inductor are generally specified in two methods: permissible DC current and saturation current. Permissible DC current is the allowable DC current that causes 40°C temperature raise. The saturation current is the allowable current that causes 10% inductance loss. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current.

The size requirements refer to the area and height requirement for a particular design. For better efficiency, choose a low DC resistance inductor. DCR is usually inversely proportional to size.

Input Capacitor Selection

The synchronous-rectified Buck converter draws pulsed current with sharp edges from the input capacitor, resulting in ripples and spikes at the input supply voltage. Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time upper MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs to avoid the stray inductance along the connection trace.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck converter is calculated as:

$$I_{IN(RMS)} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{IN(REMS)} = I_{OUT(RMS)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

For a through-hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can also be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

Output Capacitor Selection

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The equivalent ripple current into the output capacitor is half of the inductor ripple current while the equivalent frequency is double of phase operation frequency due to two phase operation The output ripple DV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} = \frac{\Delta I_L}{2}\left(ESR + \frac{1}{16 \times f_{OSC} \times C_{OUT}}\right)$$

Since DI_L increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout. Modern components and loads are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes.

Bootstrap Capacitor Selection

An external bootstrap capacitor C_{BOOT} connected to the BOOT pin supplies the gate drive voltage for the upper MOSFET. This capacitor is charged through the internal diode when the PH node is low. When the upper MOSFET turns on, the PH node rises to V_{IN} and the BOOT pin rises to approximately $V_{IN} + V_{CC}$. The boot capacitor needs to store about 100 times the gate charge required by the upper MOSFET. In most applications 0.47mF to 1mF, X5R or X7R dielectric capacitor is adequate.

Checking Transient Response

Application Information

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to DI_{LOAD}x(ESR), where ESR is the effective series resistance of C_{OUT}. DI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value.

During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

PCB Layout Considerations

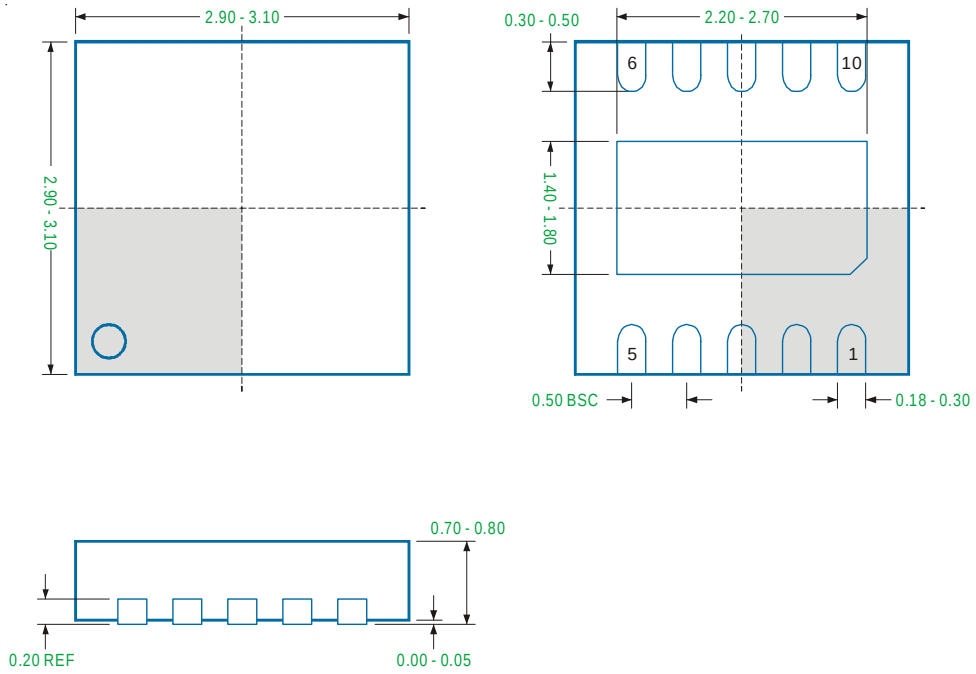
High speed switching and relatively large peak currents in a synchronous-rectified buck converter make the PCB layout a very important part of design. Fast current switching from one device to another in a synchronous-rectified buck converter causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise that result in overvoltage stress on devices. Careful component placement layout and printed circuit board design minimizes the voltage spikes induced in the converter.

Follow the layout guidelines for optimal performance of uP1540.

- The upper and lower MOSFETs turn on/off and conduct pulsed current alternatively with high slew rate transition. Any inductance in the switched current path generates a large voltage spike during the switching. The interconnecting wires indicated by red heavy lines conduct pulsed current with sharp transient and should be part of a ground or power plane in a printed circuit board to minimize the voltage spike. Make all the connection the top layer with wide, copper filled areas.
- Place the power components as physically close as possible.
  - Place the input capacitors, especially the high frequency ceramic decoupling capacitors, directly to the drain of upper MOSFET ad the source of the lower MOSFET. To reduce the ESR replace the single input capacitor with two parallel units
  - Place the output capacitor between the converter and load.
- Place the uP1540 near the upper and lower MOSFETs with UG and LG facing the power components. Keep the components connected to noise sensitive pins near the uP1540 and away from the inductor and other noise sources.
- Use a dedicated grounding plane and use vias to ground all critical components to this layer. The ground plane layer should not have any traces and should be as close as possible to the layer with power MOSFETs. Use an immediate via to connect the components to ground plane including GND of uP1540. Use several bigger vias for power components.
- Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes to maintain good voltage filtering and to keep power losses low. Also, for higher currents, it is recommended to use a multilayer board to help with heat sinking power components.
- The PH node is subject to very high dV/dt voltages. Stray capacitance between this island and the surrounding circuitry tend to induce current spike and capacitive noise coupling. Keep the sensitive circuit away from the PH node and keep the PCB area small to limit the capacitive coupling. However, the PCB area should be kept moderate since it also acts as main heat convection path of the lower MOSFET.
- The uP1540 sources/sinks impulse current with 2A peak to turn on/off the upper and lower MOSFETs. The connecting trance between the controller and gate/source of the MOSFET should be wide and short to minimize the parasitic inductance along the traces.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component.
- Provide local VCC decoupling between VCC and GND pins. Locate the capacitor, C_{BOOT} as close as possible to the BOOT and PH pins.

Package Information

WDFN3x3 - 10L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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