Synchronous Buck Controller with 3A VTT LDO for Memory Power Solution

General Description

The uP1561 is a high performance synchronous buck controller with 3A source/sink VTT LDO for memory systems power. It also provides the buffered low noise reference. The uP1561 has wide operation ranging from 3.0V to 26V for input power and 0.75V~3.0V for memory output voltage.

The synchronous buck of the uP1561 adopts constant-on-time PWM scheme that features easy-to-use, low external component count, fast transient response and quasi- constant frequency operation over the operation range or in current mode to support ceramic output capacitors.

The 3A source/sink VTT LDO has fast transient response, requiring only two 10uF of ceramic output capacitors. In addition, the LDO supply input is available externally to significantly reduce the total power losses. The uP1561 supports all the sleep state controls, in S3 state (suspend to RAM) VTT is at high-Z and in S4/S5 (suspend to disk) VDDQ, VTT and VTTREF soft off.

The uP1561 has complete functions including under voltage protection, over current protection, over voltage protection, power-up sequencing, power OK output, and thermal shutdown. The uP1561 is available in VQFN4x4-24L and WQFN3x3-20L packages.

Applications

- **Desktop PCs, Notebooks, and Workstations**
- **Microprocessor and Chipset Supplies**
- **DDR3/DDR2 Memory Power Supplies**
- **SSTL-2 SSTL-18 and HSTL Bus Termination**

Features

- **Synchronous Buck Controller (VDDQ)**
  - **Wide Input Voltage Range 3.0V to 26V**
  - **Fast Load Transient Response**
  - **Current Mode Option Supports Ceramic Output Capacitors**
  - **Soft-Off in S4/S5 States**
  - **$R_{DS(ON)}$ Current Sensing Technique**
  - **1.5V (DDR3), 1.8V (DDR2) Fixed Output or Adjustable Output (0.75V to 3.0V)**
  - **POK, OVP, and UVP**
- **3A LDO (VTT)**
  - **3A Source/Sink Capability**
  - **Two 10uF Ceramic Output Capacitors**
  - **Support High Z in S3 and Soft-Off in S4/S5**
  - **Thermal Shutdown**
  - **±20mV Accuracy**
- **Reference Voltage (VTTREF)**
  - **±20mV Accuracy**
  - **Low Noise ±10mA Output**

Ordering Information

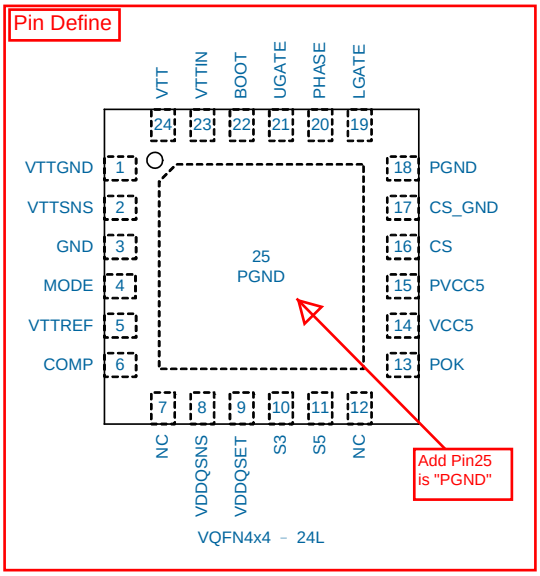
Order Number	Package Type	Remark
uP1561PQAG	VQFN4x4-24L	
uP1561QQKF	WQFN3x3-20L	

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

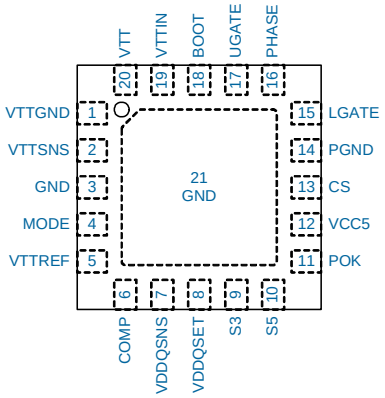
The symbol arrange same as 74.51116.073
The pin define same as spec.

Pin Configuration

Pin Define

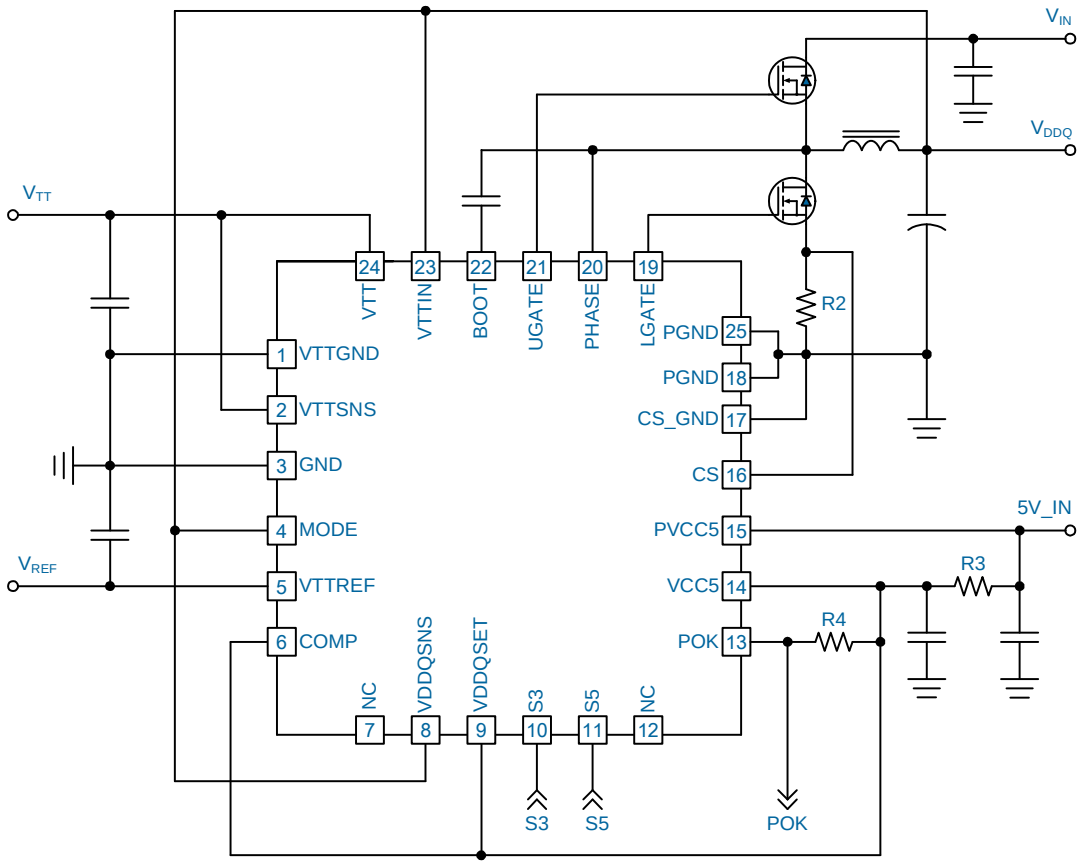


VQFN4x4 – 24L



WQFN3x3 – 20L

Typical Application Circuit



VQFN4x4-24L

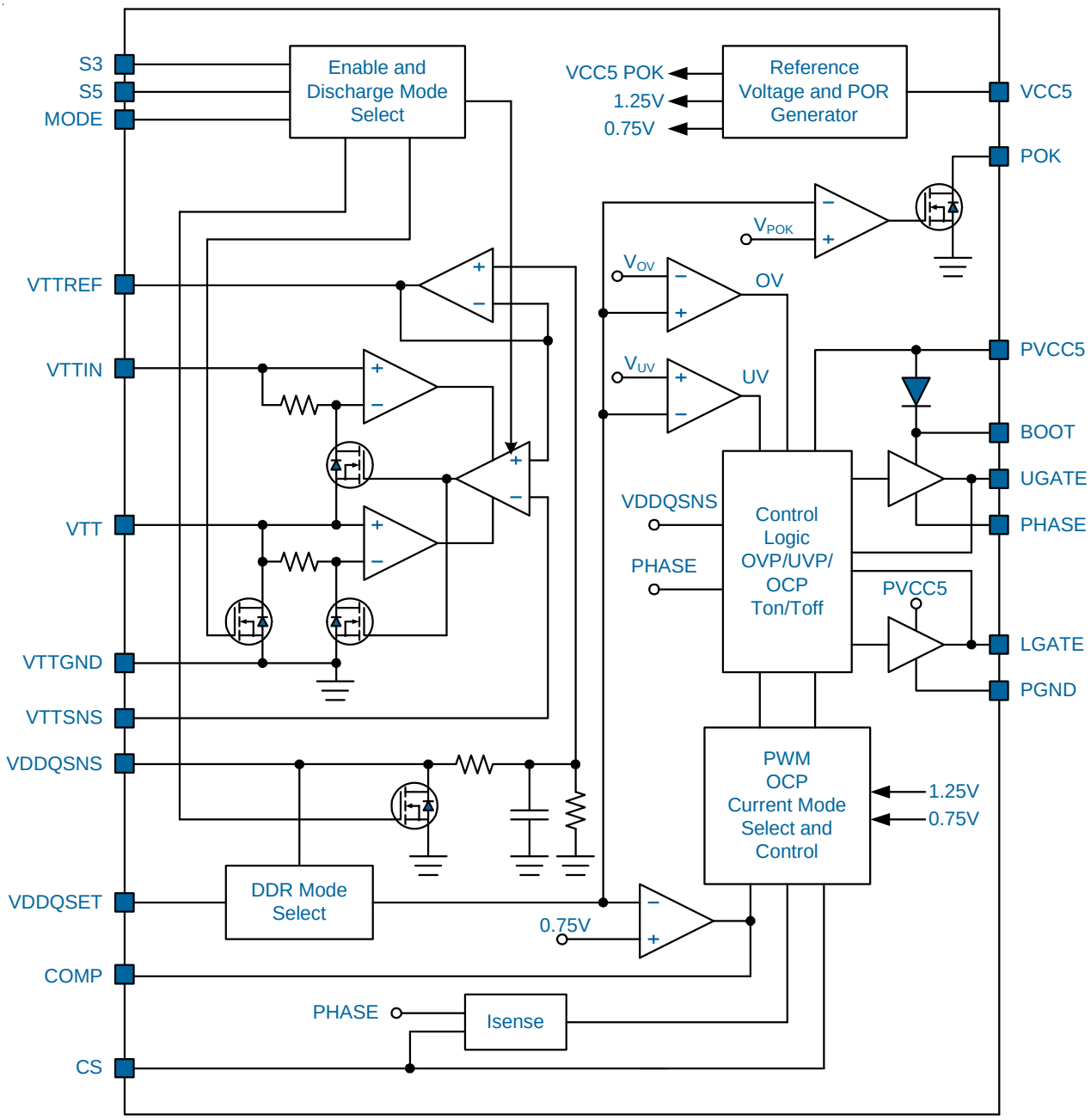
Functional Pin Description

Pin Name	Pin Function
VTTGND	**Power Ground for the VTT LDO.**
VTTSNS	**Positive Terminal of VTT LDO Sense Feedback.** Connect to plus terminal of the VTT LDO output capacitors.
GND	**Negative Terminal of VTT LDO Sense Feedback.** Connect to minus terminal of the VTT LDO output capacitor.
MODE	**Discharge Mode Setting.** No Discharge: Connect this pin to VCC5. Tracking Discharge: Connect this pin to VDDQ. Non Tracking Discharge: Connect this pin to GND.
VTTREF	**VTT Buffered Reference Output.** Bypass this pin with a 0.033uF ceramic capacitor to GND. This pin is capable of sourcing up to 10mA current for external loads.
COMP	**Trans-conductance Amplifier Output.** Connect to VCC5 to disable GM amplifier and use constant on time mode. Use this pin in combination with the FB pin to compensate the control loop of the converter.
NC	**Not Internally Connected.**
VDDQSNS	**VDDQ Reference Input for VTT and VTTREF.** Power supply for the VTTREF. Discharge current sinking terminal for VDDQ Non-tracking discharge. Output voltage feedback input for VDDQ output if VDDQSET pin is connected to VCC5 or GND.
VDDQSET	**VDDQ Output Voltage Setting.** 1.5V fixed voltage: Connect this pin to GND 1.8V fixed voltage: Connect this pin to VCC5 Adjustable voltage: Connect this pin to center of two resistors voltage divider from VDDQ to GND.
S3	**S3 Signal Input.** Connect this pin to the computer system's SLP_S3 signals .This pin companied with S5 switches the IC's operating state from active (S0, S1/S2) to S3 and S4/S5 sleep states.
S5	**S5 Signal Input.** Connect this pin to the computer system's SLP_S5 signals .This pin companied with S3 switches the IC's operating state from active (S0, S1/S2) to S3 and S4/S5 sleep states.
NC	**Not Internally Connected.**
POK	**VDDQ Power OK Indicator.** This pin is an open drain output. When VDDQ output voltage is within the target range, it is set to high state.
VCC5	**5V Power Supply Input.** This pin provides power for internal circuit. Bypass this pin with a 1uF ceramic capacitor to GND.
PVCC5	**Supply voltage for the MOSFET driver.** Connect a 5V power source to the PVCC5 pin. Make sure that both VCC5 and PVCC5 are bypassed with 1uF MLCC capacitors.
CS	**Over Current Protection Setting:** Over current trip voltage setting input for $R_{DS(ON)}$ current sense if connected to VCC5 through the voltage setting resistor.
CS_GND	**Over Current Protection Setting GND:** Over current trip voltage setting input GND for $R_{DS(ON)}$ current sense.

Functional Pin Description

Pin Name	Pin Function
PGND	**Power Ground of MOSFET Gate Driver.**
LGATE	**Lower Gate Driver Output for Synchronous Buck.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
PHASE	**Switch Node for Synchronous Buck.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. A Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.
UGATE	**Upper Gate Driver Output for Synchronous Buck.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
BOOT	**Bootstrap Supply** for the floating upper gate driver of synchronous buck. Connect the bootstrap capacitor C_{BOOT} between BOOT pin and the PHASE pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Ensure that C_{BOOT} is placed near the IC.
VTTIN	**Input for the VTT LDO.** This is the drain input to the power device that supplies current to the output pin.
VTT	**Output for the VTT LDO.** Typical value of two 10uF ceramic capacitors are recommended to reduce the effects of current transients on V_{OUT}. A pull low resistance exists when the device is disabled.
Exposed Pad PGND	**Power Ground.** The exposed pad is the dominant heat conduction path of the IC and should be well soldered to the PCB for optimal thermal performance.

Functional Block Diagram



Functional Description

The uP1561 is a high performance synchronous buck controller with 3A source/sink VTT LDO for memory systems power. It also provides the buffered low noise reference with 10mA capability.

The buck controller adopts constant-on-time PWM scheme that features easy-to-use, low external component count, fast transient response and quasi-constant frequency operation over the operation range or in current mode to support ceramic output capacitors.

The 3A source/sink VTT LDO has fast transient response that only requires two 10uF of ceramic output capacitors.

The reference voltage tracks VDDQ/2 within 1% of VDDQ. The VTT tracks VTTREF within 20mV at no load condition and within 40mV over all load conditions.

The uP1561 supports all the sleep state controls, and also has complete functions including over current protection, over voltage protection, thermal shutdown, power-up sequencing, power OK output, and thermal shutdown. The uP1561 is available in space-saving VQFN4X4-24L and WQFN3x3-20L package.

Soft Start and POK

The soft start function of the uP1561 SMPS is achieved by two-stage current clamp and ramping up reference as shown in Figure 1. It takes about 40us for the V_{DDQ} to ramp up after S5 is set high.

At the first stage, the reference voltage is set as 87% of nominal level (650mV) and the current clamp level is set as 1/2 of nominal level. The output voltage ramping-up slew rate is decided by the current clamp level and the output capacitors.

When the uP1561 detects V_{DDQ} becoming greater than 80% of its target value, the second stage begins and the reference voltage ramps up raised toward 750mV. The output voltage ramping-up slew rate is decided by the ramping up reference voltage. When the V_{DDQ} is above 95% of its target level, the uP1561 asserts soft start end and set the current clamp to its nominal level. It takes about 100us for the V_{DDQ} to ramp up from 87% to 95%. The uP1561 turns off the POK open-drain MOS 45us after the soft start end. Consequently, the total soft start time (from S5 high to POK high) can be calculated as:

$$T_{VDDQSS} = \frac{2 \times C_{VDDQ} \times V_{VDDQ} \times 0.87}{I_{VDDQLIM}} + 185us$$

where $I_{VDDQLIM}$ is the current limit value for VDDQ switcher. Please see the *Output Current Limit* section for detail calculation of $I_{VDDQLIM}$.

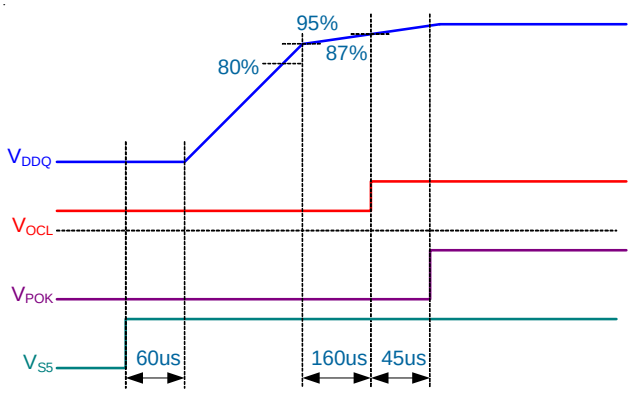


Figure 1. VDDQ Soft Start and POK Timing

The soft-start function of the VTT LDO is achieved by current limit. The current limit threshold is also changed in two stages. When VTT is below the internal power OK threshold, the current limit level is 60% (2.2A). When the output comes up to the good state to target value, the current limit level is released to normal value (3.8A). The POK signal indicates only the status of VDDQ.

Consequently, the total soft start time of VTT LDO can be calculated as:

$$T_{VTTSS} = \frac{C_{VTT} \times V_{VTT}}{I_{VTTOCL}}$$

where I_{VTTOCL} is 2.2A (typ). In the above calculations, no load current during start-up are assumed. **Note that both switcher and the LDO do not start up with full load condition.**

Dual Operation Modes VDDQ

The uP1561 synchronous buck supports two control schemes which would be a current mode and a constant on time mode. Constant on time mode is used for low external component count configuration with the appropriate output capacitor ESR. Current mode control can be used to achieve stable operation with very low ESR capacitor such as ceramic capacitors.

Two operation modes are chosen by COMP pin connection. Connect this pin to VCC5, constant on time mode is selected, otherwise it works in current mode.

Constant on time control scheme is easy to use due to simple control logic. At beginning of switching cycle, the upper MOSFET is turned on at fixed on time which is determined by V_{IN} and V_{OUT} voltages. The upper MOSFET is turned off again when IC get insufficient output voltage. Current mode control is to sense feedback voltage and inductor current information for output voltage regulation.

Functional Description

VDDQ Light Load Operation

The uP1561 automatically reduces switching frequency at light load to maintain high efficiency. As the load current decreased, the rectifying MOSFET would be turned off when zero inductor current is detected, the converter runs in discontinuous conduction mode and it takes long time to discharge the output capacitor to next ON cycle.

The transition point from discontinuous to continuous conduction mode can be calculated as:

$$I_{OUT} = \frac{1}{2 \times f_{OSC} \times L_{OUT}} \times V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

VDDQ Output Voltage Selection

The uP1561 connects VDDQSET pin as shown in Table 1 for DDR2 and DDR3 and adjustable applications.

Table 1. Output Voltage Selection

VDDQSET	V_{DDQ} (V)	V_{TTREF} and V_{TT}	Note
GND	1.5	V_{DDQSNS}/2	DDR3
VCC5	1.8	V_{DDQSNS}/2	DDR2
FB Resistors	Adjustable	V_{DDQSNS}/2	0.75V < V_{DDQ} < 3V

Outputs Control by S3, S5

The uP1561 provides the output management for the sleep-mode signals such as SLP_S3 and SLP_S5 in the notebook PC system by monitoring S3, S5 status, the output control table is as shown below.

State	S3	S5	VDDQ	VTTREF	VTT
S0	High	High	On	On	On
S3	Low	High	On	On	Off (Hi-Z)
S4 S5	Low	Low	Off (discharge)	Off (discharge)	Off (discharge)

VDDQ and VTT Discharge Control

There are two different discharge modes which are set by MODE pin connection. In tracking-discharge mode, the uP1561 discharges outputs through the internal VTT regulator transistors and VTT output tracks half of VDDQ voltage during this discharge. Note that VDDQ discharge current flows via VTTIN to VTTGND thus VTTIN must be connected to VDDQ output in this mode. In non-tracking-discharge mode, the uP1561 discharges outputs using internal MOSFETs which are connected to VDDQSNS and VTT.

MODE	Discharge Mode
VCC5	No Discharge
VDDQ	Tracking Discharge
GND	Non Tracking Discharge

Output Current Limit

The uP1561 synchronous buck VDDQ monitors the inductor current by lower MOSFET $R_{DS(ON)}$ when it turns on. The over current limit is triggered once the sensing current level is higher than V_{OCSET}. When triggered, the over current limit will keep upper MOSFET off even the voltage loop commands it to turn on.

The output voltage will decrease if the load continuously demands more current than current limit level. The current limit level is set at I_{LIM}/2 if the outupt voltage is lower than 90% of its target level, letting V_{OUT} decrease faster until UVP occurs and shuts down the uP1561.

The uP1561 features two different current limit level configurations: using an external resistor or lower MOSFET $R_{DS(ON)}$ as a current sensing slements. The configurations are selected by the connection of CS pin.

A. Connect CS to VCC5 with R1 to select $R_{DS(ON)}$ configuration. The CS pin will sink a 10uA current source and create a voltage drop across R1 as the V_{OCSET}.

V_{OCSET} = 10uA x R1.

The voltage across PHASE and PGND pins is compared with V_{OCSET} for current limit. The current limit level is calculated as:

$$I_{LIM} = \frac{V_{OCSET}}{R_{DS(ON)}} + \frac{I_{RIPPIE}}{2}$$

where I_{RIPPLE} is the peak-to-peak inductor ripple current at steady state.

B. Connect CS to source of lower MOSFET to select external resistor sensing configuration. A current sensing resistor R2 between CS and PGND is required for this configuration. The voltage across CS and PGND is compared with a fixed 60mV V_{OCSET} for current limit.

$$I_{LIM} = \frac{V_{OCSET}}{R2} + \frac{I_{RIPPIE}}{2} = \frac{60mV}{R2} + \frac{I_{RIPPLE}}{2}$$

The LDO has an internally fixed constant overcurrent limiting of 3.8 A while operating at normal condition. This trip point is reduced to 2.2A before the output voltage comes within 5% of the target voltage or goes outside of 10% of the target voltage.

Over Voltage/Under Voltage Protection

The uP1561 monitors a resistor divided feedback voltage to detect overvoltage and undervoltage. When VDDQSET is connected to VCC5 or GND, the feedback voltage is from an internal resistor divider inside VDDQSNS pin. When an external resistor divider is connected to VDDQSET pin, the feedback voltage is VDDQSET voltage itself.

When the feedback voltage becomes higher than 115% of the target voltage, the OVP is triggered, high side MOSFET is off and low side MOSFET is on. When the feedback voltage is lower than 70% of the target voltage, the UVP is triggered after 80us fault detection, high side MOSFET and low side MOSFET are latched. This function is enabled after 1007 cycles of SMPS operation to ensure startup.

VCC5 UVLO

The uP1561 has VCC5 under voltage lockout protection (UVLO). When the VCC5 voltage is lower than UVLO threshold voltage, all functions are turned off. This is non-latch protection.

Thermal Protection

The uP1561 monitors the temperature of itself. If the temperature exceeds typical 160^{O}C, the uP1561 will be turned off. This is non-latch protection.

Absolute Maximum Rating

Supply Input Voltage, V_{IN} (Note1) ---------- -0.3V to +28V
BOOT to PHASE ---------- -0.3V to (PVCC5 + 0.3V)
PHASE to GND
DC ---------- -0.3V to 28V
< 100ns ---------- -5V to 38V
LGATE to GND
DC ---------- -0.3V to (PVCC5 + 0.3V)
< 100ns ---------- -2V to (PVCC5 + 2V)
Other Pins ---------- -0.3V to +6V
Storage Junction Temperature Range ---------- -65°C to +150°C
Lead Temperature Range(Soldering 10sec) ---------- 260°C
ESD Rating (Note2)
HBM(Human Body Mode)----------2KV
MM(Mechine Mode)----------200V

Thermal Information

Package Thermal Resistance (Note 3)
VQFN4x4-24L θ_{JA} ---------- 40°C/W
VQFN4x4-24L θ_{JC} ---------- 4°C/W
VQFN3x3-20L θ_{JA} ---------- 68°C/W
VQFN3x3-20L θ_{JC} ---------- 6°C/W
Power Dissipation, P_D @ T_A = 25°C
VQFN4x4-24L ---------- 2.50W
VQFN3x3-20L ---------- 0.81W

Recommended Operation Conditions

Input Voltage ---------- 3.0V to 26V
Operating Junction Temperature Range (Note 4) ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{PVCC5} = V_{VCC5} = 5V, VTTIN is connected to VDDQ output, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
Supply Current 1, VCC5	I_{VCC51}	No load, V_{S3} = V_{S5} = 5V, COMP connected to capacitor.	0.5	0.8	2	mA
Supply Current 2, VCC5	I_{VCC52}	No load, V_{S3} = 0V, V_{S5} = 5 V, COMP connected to capacitor.	200	300	600	uA
Supply Current 3, VCC5	I_{VCC53}	No load, V_{S3} = 0V, V_{S5} = 5 V, V_{COMP} = 5V	150	250	500	uA
Shutdown Current, VCC5	I_{VCC5_SD}	No load, V_{S3} = V_{S5} = 0V	--	0.1	1.0	uA
Supply Current 1, VTTIN	I_{VTTIN1}	No load, V_{S3} = V_{S5} = 5V	--	0.1	10	uA
Supply Current 2, VTTIN	I_{VTTIN2}	No load, V_{S3} = 5V, V_{S5} = 0V	--	0.1	10	uA
Standby Current, VTTIN	I_{VTTIN_SD}	No load, V_{S3} = V_{S5} = 0V	--	0.1	1.0	uA
VTTREF Output						
Output voltage, VTTREF	V_{VTTREF}	V_{IN} = 5.5V to 26V	$V_{VDDQSNS}$/2			V
Output Voltage Tolerance	$V_{VTTREFTO}$	-10mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 1.5V, Tolerance to $V_{VDDQSNS}$/2	-15	--	15	mV
		-10mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 1.8V, Tolerance to $V_{VDDQSNS}$/2	-18	--	18	mV
Source Current	$V_{VTTREFSRC}$	$V_{VDDQSNS}$ = 1.5V, V_{VTTREF} = 0V	-80	-30	-20	mA
Sink Current	$V_{VTTREFSNK}$	$V_{VDDQSNS}$ = 1.5V, V_{VTTREF} = 1.5V	20	40	80	mA
VTT Output						
Output Voltage, VTT	V_{VTTSNS}	V_{S3} = V_{S5} = 5V, V_{VTTIN} = $V_{VDDQSNS}$ = 1.5V	--	0.75	--	V
		V_{S3} = V_{S5} = 5V, V_{VTTN} = $V_{VDDQSNS}$ = 1.8V	--	0.9	--	V
VTT Output Voltage Tolerance to VTTREF	$V_{VTTTOL15}$	V_{S3} = V_{S5} = 5V, I_{VTT} = 0A	-20	--	20	mV
		V_{S3} = V_{S5} = 5V, | I_{VTT} | = 0A < 1.5A	-30	--	30	mV
		V_{S3} = V_{S5} = 5V, | I_{VTT} | = 0A < 3A	-40	--	40	mV
VTT Output Voltage Tolerance to VTTREF	$V_{VTTTOL18}$	V_{S3} = V_{S5} = 5V, I_{VTT} = 0A	-20	--	20	mV
		V_{S3} = V_{S5} = 5V, | I_{VTT} | = 0A < 1A	-30	--	30	mV
		V_{S3} = V_{S5} = 5V, | I_{VTT} | = 0A < 2A	-40	--	40	mV
Source Current Limit, VTT	$I_{VTTTOCLSRC}$	V_{VLDOIN} = $V_{VDDQSNS}$ = 1.8V, V_{VTT} = V_{VTTSNS} = 0.85 V, POK = High	3.0	3.8	6.0	A
		V_{VLDOIN} = $V_{VDDQSNS}$ = 1.8V, V_{VTT} = 0V	1.5	2.2	3.0	A
Sink Current Limit, VTT	$I_{VTTTOCLSNK}$	V_{VLDOIN} = $V_{VDDQSNS}$ = 1.8V, V_{VTT} = V_{VTTSNS} = 0.95V, POK = High	3.0	3.6	6.0	A
		V_{VLDOIN} = $V_{VDDQSNS}$ = 1.8V, V_{VTT} = V_{VDDQ}	1.5	2.2	3.0	A
Leakage Current, VTT	I_{VTTLK}	V_{S3} = 0V, V_{S5} = 5V, V_{VTT} = $V_{VDDQSNS}$/2	-10	--	10	uA
Input bias Current, VTTSNS	$I_{VTTBIAS}$	V_{S3} = 5V, V_{VTTSNS} = $V_{VDDQSNS}$/2	-1	-0.1	1	uA
Leakage Current, VTTSNS	$I_{VTTDisch}$	V_{S3} = 0V, V_{S5} = 5V, V_{VTT} = $V_{VDDQSNS}$/2	-1	--	1	uA
Discharge Current, VTT	$I_{VTTDisch}$	V_{S3} = V_{S5} = $V_{VDDQSNS}$ = 0V, V_{VTT} = 0.5V	10	24	--	mA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDDQ Output						
Output Voltage, VDDQ	V_{VDDQ}	$V_{VDDQSET}$ = 0V, No load	1.477	1.500	1.523	V
		$V_{VDDQSET}$ = 5V, No load	1.776	1.800	1.824	V
		Adjustable mode, No load	0.75	--	3.0	V
VDDQSET Regulation Voltage	$V_{VDDQSET}$	Adjustable mode	742.5	750.0	757.5	mV
Input impedance, VDDQSNS	$R_{VDDQSNS}$	$V_{VDDQSET}$ = 0V	--	125	--	kΩ
		$V_{VDDQSET}$ = 5V	--	180	--	kΩ
		Adjustable mode	--	460	--	kΩ
Input Current, VDDQSET	$I_{VDDQSET}$	$V_{VDDQSET}$ = 0.78V, COMP = Open	--	-0.04	--	uA
		$V_{VDDQSET}$ = 0.78V, COMP = 5V	--	-0.06	--	uA
Discharge Current, VDDQ	$I_{VDDQDisch}$	V_{S3} = V_{S5} = 0V, $V_{VDDQSNS}$ = 0.5V, V_{MODE} = 0V	10	40	--	mA
Discharge Current, VTTIN	$I_{VTTINDisch}$	V_{S3} = V_{S5} = 0V, $V_{VDDQSNS}$ = 0.5V, V_{MODE} = 2.5V	200	400	800	mA
Trans-Conductance Amplifier						
Gain	GM		280	340	400	uS
COMP Maximum Sink Current	$I_{COMPSNK}$	V_{S3} = 0V, V_{S5} = 5V, $V_{VDDQSET}$ = 0V, $V_{VDDQSNS}$ = 1.6V, V_{COMP} = 1.28V	--	30	--	uA
COMP maximumsource current	$I_{COMPSRC}$	V_{S3} = 0V, V_{S5} = 5V, $V_{VDDQSET}$ = 0V, $V_{VDDQSNS}$ = 1.4V, V_{COMP} = 1.28V	--	-30	--	uA
COMP high clamp voltage	V_{COMPHI}	V_{S3} = 0V, V_{S5} = 5V, $V_{VDDQSET}$ = 0V, $V_{VDDQSNS}$ = 1.4V, V_{CS} = 0V	1.32	1.35	1.38	V
COMP low clamp voltage	V_{COMPLO}	V_{S3} = 0V, V_{S5} = 5V, $V_{VDDQSET}$ = 0V, $V_{VDDQSNS}$ = 1.6V, V_{CS} = 0V	1.17	1.20	1.23	V
Duty Control						
Operating On-Time	T_{ON}	V_{IN} = 12V, $V_{VDDQSET}$ = 0V	--	300	--	ns
Startup On-Time	T_{ON0}	V_{IN} = 12V, $V_{VDDQSNS}$ = 0V	--	125	--	ns
Minimum On-Time	$T_{ON(min)}$		--	100	--	ns
Minimum Off-Time	$T_{OFF(min)}$		--	350	--	ns
Zero Current Comparator						
Zero Crossing Comparator Offset	V_{ZC_OF}		-6	0	5	mV
Drivers Output						
UGATE Resistance	R_{UGATE}	Source, I_{UGATE} = -100 mA	--	3	6	Ω
		Sink, I_{UGATE} = 100 mA	--	0.6	1.2	Ω
LGATEL Resistance	R_{LGATE}	Source, I_{LGATE} = -100 mA	--	1.5	3	Ω
		Sink, I_{LGATE} = 100 mA	--	0.6	1.2	Ω
Dead Time	T_D	PHASE-low to UGATE-on	--	10	--	ns
		LGATE-off to UGATE-on	--	20	--	ns

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Internal Bootstrape Diode						
Forward Voltage	V_{FBOOT}	$V_{PVCC5-VBOOT}$, I_F = 10mA	0.75	0.85	0.95	V
BOOT Leakage Current	I_{BOOTLK}	V_{BOOT} = 34V, V_{PHASE} = 26V, V_{VDDQ} = 2.6V	--	0.1	1.0	uA
OCP						
Current Limit Threshold	V_{OCL}	$V_{PGND-CS}$, POK = High, V_{CS} < 0.5V	50	60	70	mV
		$V_{PGND-CS}$, POK = Low, V_{CS} < 0.5V	20	30	40	mV
Current Sense Sink Current	I_{TRIP}	V_{CS} > 4.5V, POK = High	9	10	11	uA
		V_{CS}> 4.5V, POK = Low	4	5	6	uA
Trip Current Temperature Co-efficient	TC_{ITRIP}	$R_{DS(ON)}$ sense scheme, On the basis of T_A = 25°C	--	4500	--	ppm/-°C
Overcurrent Protection Comparator Offset	$V_{OCL(off)}$	($V_{VCC5-CS}$-$V_{PGND-PHASE}$), $V_{VCC5-CS}$ = 60mV, V_{CS} > 4.5 V	-9	-4	1	mV
Current Limit Threshold Setting Range	$V_{R(trip)}$	$V_{VCC5-CS}$	30	--	300	mV
POK Comparator						
VDDQ POK Threshold	$V_{TVDDQPOK}$	POK in from lower	93	95	97	%
		POK hysteresis	--	5	--	%
POK Sink Current	$I_{POK(max)}$	V_{VTT} = 0 V, V_{POK} = 0.5 V	2.5	9.0	--	mA
POK Delay Time	$T_{POK(del)}$	Delay for POK in	80	130	200	us
Under Voltage Lockout and Logic Threshold						
VCC5 UVLO Threshold Voltage	V_{UVVCC5}	Wake up	3.7	4.0	4.3	V
		Hysteresis	--	0.3	--	V
Mode Threshold	V_{THMODE}	No discharge	4.7	--	--	V
		Non-tracking discharge	--	--	0.1	V
VDDQSET Threshold Voltage	$V_{THVDDQSET}$	1.5V output	0.15	0.28	0.35	V
		1.8V output	3.5	4.0	4.5	V
High-level Input Voltage	V_{IH}	S3, S5	2.2	--	--	V
Low-level Input Voltage	V_{IL}	S3, S5	--	--	0.3	V
Hysteresis Voltage	V_{IHYST}	S3, S5	--	0.2	--	V
Logic Input Leakage Current	V_{INLEAK}	S3, S5, MODE	-1	--	1	uA
Input Leakage/ Bias Current	$V_{INVDDQSET}$	VDDQSET	-1	--	1	uA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
UVP and OVP						
VDDQ OVP Trip Threshold Voltage	V_{OVP}	OVP detect	115	120	125	%
		Hysteresis	--	5	--	%
VDDQ OVP Propagation Delay	T_{OVPDEL}		--	1.5	--	us
Output UVP Trip Threshold	V_{UVP}	UVP detect	--	70	--	%
		Hysteresis	--	10	--	%
Output UVP Propagation Delay	T_{UVPDEL}		--	80	--	us
Output UVP Enable Delay	T_{UVPEN}		--	3000	--	
Thermal Shuntdown						
Thermal Shutdown Threshold	T_{SDN}	Shutdown temperature	--	160	--	°C
		Hysteresis	--	10	--	°C

Typical Operation Characteristics

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Application Information

PCB Layout Considerations

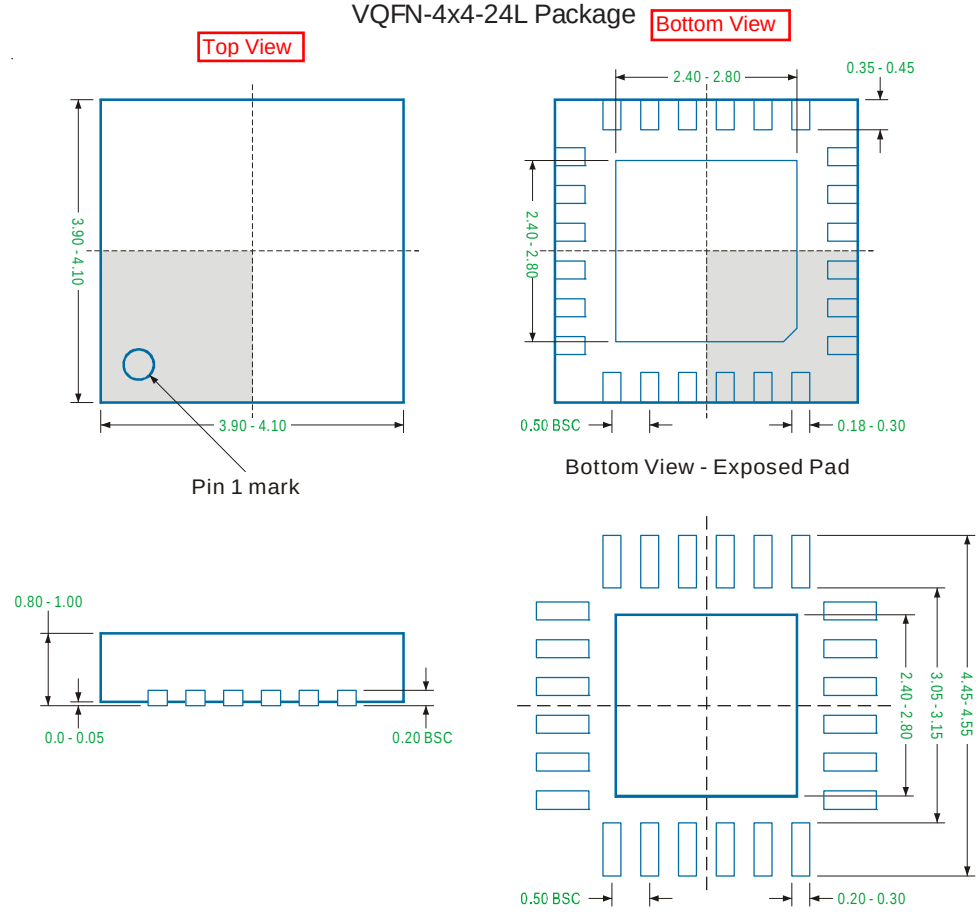
High speed switching and relatively large peak currents in a synchronous-rectified buck converter make the PCB layout a very important part of design. Fast current switching from one device to another in a synchronous-rectified buck converter causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise that result in overvoltage stress on devices. Careful component placement layout and printed circuit board design minimizes the voltage spikes induced in the converter.

Follow the layout guidelines for optimal performance of uP1561.

- Keep the PCB trace PHASE node as short and wide as possible.
- Add a sunbber circuit between PHASE and PGND to eliminate the high frequency voltage spike at PHASE node.
- Keep sensitive analog circuits such as VDDQSNS, VTTSNS and CS away from high voltage switching node such PHASE, UGATE and LGATE.
- Connect VDDQ output to VTTIN with short and wide trace. If other power source is used as VTTIN, a bypass input capacitor should be placed as close to VTTIN as possible.
- Please the output capacitor for VTT should close to the pin with short and wide trace to avoid additional ESR and/or ESL of the trace.
- Connect VTTSNS to the positive of VTT output capacitors with a separate trace.
- VDDQSNS can be connected separately from VTTIN. Remember that this sensing potential is the reference voltage of VTTREF. Avoid any noise generative lines.
- Negative node of VTT output capacitor(s) and VTTREF capacitor should be tied together by avoiding common impedance to the high current path of the VTT source/sink current.
- GND (Signal GND) pin node represents the reference potential for VTTREF and VTT outputs. Connect GND to negative nodes of VTT capacitor(s), VTTREF capacitor and VDDQ capacitor(s) with care to avoid additional ESR and/or ESL. GND and PGND (power ground) should be connected together at a single point.
- Connect CS_GND (RGE) to source of rectifying MOSFET using Kevin connection. Avoid common trace for high-current paths such as the MOSFET to the output capacitors or the PGND to the MOSFET trace. In case of using external current sense resistor, apply the same care and connect it to the positive side (ground side) of the resistor.

Package Information

VQFN-4x4-24L Package

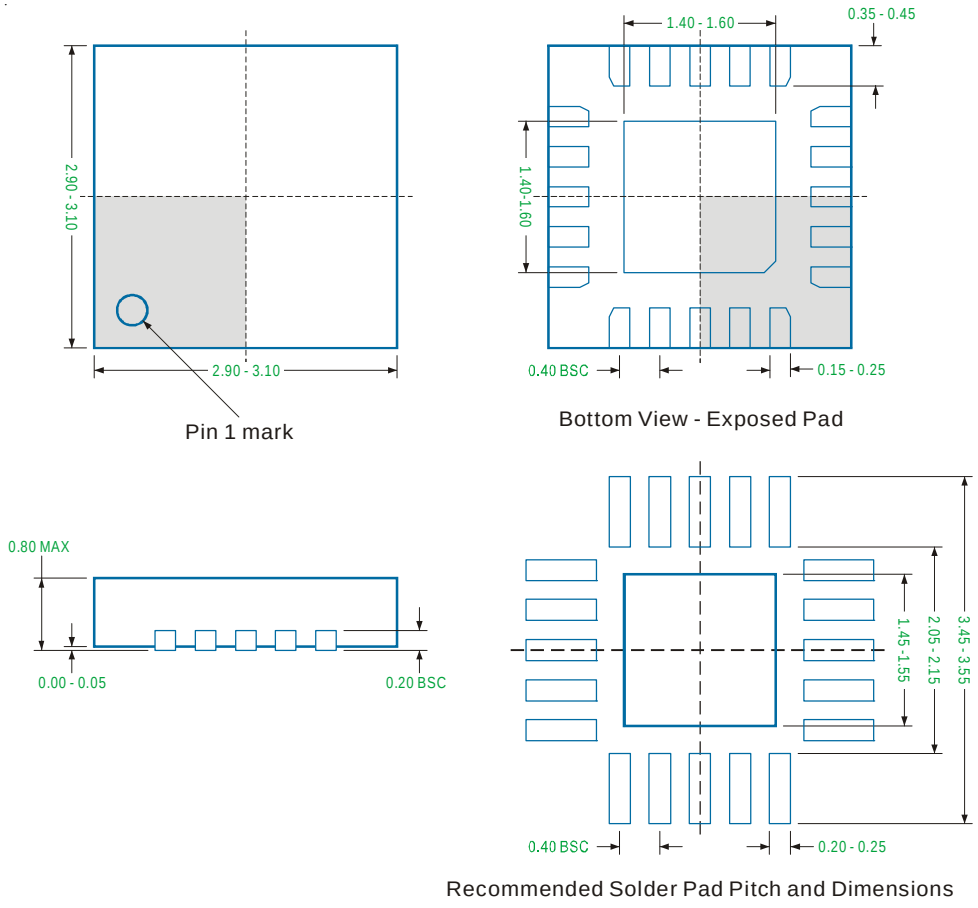


Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.

Package Information

WQFN-3x3-20L Package



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