1/2/3/4-Phase PWM Controller with SMBus Digital Interface Control for VR12.5

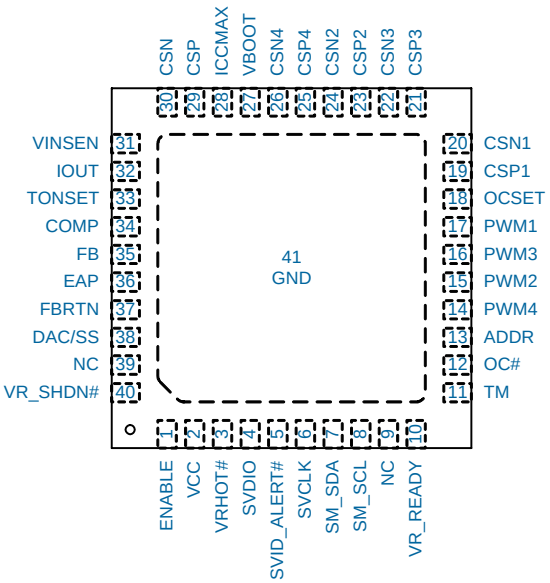
General Description

The uP1649Q is a VR12.5 compliant CPU power controller supports up to 4 phases. The integrated I2C interface programmability makes the uP1649Q high performance and easy design. Designer can define different power scenario for different current states to optimize the performance and efficiency.

The uP1649Q combines true differential voltage sensing, differential inductor DCR current sensing, input voltage feed-forward and adaptive voltage positioning to provide accurately regulated power for desktop CPUs. It adopts uPI proprietary RCOT™ (Robust Constant On-Time) topology to have fast transient response and smooth mode transition. Similar to digital based PWM controller, the loop gain is also programmable by I2C interface to achieve design flexibility.

The uP1649Q provides VR_READY indicator. It also features complete fault protection functions including over voltage, under voltage, over current, over temperature and under voltage lockout. The uP1649Q is available in VQFN5X5 - 40L package.

Pin Configuration



Features

- **Intel VR12.5 Compliant**
- **RCOT™ Control Topology**
  - **Easy Setting**
  - **Smooth Mode Transient**
  - **Fast Transient Response**
- **True Differential Current Balance Sense Amplifier**
- **Differential Remote Voltage Sensing**
- **Build-in ADC for Platform Setting**
- **I2C Interface for Performance and Efficiency Optimization**
  - **Dynamic Programmable VR Parameters**
  - **Programmable Protection Thresholds**
  - **VR Reporting**
  - **Programmable Loop Gain**
- **Enable Control and VR_READY Indicator**
- **H/W OCP Alert for System Protection**
- **System Thermal Management**
- **OCP/OVP/UVP**
- **RoHS Compliant and Halogen Free**

Applications

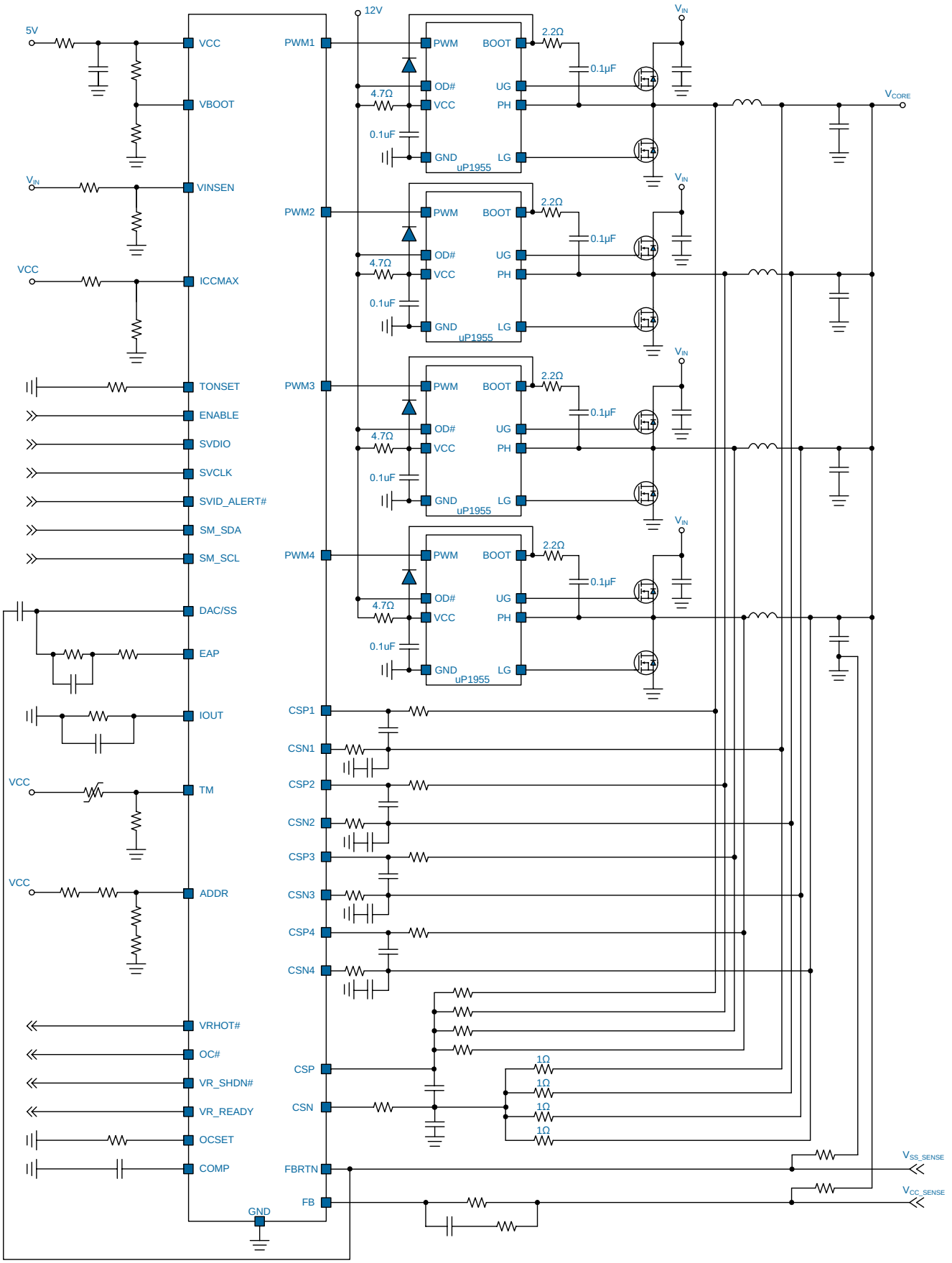
- **Desktop PC Core Power Supplies**

Ordering Information

Order Number	Package Type	Top Marking
uP1649QQGJ	VQFN5x5 - 40L	uP1649Q

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Typical Application Circuit



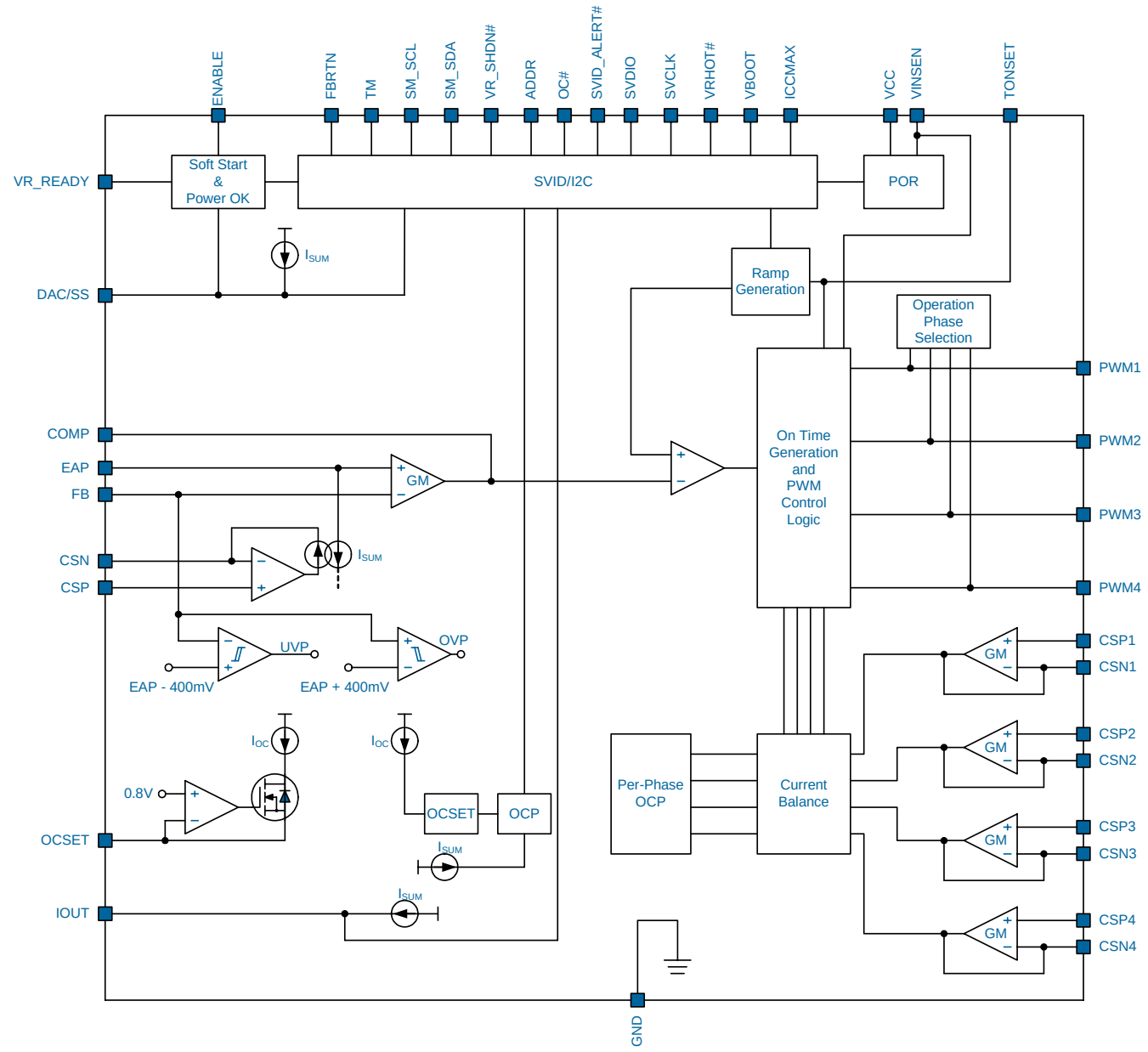
Functional Pin Description

No.	Name	Pin Function
1	ENABLE	**Chip Enable Control.** Pull this pin above 0.8V enables the chip. Connect this pin below 0.3V to disable the chip. It's typically connected to the output of the VTT voltage power rail in the motherboard.
2	VCC	**Supply Input for the IC Control Circuit.** Connect this pin to a 5V voltage source with an RC filter.
3	VRHOT#	**Thermal Indicator.** Open drain logic output and active low output indicating. The uP1649Q asserts VRHOT# when the VR temperature is higher than SMBUS setting threshold programmed by I2C.
4	SVDIO	**SVID Data I/O.**
5	SVID_ALERT#	**SVID Alert# Line.**
6	SVCLK	**SVID Clock.**
7	SM_SDA	**SMBUS Data Input.** This pin is input or output of serial bus data signal.
8	SM_SCL	**SMBUS Clock Input.** This pin receives serial bus clock signal.
9	NC	**Not Internally Connected.**
10	VR_READY	**VR Ready Indicator.** Open drain logic output and active high indicating VR completes soft-start to boot voltage.
11	TM	**Thermal Monitoring Input.** Connect NTC network to this pin for sensing VR temperature. The low resistor recommend value is 6kΩ.
12	OC#	**Over Current Indicator.** This pin is open drain output and is active low for over current indication. OC# will go low when output current is higher than the OCP_L threshold programmed by I2C.
13	ADDR	**SMBUS & SVID Address Setting.** Connect a voltage divider to this pin sets the SMBUS & SVID address.
14	PWM4	**Phase 4 PWM Output.** Connect this pin to PWM input of MOSFET driver.
15	PWM2	**Phase 2 PWM Output.** Connect this pin to PWM input of MOSFET driver.
16	PWM3	**Phase 3 PWM Output.** Connect this pin to PWM input of MOSFET driver.
17	PWM1	**Phase 1 PWM Output.** Connect this pin to PWM input of MOSFET driver.
18	OCSET	**OCP Level Setting.** Connect a resistor R_{OCSET} from this pin to GND for OCP level setting. The resistance value of R_{OCSET} should be the same as the resistor used in IOUT pin setting, i.e. $R_{OCSET} = R_{IOUT}$. Avoid adding any capacitor from the this pin to GND, or the OCP function will not work properly.
19	CSP1	**Phase 1 Positive Differential Current Sense Input.**
20	CSN1	**Phase 1 Negative Differential Current Sense Input.**

Functional Pin Description

No.	Name	Pin Function
21	CSP3	**Phase 3 Positive Differential Current Sense Input.**
22	CSN3	**Phase 3 Negative Differential Current Sense Input.**
23	CSP2	**Phase 2 Positive Differential Current Sense Input.**
24	CSN2	**Phase 2 Negative Differential Current Sense Input.**
25	CSP4	**Phase 4 Positive Differential Current Sense Input.**
26	CSN4	**Phase 4 Negative Differential Current Sense Input.**
27	VBOOT	**Output VBOOT Voltage Setting.** Connect a resistor voltage divider from VCC to GND to set the output VBOOT voltage (See Table 1 for detail).
28	ICCMAX	**ICCMAX Setting Input.** Connect a resistor voltage divider from VCC to GND to set the ICCMAX.
29	CSP	**Non-inverting Input of Total Current Sense Amplifier.**
30	CSN	**Inverting Input of Total Current Sense Amplifier.**
31	VINSEN	**Power Stage & Driver Supply Voltage Detection.** Connect a resistor voltage divider to this pin with 1/10 scaling ratio from power stage VIN to GND. The VINSEN voltage is used for input voltage detection and PWM on-time calculation.
32	IOUT	**Output Current Monitor**. IOUT current is proportional to total load current. Connect a resistor R_{IOUT} between IOUT and GND to achieve a voltage proportional to load current. A capacitor may be connected between IOUT and GND to adjust the response time of IOUT. The IOUT voltage is converted to digital content by internal A/D converter with a data update rate of 500us. IOUT voltage is used for output current reporting. When IOUT voltage reaches to 1.3V, it will trigger ICCMAX Alert# of SVID.
33	TONSET	**PWM On-Time Setting Pin.** Connect a resistor from this pin to GND to set the PWM on-time.
34	COMP	**Output of Control Loop Error Amplifier.**
35	FB	**Inverting Input of the Error Amplifier.**
36	EAP	**Non-inverting Input of the Error Amplifier.**
37	FBRTN	**Buck Converter Output Voltage Feedback Return.** Inverting input to the differential voltage sense amplifier. Connect this pin to the output voltage feedback return point.
38	DAC/SS	**DAC Output and Soft Start.**
39	NC	**Not Internally Connected.**
40	VR_SHDN#	**VR_SHDN# Indicator.** Open drain logic output and active low indicating. The uP1649Q asserts VR_SHDN# when VR temperature is higher than the threshold in the VRSD register programmed by I2C.
41	Exposed Pad	**Ground.** The exposed pad must be soldered to a large PCB and connected to GND.

Functional Block Diagram



Functional Description

The uP1649Q is a VR12.5 compliant CPU power controller supports up to 4 phases.

Power Input and Power On Reset

Figure 1 shows the power ready detection of the uP1649Q. RC filters are required for locally bypassing the supply input pin. The VCC pin is monitored for power on reset, the POR level is typically 4.3V at VCC rising. When ENABLE pin is driven above 0.8V, the controller status is dependent of the VINSEN, the internal UVLO and pending fault states. When ENABLE pin is driven below 0.3V will turn off the controller, clear all fault states and prepare the controller to soft-start when re-enabled.

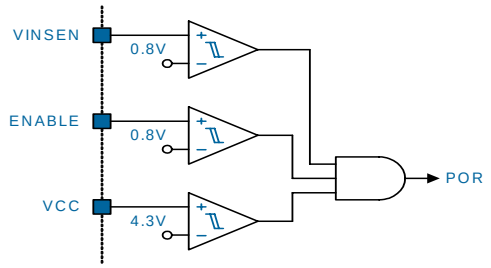


Figure 1. Circuit for Power Ready Detection

Operation Phase Selection

The uP1649Q controller supports 4/3/2/1-phase operation. The operation phase number is set by the status of PWM4, PWM3 and PWM2 pins at power on reset. Normally, the controller operates as a 4-phase PWM controller. Pull PWM4 to +5V for 3-phase operation; PWM4 and PWM3 to +5V for 2-phase operation; PWM4, PWM3 and PWM2 to +5V for 1-phase operation. If the controller is set to 3/2/1-phase operation, the CSP and CSN pin of unused channel can be left open.

Initial Parameters Setting

The ADDR, ICCMAX and VBOOT pins set the parameters required for VR12.5 as shown in Figure 2.

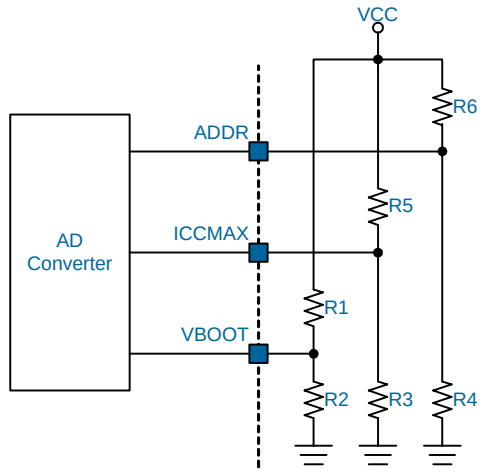


Figure 2. Initial Parameter Setting

The ICCMAX sets the maximum supported current of VR. The ICCMAX voltage is digitized by internal 8-bit A/D converter as follows.

The ADC scales one-fourth of VCC (0V to VCC/4) into 256 levels in Iccmax setting (SVID register 0x21h). The ratio of ICCMAX pin voltage to VCC determines the SVID register 0x21h value, which means (VCC/1024) equals 1A. Use voltage divider resistor from VCC to the ICCMAX pin to set the Iccmax value. If the ICCMAX pin voltage is equal to or greater than (VCC/4), the SVID register 0x21h value will be FFh. If VCC = 5V, the LSB = 1.25V / 256 = 4.9mV, which means 4.9mV applied to ICCMAX pin equals to 1A setting. For example, if the maximum level of current is 100A, the ICCMAX pin voltage should be 4.9mV x 100 = 0.49V. Note that the ICCMAX setting is dependent on VCC voltage (it tracks VCC voltage). Therefore make sure to use resistor voltage divider in ICCMAX setting.

Connect the VBOOT pin to a resistor voltage divider from VCC to GND, to set the output initial start up voltage. There are 4 levels of Vboot as shown in Table 1.

Table 1. VBOOT Voltage

No.	VBOOT pin voltage	Vboot	Recommended Value	
			R1 (kΩ)	R2 (kΩ)
1	0V	0V	NC	10
2	(3/32) x VCC	1.65V	28.7	3
3	(5/32) x VCC	1.70V	27	4.99
4	(1/4) x VCC	1.75V	30	10

The ADDR pin programs the address of the controller. Connect a resistor voltage divider to the ADDR pin to set the physical address of SMBus and SVID. Table 2 shows the recommended resistance value of the resistor voltage divider.

Table 2. SVID and SMBUS Address Table

		R6/R4 for SVID Address (kΩ)									
V_{ADDR} = % of VCC	SM_ADDR	00h		02h		04h		06h		08h	
		R6	R4	R6	R4	R6	R4	R6	R4	R6	R4
40.63%	0x88	4.92	3.37	24.61	16.84	44.30	30.32	73.84	50.53	147.67	101.06
46.88%	0x8A	4.27	3.77	21.33	18.83	38.40	33.89	63.99	56.48	127.99	112.95
53.13%	0x8C	3.76	4.27	18.82	21.34	33.88	38.40	56.47	64.01	112.93	128.01
59.38%	0x8E	3.37	4.92	16.84	24.62	30.31	44.31	50.52	73.86	101.04	147.71
65.63%	0xB8	3.05	5.82	15.24	29.10	27.43	52.37	45.71	87.29	91.42	174.57
71.88%	0xBA	2.78	7.11	13.91	35.56	25.04	64.01	41.74	106.69	83.47	213.37
78.13%	0xBC	2.56	9.14	12.80	45.72	23.04	82.30	38.40	137.17	76.80	274.35
84.38%	0xBE	2.37	12.80	11.85	64.02	21.33	115.24	35.55	192.06	71.11	384.12

PWM On Time Setting

The PWM on-time of the uP1649Q is set by an external resistor connected between TONSET pin and GND. The PWM on-time can be calculated as below

$$T_{ON} = \left(\frac{V_{OUT}}{V_{IN}} \right) \times R_{TON} \times 92.6 \text{ (ns)}$$

The operation frequency and resistor option as shown in Table 3. For example, given V_{IN} = 12V, V_{OUT} = 1.7V, R_{TON} = 36kΩ, T_{ON} is about 472ns by above equation. The PWM frequency is about 300kHz.

Table 3. Operation Frequency v.s. Resistor

Operation Frequency (kHz)	Recommend Value R_{TON}(kΩ)
200	53.6
250	43.2
300	36
350	30.9
400	27
450	24
500	21
550	18.7
600	17.4

Soft Start

The slew rate of output voltage during soft start and dynamic VID change is programmable by I2C register 0x1Ch. The slew rate during soft start is always slow. The recommended capacitance of C_{SS} is 10nF.

Dynamic VID

The uP1649Q can accept VID input changes during normal operation. This allows the output voltage V_{OUT} to change while the DC/DC converter is running and supplying current to the load. This is commonly referred to as VID on-the-fly (VID_OTF). A VID_OTF may occur under either light or heavy load conditions. This change can be positive or negative.

The VID_OTF slew rate ranges from 7mV/us to 38mV/us with a total of 32 steps and 1mV/LSB resolution. This VID_OTF slew rate is programmed by I2C setting.

Output Voltage Differential Sensing

The uP1649Q uses differential sensing by a high-gain low-offset error amplifier as shown in Figure 3. The CPU voltage is sensed between the FB and FBRTN pins. A resistor R_{FB} connects FB pin and the positive remote sense pin of the CPU V_{CCP}. FBRTN pin connects to the negative remote sense pin of CPU V_{CCN} directly. The error amplifier compares the V_{FB} with V_{EAP} = ($V_{DAC/SS}$ - I_{SUM} x R_{DRP}) to regulate the output voltage.

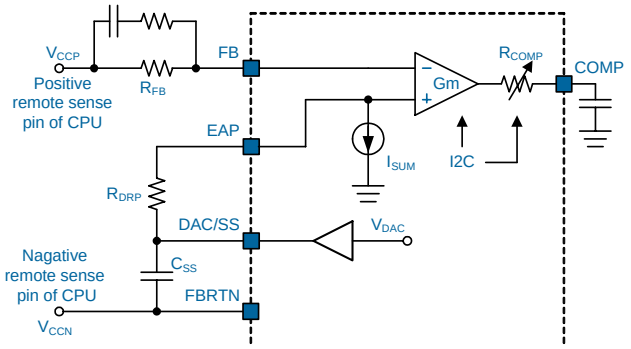


Figure 3. Circuit for V_{CORE} Differential Sensing.

Droop (Load Line) Setting

The sensed current I_{SUM} is mirrored to EAP pin as shown in Figure 3. This creates voltage drop across R_{DRP} and makes V_{EAP} lower than the $V_{DAC/SS}$ as follows.

$$V_{EAP} = V_{DAC/SS} - I_{SUM} \times R_{DRP} = V_{DAC/SS} - \frac{I_{OUT} \times R_{DC} \times R_{DRP}}{R_{SUM} \times N}$$

where R_{DC} is the DCR of inductor and N is the operation phase number.

In steady state, output voltage is equal to V_{EAP}. Thus, the output voltage decreasing linearly with I_{OUT} is obtained.

The load line is defined as:

$$LoadLine = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{R_{DC} \times R_{DRP}}{R_{SUM} \times N}$$

Total Current Sensing

The uP1649Q provides low input offset current sense amplifier (CSA) to monitor the total load current flowing through inductor as shown in Figure 4.

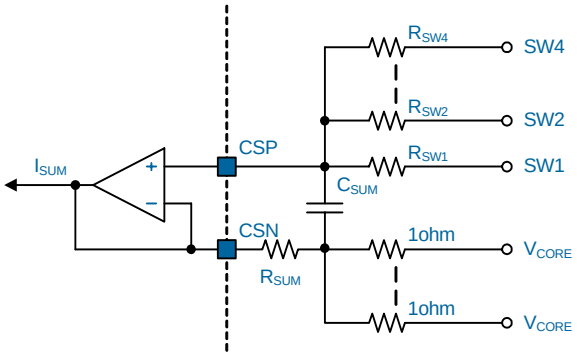


Figure 4. Total Current Sensing

Output current of CSA (I_{SUM}) is used for adaptive voltage positioning (AVP), load current monitoring and over current protection. The sensed current I_{SUM} represents the total output current of the VR, and it can be calculated as follows.

$$I_{SUM} = \frac{I_{OUT} \times \frac{R_{DC}}{N}}{R_{SUM}}$$

In this inductor current sensing topology, R_{SW} and C_{SUM} must be selected according to the equation below:

$$k \times \frac{L}{R_{DC}} = \frac{R_{SW} \times C_{SUM}}{N}$$

where R_{DC} is the DCR of the output inductor, N is the operation phase number. Theoretically, k should be equal to 1 to sense the instantaneous total load current. But in real application K is usually between 1.2 to 1.8 for better load transient response.

Output Current Monitoring

The I_{SUM} is mirrored to IOUT pin for output current monitoring and is separately mirrored internally for over current protection. The I_{SUM} flows through the resistor R_{IMON} and creates a voltage that is proportional to the output current. The controller asserts SVID Iccmax ALERT when the sensed currnet I_{SUM} reaches I_{SUM_ALERT} as follows.

$$\frac{1.3V}{R_{OCSET}} = \frac{I_{CCMAX} \times R_{DC}}{R_{SUM} \times N} = I_{SUM\_ALERT}$$

The recommended value of R_{IOUT} is between 20kΩ to 50kΩ. The resistance value used in IOUT pin setting should be the same as R_{OCSET}, i.e. $R_{IOUT} = R_{OCSET}$.

Total Output Over Current Protection

The sensed current I_{SUM} is mirrored internally for over current protection (OCP). If the sensed current I_{SUM} is higher than the I_{SUM_ALERT} times the I2C programmable OCP ratio (I_{SUM_OCP} = I_{SUM_ALERT} x OCP ratio), the total current OCP is triggered. There is a time delay (default is 20us, also I2C programmable) for the total current OCP. The OCP is latch-off type and can be reset only by POR toggling. Connect a resistor R_{OCSET} from OCSET pin to GND for OCP level setting.

Control Loop

The uP1649Q adopts the uPI proprietary RCOT™ control technology. The RCOT uses the constant on-time modulator. The output voltage is sensed to compare with the internal high accurate DAC. The DAC is commanded by CPU through the SVID interface or by system through I2C interface. The amplified error signal, V_{COMP}, is compared to the internal ramp to initiate an on-time to PWM. The RCOT features easy design, fast transient response and is smooth mode transition and especially suitable for powering the microprocessor.

Over Voltage Protection (OVP)

The over voltage protection monitors the output voltage via the FB pin. Once V_{FB} exceeds V_{EAP} + 400mV (default, I2C programmable), OVP is triggered and latched. The PWM outputs will be low to turn on low side MOSFET and turn off high side MOSFET to protect CPU. A 20us delay is used in OVP detection circuit to prevent false trigger. Only re-start up can release OVP latch.

Under Voltage Protection (UVP)

The under voltage protection monitors the output voltage via the FB pin. After the uP1649Q starting up and V_{OUT} ramping up to Vboot, the uP1649Q initiates UVP function. Once V_{FB} is lower than V_{EAP} - 400mV (default, I2C programmable), UVP is triggered and latched. The uP1649Q will try to turn off both high side and low side MOSFETs. A 5us delay is used in UVP detection circuit to prevent false trigger. Only re-start up can release UVP latch.

Phase Current Sensing

The uP1649Q senses the phase current by DCR current sensing technique for current balance and per-phase over current protection as shown in Figure 5. An R_{CSP}/C_{CS} network is paralleled with the output inductor. The time constant can be express as:

$$k \times \frac{L}{R_{DC}} = R_{CSP} \times C_{CS}$$

where L is the output inductor, R_{DC} is its parasitic resistance and k is a constant. Theoretically, if k = 1, the sensed current signal I_{CSN} can be expressed as:

$$I_{CSN} = \frac{I_L \times R_{DC}}{R_{CSN}}$$

where I_L is the phase current.

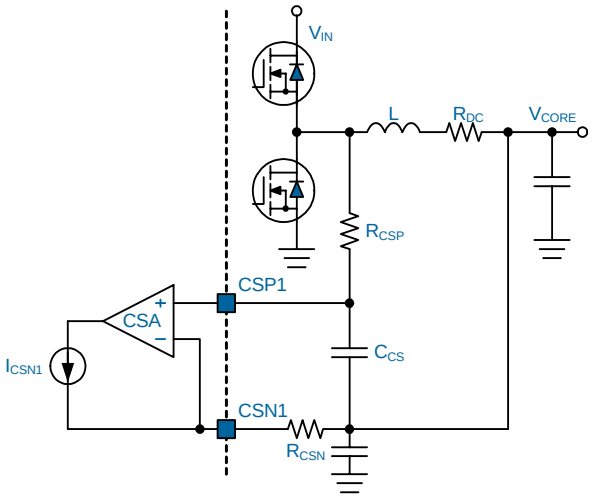


Figure 5. Channel Current Sensing.

Per-Phase Over Current Protection

In addition to the total output current OCP, the uP1649Q provides per-phase current OCP to protect the VR. If the inductor current in any of the active operating phase exceeds the threshold, the OCP is tripped. Figure 5 shows the current sensing in one of the four channels. The sensed current ICSNx represents the current in each phase, and it is compared to a current (default = 100uA, I2C programmable) for OCP. When per-phase OCP is triggered, all the PWM outputs are in high-impedance state to make all MOSFETs off. There is a time delay (default is 6us, I2C programmable) for the total current OCP. The per-phase OCP is latch-off type and can be reset only by POR toggling. Referring to Figure 5, the per phase current sense amplifier output current is the voltage across C_{CS} divided by resistor R_{CSN}. Since the per phase OCP current threshold is 100uA, the resistance of R_{CSN} and the per phase OCP level can be obtained using equation as follows.

$$R_{CSN} = \frac{I_{OCP\_perphase} \times R_{DC}}{100uA}$$

Thermal Indicator

The VRHOT# pin is for over temperature indication. VRHOT trigger threshold is set by I2C TEMP_VRHOT register (0x22). VRHOT is asserted when sensed temperature is higher than TEMP_Max. The VRHOT threshold hysteresis is 3%.

Over Current Indicator

The OC# threshold is set by I2C OCP_L register, and is refer to the percentage of Iccmax current. The OC# goes low when output current is higher than OCP_L threshold and deasserts to high when output current is lower than OCP_L threshold again.

Table 4. SVID Register

Index	Register Name	Access	Default	Description
00h	Vender_ID	RO	26h	Vender ID.
01h	Product_ID	RO	1Ah	Product ID.
02h	Product_Revision	RO	08h	Product Revision.
05h	Product_Version	RO	03h	SVID Protocol Version.
06h	VR_Capability	RO	81h	Bit mapped register, identifies the SVID VR capabilities and which of the optional telemetry are supported.
10h	Status_1	R-M, W-PWM	00h	Data register containing the status of VR.
11h	Status_2	R-M, W-PWM	00h	Data register containing the status of transmission.
12h	Temperature_Zone	R-M, W-PWM	00h	Data register showing temperature zone that have been entered.
15h	Output_Current	R-M, W-PWM	--	Data register showing output current that have been entered.
1Ch	Status_2_LastRead	R-M, W-PWM	00h	This register contains a copy of the Status_2.
21h	ICC_Max	RO Platform	--	Data register containing the maximum output the platform supports.
22h	Temp_Max	RO Platform	64h	Data register containing the maximum temperature the platform supports. Binary format in ^{O}C, i.e. 64h = 100^{O}C.
24h	SR_Fast	RO	0Ah	Data register containing the capability of fast slew rate the platform can sustain. Binary format in mV/us, i.e. 0Ah =10mV/us.
25h	SR_Slow	RO	02h	Data register containing the capability of slow slew rate the platform can sustain. Binary format in mV/us, i.e. 02h =2.5mV/us.
26h	VBOOT	RO Platform	--	Data register containing Vboot voltage in VID steps.
30h	VOUT_Max	RW Master	FFh	This register is programmed by master and sets the maximum VID.
31h	VID_Setting	RW Master	00h	Data register containing currently programmed VID.
32h	Power_State	RW Master	00h	Register containing the programmed power state.
33h	Offset	RW Master	00h	Set offset in VID steps.
34h	Multi_VR_Config	RW Master	00h	Bit mapped data register which configures multiple VRs behavior on the same bus.
35h	Pointer	RW Master	--	Scratch pad register for temporary storage of the SetRegADR pointer register.

I2C Interface

The uP1649Q features an I2C interface and lots of data registers to allow user to adjust various platform operating parameters. Operating parameters that can be adjusted through the I2C are summarized as Table 11. One of the programmable function is to change voltage, switching frequency and operating phase number of VR controller according to the total load current dynamically. There are four load current states to set, and the switching frequency, offset voltage and operating phase number in each state can be programmed independently. This function is called Auto Phase, and it provides user the most flexibility in the platform design to maximize VR efficiency and CPU performance as well.

VM0~2: Define the 4 load current states (LCS0~3)

The uP1649Q converts V_{IOUT} to a digital content, which represents the total output current. There are four load current state registers VM0~3 to program. Each load current state register has 6bits to set the level of output current that the load current state is entered. uP1649Q compares the VM0~3 content and the I_{SUM_ALERT} (refer to Output Current Monitoring section) to determine which load current state should be entered and executes the corresponding operating parameter settings (frequency, offset and operating phase number).
VM0~3 setting is defined as the ratio to I_{SUM_ALERT} (sensed current when output current reaches Iccmax). It takes I_{SUM_ALERT} as the full scale, and 6-bits means that there are 64 steps for user to choose from.
LCS0: V_{IOUT} > VM0, highest load current.

LCS1: VM0 > V_{IOUT} > VM1

LCS2: VM1 > V_{IOUT} > VM2

LCS3: VM3 > V_{IOUT}, lowest load current.

VM_Hys

Define the VM0~2 state hystersis VMx_Hys as shown in Table 5.

Table 5. V_{HYS} Setting Table

VM0~2_Hys (bin)	VM0~2_Hys (A)
000	(2/100) x Iccmax
001	(3/100) x Iccmax
010	(4/100) x Iccmax
011	(5/100) x Iccmax
100	(6/100) x Iccmax
101	(7/100) x Iccmax
110	(8/100) x Iccmax
111	(9/100) x Iccmax

VOFS0~3

Define voltage offset of the 4 load current states: 4 I2C programmable registers VOFS0~3 define the voltage offset in load current status LCS0~3 respectively.

IICF0~3

Frequency adjust of the 4 load current states: IICF0~3 define the frequency in load current states LCS0~3 respectively as show in Table 6.

Table 6. IICF Setting Table

IICF0~3	Frequqncy of LCS0 to 3
0000	70%
0001	85%
0010	100%
0011	120%
0100	140%
0101	160%
0110	180%
0111	200%

IICP0~3

Operating phase number of the 4 load current states: 4 I2C programmable registers IICP0~3 define the operating phase number in load current states LCS0~3 respectively as shown in Table 7.

Table 7. IICP Setting Table

IICP0 to 3	Operating Phase Number
00	4-phase
01	3-phase
10	2-phase
11	1-phase

Misc2[5:0]

Register Misc2[5:0] enables/disables the I2C functions as:

Bit[5]:
0 = Disable Offset
1 = Enable Offset
Bit[4] :
0 = Disable Auto Phase (Follow SVID)
1 = Enable Auto Phase
Bit[3]:
0 = Disable PSM (Always CCM)
1 = Enable PSM
Bit[2]:
0 = Disable Load Line (LL=0)
1 = Enable Load Line
Bit[1]: Reserved
Bit [0]:
0 = Disable OC# (OCP function remain active)
1 = Enable OC#

WD[7:5]

WD[7]: [1] = enables watch dog timer.

[0] = Disable watching dog timer.

WD[6]: Watching Dog Timer (If set to 1, reset all I2C register content to default value after reading).

WD[5]: [0] = 800ms

WD[5]: [1] = 1600ms

RCOMP[7:0]

RCOMP is compensation resistor, it can be programming by 0x13 register as show in Table 8. Bit[7:4] sets the R_{COMP} value for VR in single-phase operation, and bit[3:0] sets the R_{COMP} value for VR in multi-phase operation.

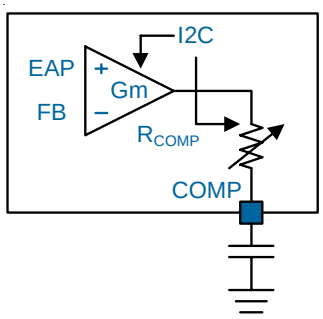


Table 8. RCOMP Setting Table

Bit[7:4] / Bit[3:0]	R_{COMP}(ohm)
0000	2.5K
0001	5K
0010	7.5K
0011	10K
0100	12.5K
0101	15K
0110	17.5K
0111	20K
1000	22.5K
1001	25K
1010	27.5K
1011	30K
1100	32.5K
1101	35K
1110	37.5K
1111	40K

LCHVID[7:0]:Latch VID

The register LCHVID stores the 8 bits VID code that user defined, when enable this function,VR will ignore CPU SetVID command.

IOUT[7:0]:Output Current Reading

The register reports real IOUT (output 1.3V = FFh).

VOUT[7:0]:V_{CORE} Output Voltage Reading

The register VCORE_VOUT stores the VCORE output voltage that is converted by internal ADC with 10mV/LSB.

SIMON/OC/UV/OV[7:0] Protection Setting

The Bit[7:6] for overwrite SVID 0x15h

Bit[7]:

0 = Disable; 1 = Enable

Bit[6]: 0 = 1/4; 1 = 1/2

The Bit[5:4] for per-phase OCP used to adjust V_{CORE} per-phase OCP Level as:

Bit[5:4]=[00]= 100uA

Bit[5:4]=[01]= 120uA

Bit[5:4]=[10]= 140uA

Bit[5:4]=[11]= 160uA

The Bit[3:2] for UVP used to adjust V_{CORE} UVP level as:

Bit[3:2]=[00]= 400mV

Bit[3:2]=[01]= 500mV

Bit[3:2]=[10]= 600mV

Bit[3:2]=[11]= 700mV

The Bit[1:0] for OVP used to adjust V_{CORE} OVP level as:

Bit[1:0]=[00]= 400mV

Bit[1:0]=[01]= 500mV

Bit[1:0]=[10]= 600mV

Bit[1:0]=[11]= 700mV

TEMP_VRHOT[4:0]: TEMPMAX Setting

The register TEMP_VRHOT used to adjust VRHOT# trigger point.

TEMP_VRHOT[4]: VRHOT#

0: Enable

1: Disable

TEMP_VRHOT[3:0]: SVID 0x12 shift left by LSB, temperature range from 91°C to 121°C, default = 100°C, 3°C/LSB

GCOMP[3:0]: OTA Transconductance Gain Setting

The register GCOMP[3:0] is used to adjust error amplifier Gm(uA/V) for loop gain tuning as show in Table 9.

GCOMP[3]=[0]=>2020uA/V(default value)

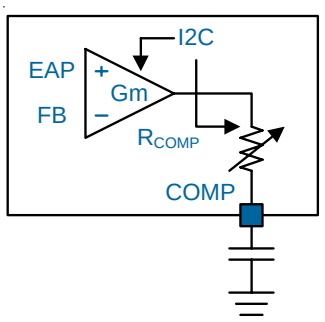


Table 9. GCOMP Setting Table

Bit[3] = 1, Bit[2:0]	Gm(uA/V)
000	X1
001	X1.17
010	X1.31
011	X1.45
100	X1.69
101	X0.81
110	X0.6
111	X0.33

IICLL0~3

Load line adjust of 4 load current state: IICLL0~3 define the DC load line slope in load current state LCS0~3 respectively as shown in Table 10.

Table 10. IICLL0~3

IICL0~3	Load Line
0000	0%
0001	12.5%
0010	25%
0011	37.5%
0100	50%
0101	62.5%
0110	75%
0111	87.5%
1000	100%
1001	112.5%
1010	125%
1011	137.5%
1100	150%
1101	162.5%
1110	175%
1111	187.5%

Table 11. I2C Configuration Registers.

Reg Addr	Register Name	Access	Default	Description
0x01	VM0[7:0]	R/W	00h	Set internal IOUT voltage level 0 VIOUT > Level 0 => LCS0 (highest current state) Bit[1:0] don't care VM0 setting is defined as the ratio to I_{SUM_ALERT} (sensed current when output current reaches Iccmax). VM0 = (Bit[7:2]/64) x Iccmax
0x02	VM1[7:0]	R/W	00h	Set internal IOUT voltage level 1 VIOUT > Level 1 => LCS1 Bit[1:0] don't care VM0 setting is defined as the ratio to I_{SUM_ALERT} (sensed current when output current reaches Iccmax). VM0 = (Bit[7:2]/64) x Iccmax
0x03	VM2[7:0]	R/W	00h	Set internal IOUT voltage level 2 VIOUT > Level 2 => LCS2 VIOUT < Level 2 => LCS3 (lowest current state) Bit[1:0] don't care VM0 setting is defined as the ratio to I_{SUM_ALERT} (sensed current when output current reaches Iccmax). VM0 = (Bit[7:2]/64) x Iccmax
0x04	VM0_Hys[2:0] VM1_Hys[6:4]	R/W	00h	Bit[2:0] : Set VM0 Hysteresis, 8 steps Hys = (Iccmax / 100) x (2 + bit[2:0]) Bit[6:4] : Set VM1 Hysteresis, 8 steps Hys = (Iccmax / 100) x (2 + bit[6:4])
0x05	VM2_Hys[2:0]	R/W	00h	Bit[2:0] : Set VM2 Hysteresis, 8 steps Hys = (Iccmax / 100) x (2 + bit[2:0])
0x06	IICP3[7:6]; IICP2[5:4] IICP1[3:2]; IICP0[1:0]	R/W	00h	Operation Phase Number Setting Bit[7:6] : Phase Number of LCS3 Bit[5:4] : Phase Number of LCS2 Bit[3:2] : Phase Number of LCS1 Bit[1:0] : Phase Number of LCS0 00 = 4 Phase, 01 = 3 Phase, 10 = 2 Phase, 11 = 1 Phase
0x07	VOFS0[7:0]	R/W	00h	Voltage offset of LCS0. (10mV / step)
0x08	VOFS1[7:0]	R/W	00h	Voltage offset of LCS1. (10mV / step)
0x09	VOFS2[7:0]	R/W	00h	Voltage offset of LCS2. (10mV / step)
0x0A	VOFS3[7:0]	R/W	00h	Voltage offset of LCS3. (10mV / step)
0x0B	IICF0[7:4] IICF1[3:0]	R/W	22h	IICF0[7:4]: operating frequency of LCS0 ; IICF1[3:0]: operating frequency of LCS1 0000 = 70%; 0001 = 85%; 0010 = 100%; 0011 = 120% 0100 = 140%; 0101 = 160% 0110 = 180%; 0111 = 200%
0x0C	IICF2[7:4] IICF3[3:0]	R/W	22h	IICF2[7:4]: operating frequency of LCS2 ; IICF3[3:0]: operating frequency of LCS3 0000 = 70%; 0001 = 85%; 0010 = 100%; 0011 = 120% 0100 = 140%; 0101 = 160%; 0110 = 180%; 0111 = 200%
0x0D	IICLL0[7:4] IICLL1[3:0]	R/W	88h	I2CLL0[7:4] : load line setting of LCS0 (default 100%, min 0%, max 187.5%, 12.5 % / step) I2CLL1[3:0] : load line setting of LCS1 (default 100%, min 0%, max 187.5%, 12.5 % / step)
0x0E	IICLL2[7:4] IICLL3[3:0]	R/W	88h	I2CLL2[7:4] : load line setting of LCS2 (default 100%, min 0%, max 187.5%, 12.5 % / step) I2CLL3[3:0] : load line setting of LCS3 (default 100%, min 0%, max 187.5%, 12.5 % / step)

Table 11. I2C Configuration Registers(cont).

Reg Addr	Register Name	Access	Default	Description
0x0F	PH1_IGAIN[6:4] PH2_IGAIN[2:0]	R/W	44h	PHASE1 Current Balance Gain Adjust Bit[7]: Don't care PH1_IGAIN[6:4] 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5% PHASE2 Current Balance Gain Adjust Bit[3]: Don't care PH2_IGAIN[2:0] 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5%
0x10	PH3_IGAIN[6:4] PH4_IGAIN[2:0]	R/W	44h	PHASE3 Current Balance Gain Adjust Bit[7]: Don't care PH3_IGAIN[6:4] 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5% PHASE4 Current Balance Gain Adjust Bit[3]: Don't care PH4_IGAIN[2:0] 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5%
0x11	PH1_IOS[6:4] PH2_IOS[2:0]	R/W	00h	PHASE1 Current Balance Offset Adjust Bit[7]: Don't care PH1_IOS[6:4]: 000 = 0uA; 001 = 2uA; 010 = 4uA; 011 = 6uA; 100 = 8uA; 101 = 10uA; 110 = 12uA; 111 = 14uA PHASE2 Current Balance Offset Adjust Bit[3]: Don't care PH2_IOS[2:0]: 000 = 0uA; 001 = 2uA; 010 = 4uA; 011 = 6uA; 100 = 8uA; 101 = 10uA; 110 = 12uA; 111 = 14uA
0x12	PH3_IOS[6:4] PH4_IOS[2:0]	R/W	00h	PHASE3 Current Balance Offset Adjust Bit[7]: Don't care PH3_IOS[6:4]: 000 = 0uA; 001 = 2uA; 010 = 4uA; 011 = 6uA; 100 = 8uA; 101 = 10uA; 110 = 12uA; 111 = 14uA PHASE4 Current Balance Offset Adjust Bit[3]: Don't care PH4_IOS[2:0]: 000 = 0uA; 001 = 2uA; 010 = 4uA; 011 = 6uA; 100 = 8uA; 101 = 10uA; 110 = 12uA; 111 = 14uA
0x13	RCOMP[7:0]	R/W	71h	RCOMP Resistor Setting Bit[7:4]: single-phase operation compensation resistor setting, RCOMP = 2.5K x (1+[7:4]), default = 20K. Bit[3:0]: multi-phase operation compensation resistor setting, RCOMP = 2.5K x (1+[3:0]), default = 5K.
0x14	GCOMP[3:0]	R/W	00h	OTA Gm GCOMP[3:0] = 2020uA/V (default)
0x15	LCHVID[7:0]	R/W	88h	Latch VID Register.
0x16	IOUT[7:0]	RO	--	Report Real IOUT (FFh when V_{IOUT} > 1.3V)
0x17	VOUT[7:0]	RO	--	V_{CORE} Voltage Reading.

Table 11. I2C Configuration Registers(cont).

Reg Addr	Register Name	Access	Default	Description
0x18	Protection Indicator[5:0]	RO	00h	Bit[5] : OCP Indicator 0 = Not Active; 1 = Active Bit[4] : Per phase OCP Indicator 0 = Not Active; 1 = Active Bit[3] : OVP Indicator 0 = Not Active; 1 = Active Bit[2] : UVP Indicator 0 = Not Active; 1 = Active Bit[1:0] : Per phase OCP indicator if Bit[4] = 1 phase1 = 01; phase2 = 10; phase3 = 11; phase4 = 00
0x19	Total OCP/OCP_L/OCP_L Hys [7:0]	R/W	8Ah	OCP[7:4] : Total Current OCP refer to % of ICCMAX 0000 = 50%; 0001 = 60%; 0010 = 70%; 0011 = 80%; 0100 = 90%; 0101 = 100%; 0110 = 110%; 0111 = 120%; 1000 = 130%(Default); 1001 = 140%; 1010 = 150%; 1011 = 160%; 1100 = 170%; 1101 = 180%; 1110 = 190%; 1111 = 200% OCP_L[3:1] : OCP_L refer to % of ICCMAX 000 = 50%; 001 = 60%; 010 = 70%; 011 = 80%; 100 = 90%; 101 = 100%(Default); 110 = 110%; 111 = 120% OCP_L Hys[0] : Set OCP_L Hysteresis, refering to % of Iccmax 0: 10% (Default); 1: 20%
0x1A	SIMON/OC/UV/OV [7:0]	R/W	40h	SIMON[7]: Overwrite SVID 0x15h (IOUT) 1 = Enable; 0 = Disable SIMON[6]: Overwrite SVID 0x15h (IOUT) 1: 1/2; 0: 1/4 OCP[5:4] : Per Phase OCP 00 = 100uA(Default); 01 = 120uA; 10 = 140uA; 11 = 160uA Bit[3:2] : UVP Setting 00 = 400mV(Default); 01 = 500mV; 10 = 600mV; 11 = 700mV Bit[1:0] : OVP Setting 00 = 400mV(Default); 01 = 500mV; 10 = 600mV; 11 = 700mV
0x1B	OCP_delay[7:0]	R/W	68h	OCP_delay[7:5] : Total OCP delay 000 = 5us; 001 = 10us; 010 = 15us; 011 = 20us (Default); 100 = 25us; 101 = 30us; 110 = 35us; 111 = 40us OCP_delay[4:2] : Per Phase OCP delay 000 = 2us; 001 = 4us; 010 = 6us(Default); 011 = 8us; 100 = 10us; 101 = 12us; 110 = 14us; 111 = 16us OCP_delay[1:0] : reserved
0x1C	VR_SR	R/W	03h	VR_SR [4:0] DVID slew rate from 7~38mV/us. Total 32 steps and 1mV/us per-LSB. Default is 10mV/us. (Note: Alert# assertion timing follows SetVID command) 00 = 7mV/us

Table 11. I2C Configuration Registers(cont).

Reg Addr	Register Name	Access	Default	Description
0x1D	Misc1[6:0]	R/W	0Fh	Bit[6]: V_{DAC} Control 0 = SVID 0x31 V_{DAC} follow SVID 1 = SVID 0x31 V_{DAC} ignore SVID Bit[5] : Power state control 0 = SVID 0x32 Power state follow SVID 1 = SVID 0x32 Power state ignore SVID Bit[4]: Offset control 0 = SVID 0x33 Offset follow SVID 1 = SVID 0x33 Offset ignore SVID Bit[3]: Total OCP enable control 0 = Disable total OCP function (OC# = H) 1 = Enable total OCP function Bit[2]: Per-phase OCP enable control 0 = Disable per-phase OCP function 1 = Enable per-phase OCP function Bit[1]: OVP enable control 0 = Disable OVP function 1 = Enable OVP function Bit[0]: UVP enable control 0 = Disable UVP function 1 = Enable UVP function
0x1E	Misc2[5:0]	R/W	0Fh	Bit[5]: Output voltage offset enable control 0 = Disable I2C Offset (Offset defined in 0x07 ~ 0x0A) 1 = Enable I2C Offset Bit[4]: Auto Phase function enable control 0 = Disable Auto Phase (= Follow (1) IICP0 if 0x1D[5] = 1 or (2) SVID_PS if 0x1D[5] = 0) 1 = Enable Auto Phase Bit[3]: PSM enable control 0 = Disable PSM (Always CCM) 1 = Enable PSM Bit[2]: Load line enable control 0 = Disable Load Line (LL = 0) 1 = Enable Load Line Bit[1]: reserved Bit[0]: OC# enable control 0 = Disable OC# (OCP function remain active) 1 = Enable OC#
0x1F	WD[7:5]	R/W	00h	Watchdog timer Bit[7]: 1 = Enable ; 0 = Disable Bit[6]: If set to 1, reset all I2C register content to default vaule after reading Bit[5]: Timer 0 = 800ms ; 1 = 1600ms

Table 11. I2C Configuration Registers(cont).

Reg Addr	Register Name	Access	Default	Description
0x20	VRSD[4:0]	R/W	11h	VR_SHDN# threshold setting Bit[4]: 1 = Enable; 0 = Disable Bit[3:0]: 16 steps, 2°C/step VR_SHDN#=123°C + Bit[3:0], temp range from 123°C to 153°C, default = 125°C
0x21	VRSD Hys[4:0]	R/W	00h	VR_SHDN# Hysteresis Setting Bit[4:0]: 32 steps
0x22	DB1PHOC[5]/ TEMP_VRHOT[4:0]	R/W	03h	Bit[5]:Single-phase operation OCP threshold control 0 = Default; 1 = Double Bit[4]: VRHOT# 0 = Enable; 1 = Disable Bit[3:0]: SVID 0x12 Shift left by LSB, Temp range from 91°C to 121°C, default = 100°C, 3°C/LSB 0000 = No Shift; 0001 = Shift 1LSB; 0010 = Shift 2LSB; 0011 = Shift 3LSB(Default); 0100 = Shift 4LSB; 0101 = Shift 5LSB; 0110 = Shift 6LSB; 0111 = Shift 7LSB; 1000 = Shift 8LSB; 1001 = Shift 9LSB; 1010 = Shift 10LSB
0x23	TB[7:0]	R/W	00h	TB in PS0 Bit[7]: 0 = Disable ; 1 = Enable Bit[6:4]: 000 = 0mV ; 001 = 10mV ; 010 = 20mV ; 011 = 30mV ; 100 = 40mV ; 101 = 50mV ; 110 = 60mV ; 111 = 70mV TB in PS1/2 Bit[3]: 0 = Disable ; 1 = Enable Bit[2:0]: 000 = 0mV; 001 = 10mV; 010 = 20mV; 011= 30mV; 100 = 40mV; 101 = 50mV; 110 = 60mV; 111 = 70mV
0x24	TRIG[7:0]	R/W	00h	TB Vtrig Limit in PS0 Bit[7]: 0 = Disable; 1 = Enable Bit[6:0]: 000 = 1.25 V; 001 = 1.35 V; 010 = 1.45 V; 011 = 1.55 V; 100 = 1.65 V; 101 = 1.75 V; 110 = 1.85 V; 111 = 1.95 V TB Vtrig Limit in PS1/2 Bit[3]: 0 = Disable; 1 = Enable Bit[2:0]: 000 = 1.25V; 001 = 1.35V; 010 = 1.45V; 011 = 1.55V; 100 = 1.65V; 101 = 1.75V; 110 = 1.85V; 111 = 1.95V
0x25	TBCUTOFF[7:6] TBTON[5:0]	R/W	00h	Bit[7:6] TB cut-off frequency control 00 = 100kHz; 01 = 100kHz; 10=200kHz; 11=300kHz TB ON time Bit[5:3]: PS0 TB ON time 000 = 200ns; 001 = 300ns; 010 = 400ns; 011 = 500 ns; 100 = 600ns; 101 = 700ns; 110 = 800ns; 111 = 900 ns Bit[2:0]: PS1/2 TB ON time 000 = 200ns; 001 = 300ns; 010 = 400ns; 011 = 500ns; 100 = 600ns; 101 = 700ns; 110 = 800ns; 111 = 900ns

Table 11. I2C Configuration Registers(cont).

Reg Addr	Register Name	Access	Default	Description
0x26	ITB[7:4] IOUT_OFS[3:0]	R/W	80h	Internal Testing Bit: 10mV x Bit[7:4] IOUT Offset for both digital reporting: SVID: 0x15h + Bit[3:0] I2C: 0x16h + Bit[3:0] Bit[3] is sign bit, 0 = positive offset, 1 = negative offset 0001 = "+1", 0111 = "+7" (positive maximum) 1001 = "-7", 1111 = "-1", 1000 = "-8" (negative maximum) digital content after offset is confined between 00h and FFh.
0x27	CPU_VID[7:0]	RO	--	A copy of SVID register 0x31h (VID_Setting) content
0x48	Version ID	RO	08h	
0xB2	CHIP ID	RO	27h	

Table 12. Intel SVID Table

SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)
0x00	0	0x25	0.86	0x4A	1.23	0x6F	1.6	0x94	1.97	0xB8	2.33	0xDC	2.69
0x01	0.5	0x26	0.87	0x4B	1.24	0x70	1.61	0x95	1.98	0xB9	2.34	0xDD	2.7
0x02	0.51	0x27	0.88	0x4C	1.25	0x71	1.62	0x96	1.99	0xBA	2.35	0xDE	2.71
0x03	0.52	0x28	0.89	0x4D	1.26	0x72	1.63	0x97	2	0xBB	2.36	0xDF	2.72
0x04	0.53	0x29	0.9	0x4E	1.27	0x73	1.64	0x98	2.01	0xBC	2.37	0xE0	2.73
0x05	0.54	0x2A	0.91	0x4F	1.28	0x74	1.65	0x99	2.02	0xBD	2.38	0xE1	2.74
0x06	0.55	0x2B	0.92	0x50	1.29	0x75	1.66	0x9A	2.03	0xBE	2.39	0xE2	2.75
0x07	0.56	0x2C	0.93	0x51	1.3	0x76	1.67	0x9B	2.04	0xBF	2.4	0xE3	2.76
0x08	0.57	0x2D	0.94	0x52	1.31	0x77	1.68	0x9C	2.05	0xC0	2.41	0xE4	2.77
0x09	0.58	0x2E	0.95	0x53	1.32	0x78	1.69	0x9D	2.06	0xC1	2.42	0xE5	2.78
0x0A	0.59	0x2F	0.96	0x54	1.33	0x79	1.7	0x9E	2.07	0xC2	2.43	0xE6	2.79
0x0B	0.6	0x30	0.97	0x55	1.34	0x7A	1.71	0x9F	2.08	0xC3	2.44	0xE7	2.8
0x0C	0.61	0x31	0.98	0x56	1.35	0x7B	1.72	0xA0	2.09	0xC4	2.45	0xE8	2.81
0x0D	0.62	0x32	0.99	0x57	1.36	0x7C	1.73	0xA1	2.1	0xC5	2.46	0xE9	2.82
0x0E	0.63	0x33	1	0x58	1.37	0x7D	1.74	0xA2	2.11	0xC6	2.47	0xEA	2.83
0x0F	0.64	0x34	1.01	0x59	1.38	0x7E	1.75	0xA3	2.12	0xC7	2.48	0xEB	2.84
0x10	0.65	0x35	1.02	0x5A	1.39	0x7F	1.76	0xA4	2.13	0xC8	2.49	0xEC	2.85
0x11	0.66	0x36	1.03	0x5B	1.4	0x80	1.77	0xA5	2.14	0xC9	2.5	0xED	2.86
0x12	0.67	0x37	1.04	0x5C	1.41	0x81	1.78	0xA6	2.15	0xCA	2.51	0xEE	2.87
0x13	0.68	0x38	1.05	0x5D	1.42	0x82	1.79	0xA7	2.16	0xCB	2.52	0xEF	2.88
0x14	0.69	0x39	1.06	0x5E	1.43	0x83	1.8	0xA8	2.17	0xCC	2.53	0xF0	2.89
0x15	0.7	0x3A	1.07	0x5F	1.44	0x84	1.81	0xA9	2.18	0xCD	2.54	0xF1	2.9
0x16	0.71	0x3B	1.08	0x60	1.45	0x85	1.82	0xAA	2.19	0xCE	2.55	0xF2	2.91
0x17	0.72	0x3C	1.09	0x61	1.46	0x86	1.83	0xAB	2.2	0xCF	2.56	0xF3	2.92
0x18	0.73	0x3D	1.1	0x62	1.47	0x87	1.84	0xAC	2.21	0xD0	2.57	0xF4	2.93
0x19	0.74	0x3E	1.11	0x63	1.48	0x88	1.85	0xAD	2.22	0xD1	2.58	0xF5	2.94
0x1A	0.75	0x3F	1.12	0x64	1.49	0x89	1.86	0xAE	2.23	0xD2	2.59	0xF6	2.95
0x1B	0.76	0x40	1.13	0x65	1.5	0x8A	1.87	0xAF	2.24	0xD3	2.6	0xF7	2.96
0x1C	0.77	0x41	1.14	0x66	1.51	0x8B	1.88	0xB0	2.25	0xD4	2.61	0xF8	2.97
0x1D	0.78	0x42	1.15	0x67	1.52	0x8C	1.89	0xB1	2.26	0xD5	2.62	0xF9	2.98
0x1E	0.79	0x43	1.16	0x68	1.53	0x8D	1.9	0xB2	2.27	0xD6	2.63	0xFA	2.99
0x1F	0.8	0x44	1.17	0x69	1.54	0x8E	1.91	0xB3	2.28	0xD7	2.64	0xFB	3
0x20	0.81	0x45	1.18	0x6A	1.55	0x8F	1.92	0xB4	2.29	0xD8	2.65	0xFC	3.01
0x21	0.82	0x46	1.19	0x6B	1.56	0x90	1.93	0xB5	2.3	0xD9	2.66	0xFD	3.02
0x22	0.83	0x47	1.2	0x6C	1.57	0x91	1.94	0xB6	2.31	0xDA	2.67	0xFE	3.03
0x23	0.84	0x48	1.21	0x6D	1.58	0x92	1.95	0xB7	2.32	0xDB	2.68	0xFF	3.04
0x24	0.85	0x49	1.22	0x6E	1.59	0x93	1.96						

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCC ---------- -0.3V to +6V
Other Pins ---------- 0V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
VQFN5x5 - 40L θ_{JA} ---------- 36°C/W
VQFN5x5 - 40L θ_{JC} ---------- 3°C/W
Power Dissipation, P_D @ T_A = 25°C
VQFN5x5 - 40L ---------- 2.78W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC} ---------- 4.5V to 5.5V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(T_A = 25°C, VCC = 5V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
VCC POR Threshold	POR_{VCC_r}	VCC rising	4.0	4.3	4.5	V
VCC POR Threshold	POR_{VCC_f}	VCC falling	3.9	4.0	4.1	V
Shutdown Current	I_{SHDN}	ENABLE=0V	--	6	--	mA
Supply Current	I_{VCC}		--	7	--	mA
Error Amplifier						
Offset Voltage	$V_{OS(EA)}$		-1	--	1	mV
Trans-Conductance	GM		--	2020	--	uA/V
Gain Bandwidth Product	$G_{BW(EA)}$	Guaranteed by Design	--	10	--	MHz
DAC Voltage Accuracy						
DAC Output Accuracy	$V_{DAC/SS}$	1.50V to 3.04V	-0.5	--	0.5	%
		1.00V to 1.49V	-8	--	8	mV
		0.50V to 0.99V	-10	--	10	mV
Slew Rate						
Slew Rate Fast	SR_Fast	SetVID_Fast	10	--	--	mV/us
Slew Rate Slow	SR_Slow	SetVID_Slow	2.5	--	--	mV/us
ENABLE Input						
Input Low	V_{IL}		--	--	0.3	V
Input High	V_{IH}		0.8	--	--	V
Leakage Current of ENABLE	I_{ENABLE}	ENABLE = 0V	--	0	1	uA
Leakage Current of ENABLE	I_{ENABLE}	ENABLE = 1V	-1	0	--	uA
PWM On-Time Setting						
Frequency Range	f_{OSC}		200	--	600	kHz
On Time Accuracy	T_{ON}	Vin = 12V, Vout = 1.7V, R_{TON} = 36kΩ	--	472	--	ns

Electrical Characteristics

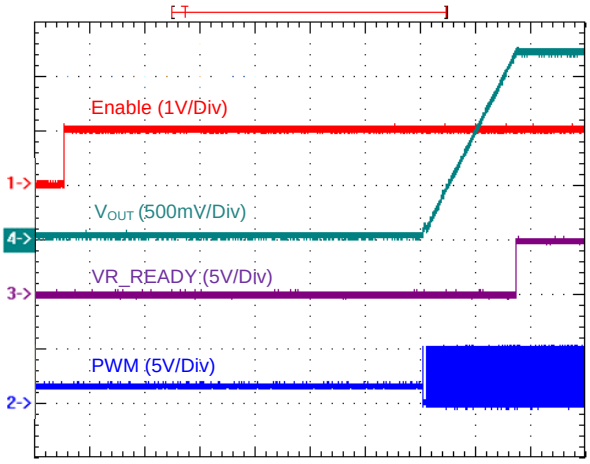
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Current Sense Amplifier for Current Summing						
Offset Voltage	$V_{OS(CSA)}$		-1	--	1	mV
Input Bias Current	I_{EA}	V_{CSP} = 1.7V	-10	--	10	nA
Maximum Sourcing Current	I_{MAXSRC}		100	--	--	uA
Gain Bandwidth Product	$G_{BW(CSA)}$	Guarantee by design	--	10	--	MHz
Current Sense Amplifier for Current Balance						
Offset Voltage	$V_{OS(CSA)}$		-1	--	1	mV
Input Bias Current	I_{EA}	V_{CSP} = 1.7V	-10	--	10	nA
Maximum Sourcing Current	I_{MAXSRC}		100	--	--	uA
Gain Bandwidth Product	$G_{BW(CSA)}$	Guarantee by design	--	10	--	MHz
PWM Output						
Output Low Voltage	$V_{OL(PWM)}$	I_{SINK} = 4mA	--	--	0.2	V
Output High Voltage	$V_{OH(PWM)}$	I_{SOURCE} = 4mA	4.7	--	--	V
High Impedance State Leakage		V_{PWM} = 0V ~ 5V	-1	--	1	uA
SVDIO, SVID_ALERT#, VRHOT#						
Pull Down Resistance	R_{on_SVID}		4	--	13	Ω
Leakage Current	I_{L_SVID}		-100	--	100	uA
Input Low Voltage	V_{IL_SVID}		--	--	0.45	V
Input High Voltage	V_{IH_SVID}		0.65	--	--	V
VR_READY, OC#, VR_SHDN#						
Output Low Voltage	V_{OL}	I_{SINK} = 4mA	--	--	0.2	V
Output Leakage Current	I_L	Pull up to 5V	--	--	1	uA
Current Monitoring (IOUT)						
IOUT Current Mirror Accuracy		I_{OUT} to I_{CSN} ratio	95	100	105	%
Droop						
Current Mirror Ratio Accuracy		I_{EAP} / I_{CSN}	95	100	105	%
ADDR Setting						
Source Current			--	50	--	uA
ICCMAX Setting						
A/D Accuracy		ICCMAX pin voltage = 0.74V, read SVID register 0x21h	147	151	155	DEC
VINSEN						
POR Threshold			--	0.8	--	V
POR Hysteresis			--	200	--	mV

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Thermal Monitoring (TM)						
A/D Accuracy		V_{TM} = 4.3V	--	100	--	DEC
A/D Accuracy		V_{TM} = 4.12V to 4.43V	-3	--	3	DEC
Protection						
OVP Threshold	V_{OVP}	V_{FB} - V_{EAP}	--	400	--	mV
OVP Delay	T_{OVP}		--	5	--	us
UVP Threshold	V_{UVP}	V_{EAP} - V_{FB}	--	400	--	mV
UVP Delay	T_{UVP}		--	7.5	--	us
Total Current OCP Threshold	I_{OCP}	Rocset = 20k, measure I_{CSN} current, default value	--	84.5	--	uA
ICCMAX ALERT Threshold	I_{ALERT}	Rocset = 20k, measure I_{CSN} current	--	65	--	uA
Total Current OCP Delay time	T_{OCP1}		--	20	--	us
Per-Phase OCP Threshold	I_{OCP2}	measure I_{CSNx}	--	100	--	uA
Per-Phase OCP Delay time	T_{OCP2}		--	6	--	us

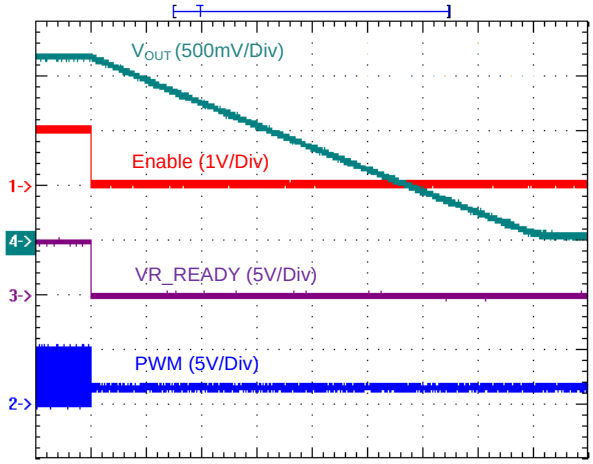
Typical Operation Characteristics

Power On from EN



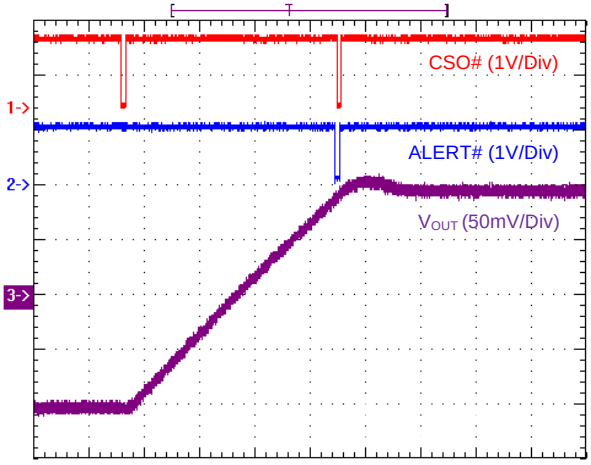
Time：400us/Div
V_{BOOT} = 1.7V

Power Off from EN



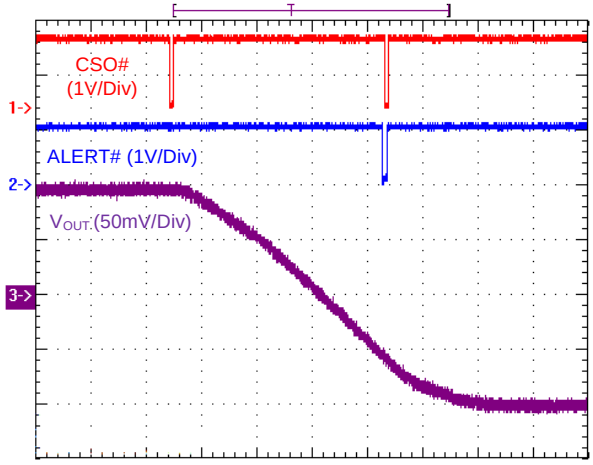
Time：400us/Div
V_{BOOT} = 1.7V

VID Transition Up_Slow



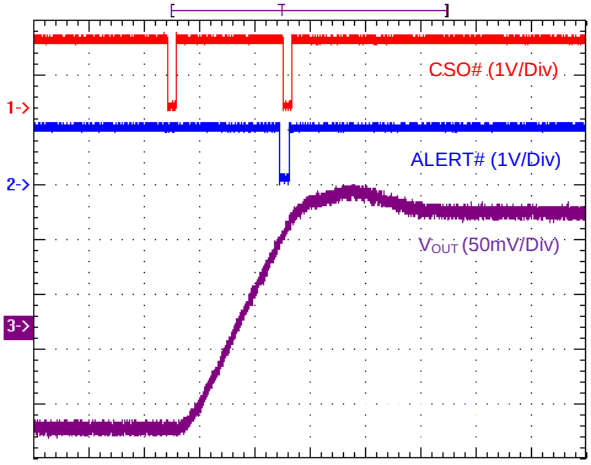
Time：20us/Div
VID = 1.6V to 1.8V, Slew Rate = Slow

VID Transition Down_Slow



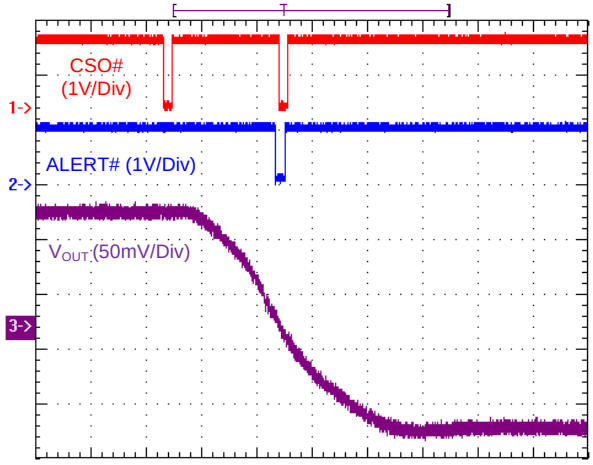
Time：20us/Div
VID = 1.8V to 1.6V, Slew Rate = Slow

VID Transition Up_Fast



Time：10us/Div
VID = 1.6V to 1.8V, Slew Rate = Fast

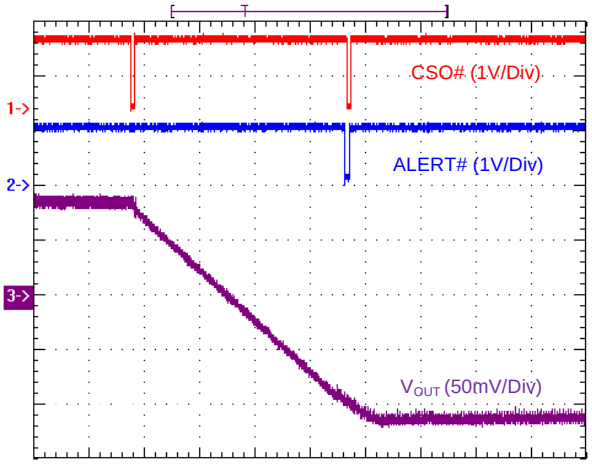
VID Transition Down_Fast



Time：20us/Div
VID = 1.8V to 1.6V, Slew Rate = Fast

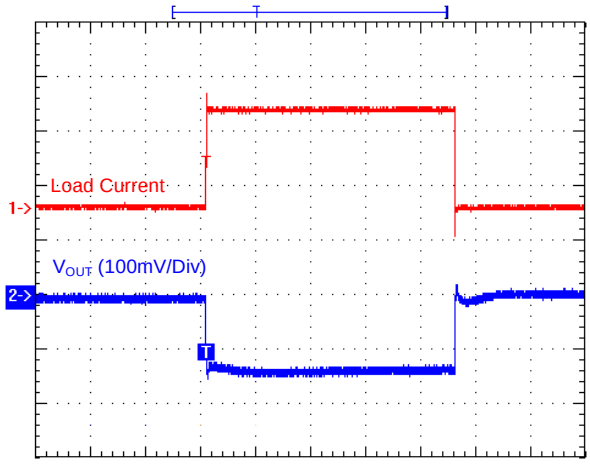
Typical Operation Characteristics

VID Transition Down_Decay



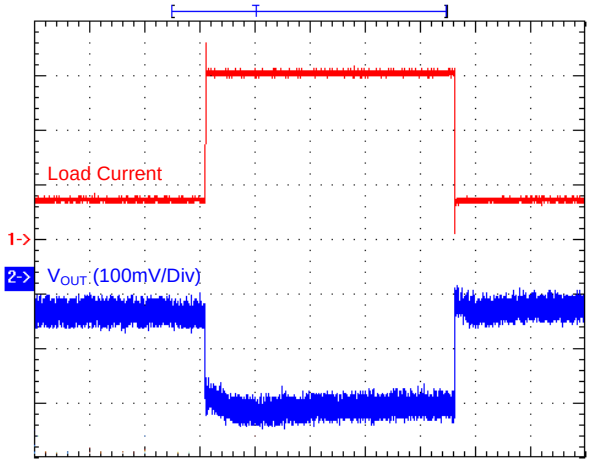
Time：20us/Div
VID = 1.8V to 1.6V, Load = 2A, Slew Rate = Decay

PS0 Load Transient



Time：40us/Div
PS0, Load Current = 1A to 61A

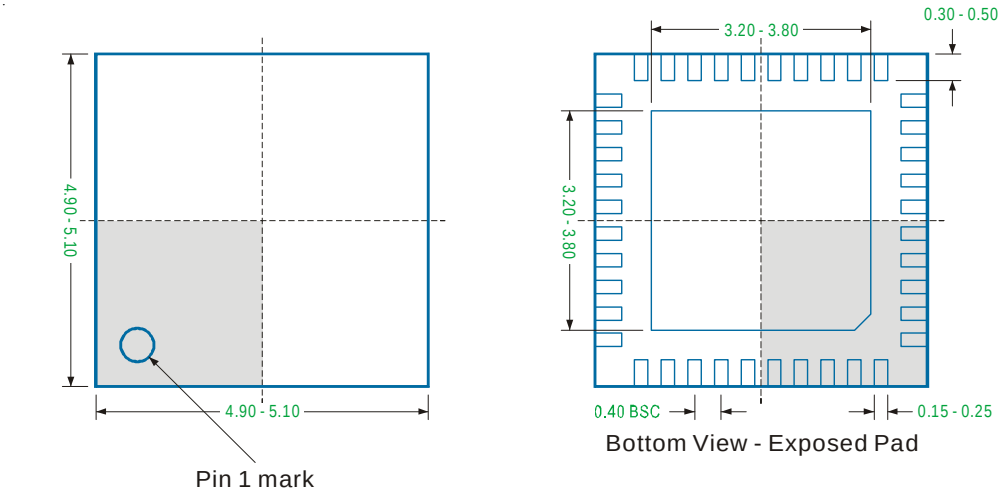
PS1 Load Transient

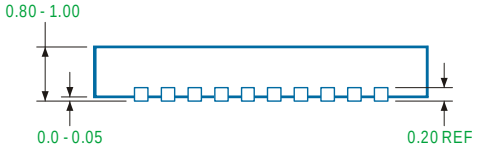


Time：40us/Div
PS1, Load Current = 4A to 20A

Package Information

VQFN5x5-40L





Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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