3/2-Phase SDPWM Controller with SMBus for VR12

General Description

The uP1674 is a Simulated Digital PWM controller that integrates a 3/2-phase PWM controller. uP1674 accurately reports output voltages and output currents to comply with VR12 specification.

The uP1674 integrates 2 bootstrapped drivers that support 12V + 12V driving capability. 3/2 phase operation is enabled by a logic level PWM output, achieving optimal balance between cost and flexibility.

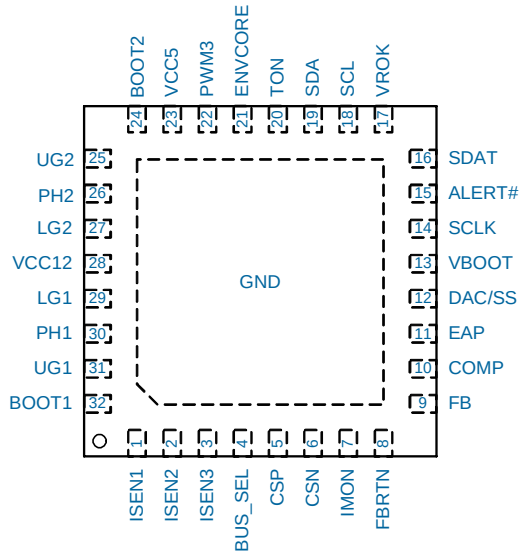
The uP1674 supports phase adding/dropping that is activated by PSI command from SVID or by PS state from SMBUS. The uP1674 operates in diode emulation mode at extreme light load condition and achieves maximum efficiency over entire load current range.

Other features include adjustable soft start, transient boost function, under/over voltage protection and over current protection. The uP1674 is available in VQFN5x5-32L package.

Applications

- **Desktop and Notebook PC Core Power Supplies**

Pin Configuration



Features

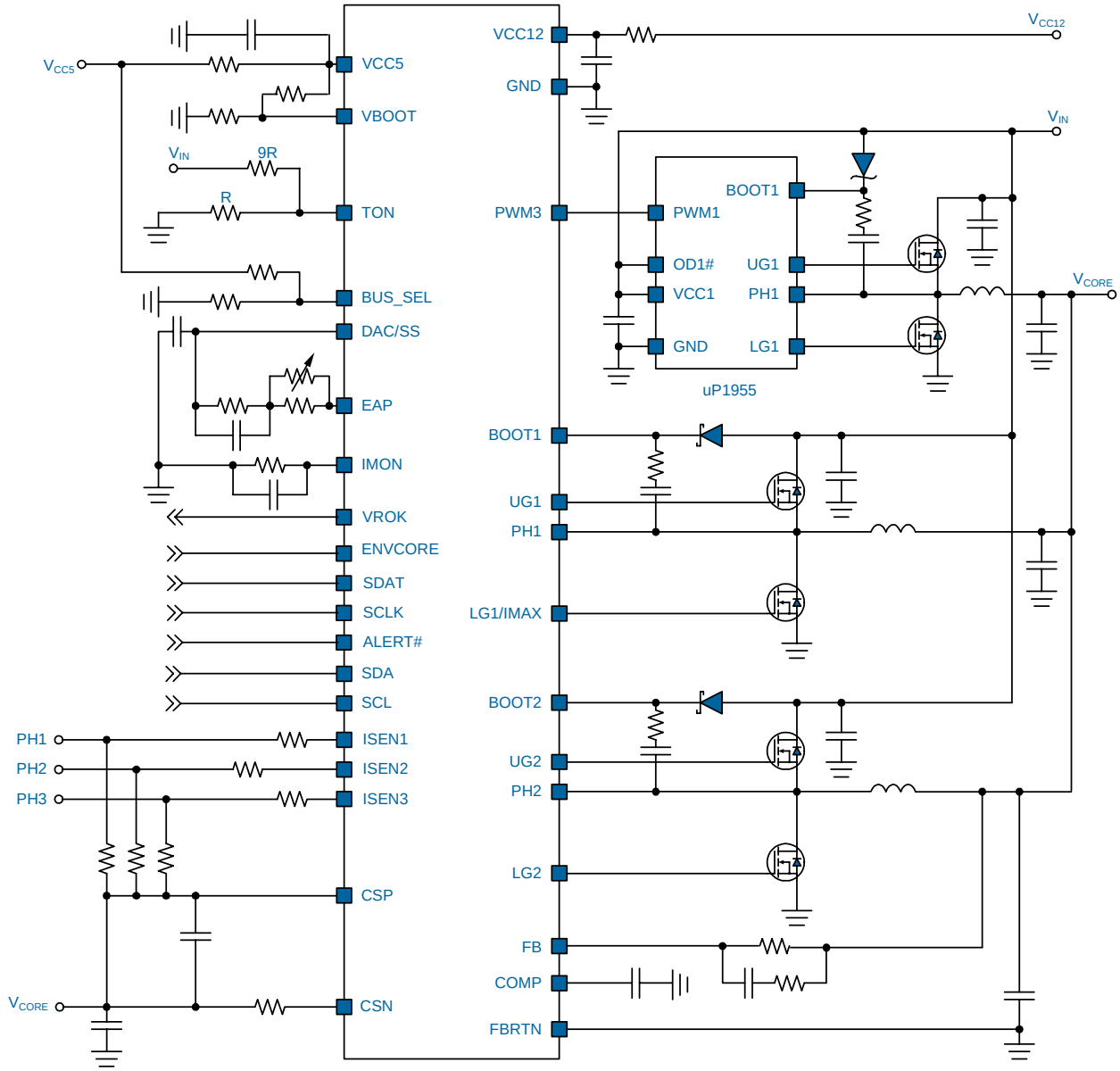
- **Intel VR12/IMVP7 Compliant**
  - **I_{OUT} and V_{OUT} Reporting**
  - **Programmable IMAX, VBOOT, and SVID/SMBUS Address**
- **Selectable 3/2 Phase Operation**
- **RCOT™ Control Topology**
  - **Easy Setting**
  - **Smooth Mode Transition**
  - **Fast Transient Response**
- **Simulated Digital PWM Control**
- **Transient Boost Technology**
- **High Accuracy DAC**
- **Programmable Operation Frequency**
- **Adjustable Soft-Start**
- **OCP/UVP/OVP**
- **RoHS Compliant and Halogen Free**

Ordering Information

Order Number	Package Type	Top Marking
uP1674PQAI	VQFN5x5-32L	uP1674P

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Typical Application Circuit



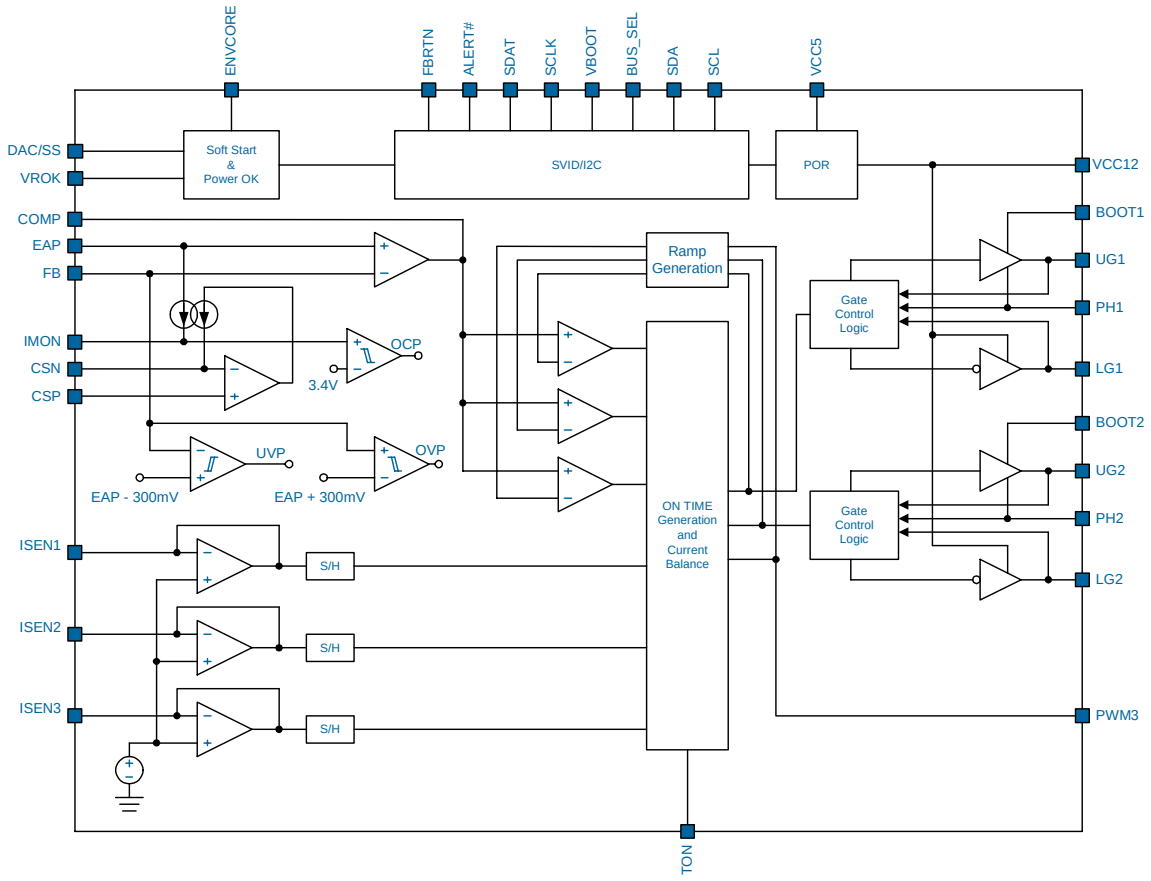
Functional Pin Description

No.	Pin Name	Pin Function
1	ISEN1	**Current Sense for Phase 1.**
2	ISEN2	**Current Sense for Phase 2.**
3	ISEN3	**Current Sense for Phase 3.**
4	BUS_SEL	**SVID and I2C Address selection.** Connect a voltage divider from V_{CC5} - BUS_SEL - GND to set SVID and I2C address.
5	CSP	**Non-inverting Input of the Current Sensing Amplifier for Total Current.** Resistors from each switch node to this pin average the inductor currents on the capacitor between CSP and VCORE.
6	CSN	**Inverting Input of the Current Sensing Amplifier for total Current.** Connect a 1 ohm resistor between CSN and the VCORE side of all output inductors. The selected VCORE point should have equal resistance to the VCORE side of all inductors. PCB trace resistance should be taken into consideration.
7	IMON	**Output Current Monitor.** Output current of IMON is proportional to total load current. Connect a resistor between IMON and GND then the voltage of IMON is proportional to total load current. A capacitor may be connected between IMON and GND also to adjust the response time of IMON.
8	FBRTN	**Feedback Return.** VID DAC and error amplifier reference for remote sensing of the output voltage.
9	FB	**Feedback Pin.** Error amplifier inverting input for remote sensing of the output voltage.
10	COMP	**Error Amp Output.**
11	EAP	**Non-Inverting Input of the Error Amplifier.** A resistor between EAP and the DAC/SS sets the load line.
12	DAC/SS	**DAC Output and Soft start.** A capacitor connected between DAC/SS and FB_RTN sets the soft start ramp-up time.
13	VBOOT	**Boot Voltage Setting.** Connect a voltage divider from V_{CC5} - V_{BOOT} - GND to set boot-up voltage.
14	SCLK	**SVID Clock.**
15	ALERT#	**SVID Alert#.**
16	SDAT	**SVID DATA.**
17	VROK	**Power Good.** This pin is an open-drain output that indicates the soft start end of VCORE is completed and no fault happens.
18	SCL	**SMBUS Clock Input.** This pin receives serial bus clock signal.
19	SDA	**SMBUS Data Input.** This pin is input or output of serial bus data signal.
20	TON	**Input Voltage Detect.** Connect a voltage divider from V_{IN}-TON-GND to set PWM on time.
21	ENVCORE	**Enable Control.** Voltage of this pin higher than 0.65V enables the V_{CORE} while it is lower than 0.45V and will disable it.
22	PWM3	**PWM3 Output.** Connect this pin to the PWM input of external MOSFET Driver.

Functional Pin Description

No.	Pin Name	Pin Function
23	VCC5	**Supply Input for the IC Control Logic.**Connect this pin to a 5V voltage source with an RC filter.
24	BOOT2	**BOOT for Phase 2.** Connect a capacitor from this pin to PH2 to form a bootstrap circuit for upper gate driver of the phase 2.
25	UG2	**Upper Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 upper MOSFET
26	PH2	**Phase Pin for Phase 2.** This pin is the return path of upper gate driver for phase 2. Connect a capacitor from this pin to BOOT2 to form a bootstrap circuit for upper gate driver of the phase2.
27	LG2	**Lower Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 lower MOSFET.
28	VCC12	**Supply Input for the IC Internal Drivers.**Connect this pin to a 12V voltage source with an RC filter.
29	LG1	**Lower Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 lower MOSFET.
30	PH1	**Phase Pin for Phase 1.** This pin is the return path of upper gate driver for phase 1. Connect a capacitor from this pin to BOOT1 to form a bootstrap circuit for upper gate driver of the phase1.
31	UG1	**Upper Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 upper MOSFET.
32	BOOT1	**BOOT for Phase 1.** Connect a capacitor from this pin to PH1 to form a bootstrap circuit forupper gate driver of the phase 1.

Functional Block Diagram



Functional Description

The uP1674 is a VR12/IMVP7 compliant PWM controller for CPU power. It integrates SMBus to provide variety of VR adjustment. Compensator is dynamically adjustable through the SMBus as well.

Power Input and Power On Reset

Figure 1 shows the power ready detection of the uP1674. The uP1674 receives supply input from VCC12 pin to provide current to gate drivers. RC filters are required for locally bypassing the supply input pin. The VCC12 pin is monitored for power on reset, the POR level is typically 4.2V at VCC12 rising.

The VCC5 pin receives a well-decoupled 5V voltage source to power the internal control circuit. Place a 0.1uF ceramic capacitor physically near the VCC5 pin for locally bypassing the VCC5 voltage. The VCC5 voltage is continuously monitored for power on reset. The POR level is typical 4.3V at VCC5 rising.

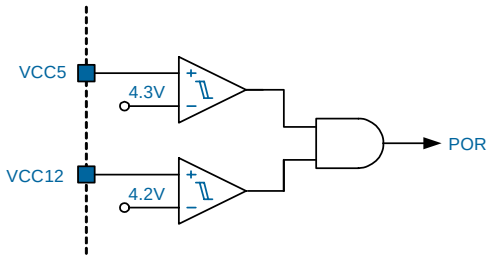


Figure1. Circuit for Power Ready Detection

Phase Number of Operation

The controller supports 3/2-phase operation. During POR, uP1674 detects PWM3 to determine the operation phase number of V_{CORE}. The operation phase number is latched by uP1674 once it is determined. Leave the unused ISEN pin floating.

Initial Parameters Setting

The LG1/IMAX, BUS_SEL and VBOOT pins set the parameters required for VR12/IMVP7 as shown in Figure 2.

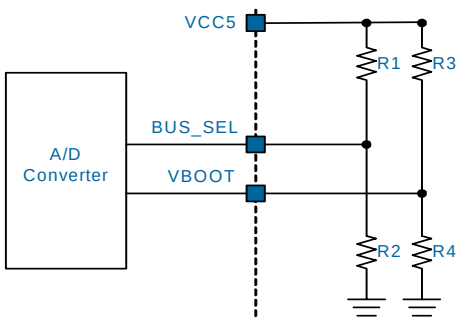


Figure 2. Initial Parameter Setting

IMAX sets the rated current of the uP1674 Converter. The IMAX voltage is digitized by internal 8-bit A/D converter as:

$$IMAX[7:0] = \frac{V_{IMAX} \times 8 \times 256}{V_{CC5}}$$

The LSB of the register is 1A. The maximum value of the register is 255A.

VBOOT pin sets the boot-up voltage as shown in Table 1.

Table 1. Boot-up Voltage Table

VBOOT Voltage	VCORE(V)
0	0
37.5%*VDD	1
62.5%*VDD	1.1
VDD	1.5

BUS_SEL pin sets the I2C address and SVID address as shown in Table 2.

Table 2. SVID and I2C address Table

SVID Address	I2C Address (Hex)	BUE_SEL Voltage (V)
2	70	0
	72	9.375%*VDD
	74	15.625%*VDD
	76	21.875%*VDD
4	70	28.125%*VDD
	72	34.375%*VDD
	74	40.625%*VDD
	76	46.875%*VDD
6	70	53.125%*VDD
	72	59.375%*VDD
	74	65.625%*VDD
	76	71.875%*VDD
8	70	78.125%*VDD
	72	84.375%*VDD
	74	90.625%*VDD
	76	VDD

PWM On Time Setting

uP1674 uses TON pin for power stage input voltage sensing and connects a voltage divider from VIN-TON-GND to set PWM on time. Please keep the ratio of VIN-TON resistor and TON-GND resistor 9:1 for controller on time calculation.

V_{DAC} Generator

The uP1674 builds in precise bandgap reference circuit as shown in Figure 3. The output voltage of bandgap reference is 2.1V with respective to FBRTN. The uP1674 uses plural resistors to generate precise reference voltages ranging from 0.0V to 2.1V, with 5mV increments. All the voltages connect to a multiplexer (MUX). The multiplexer outputs V_{DAC} according to the SVID inputs. Please note that all the voltage values in Figure 3 are referred to FBRTN.

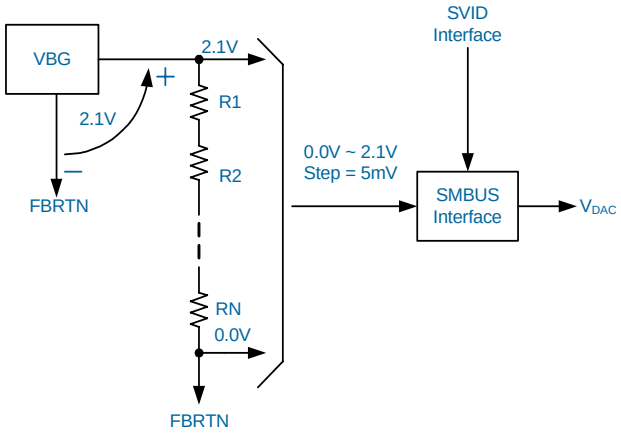


Figure 3. V_{DAC} Generator Circuit

The V_{DAC} voltage is expressed as:

$$V_{DAC} = \text{SetVID} + \text{Offset}$$

where SetVID and Offset can be programmed by SVID or SMBUS. Table 3 illustrates the SetVID voltages according to VID code.

State Transition

Figure 4 illustrates the state diagram of the uP1674. The uP1674 initiates it soft start cycle whenever POR transits from Low to High. VROK sets high when soft start cycle completes and no fault occurs. When any faults occurs, the uP1674 shutdown both power rails and latches. The latch state can only be reset by POR.

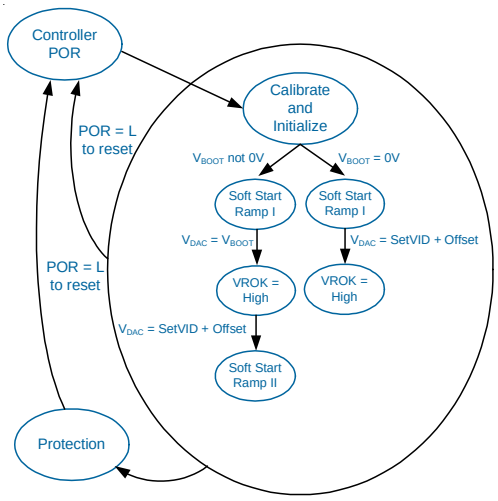


Figure 4. State Diagram.

Soft Start

The soft start slew rate is programmable. The soft start function limits the output voltage slew rate during both soft start and VID on the fly (VID_OTF) periods as shown in Figure 5. The soft start buffer is a current limited buffer and output current I_{SS} is used to charge/discharge the soft start capacitor C_{SS} when V_{DAC} transition during soft start and VID_OTF. This limits the slew rate of $V_{DAC/SS}$. Consequently EAP and FB pin voltages will follow the slew rate of $V_{DAC/SS}$.

Table 3. Intel SVID Table

SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)
0x00	0.000	0x25	0.430	0x4A	0.615	0x6F	0.800	0x94	0.985	0xB8	1.165	0xDC	1.345
0x01	0.250	0x26	0.435	0x4B	0.620	0x70	0.805	0x95	0.990	0xB9	1.170	0xDD	1.350
0x02	0.255	0x27	0.440	0x4C	0.625	0x71	0.810	0x96	0.995	0xBA	1.175	0xDE	1.355
0x03	0.260	0x28	0.445	0x4D	0.630	0x72	0.815	0x97	1.000	0xBB	1.180	0xDF	1.360
0x04	0.265	0x29	0.450	0x4E	0.635	0x73	0.820	0x98	1.005	0xBC	1.185	0xE0	1.365
0x05	0.270	0x2A	0.455	0x4F	0.640	0x74	0.825	0x99	1.010	0xBD	1.190	0xE1	1.370
0x06	0.275	0x2B	0.460	0x50	0.645	0x75	0.830	0x9A	1.015	0xBE	1.195	0xE2	1.375
0x07	0.280	0x2C	0.465	0x51	0.650	0x76	0.835	0x9B	1.020	0xBF	1.200	0xE3	1.380
0x08	0.285	0x2D	0.470	0x52	0.655	0x77	0.840	0x9C	1.025	0xC0	1.205	0xE4	1.385
0x09	0.290	0x2E	0.475	0x53	0.660	0x78	0.845	0x9D	1.030	0xC1	1.210	0xE5	1.390
0x0A	0.295	0x2F	0.480	0x54	0.665	0x79	0.850	0x9E	1.035	0xC2	1.215	0xE6	1.395
0x0B	0.300	0x30	0.485	0x55	0.670	0x7A	0.855	0x9F	1.040	0xC3	1.220	0xE7	1.400
0x0C	0.305	0x31	0.490	0x56	0.675	0x7B	0.860	0xA0	1.045	0xC4	1.225	0xE8	1.405
0x0D	0.310	0x32	0.495	0x57	0.680	0x7C	0.865	0xA1	1.050	0xC5	1.230	0xE9	1.410
0x0E	0.315	0x33	0.500	0x58	0.685	0x7D	0.870	0xA2	1.055	0xC6	1.235	0xEA	1.415
0x0F	0.320	0x34	0.505	0x59	0.690	0x7E	0.875	0xA3	1.060	0xC7	1.240	0xEB	1.420
0x10	0.325	0x35	0.510	0x5A	0.695	0x7F	0.880	0xA4	1.065	0xC8	1.245	0xEC	1.425
0x11	0.330	0x36	0.515	0x5B	0.700	0x80	0.885	0xA5	1.070	0xC9	1.250	0xED	1.430
0x12	0.335	0x37	0.520	0x5C	0.705	0x81	0.890	0xA6	1.075	0xCA	1.255	0xEE	1.435
0x13	0.340	0x38	0.525	0x5D	0.710	0x82	0.895	0xA7	1.080	0xCB	1.260	0xEF	1.440
0x14	0.345	0x39	0.530	0x5E	0.715	0x83	0.900	0xA8	1.085	0xCC	1.265	0xF0	1.445
0x15	0.350	0x3A	0.535	0x5F	0.720	0x84	0.905	0xA9	1.090	0xCD	1.270	0xF1	1.450
0x16	0.355	0x3B	0.540	0x60	0.725	0x85	0.910	0xAA	1.095	0xCE	1.275	0xF2	1.455
0x17	0.360	0x3C	0.545	0x61	0.730	0x86	0.915	0xAB	1.100	0xCF	1.280	0xF3	1.460
0x18	0.365	0x3D	0.550	0x62	0.735	0x87	0.920	0xAC	1.105	0xD0	1.285	0xF4	1.465
0x19	0.370	0x3E	0.555	0x63	0.740	0x88	0.925	0xAD	1.110	0xD1	1.290	0xF5	1.470
0x1A	0.375	0x3F	0.560	0x64	0.745	0x89	0.930	0xAE	1.115	0xD2	1.295	0xF6	1.475
0x1B	0.380	0x40	0.565	0x65	0.750	0x8A	0.935	0xAF	1.120	0xD3	1.300	0xF7	1.480
0x1C	0.385	0x41	0.570	0x66	0.755	0x8B	0.940	0xB0	1.125	0xD4	1.305	0xF8	1.485
0x1D	0.390	0x42	0.575	0x67	0.760	0x8C	0.945	0xB1	1.130	0xD5	1.310	0xF9	1.490
0x1E	0.395	0x43	0.580	0x68	0.765	0x8D	0.950	0xB2	1.135	0xD6	1.315	0xFA	1.495
0x1F	0.400	0x44	0.585	0x69	0.770	0x8E	0.955	0xB3	1.140	0xD7	1.320	0xFB	1.500
0x20	0.405	0x45	0.590	0x6A	0.775	0x8F	0.960	0xB4	1.145	0xD8	1.325	0xFC	1.505
0x21	0.410	0x46	0.595	0x6B	0.780	0x90	0.965	0xB5	1.150	0xD9	1.330	0xFD	1.510
0x22	0.415	0x47	0.600	0x6C	0.785	0x91	0.970	0xB6	1.155	0xDA	1.335	0xFE	1.515
0x23	0.420	0x48	0.605	0x6D	0.790	0x92	0.975	0xB7	1.160	0xDB	1.340	0xFF	1.520
0x24	0.425	0x49	0.610	0x6E	0.795	0x93	0.980						

Functional Description

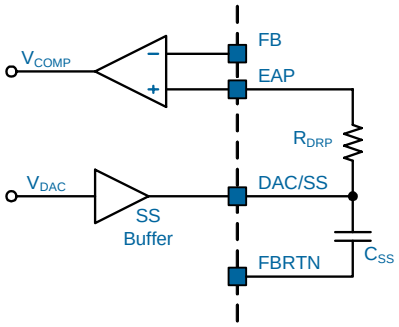


Figure 5. Circuit for Soft Start and Dynamic VID.

The DAC/SS level can be dynamically programmed by SVID/SMBUS interfaces.

Figure 6 shows a typical soft start waveforms of V_{BOOT} ≠ 0V. When ENABLE = Low, the DAC/SS pin is hold at GND. The uP1674 takes about 2ms (T1) for initialization before the $V_{DAC/SS}$ begins to rise to V_{BOOT}. The ramping up period T2 is decided by V_{BOOT}, C_{SS} and I_{SS} and is calculated as:

$$T2 = \frac{V_{BOOT} \times C_{SS}}{I_{SS}}, \; I_{SS} = 50uA$$

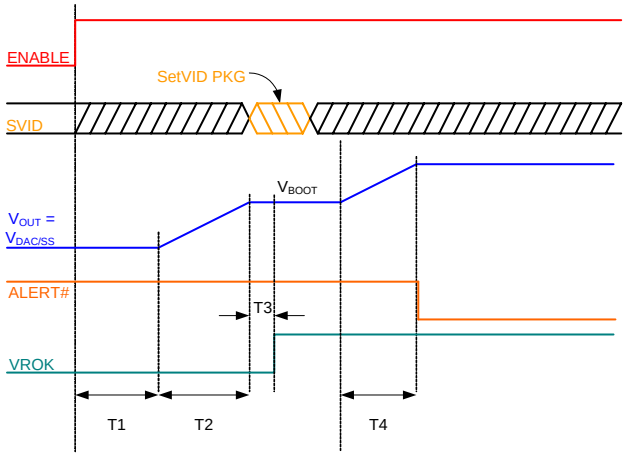


Figure 6. Soft Start Waveforms of V_{BOOT} ≠ 0V.

The VROK is asserted with an extra 200us time delay T3.

When the SetVID command is acknowledged, the $V_{DAC/SS}$ starts to ramp to the new V_{DAC} level with a typical 600ns delay time. The ramping period T4 is decided by V_{DAC}, V_{BOOT}, C_{SS} and I_{SS} and is calculated as:

$$T4 = \frac{(V_{DAC} - V_{BOOT}) \times C_{SS}}{I_{SS}}$$

SVID-FAST I_{SS} = 200uA

SVID-SLOW I_{SS} = 50uA

The uP1674 asserts soft start end when $V_{DAC/SS}$ is within 10mV of it target level and sets ALERT# low.

Figure 7 shows a typical soft start waveforms of V_{BOOT} = 0V. When ENABLE = Low, the DAC/SS pin is hold at GND. The uP1674 takes about 2ms (T1) for initialization.

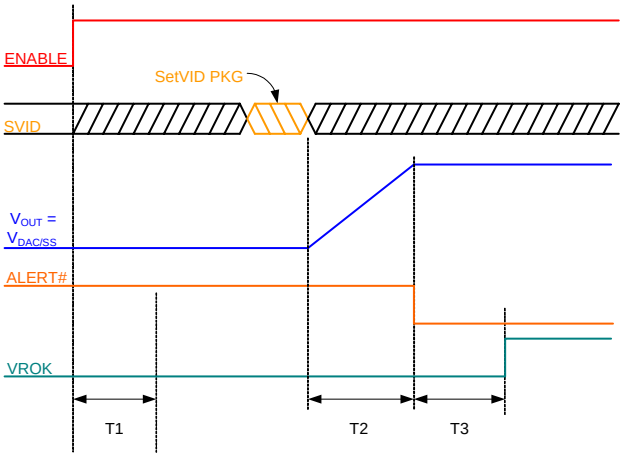


Figure 7. Soft Start Waveforms of V_{BOOT} = 0V.

When the SetVID command is acknowledged, the $V_{DAC/SS}$ starts to ramp to the new V_{DAC} level with a typical 600ns delay. The ramping period T2 is decided by V_{DAC}, C_{SS} and I_{SS} and is calculated as:

$$T2 = \frac{V_{DAC} \times C_{SS}}{I_{SS}}, \; I_{SS} = 50uA$$

The uP1674 asserts soft start end when $V_{DAC/SS}$ is within 10mV of its target level and sets ALERT# low. The VROK is asserted with an extra 200us time delay T3.

Dynamic VID

The uP1674 can accept VID input changes during normal operation. This allows the output voltage V_{OUT} to change while the DC/DC converter is running and supplying current to the load. This is commonly referred to as VID on-the-fly (VID_OTF). A VID_OTF may occur under either light or heavy load conditions. This change can be positive or negative. During VID_OTF, V_{DAC} is a staircase waveform. In the uP1674, C_{SS} is also used to filter the $V_{DAC/SS}$. By properly selecting C_{SS}, VID_OTF performance can be improved.

Output Voltage Differential Sensing

The uP1674 uses differential sensing by a high-gain low-offset error amplifier as shown in Figure 8. The CPU voltage is sensed between the FB and FBRTN pins. A resistor R_{FB} connects FB pin and the positive remote sense pin of the CPU V_{CCP}. FBRTN pin connects to the negative remote sense pin of CPU V_{CCN} directly. The error amplifier compares the V_{FB} with V_{EAP} (= $V_{DAC/SS}$ - I_{SUM} x R_{DRP}) to regulate the output voltage.

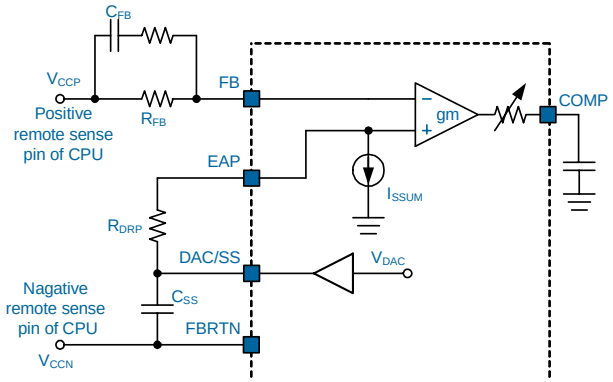


Figure 8. Circuit for V_{OUT} Differential Sensing.

Channel Current Sensing

The uP1674 extracts phase currents for current balance and over current protection by parasitic on-resistance of the lower switches when turn on as shown in Figure 9. The ISEN1/2/3 pins sense the corresponding phase current when the low side MOSFETs are turned on.

$I_{SENX} = ((I_{PHX} \times R_{DS(ON)}) + V_{DC}) / R_{SENX}$

where I_{SENX} is the sample and held phase current signal, I_{PHX} is phase current, $R_{DS(ON)}$ is the on-resistance of the low side MOSFETs, and V_{DC} is an offset voltage for the current balance circuit. The current balance circuit increases the duty cycle of the phase whose phase current is smaller than others and decrease the duty cycle of the phase whose phase current is larger than others.

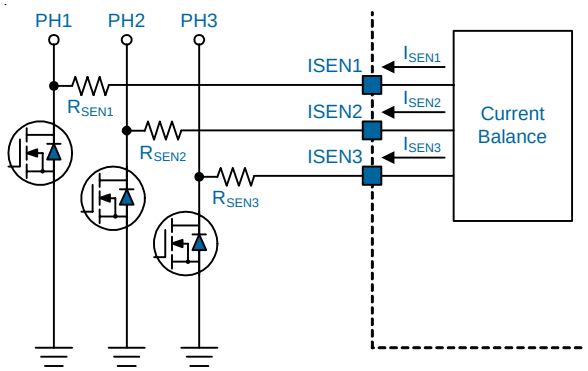


Figure 9. Phase Current Sensing and Current Balance.

Select R_{SENX} to set the current balance gain.

Total Load Current Sensing

The uP1674 provides low input offset current sense amplifier (CSA) to monitor the total load current flowing through inductor as shown in Figure 10.

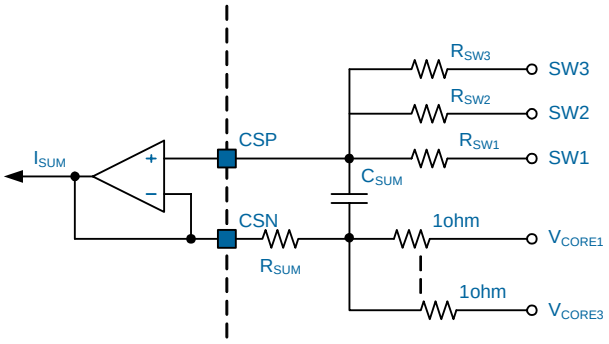


Figure 10. Total Load Current Sensing.

Output current of CSA (I_{SUM}) is used for active voltage positioning (AVP), load current monitoring and over current protection. In this inductor current sensing topology, R_{SW} and C_{SUM} must be selected according to the equation below:

$$k \times \frac{L}{R_{DC}} = \frac{R_{SW} \times C_{SUM}}{N}$$

where R_{DC} is the DCR of the output inductor, N is the phase number of operation . Theoretically, k should be equal to 1 to sense the instantaneous total load curret. But in real application usually 1.2 ~ 1.8 is better for transient response.

$I_{SUM} = I_{OUT}$ x R_{DC} / R_{SUM} / N

Droop (Load Line) Tuning

The I_{SUM} is mirrored to EAP pin as shown in Figure 8. This creates voltage drop across R_{DRP} and makes V_{EAP} as:

$$V_{EAP} = V_{DAC/SS} - I_{SUM} \times R_{DRP} = V_{DAC/SS} - \frac{I_{OUT} \times R_{DC} \times R_{DRP}}{R_{CSN} \times N}$$

Functional Description

In steady state, output voltage is equal to V_{EAP}. Thus, the output voltage decreasing linearly with I_{OUT} is obtained. The loadline is defined as:

$$LoadLine = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{R_{DC} \times R_{DRP}}{R_{SUM} \times N}$$

In real application, NTC network is used as C_{SUM} to compensate the temperature effect on DCR of inductor.

Output Current Monitoring

The I_{SUM} is mirrored to IMON pin for ourput current monitoring and over current protection. The V_{IMON} voltage is created that is proportional to the output current as:

$$\frac{2.56V}{R_{IMON}} = \frac{I_{MAX} \times R_{DC}}{R_{SUM} \times N}$$, I_{MAX} is maximun current of V_{CORE} support.

Output Over Current Protection

The V_{IMON} pin voltage is continuously monitored for over current protection (OCP). OCP is triggered and turns off the uP1674 , if V_{IMON} is higher than 3.4V with 20us delay. The OCP is latch-off type and can be reset only by POR toggling.

Control Loop

The uP1674 adopts the uPI's proprietary RCOT™ control technology. The RCOT uses the constant on-time modulator. The output voltage is sensed to compare with the internal high accurate DAC. The DAC is commanded by CPU through the SVID interface. The amplified error signal, COMP, is compared to the internal RAMP to initiate an on-time to PWM. The RCOT features easy design, fast transient response and smooth mode transition and especially suit for powering the microprocessor.

Over Voltage Protection (OVP)

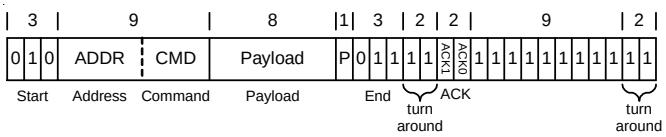
The over voltage protection monitors the output voltage via the FB pin. Once V_{FB} exceeds V_{EAP} + 300mV, OVP is triggered and latched. The uP1674 will try to turn on low side MOSFET and turn off high side MOSFET to protect CPU. A 20us delay is used in OVP detection circuit to prevent false trigger. Only re-start up can release OVP latch.

Under Voltage Protection (UVP)

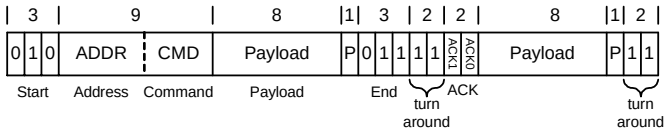
The under voltage protection monitors the output voltage via the FB pin. After the uP1674 starting up and V_{OUT} ramping up to V_{BOOT}, the uP1674 initiates UVP function. Once V_{FB} is lower than EAP-300mV, UVP is triggered and latched. The uP1674 will try to turn off both high side and low side MOSFETs. A 5uS delay is used in UVP detection circuit to prevent false trigger. Only re-start up can release UVP latch.

SerialVID(SVID)

SerialVID is a three wire(SCLK,SDAT,Alert#)serial synchronous interfaceused to transfer power management information between a micoprocessor and a VRM,The link is between one microprocessor and multiple VR Controller on the same bus.There is a 4 bit addressing scheme for the slave devices,The Clock is source synchronous from the CPU. The CPU drives the SCLK signal with a low-voltage open drain driver.The master may stop the SCLK signal to save power when no data transfer is needed. SDAT is a low-voltage,open-drain data signal that master and slave use to send information to each other,The bus will opersate are a maximum frequency of 26.25MHz,The alret line is an active low signal driven asynchronously from the slave device,indicating to the Master that the status register needs to be read.



Set Command



Get Command

Alert#

Alert is used to indicated the microporcessor that the status register needs to be read.

Alert# asserts under the following conditions:

(1) Bit0 of Status1 Reg changing from 0 to 1.

(2) Bit1 Status1 Reg changing form 0 to 1 or 1 to 0.

(3) Bit2 changing from 0 to 1 or 1 to 0.

Acknowledge Enconding

	Ack1	Ack0
Error On All Transaction.	0	0
NAK.	0	1
ACK.	1	0
Reject.	1	1

Serial VID Commands

a.SetVID-Fast(01h)

The SetVID_fast command contains the target VID in the payload byte. The range of voltage is defined in the VID table.The VR should ramp up to new VID setting with a fast slew rate.The default fast slew rate is 10 mV/us minimum.Faster slew rate are desired.

The SetVID_fast command is preemptive.IE the VR interrupts its current processes and moves to the new VID. With back to back SetVID commands,the VR resets the alert line after the ACK and it starts moving output voltage to the new target .

b.SetVID_Slow(02h)

he SetVID_Slow command contains the target VID in the payload byte. The range of voltage is defined in the VID table.The VR should ramp up to new VID setting with a slow slew rate.The default slow slew rate is 1/4 the fast slow rate.

c.SetVID_Decay(03h)

The SetVID_Decay command is the slowest of the SetVID dynamic VID transitions.It is normally used for VID down transitions.The VR does not control the slow rate,the output voltage declines with the output load current only.SetVID_Decay implies diode emulation mode of opersation.If a SetPS PS1 or PS0 occurs,the VR should jump out of decay mode and actively control the slew rate.

d.SetPS(04h)

uP1674 Support three power saving states as below:

	Opersation Mode
00h	Full Phase
01h	Single Phase
02h	PSM
03h	PSM

e.Write to register(SetRegADR(05h),SetRegDAT(06h)

The register file can be written to by the microprocessor in certain ranges through an address register and a data rigister.To program a register,SetRegADR(05h) and SetReg(06h) commands must be executed.If the event of a SetRegADR(all call), SetRegDAT(all call) the slave responds with the NAK(01).

f.Read from a register(GetReg(07h)

The payload byte in the command contains an index into the data register file.If the GetReg command cantains none supported addresss,the slave responds with the Reject (11b) acknowledge.In the event of GetReg(AllCall),the slave responds with the NAK(01b).

VR Identification Registers

(1)Vender_ID(00h)-Default 26h

(2)Product_ID(01h)-Default 15h

(3)Product_Revision(02h)-Default 01h

(4)Protocal_Version(05h)-Default 01h

(5)VR_Capability(06h)-Default 81h

Bit7	Bit6	Bit5	Bit4
Iout format (15h)	Temperature (17h)	Input Power (1Bh)	Input Voltage (1Ah)
Bit3	Bit2	Bit1	Bit0
Input Current (19h)	Pout (18h)	Vout (16h)	Iout (15h)

Bit7	Bit2	Bit1	Bit0
Read Status_2	ICC MAX Alert	Thermal Alert	VR Settled

VR Opersation Register

(6)Status_1(10h)-Default 00h

VR Settled = 1 if VR is at target voltage.

VR Settled = 0 if VR is ramping.

Thermal Alert =1 if over temperature.

Thermal Alert =0 if temperature is ok.

ICCMax Alert=1 if load current > ICCMax .

ICCMax Alert=0 if in normal current range.

Read Status_2 =1 ,go read status2 register(1Ch),

and clear to 0 when GetReg(status2) command is issued.

(7)Status_2(11h)-Default 00h

Bit1	Bit0
SVID Data Frame error	SVID Parity error

(8)Status2_lastread(1Ch)

This is register is written or over-written when a GetReg(status2) command is issued with the contents of the Status2 register. The master will issue GetReg(status2_lastread) if there is a parity error in the VR payload of the GetReg(status2) command to avoid the loss of the Status2 data.

(9)VID Setting(31h)

This register contains the current VID setting as programmed by the SETVID command.

(10)Power State(PS) register(32h)

The PS register contains the current power state setting as programed with a SetPS Command.

	Power State
00h	PS0Full Phase
01h	PS1Single Phase
02h	PS2 PSM
03h	PS3 PSM
04h~FFh	No Support VR NAK 11b

(11)Offset Register(33h)

This register sets VID offset by number of VID steps up to FFh in the VID table.The VID+Offset can be a voltage greater than the Vout_max(30h) register. VID+Offset does not extend the range of the VID table over 1.52.

Any combination of VID+offset > FFh in VID table should be rejected and stay at current VID setting.

Binary format,2's complement

Default 00h=no offset

bit 7 =sign bit

0000001=offset + 1 VID step

0000011=offset + 3 VID steps

1111111=offset - 1 VID step

Bit7~Bit2	Bit1	Bit0
TBD	Lock VID/PS	VR_Ready 0V

(12)Multi_VR_Config(34h)-Default 00h

This register is programmed during initialization phase of a AVID VR with the SetRegADR, SetRegDAT commands by the master.It is used to configure slaves in server platforms with multiple VRs on the same SVID bus. It use in notebook and desktop systems is to program the VR_Ready opersation when the VID command is set to zero volts or of condition.

Bit0=0, VR_Ready would be de-assert if the VR is given a SetVID(0.0V) command.

Bit0=1, VR_Ready would not de-assert when issue a SetVID(0.0V) command.

Bit1=0, Normal mode, not locked.

Bit1=1, VR is locked in the current VID setting and power state setting. It will reject all SETVID commands including SetVID(AllCall) and SePS(AllCall) until such time that VR is issued a SetPS(00h) returning to normal mode to unlock that VR.

VR Platform Performance Register

(13)ICCmax(21h)

This registers contains the maximum current the VR is designed to supprot.

(14)Vboot(26h)

uP1674 support 4 steps Vboot voltage setting (0V,1V,1.1V,1.5V) and programmed by Vboot pin .

VR telemetry Register

(15)Output Current Register(15h)

8 bit binary word digitized version of average output current.

Table 4. Stanstard SVID Commands

Code	Command	Master Payload Contents	Slave Payload Contents	Description	Pre-emptive	All Call
00h	not supported	NA	NA	NA	NA	NA
01h	SetVID_Fast	VID Code	NA	Set ne target VID code, VR jumps to new VID target with controlled defautl fast slew rate 10mV/us.	Yes	Yes
02h	SetVID_Slow	VID Code	NA	Set ne target VID code, VR jumps to new VID target with controlled defautl slow slew rate 2.5mV/us.	Yes	Yes
03h	SetVID_Decay	VID Code	NA	Set ne target VID code, VR jumps to new VID target but does not control the slew rate. The output voltage decays at a rate proortional to the load current.	Yes	Yes
04h	SetPS	Byte indicating power states	NA	Set power state	No	Yes
05h	SetRegADR	Pointer of registers in data table	NA	Set the pointer of the data register	No	No
06h	SetRegDAT	New data register content	NA	Write the contents to the data register	No	No
07h	GetReg	Pointer of register in data table	Specified Register Contents	Slave returns the contents of the specified refister as the payload.	No	No
08h ~ 1Fh	not supported	NA	NA	NA	NA	No

I2C Interface

The uP1674 includes an I2C interface to adjust output voltage, switching frequency and operating phase number of VR controller according to the total load current dynamically. We call it AUTOPHASE. The target of AUTOPHASE is an optimal VR design for both power conversion efficiency and CPU performance. Operating parameters that can be adjusted through the I2C are summarized as Table 11.

VM0~2: Define the 4 load current states (LCS0~3)

Voltage at IMON pin V_{IMON} is converted to an 8-bit digital value as IMONAD[7:0] = V_{IMON}/10mV. IMONAD[7:0] is compared with three I2C programmable registers VM0~2 to determine the load current states LCS0~3 as:

LCS0: VIMON > VM0, highest load current.

LCS1: VM0 > VIMON > VM1

LCS2: VM1 > VIMON > VM2

LCS3: VM3 > VIMON, lowest load current.

VM_Hys

Define the VM0~2 state hystersis VMx_Hys as shown in Table 5.

Table 5. V_{HYS} Setting Table

VM0~2_Hys	VM0~2_Hys
000	60mV
001	80mV
010	100mV
011	120mV
100	140mV
101	160mV
110	180mV
111	200mV

VOFS0~3

Define voltage offset of the 4 load current states: 4 I2C programmable registers VOFS0~3 define the voltage offset in load current status LCS0~3 respectively. See Table 12 for the voltage offset table.

IICF0~3

Frequency adjust of the 4 load current states: IICF0~3 define the frequency in load current states LCS0~3 respectively as show in Table 6.

Table 6. IICF Setting Table

IICF0~3	Freq(Hz)
000	150K
001	200K
010	250K
011	300K
100	350K
101	400K
110	450K
111	500K

IICP0~3

Operating phase number of the 4 load current states: 4 I2C programmable registers IICP0~3 define the operating phase number in load current states LCS0~3 respectively.

IICPn[1:0] = [00] => full-phase set by hardware

IICPn[1:0] = [01] => 3-phase

IICPn[1:0] = [10] => 2-phase

IICPn[1:0] = [11] => 1-phase

Misc2[7:0]

Register Misc2[7:0] enables/disables the I2C functions as:

Misc[7]=[1]=> enables AutoPhase function.

Misc[7]=[0]=> disable AutoPhase function

Misc[5]=[1]=> enables PSM operation.

Misc[5]=[0]=> disable PSM operation.

Misc[3]=[1]=> enable LoadLine.

Misc[3]=[0]=> disable LoadLine.

Misc[1]=[1]=> enable Voltage Offset

Misc[1]=[0]=> disable Voltage Offset

WD[7:4]:Watchinng Dog Timer

WD[7]=[1]=> enables watching dog timer.

[0]=> disable watching dog timer.

WD[6]: Watching Dog Timer (If time-out set to 1, cleared after reading, read only),

WD[5:4]=[00] => 800ms

WD[5:4]=[01] => 1600ms

WD[5:4]=[10] => 3200ms

WD[5:4]=[11] => 6400ms

RCOMP[3:0]

RCOMP is Compensation Resistor ,it can be programming by 0x13 Register as show in Table 7.

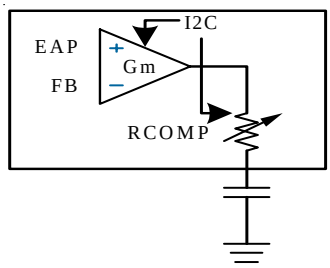


Table 7. RCOMP Setting Table

Bit[3:0]	RCOMP(ohm)
0000	5K
0001	10K
0010	15K
0011	20K
0100	25K
0101	30K
0110	35K
0111	40K
1000	45K
1001	50K
1010	55K
1011	60K
1100	65K
1101	70K
1110	75K
1111	80K

LCHVID[7:0]:Latch VID

The register LCHVID stores the 8 bits VID Code of user defined, when enable this function,VR will ignore CPU SETVID Command.

IOUT[7:0]:Output Current Reading

The register is a copy from SVID 0x15 register.

VOUT[7:0]:Output Voltage Reading

The register VOUT stores the output voltage that sampling by internal ADC with 10mV/LSB

CS[5:4] and PHN[1:0]

The register CS stores the Current State as:

CS[5:4] = [00] => LS0

CS[5:4] = [01] => LS1

CS[5:4] = [10] => LS2

CS[5:4] = [11] => LS3

The register PHN stores the real time phase number as:

PHN[1:0] = [00] => Full Phase

PHN[1:0] = [01] => 1 Phase

PHN[1:0] = [10] => 2 Phase

PHN[1:0] = [11] => 3 Phase

OCP[5:2]: Over Current Protection Setting

The register OCP[5:4] used to adjust Total Current OCP Level as:

OCP[5:4]=[00]=>120%

OCP[5:4]=[01]=>133%

OCP[5:4]=[10]=>150%

OCP[5:4]=[11]=>171%

The register OCP[3:2] used to adjust Per Phase OCP Level as:

OCP[3:2]=[00]=>60uA

OCP[3:2]=[01]=>100uA

OCP[3:2]=[10]=>140uA

OCP[3:2]=[11]=>180uA

UV/OV[7:4]: VR UV/OV Protection Setting

The register OV/UV[7:6] used to adjust UVP Level as:

UV/OV[7:6]=[00]=>200mV

UV/OV[7:6]=[01]=>300mV

UV/OV[7:6]=[10]=>400mV

UV/OV[7:6]=[11]=>500mV

The register OV/UV[5:4] used to adjust OVP Level as:

UV/OV[5:4]=[00]=>200mV

UV/OV[5:4]=[01]=>300mV

UV/OV[5:4]=[10]=>400mV

UV/OV[5:4]=[11]=>500mV

GCOMP[3:0]

GCOMP is OTA Gain ,it can be programming by 0x14 Register as show in Table 8.

GCOMP[3]=[0]=>2020uA/V(default value)

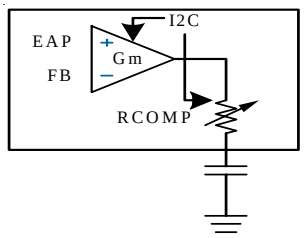


Table 8. GCOMP Setting Table

Bit[3]=1, Bit[2:0]	GCOMP(uA / V)
000	X1
001	X1.17
010	X1.31
011	X1.45
100	X1.69
101	X0.81
110	X0.6
111	X0.33

IICLL0~3

Load Line adjust of 4 load current state: IICLL0~3 define the DC Load Line slop in load current state LCS0~3 respectively as shown in TableXX.

Table 9. IICLL0~3

IICL0~3	Load Line
0000	0%
0001	12.5%
0010	25%
0011	37.5%
0100	50%
0101	62.5%
0110	75%
0111	87.5%
1000	100%
1001	112.5%
1010	125%
1011	137.5%
1100	150%
1101	162.5%
1110	175%
1111	187.5%

Table 10. SVID Data and Configuration Registers

Reg Addr	Register Name	Access	Default	Description
00h	Vender_ID	RO	26h	Vender ID
01h	Product_ID	RO	15h	Product ID
02h	Product_Revision	RO	01h	Product Revision
05h	Protocal_Version	RO	01h	SVID Protocal Version
06h	VR_Capability	RO	81h	Bit mapped register, identifies the SVID VR sapabilityes and which of the optional telemetry are supported.
10h	Status_1	R-M, W-PWM	00h	Data register containing the status of VR.
11h	Status_2	R-M, W-PWM	00h	Data register containing the status of transmission.
15h	Output_Current	R-M, W-PWM	--	Data register showing the output current that have been entered.
1Ch	Status_2_LastRead	R-M, W-PWM	00h	This register contains a copy of the Status_2.
21h	ICC_Max	RO Platform	--	Data register containing the maximum ICC the platform supports.
24h	SR_Fast	RO	0Ah	Data register containing the capability of fast slew rate the platform can sustain. Binary format i mV/ms, i.e. 0Ah = 10mV/us
25h	SR_Slow	RO	02h	Data register containing the capability of fast slew rate the platform can sustain. Binary format i mV/ms, i.e. 03h = 3mV/us
26h	VBOOT	RO Platform	--	Data register containing V_{BOOT} voltage in VID steps.
30h	VOUT_Max	RW Master	FBh	This register is programmed by maset and sets the maximum VID.
31h	VID_Setting	RW Master	00h	Data register containing currently programmed VID.
32h	Power_State	RW Master	00h	Register containing the programmed ower state.
33h	Offset	RW Master	00h	Set offset in VID steps.
34h	Multi_VR_Config	RW Master	00h	Bit mapped data register which configures multiple VRs behavior on the same bus.
35h	SetRegADR	RW Master	--	Scratch ad register for temporary storage of the SetRegADR pointer register.

Table 11. I2C Configuration Registers.

Reg Addr	Register Name	Access	Default	Description
0x01	VM0[7:0]	R/W	0x00h	Set IMON voltage level 0,VIMON > level 0 => LCS0 (highest current state)
0x02	VM1[7:0]	R/W	0x00h	Set IMON voltage level 1,VIMON > level 1 => LCS1
0x03	VM2[7:0]	R/W	0x00h	Set IMON voltage level 2,VIMON > level 2 => LCS2, VIMON < level 2 => LCS3 (lowest current state)
0x04	VM0_Hys[2:0] VM1_Hys[6:4]	R/W	0x00h	Bit[2:0] :Set VM0 Hysteresis 000:60mV ; 001=80mV ;010=100mV; 011=120mV ; 100=140mV;101=160mV;110=180 mV;111=200mV Bit[6:4] : Set VM1 Hysteresis 000:60mV ; 001=80mV ;010=100mV; 011=120mV ; 100=140mV;101=160mV;110=180 mV;111=200mV
0x05	VM2_Hys[2:0]	R/W	0x00h	Bit[2:0] :Set Vcore VM2 Hysteresis 000:60mV ; 001=80mV ;010=100mV; 011=120mV ; 100=140mV;101=160mV;110=180 mV;111=200mV
0x06	IICP3[7:6];IICP2[5:4] IICP1[3:2];IICP0[1:0]	R/W	0x00h	Operation Phase Number Setting Bit[7:6] : Phase Number of LCS3 Bit[5:4] : Phase Number of LCS2 Bit[3:2] : Phase Number of LCS1 Bit[1:0] : Phase Number of LCS0 00: 3 phase 01:3phase,10: 2phase 11:1phase
0x07	VOFS0[7:0]	R/W	0x00h	Voltage offset of LS0. 5mV/ step.
0x08	VOFS1[7:0]	R/W	0x00h	Voltage offset of LS1. 5mV/ step.
0x09	VOFS2[7:0]	R/W	0x00h	Voltage offset of LS2. 5mV/ step.
0x0A	VOFS3[7:0]	R/W	0x00h	Voltage offset of LS3. 5mV/ step.
0x0B	IICF0[6:4]; IICF1[2:0]	R/W	0x11h	IICF0[6:4]: freq of LCS0; IICF1[2:0]: freq of LCS1; 000: 150K; 001:200K ;010:250K;011:300K;100:350K;101:400K; 110:450K;111:500K
0x0C	IICF2[6:4]; IICF3[2:0]	R/W	0x11h	IICF2[6:4]: freq of LCS2; IICF3[2:0]: freq of LCS3 000: 150K; 001:200K ;010:250K;011:300K;100:350K;101:400K; 110:450K;111:500K
0x0D	IICLL0[7:4] IICLL1[3:0]	R/W	0x88h	I2CLL0[7:4] load line setting of LCS0 (default 100%, min 0%, max 187.5% ,12.5%/step) I2CLL1[3:0] load line setting of LCS1 (default 100%, min 0%, max 187.5% ,12.5%/step)
0x0E	IICLL2[7:4] IICLL3[3:0]	R/W	0x88h	I2CLL2[7:4] load line setting of LCS2 (default 100%, min 0%, max 187.5% ,12.5%/step) I2CLL3[3:0] load line setting of LCS3 (default 100%, min 0%, max 187.5% ,12.5%/step)

Table 11. I2C Configuration Registers(cont).

Reg Addr	Register Name	Access	Default	Description
0x0F	PH1_IGAIN[3:0] PH2_IGAIN[7:4]	R/W	0x00h	PHASE1 Current Balance Gain Adjust PH1_IGAIN[3]: 0:Disable 1:Enable Bit[2:0]: 000:50%; 001:62.5%; 010:75%; 011:87.5%; 100:100%; 101:112.5%; 110:125%; 111:137.5% PHASE2 Current Balance Gain Adjust PH2_IGAIN[7]: 0:Disable 1:Enable Bit[6:4]: 000:50%; 001:62.5%; 010:75%; 011:87.5%; 100:100%; 101:112.5%; 110:125%; 111:137.5%
0x10	PH3_IGAIN[3:0]	R/W	0x00h	PHASE3 Current Balance Gain Adjust PH3_IGAIN[3]: 0:Disable 1:Enable Bit[2:0]: 000:50%; 001:62.5%; 010:75%; 011:87.5%; 100:100%; 101:112.5%; 110:125%; 111:137.5%
0x11	PH1_IOS[7:4] PH2_IOS[3:0]	R/W	0x00h	PHASE1 Current Balance Offset Adjust Bit[7]: "1" => Offset enable, "0" => Offset disable Bit[6:4]: 000:0mV ; 001:3mV; 010:6mV; 011:9mV; 100:12mV; 101:15mV; 110:18mV; 111:21mV PHASE2 Current Balance Offset Adjust Bit[3]: "1" => Offset enable, "0" =>Offset disable Bit[2:0]: 000:0mV ; 001:3mV; 010:6mV; 011:9mV; 100:12mV; 101:15mV; 110:18mV; 111:21mV
0x12	PH3_IOS[7:4]	R/W	0x00h	PHASE3 Current Balance Offset Adjust Bit[7]: "1" => Offset enable, "0" => Offset disable Bit[6:4]: 000:0mV ; 001:3mV; 010:6mV; 011:9mV; 100:12mV; 101:15mV; 110:18mV; 111:21mV
0x13	RCOMP[3:0]	R/W	0x03h	RCOMP Resistor RCOMP=5K(1+[3:0])
0x14	GCOMP[3:0]	R/W	0x00h	OTA Gm Bit3:0 is default 2020 uA / V GCOMP[3:0]
0x15	LCHVID[7:0]	R/W	0x00h	Latch VID Register.
0x16	IOUT[7:0]	R	--	SVID 0X15 Reading.
0x17	VOUT[7:0]	R	--	VCORE Voltage Reading.
0x18	CS[5:4] PHN[1:0]	R	--	Current State Reading Bit[5:4] : 00:LS0 01:LS1 10:LS2 11: LS3 Phase Number Reading Bit[1:0]: "00": 3 phase "01": 1phase "10" : 2phase "11": 3phase

Table 11. I2C Configuration Registers(cont).

Reg Addr	Register Name	Access	Default	Description
0x19	OC[7:0]	R/W	0x00h	Bit[7]: "1" Enable "0"Disable Bit[6:0]: Mapping to SVID 0X15 Register.
0x25	OCP[5:0]	R/W	0x11h	Total Current OCP : Bit5~4: Vcore 00:120%, 01:133%, 10:150%, 11:171% Per Phase OCP: Bit3~2: Vcore Level 00:60uA, 01:100uA, 10:140uA, 11:180uA
0x26	UV/OV[7:0]	R/W	0x55h	UVP Setting: Bit [7:6] : 00:200mV 01:300mV 10:400mV 11:500mV OVP Setting: Bit [5:4] : 00:200mV 01:300mV 10:400mV 11:500mV
0x27	Misc1[6:0]	R/W	0x00h	Bit[5]: "0" SVID 0X31 VDAC follow SVID "1" SVID 0X31 VDAC ignore SVID Bit[4]: "0" SVID 0X32 PWR State follow SVID "1" SVID 0X32 PWR State ignore SVID Bit[3]: "0" SVID 0X33 Offset follow SVID. "1" SVID 0X33 Offset ignore SVID.
0x28	Misc2[7:0]	R/W	0x0Ch	Bit[7]: "0" Disable Auto Phase "1" Enable Auto Phase Bit[5]: "0" Disable PSM "1" Enable PSM Bit[3]: "0" Disable Load line "1" Enable Load line Bit[1]: "0" Disable Offset "1" Enable Offset
0x29	WD[7:4]	R/W	0x00h	Bit[7]: Watchdog timer "1" Enable "0" Disable Bit[6]:Timeout be issue(read clear) and clear all register to default Bit[5:4]: Timer 00:800mS 01:1600mS 10:3200mS 11:6400mS

Table 11. I2C Configuration Registers(cont).

Reg Addr	Register Name	Access	Default	Description
0x2D	TB[7:0]	R/W	0x00h	TB In PS0 Bit[7]: "0" Disable "1" Enable Bit[6:4]: 000:0mV 001:10mV 010:20mV 011:30mV 100:40mV 101:50mV 100:60mV 111:70mV TB In PS1 Bit[3]: "0" Disable "1" Enable Bit[2:0]: 000:0mV 001:10mV 010:20mV 011:30mV 100:40mV 101:50mV 100:60mV 111:70mV
0x2E	TRIG[7:0]	R/W	0x00h	TB Vtrig Limit in PS0 Bit[7]: "0" Disable "1" Enable Bit[6:4]: 000:1.25V 001:1.35V 010:1.45V 011:1.55V 100:1.65V 101:1.75V 110:1.85V 111:1.95V
0x2F	TON[5:0]	R/W	0x00h	TB ON Time Bit[5:3]: PS0 TB ON Time 000:200nS 001:300nS 010:400nS 011:500nS 100:600nS 101:700nS 110:800nS 111:900nS Bit[2:0]: PS1/2 TB ON Time 000:200nS 001:300nS 010:400nS 011:500nS 100:600nS 101:700nS 110:800nS 111:900nS
0x33	DVID_OFS[7:0]	R/W	0x68h	DVID Offset: 10mV x Bit[7:4]
0x48	Version ID	R	0x05h	
0xB2	CHIP ID	R	0x21h	

Table 12. Offset Voltage Table vs. VOFSn[7:0]

VOFSn[7:0]	Voffset (mV)	VOFSn[7:0]	Voffset (mV)	VOFSn[7:0]	Voffset (mV)	VOFSn[7:0]	Voffset (mV)
0x00	0	0x20	160	0x40	320	0x60	480
0x01	5	0x21	165	0x41	325	0x61	485
0x02	10	0x22	170	0x42	330	0x62	490
0x03	15	0x23	175	0x43	335	0x63	495
0x04	20	0x24	180	0x44	340	0x64	500
0x05	25	0x25	185	0x45	345	0x65	505
0x06	30	0x26	190	0x46	350	0x66	510
0x07	35	0x27	195	0x47	355	0x67	515
0x08	40	0x28	200	0x48	360	0x68	520
0x09	45	0x29	205	0x49	365	0x69	525
0x0A	50	0x2A	210	0x4A	370	0x6A	530
0x0B	55	0x2B	215	0x4B	375	0x6B	535
0x0C	60	0x2C	220	0x4C	380	0x6C	540
0x0D	65	0x2D	225	0x4D	385	0x6D	545
0x0E	70	0x2E	230	0x4E	390	0x6E	550
0x0F	75	0x2F	235	0x4F	395	0x6F	555
0x10	80	0x30	240	0x50	400	0x70	560
0x11	85	0x31	245	0x51	405	0x71	565
0x12	90	0x32	250	0x52	410	0x72	570
0x13	95	0x33	255	0x53	415	0x73	575
0x14	100	0x34	260	0x54	420	0x74	580
0x15	105	0x35	265	0x55	425	0x75	585
0x16	110	0x36	270	0x56	430	0x76	590
0x17	115	0x37	275	0x57	435	0x77	595
0x18	120	0x38	280	0x58	440	0x78	600
0x19	125	0x39	285	0x59	445	0x79	605
0x1A	130	0x3A	290	0x5A	450	0x7A	610
0x1B	135	0x3B	295	0x5B	455	0x7B	615
0x1C	140	0x3C	300	0x5C	460	0x7C	620
0x1D	145	0x3D	305	0x5D	465	0x7D	625
0x1E	150	0x3E	310	0x5E	470	0x7E	630
0x1F	155	0x3F	315	0x5F	475	0x7F	635

Table 12. Offset Voltage Table vs. VOFSn[7:0] (cont)

VOFSn[7:0]	Voffset (mV)	VOFSn[7:0]	Voffset (mV)	VOFSn[7:0]	Voffset (mV)	VOFSn[7:0]	Voffset (mV)
0x80	-640	0xA0	-480	0xC0	-320	0xE0	-160
0x81	-635	0xA1	-475	0xC1	-315	0xE1	-155
0x82	-630	0xA2	-470	0xC2	-310	0xE2	-150
0x83	-625	0xA3	-465	0xC3	-305	0xE3	-145
0x84	-620	0xA4	-460	0xC4	-300	0xE4	-140
0x85	-615	0xA5	-455	0xC5	-295	0xE5	-135
0x86	-610	0xA6	-450	0xC6	-290	0xE6	-130
0x87	-605	0xA7	-445	0xC7	-285	0xE7	-125
0x88	-600	0xA8	-440	0xC8	-280	0xE8	-120
0x89	-595	0xA9	-435	0xC9	-275	0xE9	-115
0x8A	-590	0xAA	-430	0xCA	-270	0xEA	-110
0x8B	-585	0xAB	-425	0xCB	-265	0xEB	-105
0x8C	-580	0xAC	-420	0xCC	-260	0xEC	-100
0x8D	-575	0xAD	-415	0xCD	-255	0xED	-95
0x8E	-570	0xAE	-410	0xCE	-250	0xEE	-90
0x8F	-565	0xAF	-405	0xCF	-245	0xEF	-85
0x90	-560	0xB0	-400	0xD0	-240	0xF0	-80
0x91	-555	0xB1	-395	0xD1	-235	0xF1	-75
0x92	-550	0xB2	-390	0xD2	-230	0xF2	-70
0x93	-545	0xB3	-385	0xD3	-225	0xF3	-65
0x94	-540	0xB4	-380	0xD4	-220	0xF4	-60
0x95	-535	0xB5	-375	0xD5	-215	0xF5	-55
0x96	-530	0xB6	-370	0xD6	-210	0xF6	-50
0x97	-525	0xB7	-365	0xD7	-205	0xF7	-45
0x98	-520	0xB8	-360	0xD8	-200	0xF8	-40
0x99	-515	0xB9	-355	0xD9	-195	0xF9	-35
0x9A	-510	0xBA	-350	0xDA	-190	0xFA	-30
0x9B	-505	0xBB	-345	0xDB	-185	0xFB	-25
0x9C	-500	0xBC	-340	0xDC	-180	0xFC	-20
0x9D	-495	0xBD	-335	0xDD	-175	0xFD	-15
0x9E	-490	0xBE	-330	0xDE	-170	0xFE	-10
0x9F	-485	0xBF	-325	0xDF	-165	0xFF	-5

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCC12 ---------- -0.3V to +15V

BOOTx to PHx ---------- -0.3V to +15V

PHx to GND

- DC ---------- -0.7V to 15V
- < 200ns ---------- -8V to 30V

BOOTx to GND

- DC ---------- -0.3V to VCC12 + 15V
- < 200ns ---------- -0.3V to 42V

UGx to PHx

- DC---------- -0.3V to (BOOTx - PHx +0.3V)
- <200ns ---------- -5V to (BOOTx - PHx + 0.3V)

LGx to GND

- DC ---------- -0.3V to + (VCC12 + 0.3V)
- <200ns ---------- -5V to VCC12 + 0.3V

Other Pins ---------- -0.3V to +6V

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- 150°C

Lead Temperature (Soldering, 10 sec) ---------- 260°C

ESD Rating (Note 2)

- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)

- VQFN5x5-32L θ_{JA} ---------- 36°C/W
- VQFN5x5-32L θ_{JC} ---------- 3°C/W

Power Dissipation, P_D @ TA = 25°C

- VQFN5x5-32L ---------- 2.78W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C

Operating Ambient Temperature Range ---------- -40°C to +85°C

Supply Input Voltage, V_{CC5} ---------- 4.5V to 5.5V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(5VCC = 5V, T_A = 25°C, unless otherwise specified)

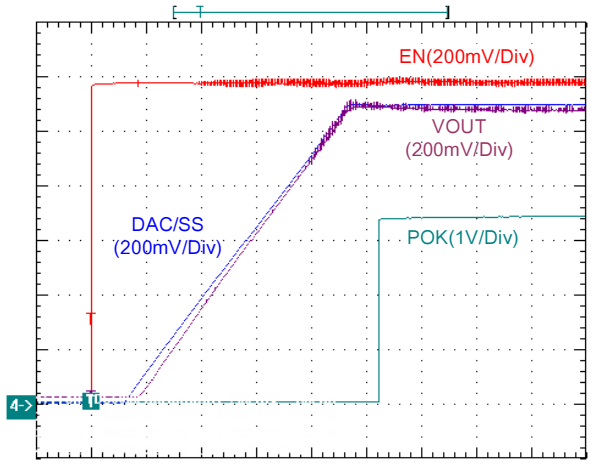
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Input Voltage	V_{CC5}		4.5	--	5.5	V
V_{CC5} POR Threshold			4	4.3	4.5	V
V_{CC5} POR Hysteresis		VCC5 Falling.	--	0.2	--	V
Supply Current	I_{VCC5}		--	9	--	mA
Supply Input Voltage	V_{CC12}		10.8	--	13.2	V
V_{CC12} POR Threshold			4	4.2	4.5	V
V_{CC12} POR Hysteresis		VCC12 Falling.	--	0.2	--	V
Supply Current	I_{VCC12}	No Switching	--	0.15	--	mA
Error Amplifier						
Offset Voltage	$V_{OS(EA)}$		-1	--	1	mV
Trans-Conductance	GM		--	2020	--	uA/V
Gain Bandwidth Product	GBW_{EA}	Guaranteed by Design.	--	10	--	MHz
DAC Voltage Accuracy						
DAC Output Accuracy	$V_{DAC/SS}$	1.0V to 1.52V	-0.5	--	0.5	%
		0.8V to 1.0V	-5	--	5	mV
		0.25V to 0.8V	-8	--	8	mV
Soft Start						
Soft Start Current	I_{SS}	SETVID_Fast	180	200	240	uA
		SETVID_Slow	45	50	58	uA
ENVCORE Input						
Input Low	V_{IL}		--	--	0.4	V
Input High	V_{IH}		0.8	--	--	V
Input Current			-1	--	1	uA
PWM On-Time Setting						
Frequency Range	f_{OSC}		150	--	500	kHz
On Time Accuracy			--	500	--	ns
Current Sense Amplifier						
Offset Voltage	$V_{OS(CSA)}$	No Load, Guaranteed by Design	-1	--	1	mV
Input Bias Current			-10	--	10	nA
Gain Bandwidth Product	$G_{BW(CSA)}$	Guaranteed by Design.	--	10	--	MHz

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWM Output						
Output Low Voltage	$V_{OL(PWM)}$	I_{SINK} = 4mA	--	--	0.2	V
Output High Voltage	$V_{OH(PWM)}$	I_{SOURCE} = 4mA	4.7	--	--	V
High Impedance State Leakage		V_{PWM} = 0V ~ 5V	-1	--	1	uA
VR Ready Output (VROK)						
Output Low Voltage	V_{OL}	I_{SINK} = 4mA	--	--	0.2	V
Output High Leakage		V_{VROK} = 5V	--	--	1	uA
Current Monitoring (IMON)						
IMON Currrent Mirror Accuracy		I_{MON} to I_{CSN} ratio	95	100	105	%
Droop						
Current Mirror Ratio for VCORE		I_{EAP} /I_{CSN}	95	100	105	%
Gate Drivers						
Upper Gate Source	R_{UG_SRC}	I_{UG} = -80mA	--	2	4	Ω
Upper Gate Sink	R_{UG_SNK}	I_{UG} = 80mA	--	1.5	3	Ω
Lower Gate Source	R_{LG_SRC}	I_{LG} = -80mA	--	2	4	Ω
Lower Gate Sink	R_{LG_SNK}	I_{LG} = 80mA	--	0.8	1.6	Ω
Dead Time	T_{DT}		--	30	--	ns
Protection						
OVP Threshold	V_{OVP}	V_{FB} - V_{EAP}	250	300	350	mV
OVP Dealy	T_{OVP}		--	20	--	us
UVP Threshold	V_{UVP}	V_{EAP} - V_{FB}	250	300	350	mV
UVP Dealy	T_{UVP}		--	5	--	us
Total Current OCP Threshold	V_{IMON}		3.35	3.4	3.45	V
2/3 Phase Total Current OCP Delay Time	T_{OCP1}		--	20	--	us
1 Phase Total Current OCP Delay Time	T_{OCP2}		--	6	--	us
Channel Current OCP Threshold	I_{SENX}		--	60	--	uA
Channel Current OCP Dealy Time	T_{OCP3}		--	20	--	us

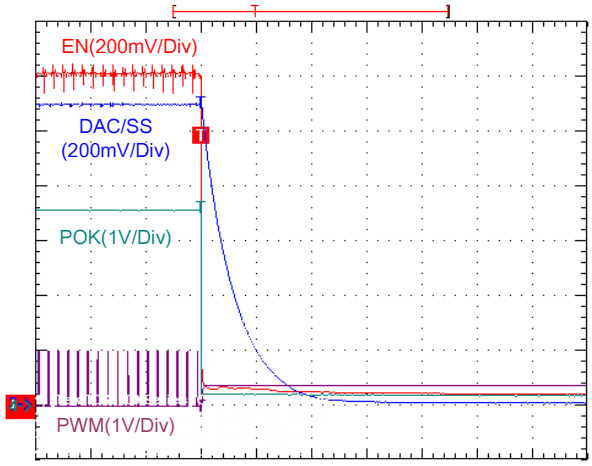
Typical Operation Characteristics

Turn On Waveforms



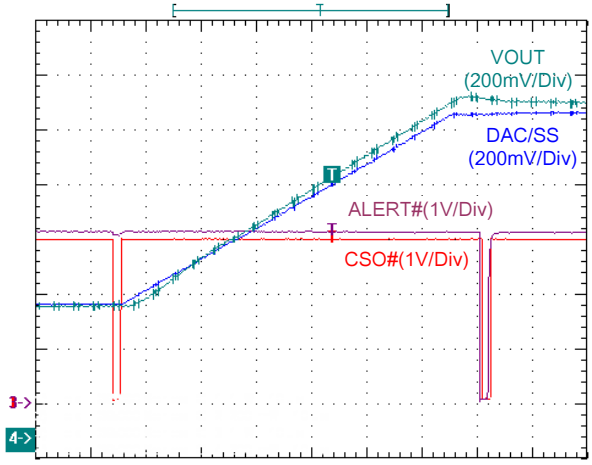
Time (100us/Div)

Turn Off Waveforms



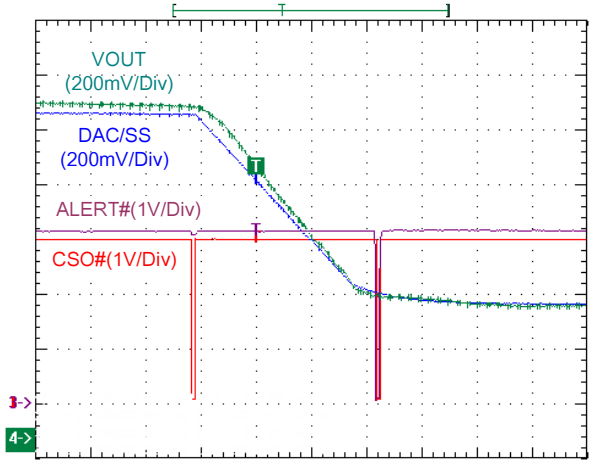
Time (20us/Div)

DVID Rising



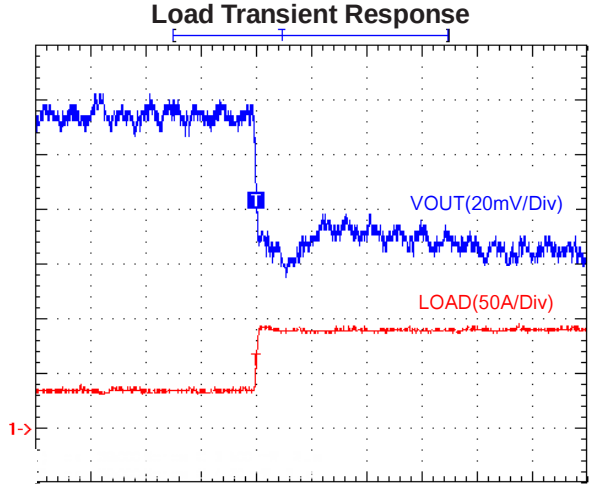
Time (10us/Div)

DVID Falling



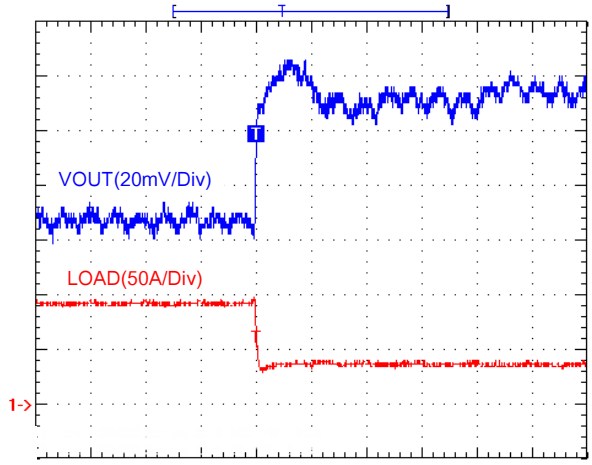
Time (20us/Div)

Load Transient Response



Time (2us/Div)

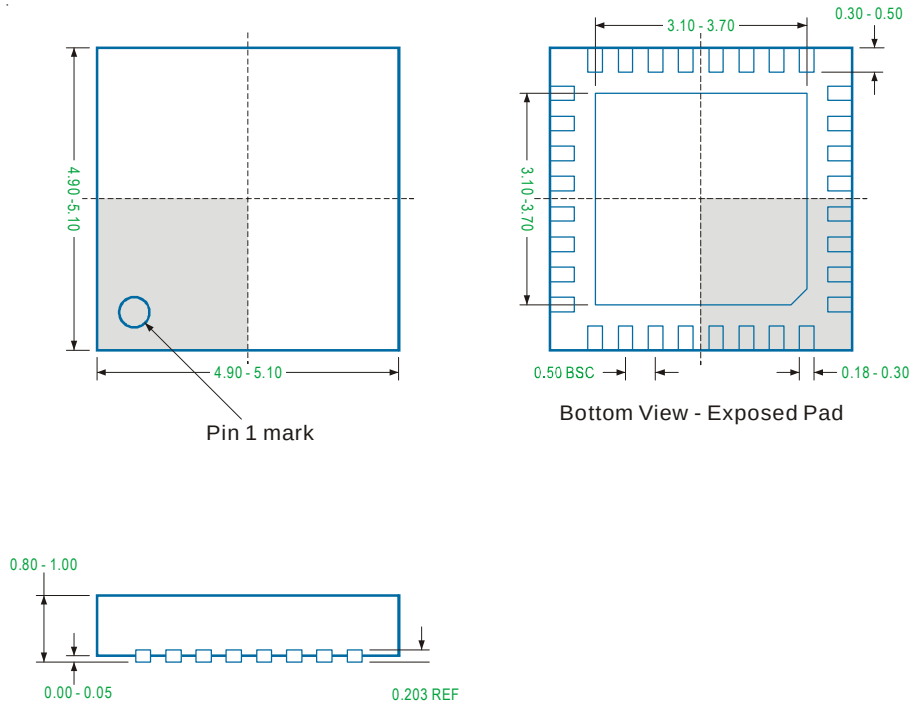
Load Transient Response



Time (2us/Div)

Package Information

VQFN5x5-32L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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