

. Features

## 1MHz, 3.0A, High-Efficiency Synchronous-Rectified Buck Converter

## General Description

The uP1712 is a high efficiency synchronous-rectified buck converter with internal power switches. Fixed 1MHz PWM operation allows possible smallest output ripple and external component size. With high conversion efficiency and small package, the uP1712 is ideally suitable for portable devices and USB/PCIE-based interface cards where PCB area is especially concerned.

With internal low  $R_{DS(ON)}$  switches, the uP1712 is capable of delivering 3.0A output current over a wide input voltage range from 2.6V to 5.5V. The output voltage is adjustable from 0.6V to  $V_{IN}$  by a voltage divider. Other features include internal soft-start, chip enable, over-voltage, undervoltage, over-temperature and over-current protections. The uP1712 is available in a space-saving WQFN3x3-16L or PSOP-8L packages.

#### Applications

- Battery-Powered Portable Devices
  - MP3 Players
  - Digital Still Cameras
  - Wireless and DSL Modems
  - Personal Information Appliances
- 802.11 WLAN Power Supplies
- FPGA/ASIC Power Supplies
- Dynamically Adjustable Power Supply for CDMA/WCSMA Power Amplifiers
- USB-Based xDSL Modems and Other Network Interface Cards
- Point-of-Load Regulation

# PGND 1 PGND 1 PGND 1 PGND 1 PGND 1 PGND 11 VIN PGND 10 VIN FB 9 VCC VIN VIN

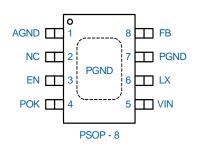
- 2.6V to 5.5V Input Voltage Range
- □ Adjustable Output from 0.6V to V<sub>IN</sub>
- Guaranteed 3.0A Output Current
- Accurate Reference: 0.6V (± 1.5%)
- Up to 95% Conversion Efficiency
- Low Quiescent Current
- Integrated Low R<sub>DS(ON)</sub> Upper and Lower MOSFET Switches: 85mΩ and 75mΩ
- Current Mode PWM Operation
- Fixed Frequency: 1MHz
- **100% Maximum Duty Cycle for Lowest Dropout**
- Internal Soft-Start
- No Schottky Diode Required
- Over-Voltage Protection
- Under-Voltage Protection for uP1712PQDD and uP1712PSU8 only
- Over-Temperature and Over-Current Protection
- WQFN3x3-16L or PSOP-8L Packages
- RoHS Compliant and Halogen Free

### Ordering Information

Order Number	Package Type	Top Marking
uP1712PQDD	WQFN3x3-16L	uP1712P
uP1712PSU8	PSOP-8L	uP1712P
uP1712QSU8		uP1712Q

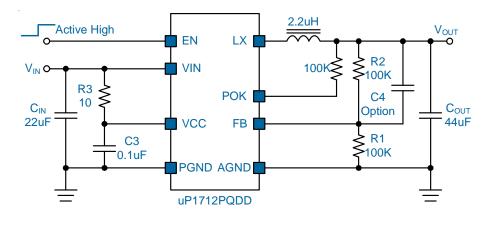
Note: uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

## Pin Configuration





## **Typical Application Circuit**



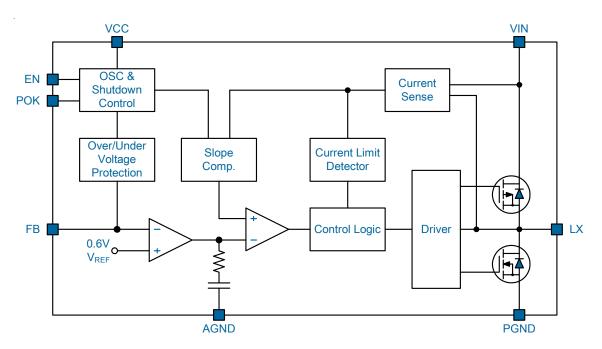
## Functional Pin Description

Pin No.					
uP1712PQDD	uP1712PSU8/ uP1712QSU8	Pin Name	Pin Function		
1,2,3	7	PGND	Power Ground. Connect to the output and input capacitors return.		
4	8	FB	<b>Feedback Input.</b> This pin is the inverting input of the error amplifier. FB senses the switcher output through an external resistor divider network.		
5	1	AGND	<b>Signal Ground.</b> Connect the return of all small signal componenets this pin.		
6,16	2	NC	Not Internally Connected.		
7	3	EN	Chip Enable (Active High). Logic low shuts down the converter.		
9		VCC	<b>Bias Supply.</b> Supplies power for the internal circuitry. Connect to input power via low pass filter with decoupling to AGND.		
10,11,12	5	VIN	<b>Power Supply Input.</b> Input voltage that supplies current to the output voltage and powers the internal control circuit. Bypass the input voltage with a minimum 10uF X5R or X7R ceramic capacitor.		
13,14,15	6	LX	Internal Switches Output. Connect these pins to the output inductor.		
8	4	POK	<b>Power OK Indication (for uP1712PQDD and uP1712PSU8 Only)</b> . This pin is set high impedance after soft start end and no fault occurs.		
Exposed Pad			<b>Power Ground.</b> The exposed pad should be well soldered to PCB with multiple vias to ground plane for optimal thermal performance.		



# uP1712

## Functional Block Diagram





## Functional Description

The uP1712 is a high efficiency synchronous-rectified buck converter with internal power switches. Fixed 1.0MHz PWM operation allows possible smallest output ripple and external component size. With high conversion efficiency and small package, the uP1712 is ideally suitable for portable devices and USB/PCIE-based interface cards where PCB area is especially concerned.

With internal low R<sub>DS(ON)</sub> switches, the uP1712 is capable of delivering 3.0A output current over a wide input voltage range from 2.6V to 5.5V. The output voltage is adjustable from 0.6V to V<sub>IN</sub> by a voltage divider. Other features include internal soft-start, chip enable, over voltage, under-voltage, over-temperature and over-current protections. The uP1712 is available in a space-saving WQFN3x3-16L or PSOP-8L packages.

### Input Supply Voltages, $\rm V_{\rm \scriptscriptstyle IN}$ & $\rm V_{\rm _{\rm CC}}$

The uP1712 features seperate power supply and ground pins for power stages and control circuit, isolating the control circuit from noise associated with the power MOSFET switching.

The VIN pins provide current to the power stage. The supply voltage range is from 2.6V to 5.5V. The uP1712 draws pulsed current with sharp edges from  $V_{\rm IN}$  each time the upper switch turns on, resulting in voltage ripples and spikes at supply input. A minimum 10uF ceramic capacitor with shortest PCB trace is highly recommended for bypassing the supply input.

The VCC pin provides currents for the internal control circuit. A power on reset (POR) continuously monitors the input supply voltage. The POR level is typically 2.3V at  $V_{cc}$  rising. Use low pass filter R3 and C3 as shown in the Typical Application Circuit to filter the input noise associated with the power switching.

#### Chip Enable/Disable and Soft Start

The uP1712 features an EN pin for enable/disable control of the output voltage. Pulling the EN pin lower than 0.4V shuts down the uP1712 and reduces its quiescent current lower than 1uA. In the shutdown mode, both upper and lower switches are turned off.

Pulling EN pin higher than 1.5V enables the uP1712 and initiates the softstart cycle once the  $V_{cc}$  POR is granted. The inductor current is limited to fractions of its rated value during the softstart cycle. Figure 1 illustrates the softstart behavior of the uP1712. The inductor current ramps up stairwisely with 250mA increments and 60us duration each step. Note that the output capacitor is large to illustrate the whole softstart behavior. The output voltage may ramp up to its target level in 2 or 3 steps in real applications

where output capacitor is about 22uF.

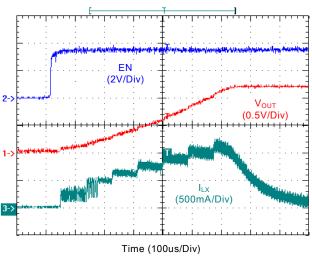


Figure 1. Softstart of uP1712.

The uP1712 asserts end of soft start and set the current limit to its normal level when the soft start duration expires. After soft start end, the POK pin is set high impedance if no fault occurs.

#### **PWM Operation**

The uP1712 adopts slope-compensated, current mode PWM control capable of achieving 100% duty cycle. During normal operation, the uP1712 operates at PWM mode to regulate output voltage by transferring the power to the output voltage cycle by cycle at a constant 1.0MHz frequency. The uP1712 turns on the upper switch at each rising edge of the internal oscillator allowing the inductor current to ramp up linearly. The switch remains on until either the current-limit is tripped or the PWM comparator turns off the switch for regulating output voltage. The upper switch current is sensed, slope compensated and compared with the error amplifier output COMP to determine the adequate duty cycle. The VOUT pin senses output feedback voltage from an external resistive divider.

When the load current increases, it causes a slight decrease in the feedback voltage relative to the 0.6V reference, which in turn, causes the error amplifier output voltage to increase until the average inductor current matches the new load current.

#### Low Dropout Mode

The uP1712 increases duty cycle to maintain output voltage within its regulation as the supply input drops gradually in the battery-powered applications. The uP1712 operates with 100% duty cycle and enters low dropout mode as the supply input approaches the output voltage. This maximizes the battery life.



## **Functional Description**

#### **Output Voltage Setting and Feedback Network**

The output voltage can be set from  $V_{\rm REF}$  to  $V_{\rm IN}$  by a voltage divider as:

$$V_{OUT} = \frac{R1 + R2}{R1} \times V_{REF}$$

The internal V<sub>REF</sub> is 0.6V with 1.5% accuracy. In real applications, a 22pF feedforward ceramic capacitor is recommended in parallel with R2 for better transient response.

#### **Current Limit Function**

The uP1712 continuously monitors the inductor current for current limit by sensing the voltage drop across the upper switch when it turns on. When the inductor current is higher than current limit threshold (5.5A typical), the current limit function activates and forces the upper switch turning off to limit inductor current cycle by cycle. If the load continuously demands more current than what uP1712 could provide, uP1712 can not regulate the output voltage. Eventually under voltage protection will be triggered and shuts down the uP1712 if V<sub>OUT</sub> is too low.

#### **Under Voltage Protection**

Under voltage Protection is triggered if the FB voltage is lower than 0.3V and shuts down uP1712. The under voltage protection is latch-off type and can only be reset by POR of  $V_{cc}$  or toggling the EN pin.

#### **Over Voltage Protection**

Over voltage protection (OVP) is triggered if the FB voltage is higher than 0.8V and forces the uP1712 to continuous PWM mode that allows the inductor current to be negative. The voltage control loop will continuously turn on the lower switch to sink charges from the output capacitor to lower the output voltage. The lower switch turns off only the sinking current is higher than it current limit level, typical 2.0A. The uP1712 resumes normal operation if the OVP is removed.

#### **Over Temperature Protection (OTP)**

The OTP is triggered and shuts down the uP1712 if the junction temperature is higher than  $150^{\circ}$ C. The OTP is a non-latch type protection. The uP1712 automatically initiates another soft start cycle if the junction temperature drops below  $130^{\circ}$ C.



# uP1712

## Absolute Maximum Rating

Supply Input Voltage, V <sub>IN</sub> , V <sub>CC</sub> (Note 1)	0.3V to +6.5V
LX Pin Voltage	
DC	0.3V to +(V <sub>IN</sub> +0.3V)
<50ns	5V to +( $V_{IN}$ +5V)
Other Pins	0.3V to (V <sub>cc</sub> + 0.3V
Storage Temperature Range	
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C
ESD Rating (Note 2)	
HBM (Human Body Mode)	2kV
MM (Machine Mode)	200V

## Thermal Information

Package Thermal Resistance (Note 3)	
WQFN3x3-16L θ <sub>.ι</sub>	68°C/W
WQFN3x3-16L $\theta_{10}^{2}$	6°C/W
PSOP-8L θ <sub>μ</sub>	50°C/W
PSOP-8L $\tilde{\theta_{ic}}$	
Power Dissipation, $P_{D} @ T_{A} = 25^{\circ}C$	
DFN3x3-16L	1.47W
PSOP-8L	2.0W

## \_\_\_\_\_ Recommended Operation Conditions

Operating Junction Temperature Range (Note 4)	40°C to +125°C
Operating Ambient Temperature Range	40°C to +85°C
Supply Input Voltage, V <sub>IN</sub>	+2.6V to +5.5V

## \_\_\_\_\_ Electrical Characteristics

( $V_{cc} = V_{IN} = 5V$ ,  $T_A = 25^{\circ}C$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Тур	Мах	Units	
Supply Current							
Supply Voltage Range	V <sub>IN</sub>	$V_{IN} = V_{CC}$	2.6		5.5	V	
Under Voltage Lockout	V <sub>UVLO</sub>	$V_{cc}$ Rising, $V_{EN} = V_{cc}$			2.5	V	
		$V_{cc}$ Falling, $V_{EN} = V_{cc}$	2.2				
Quiescent Current	ا <sub>م</sub>	$V_{FB} = 0.8V, I_{OUT} = 0mA$		3.4		mA	
Shutdown Current		$V_{EN} = 0V$		0.01	1	uA	
Reference							
Reference Voltage	V <sub>FB</sub>	I <sub>out</sub> = 0mA	0.59	0.60	0.61	V	
Output Voltage Accuracy	$\Delta V_{OUT}$	I <sub>out</sub> = 0mA	-1.5		+1.5	%	
Output Voltage Line Regulation	$\Delta V_{OUT}$	$V_{IN} = 2.6V$ to 5.5V, $I_{OUT} = 0$ mA		0.04	0.4	%/V	
Output Voltage Load Regulation	$\Delta V_{OUT}$	I <sub>out</sub> = 0A ~ 3A		0.5		%/A	



## Electrical Characteristics

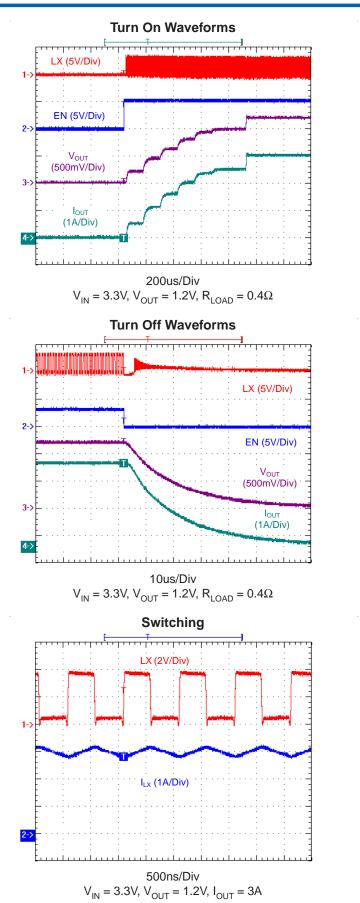
Parameter	Symbol	Test Conditions	Min	Тур	Max	Units
Oscillator	4	L	1	Į	ļ	4
Switching Frequency Range	f <sub>osc</sub>		0.8	1.0	1.2	MHz
Maximum Duty Cycle	DC	V <sub>IN</sub> = V <sub>OUT</sub> ; V <sub>FB</sub> = 0.55V	100			%
Power Switches						
R <sub>DS(ON)</sub> of Upper Switch	R <sub>P_FET</sub>	V <sub>IN</sub> = 3.6V, I <sub>LX</sub> = 100mA		85		mΩ
R <sub>DS(ON)</sub> of Lower Switch	R <sub>N_FET</sub>	V <sub>IN</sub> = 3.6V, I <sub>LX</sub> = -100mA		75		mΩ
Logic Input			•			
EN Logic Low Threshold	VL	V <sub>IN</sub> = 2.6V to 5.5V, Shutdown			0.4	V
EN Logic High Threshold	V <sub>H</sub>	$V_{IN} = 2.6V$ to 5.5V, Enable	1.5			V
Power OK Output						
Logic High Leakage Current	I <sub>POK</sub>	$V_{POK} = V_{CC} = 5V$			1	uA
Logic Low Voltage	V <sub>POK</sub>	I <sub>POK</sub> = 1mA			0.2	V
Protection						
FB Under Voltage Protection		FB Falling, for uP1712PSU8		50		0/1/
	$\Delta_{FB\_UVP}$	FB Falling, for uP1712QSU8		0		%V <sub>REF</sub>
Current Limit Protection	I <sub>OUT_OCP</sub>			5.5		A
Thermal Shutdwon Temperature	T <sub>SHDN</sub>	by design		150		°C
Thermal Shutdown Hysteresis	$\Delta T_{SHDN}$	by design		20		°C

**Note 1.** Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

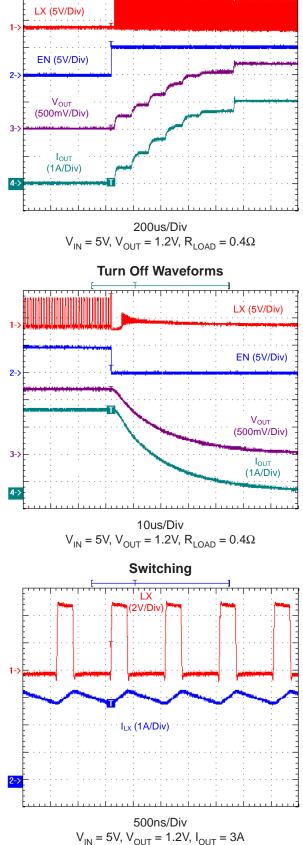
- **Note 3.**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^{\circ}C$  on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.
- Note 4. The device is not guaranteed to function outside its operating conditions.



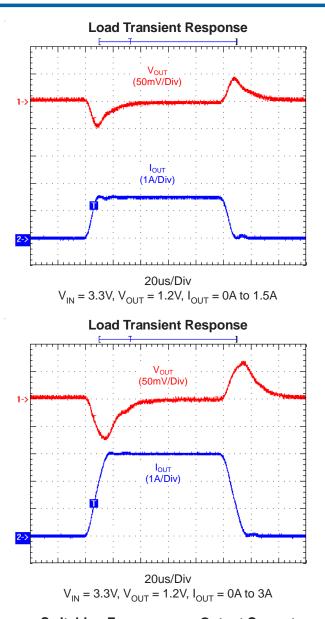


## **Typical Operation Characteristics**

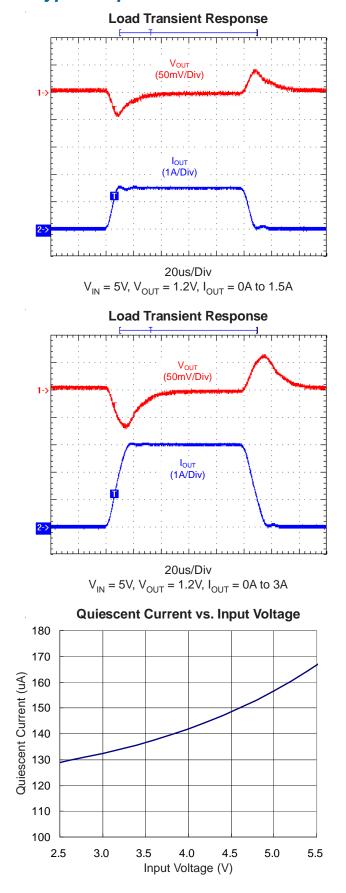
**Turn On Waveforms** 

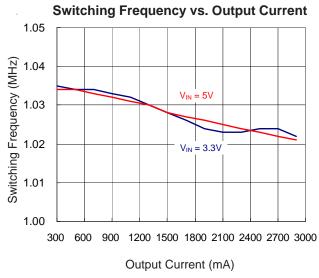






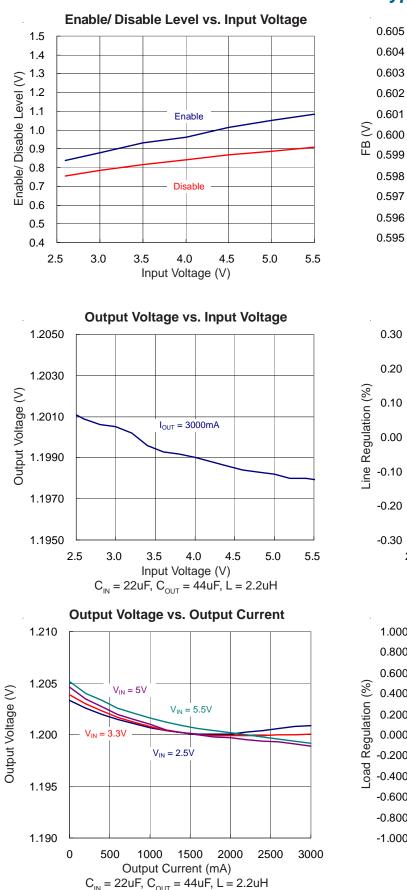
## **Typical Operation Characteristics**





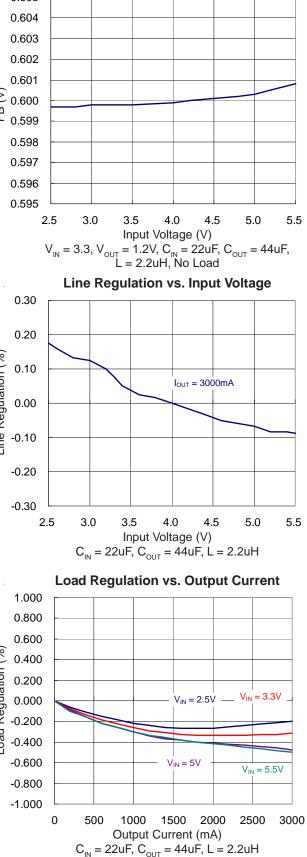
uPI Semiconductor Corp., http://www.upi-semi.com Rev. P01, File Name: uP1712-DS-P0100





## **Typical Operation Characteristics**

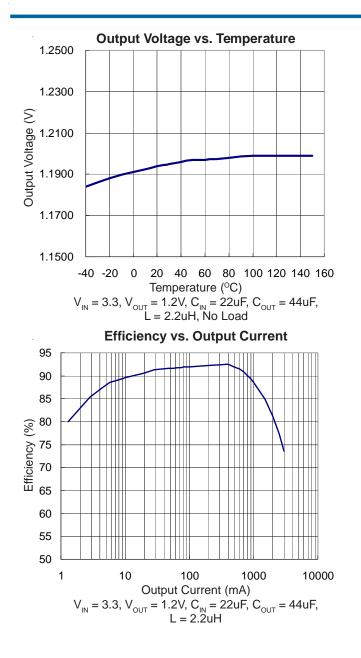
FB vs. Input Voltage



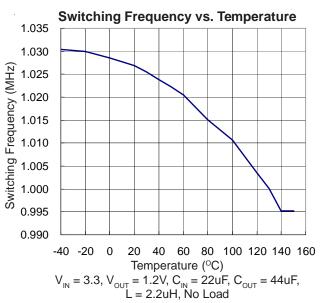
uPI Semiconductor Corp., http://www.upi-semi.com Rev. P01, File Name: uP1712-DS-P0100



# uP1712



## **Typical Operation Characteristics**





#### **Output Inductor Selection**

Output inductor selection is usually based the considerations of inductance, rated current value, size requirements and DC resistance (DCR).

The inductance is chosen based on the desired ripple current. Large value inductors result in lower ripple currents and small value inductors result in higher ripple currents. Higher  $V_{IN}$  or  $V_{OUT}$  also increases the ripple current as shown in the equation below. A reasonable starting point for setting ripple current is  $\Delta I_L = 600$ mA (30% of 2A).

$$\Delta I_{L} = \frac{1}{f_{OSC} \times L_{OUT}} \times V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

For most applications, the value of the inductor will fall in the range of 1uH to 10uH.

Maximum current ratings of the inductor are generally specified in two methods: permissible DC current and saturation current. Permissible DC current is the allowable DC current that causes 40°C temperature raise. The saturation current is the allowable current that causes 10% inductance loss. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current. If possible, choose an inductor with rated current higher than 5.5A so that it will not saturate even under current limit condition.

The size requirements refer to the area and height requirement for a particular design. For better efficiency, choose a low DC resistance inductor. DCR is usually inversely proportional to size.

Different core materials and shapes will change the size/ current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends on the price vs. size requirements and any radiated field/EMI requirements.

#### **Input Capacitor Selection**

The uP1712 draws pulsed current with sharp edges from the input capacitor resulting in ripple and noise at the input supply voltage. A minimum 10uF X5R or X7R ceramic capacitor is highly recommended to filter the pulsed current. The input capacitor should be placed as near the device as possible to avoid the stray inductance along the connection trace. Y5V dielectrics, aside from losing

## Application Information

most of their capacitance over temperature, they also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

The capacitor with low ESR (equivalent series resistance) provides the small drop voltage to stabilize the input voltage during the transient loading. For input capacitor selection, the ceramic capacitors larger than 1uF is recommend. The capacitor must conform to the RMS current requirement. The maximum RMS ripple current is calculated as:

$$I_{IN(RMS)} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at  $V_{IN} = 2xV_{OUT}$ , where  $I_{IN(RMS)} = I_{OUT(MAX)}/2$ . This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

#### **Output Capacitor Selection**

The uP1712 is specifically design to operate with minimum 10uF X5R or X7R ceramic capacitor. The value can be increased to improve load/line transient performance. Y5V dielectrics, aside from losing most of their capacitance over temperature, they also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

The ESR of the output capacitor determines the output ripple voltage and the initial voltage drop following a high slew rate load transient edge. The output ripple voltage can be calculated as:

$$\Delta V_{OUT} = \Delta I_{C} \times (ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}})$$

where  $f_{OSC}$  = operating frequency,  $C_{OUT}$  = output capacitance and  $\Delta I_{C} = \Delta I_{L}$  = ripple current in the inductor. The ceramic capacitor with low ESR value provides the low output ripple and low size profile. Connect a 22uF ceramic capacitor at output terminal for good performance and place the input and output capacitors as close as possible to the device.

#### **Using Ceramic Capacitors**

Higher value, lower cost ceramic capacitors are now available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the uP1712



control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used to achieve very low output ripple and small circuit size.

However, care must be taken when these capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input,  $V_{IN}$ . At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at  $V_{IN}$ , large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

#### **Thermal Considerations**

In most applications the uP1712 does not dissipate much heat due to its high efficiency. However, overtemperature protection is implemented in case of applications where the uP1712 is operating at high ambient temperature. If the junction temperature reaches approximately 150°C, the OTP turns both power switches and let the LX node become high impedance. The uP1712 restores to normal operation if the junction temperature drops to 130°C.

It is helpful to analysis the power dissipation of uP1712 for avoding the uP1712 from exceeding the maximum junction temperature. In typical applications, the conduction loss dominates the total power loss in uP1712. The conduction loss has its maximum at high duty-ratio, low input voltage, and high ambient temperatures.

Consider the uP1712 in dropout mode operation at an input voltage of 2.5V, a load current of 1.5A and an ambient temperature of 75°C. The on-resistance of the upper swith is about 100m $\Omega$  at this condition. Therefore the power dissipation P<sub>p</sub> is:

## $P_D = I_{OUT}^2 \times R_{DS(ON)} = 225 mW$

This results in 50 x 0.225 =  $12^{\circ}$ C temperature raise at junction. The juction temperature is  $87^{\circ}$ C and is lower than it maximum rating  $125^{\circ}$ C.

#### Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs,  $V_{OUT}$  immediately shifts by an amount equal to ( $\Delta I_{OUT} \times ESR$ ), where ESR is the effective series resistance of  $C_{OUT}$ .  $\Delta I_{OUT}$  also begins to discharge or charge

## Application Information

 $C_{OUT}$ , which generates a feedback error signal. The regulator loop then acts to return  $V_{OUT}$  to its steady state value. During this recovery time  $V_{OUT}$  can be monitored for overshoot or ringing that would indicate a stability problem.

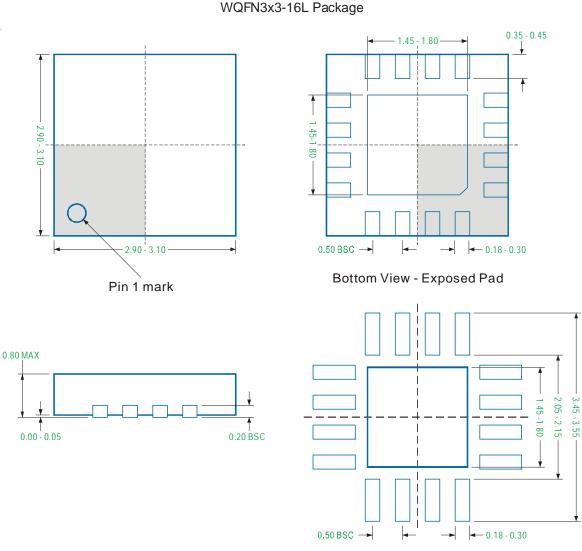
#### **PCB Layout Considerations**

High switching frequencies and relatively large peak currents make the PCB layout a very important part of switching mode power supply design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Follow the PCB layout guidelines for optimal performance of uP1712.

- 1. For the main current paths, keep their traces short, direct and wide.
- 2. Put the input/output capacitors as close as possible to the device pins.
- 3. LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
- 4. Connect feedback network behind the output capacitors. Place the feedback components near the uP1712 and keep the loop area small.
- A ground plane is preferred, but if not available, keep the signal and power grounds sepregated with small signal components returning to the GND pin at one point. They should not share the high current path of C<sub>IN</sub> or C<sub>OUT</sub>.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to V<sub>IN</sub> or GND.



## . Package Information



Recommended Solder Pad Pitch and Dimensions

#### Note

1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

TYP. Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

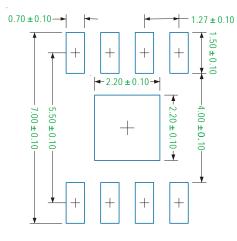
3. Drawing not to scale.

4. These dimensions no not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.



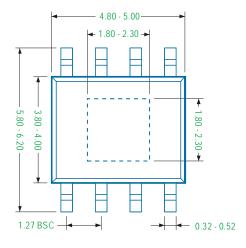
## . Package Information

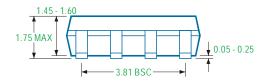
PSOP-8L Package



Recommended Solder Pad Layout







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