1.0MHz, 3.0A, High-Efficiency Synchronous-Rectified Buck Converter

General Description

The uP1727Q is a high efficiency synchronous-rectified buck converter with internal power switches. Fixed 1.0MHz PWM operation allows possible smallest output ripple and external component size. With high conversion efficiency and small package, the uP1727Q is ideally suitable for portable devices and USB/PCIE-based interface cards, where PCB area is especially concerned.

With internal low $R_{DS(ON)}$ switches, the uP1727Q is capable of delivering 3.0A output current over a wide input voltage range from 2.6V to 5.5V. The output voltage is adjustable from 0.6V to V_{IN} by a voltage divider.

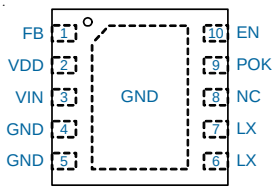
Other features include internal soft-start, chip enable, over-voltage, under-voltage, over-temperature and over-current protections. The uP1727Q is available in a space-saving WDFN3x3-10L package.

Ordering Information

Order Number	Package Type	Top Marking
uP1727QDDA	WDFN3x3-10L	uP1727Q

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



WDFN3x3-10L

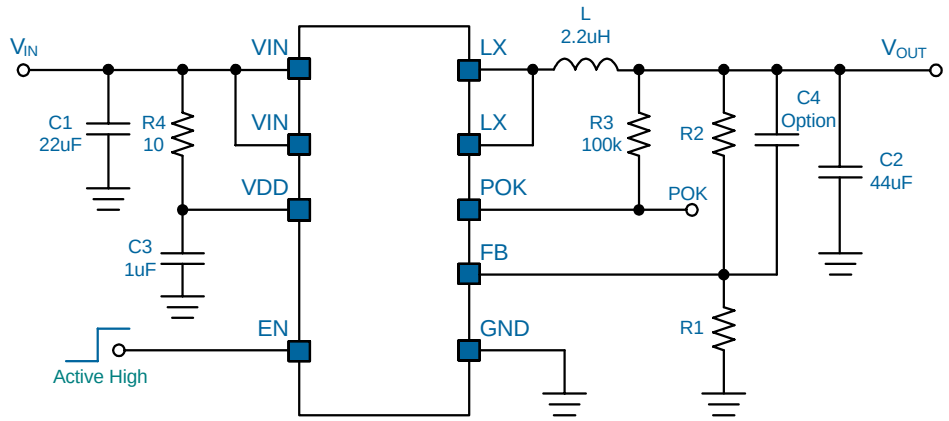
Features

- 2.6V to 5.5V Input Voltage Range
- Adjustable Output from 0.6V to V_{IN}
- Guaranteed 3.0A Output Current
- Accurate Reference: 0.6V (±1%)
- Up to 95% Conversion Efficiency
- Low Quiescent Current
- Integrated Low $R_{DS(ON)}$ Upper and Lower MOSFET Switches: 70mΩ and 50mΩ
- Current Mode PWM Operation
- Fixed Frequency : 1.0MHz
- 100% Maximum Duty Cycle for Lowest Dropout
- Internal Soft-Start
- Over Voltage and Under Voltage Protection
- Over Temperature and Over Current Protection
- WDFN3x3-10L Package
- RoHS Compliant and Halogen Free

Applications

- Battery-Powered Portable Devices
  - MP3 Players
  - Notebook Computers
  - Wireless and DSL Modems
  - Personal Information Appliances
  - IP Phones
  - Digital Cameras
- 802.11 WLAN Power Supplies
- FPGA/ASIC Power Supplies
- Dynamically Adjustable Power Supply for CDMA/WCDMA Power Amplifiers
- USB-Based xDSL Modems and Other Network Interface Cards
- Point-of-Load Regulation

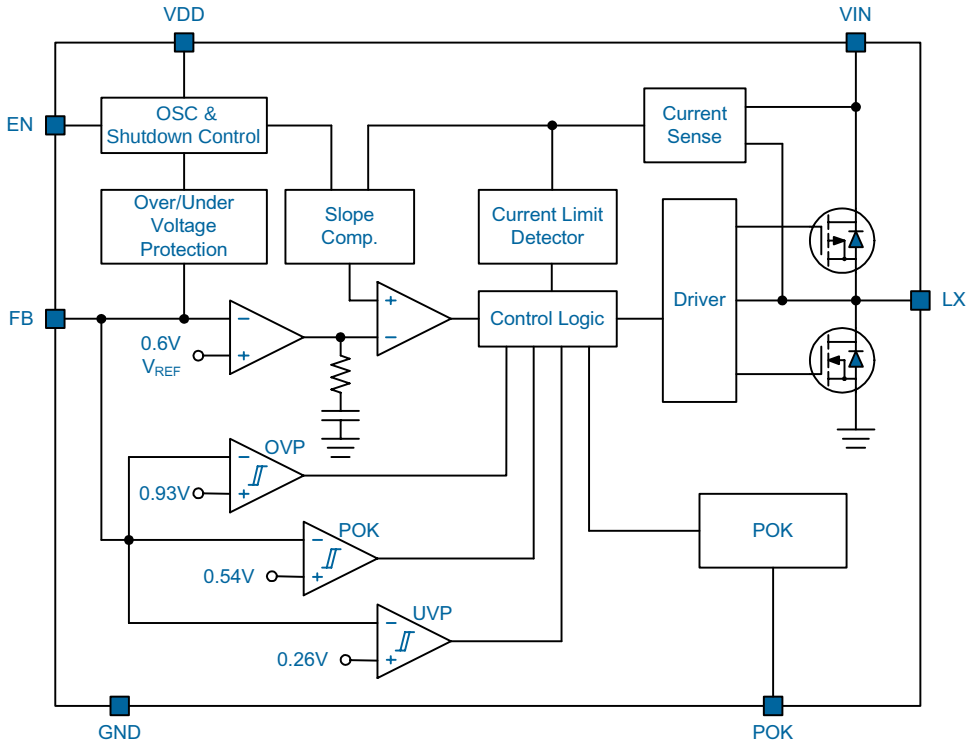
Typical Application Circuit



Functional Pin Description

Pin Name	Pin Function
LX	**Internal Switches Output.** Connect these pins to the output inductor.
POK	**Power OK Indication.** This pin is set high impedance after soft start end and no fault occurs.
EN	**Chip Enable (Active High).** Logic low shuts down the converter. No floating.
FB	**Feedback Input.** This pin is the inverting input of the error amplifier. FB senses the switcher output through an external resistor divider network.
NC	**Not Internally Connected.**
VDD	**Bias Supply.** Supplies power for the internal circuitry. Connect to input power via low pass filter with decoupling to GND.
VIN	**Power Supply Input.** Input voltage that supplies current to the output voltage. Decouple this pin to GND with at least 10uF X5R or X7R ceramic capacitor.
Exposed Pad	**Ground.** The exposed pad GND must be soldered to PCB and connected to ground plane for optimal performance.

Functional Block Diagram



Functional Description

The uP1727Q is a high efficiency synchronous-rectified buck converter with internal power switches. Fixed 1.0MHz PWM operation allows possible smallest output ripple and external component size. With high conversion efficiency and small package, the uP1727Q is ideally suitable for portable devices and USB/PCIE-based interface cards where PCB area is especially concerned. With internal low $R_{DS(ON)}$ switches, the uP1727Q is capable of delivering 3A output current over a wide input voltage range from 2.6V to 5.5V. The output voltage is adjustable from 0.6V to V_{IN} by a voltage divider. Other features include internal soft-start, chip enable, over-voltage, under-voltage, over-temperature and over-current protections. The uP1727Q is available in a space-saving WDFN3x3-10L package.

Input Supply Voltages, V_{IN} & V_{DD}

The uP1727Q features separate power supply and ground pins for power stages and control circuit, isolating the control circuit from noise associated with the power MOSFET switching. The VIN pins provide current to the power stage. The supply voltage range is from 2.6V to 5.5V. The uP1727Q draws pulsed current with sharp edges from V_{IN} each time the upper switch turns on, resulting in voltage ripples and spikes at supply input. A minimum 10uF ceramic capacitor with shortest PCB trace is highly recommended for bypassing the supply input. The VDD pin provides currents for the internal control circuit. A power on reset (POR) continuously monitors the input supply voltage. The POR level is typically 2.4V at VDD rising. Use low pass filter R4 and C3 as shown in the Typical Application Circuit to filter the input noise associated with the power switching.

Chip Enable/Disable and Soft-Start

The uP1727Q features an EN pin for enable/disable control of the output voltage. Pulling the EN pin lower than 0.4V shuts down the uP1727Q and reduces its quiescent current lower than 1uA. In the shutdown mode, both upper and lower switches are turned off. Pulling EN pin higher than 1.5V enables the uP1727Q. Once the chip is enabled, the V_{DD} POR is granted. The internal soft-start capacitor becomes charged and generates a linear ramping up voltage across the capacitor. This voltage clamps the voltage at the FB pin causing PWM pulse width to increase slowly and in turn reduce the output surge current. The internal 0.6V reference takes over the loop control once the internal ramping-up voltage becomes higher than 0.6V.

PWM Operation

The uP1727Q adopts slope-compensated, current mode PWM control capable of achieving 100% duty cycle. During normal operation, the uP1727Q operates at PWM mode to regulate output voltage by transferring the power to the output voltage cycle by cycle at a constant 1.0MHz frequency. The uP1727Q turns on the upper switch at each rising edge of the internal oscillator allowing the inductor current to ramp up linearly. The switch remains on until either the current-limit is tripped or the PWM comparator turns off the switch for regulating output voltage. The upper switch current is sensed, slope compensated and compared with the error amplifier output COMP to determine the adequate duty cycle. The VOUT pin senses output feedback voltage from an external resistive divider. When the load current increases, it causes a slight decrease in the feedback voltage relative to the 0.6V reference, which in turn, causes the error amplifier output voltage to increase until the average inductor current matches the new load current.

Low Dropout Mode

The uP1727Q increases duty cycle to maintain output voltage within its regulation as the supply input drops gradually in the battery-powered applications. The uP1727Q operates with 100% duty cycle and enters low dropout mode as the supply input approaches the output voltage. This maximizes the battery life.

Output Voltage Setting and Feedback Network

The output voltage can be set from V_{REF} to V_{IN} by a voltage divider as:

$$V_{OUT} = \frac{R1+R2}{R1} \times V_{REF}$$

The internal V_{REF} is 0.6V with 1% accuracy. In real applications, a 22pF feed-forward ceramic capacitor is recommended in parallel with R2 for better transient response.

Current Limit Function

The uP1727Q continuously monitors the inductor current for current limit by sensing the voltage drop across the upper switch when it turns on. When the inductor current is higher than current limit threshold (6A typical), the current limit function activates and forces the upper switch turning off to limit inductor current cycle by cycle. If the load continuously demands more current than what uP1727Q could provide, uP1727Q can not regulate the output voltage. Eventually under voltage protection will be triggered and shuts down the uP1727Q if V_{OUT} is too low.

Under Voltage Protection

Under voltage Protection is triggered if the FB voltage is lower than 0.26V. Once UVP is triggered , the uP1727Q turn off high-side and low-side MOSFET. The under voltage protection is latch-off function and can only be reset by toggling EN threshold or re-POR.

Over Voltage Protection

Over voltage protection (OVP) is triggered if the FB voltage is higher than 0.93V. Once OVP is triggered, the uP1727Q turn on low-side MOSFET and turn off high-side MOSFET. The over voltage protection is latch-off function and can only be reset by toggling EN threshold or re-POR.

Over Temperature Protection (OTP)

The OTP is triggered and shuts down the uP1727Q if the junction temperature is higher than 150°C. The OTP is a non-latch type protection. The uP1727Q automatically initiates another soft start cycle if the junction temperature drops below 130°C.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, V_{IN} ---------- -0.3V to +6.5V

LX Pin Voltage

DC ---------- -0.3V to +(V_{IN} +0.3V)

<50ns ---------- -5V to +(V_{IN} +5V)

Other Pins ---------- -0.3V to (V_{DD} + 0.3V)

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- 150°C

Lead Temperature (Soldering, 10 sec) ---------- 260°C

ESD Rating (Note 2)

HBM (Human Body Mode) ---------- 2kV

MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)

WDFN3x3-10L θ_{JA} ---------- 68°C/W

WDFN3x3-10L θ_{JC} ---------- 6°C/W

Power Dissipation, P_D @ T_A = 25°C

WDFN3x3-10L ---------- 1.47W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C

Operating Ambient Temperature Range ---------- -40°C to +85°C

Supply Input Voltage, V_{IN} ---------- +2.6V to +5.5V

Electrical Characteristics

(V_{IN} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Current						
Supply Voltage Range	V_{IN}	V_{IN} = V_{DD}	2.6	--	5.5	V
Under Voltage Lockout	V_{UVLO}	V_{DD} Rising, V_{EN} = V_{DD}	2.5	--	--	V
		V_{DD} Falling V_{EN} = V_{DD}	--	--	1.8	V
Quiescent Current	I_Q	V_{FB} = 0.8V, no switching	--	100	--	uA
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	0.01	1	uA
Reference						
Reference Voltage	V_{REF}	I_{OUT} = 0mA	0.594	0.600	0.606	V
Output Voltage Line Regulation	ΔV_{OUT}	VIN = 2.6V to 5.5V, I_{OUT} = 0A	--	0.3	--	%/V
Output Voltage Load Regulation	ΔV_{OUT}	I_{OUT} = 0A ~3A	-1	--	+1	%

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Oscillator						
Switching Frequency	f_{OSC}		--	1	--	MHz
Maximum Duty Cycle	DC	V_{IN} = V_{OUT}, V_{FB} = 0.55V	100	--	--	%
Power Switches						
$R_{DS(ON)}$ of Upper Switch	R_{P_FET}	V_{IN} = 3.6V, I_{LX} = 100mA	--	70	--	mΩ
$R_{DS(ON)}$ of Lower Switch	R_{N_FET}	V_{IN} = 3.6V, I_{LX} = -100mA	--	50	--	mΩ
Logic Input						
EN Logic Low Threshold	V_{IL}	V_{IN} = 2.6V to 5.5V, Shutdown	--	--	0.4	V
EN Logic High Threshold	V_{IH}	V_{IN} = 2.6V to 5.5V, Enable	1.5	--	--	V
EN Pull Low Resistance	R_{EN}		--	500	--	kΩ
Power OK Output						
Logic High Leakage Current	I_{POK}	V_{POK} = V_{DD} = 5V	--	--	1	uA
Logic Low Voltage	V_{POK}	I_{POK} = 1mA	--	--	0.2	V
POK Output High Threshold		Measured FB with Respect to V_{REF}	85	90	--	%
POK Hysteresis			--	5	--	%
Power ON/OFF						
Soft-Start Time	T_{SS}		0.8	1.4	2.0	ms
V_{OUT} Discharge Resistance			--	100	--	Ω
Protection						
V_{OUT} Under Voltage Protection (Latch-Off)			--	44	50	%
V_{OUT} Over Voltage Protection (Latch-Off, Delay Time =10us)			150	155	--	%
P-MOSFET Current Limit	I_{PLIM}		5	6	--	A
Thermal Shutdown Temperature	T_{SHDN}	By design	--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SHDN}	By design	--	20	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

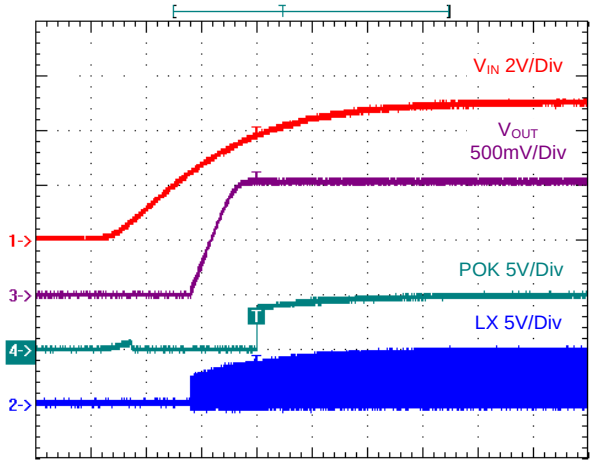
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

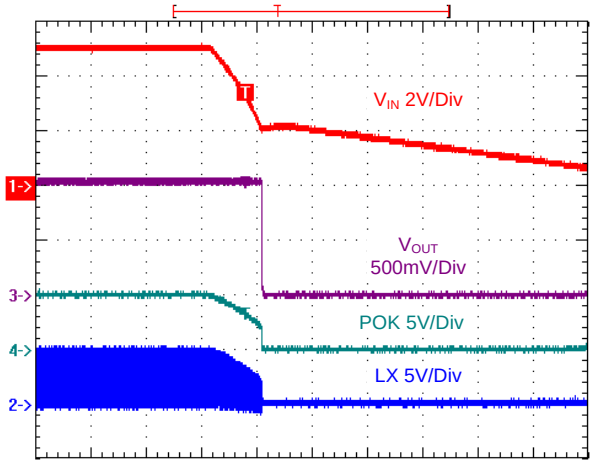
Typical Operation Characteristics

Power On from V_{IN}



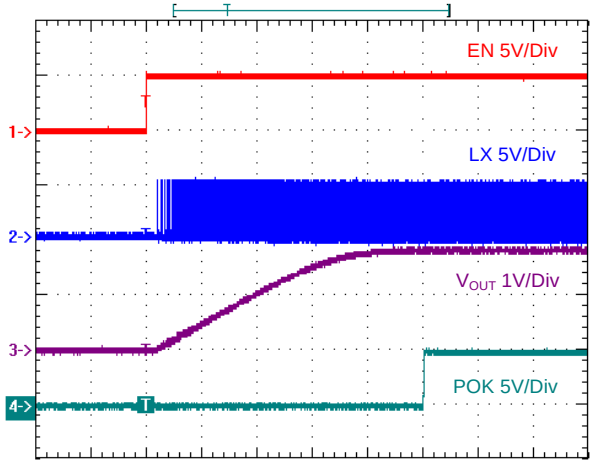
Time (2ms/Div)
V_{IN} = 5V, V_{OUT} = 1.05V, I_{OUT} = 3A

Power Off from V_{IN}



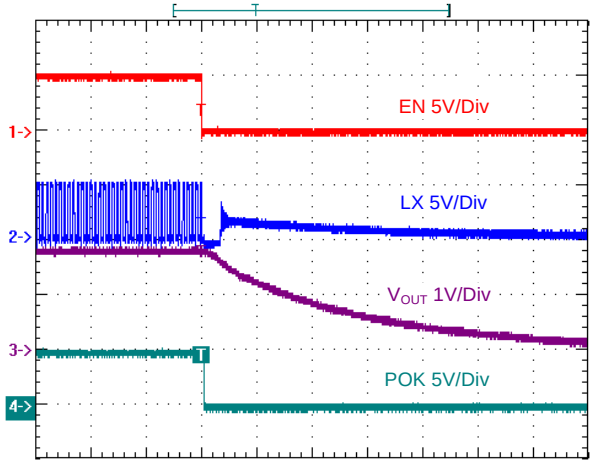
Time (4ms/Div)
V_{IN} = 5V, V_{OUT} = 1.05V, I_{OUT} = 3A

EN Turn On



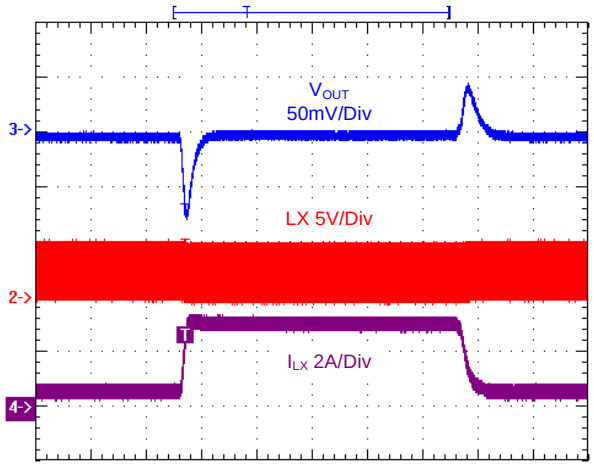
Time (400us/Div)
V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 3A

EN Turn Off



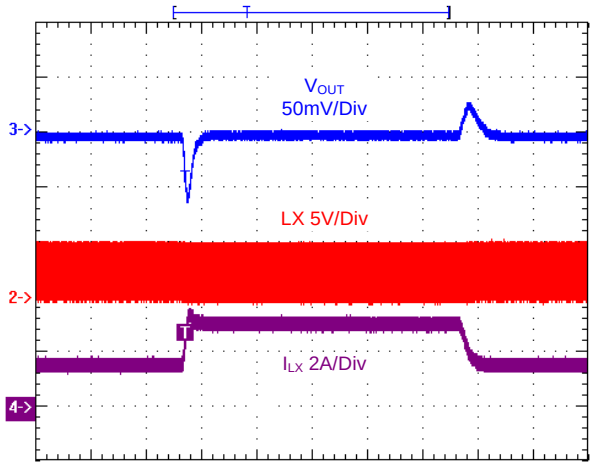
Time (10us/Div)
V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 3A

Load Transient



Time (100us/Div)
V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 0A ~ 3A

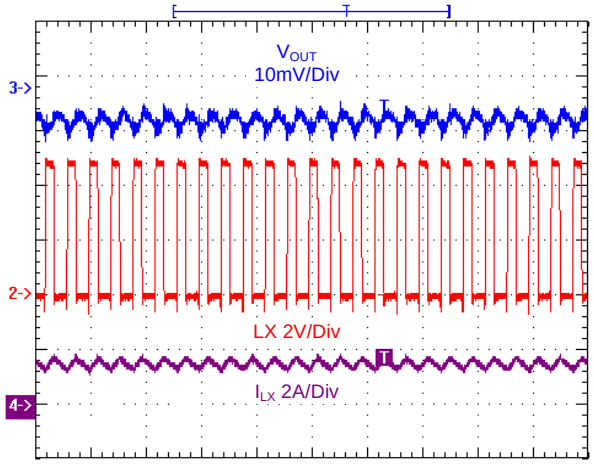
Load Transient



Time (100us/Div)
V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 1.5A ~ 3A

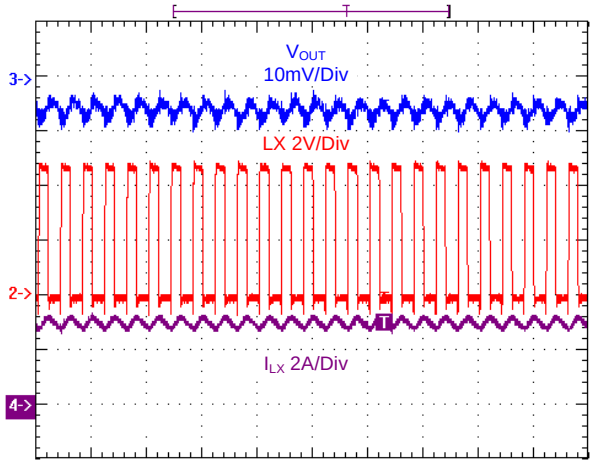
Typical Operation Characteristics

Switching



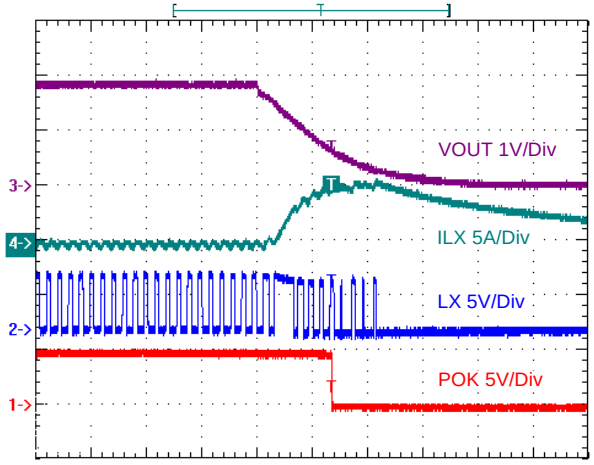
Time (2us/Div)
V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 1.5A

Switching



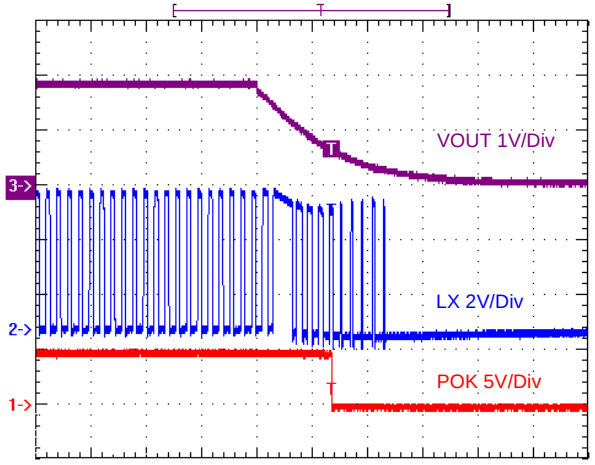
Time (2us/Div)
V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 3A

Over Current Protection



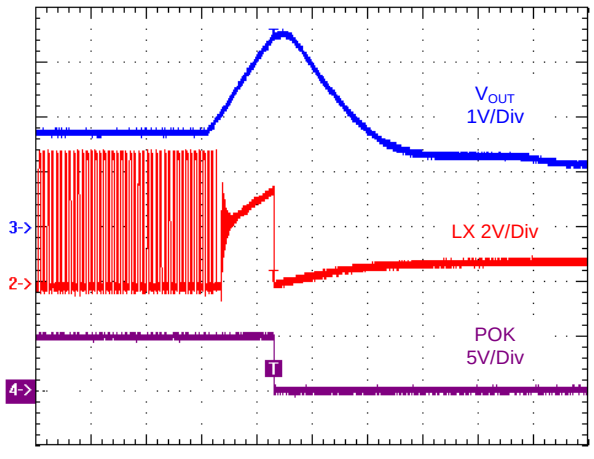
Time (4us/Div)
V_{IN} = 5.0V, V_{OUT} = 1.8V

Under Voltage Protection



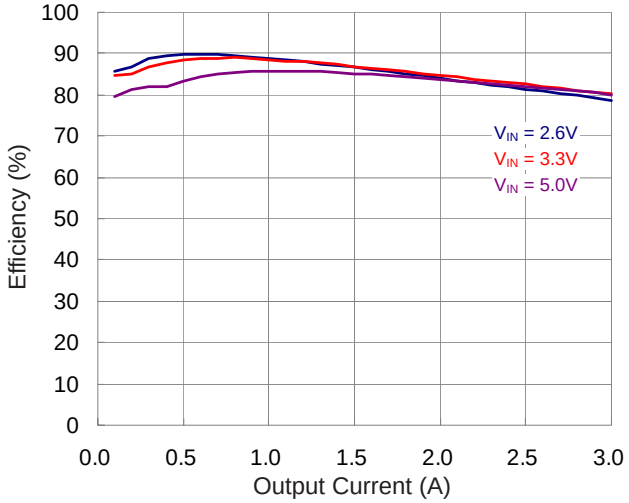
Time (4us/Div)
V_{IN} = 5.0V, V_{OUT} = 1.8V

Over Voltage Protection



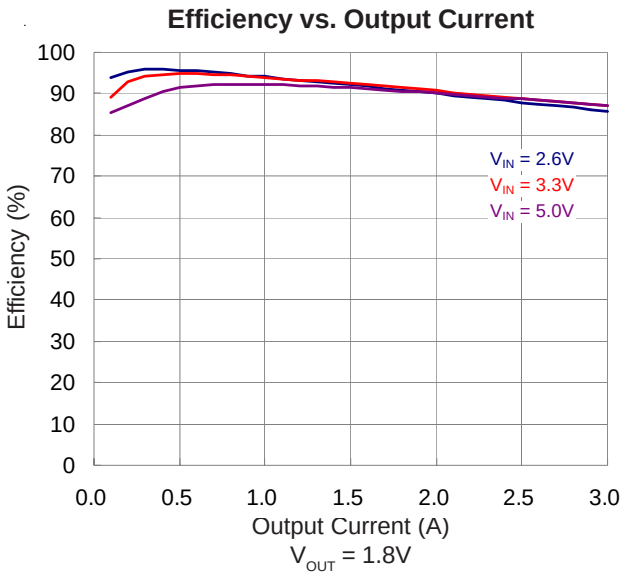
Time (10us/Div)
V_{IN} = 5.0V, V_{OUT} = 1.8V

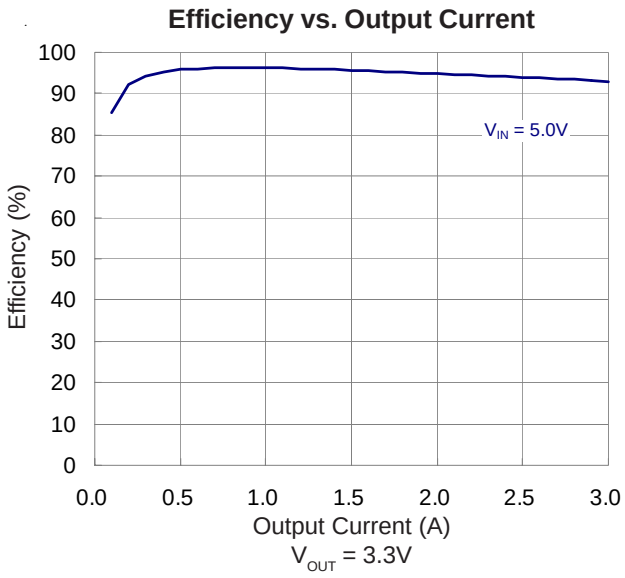
Efficiency vs. Output Current



V_{OUT} = 1.05V

Typical Operation Characteristics





PCB Layout Recommendation

Figure 1 shows the pin configuration and typical application circuit of uP1727Q. The VIN pin is the drain of the high side MOSFET, the GND pin is the source of the low side MOSFET, and the switching node, LX, is the joint of high side MOSFET and low side MOSFET. These three pins are directly connected to the power MOSFETs, and they not only conduct current but also provide heat conduction path. Therefore special attention should be paid to these pins and pad.

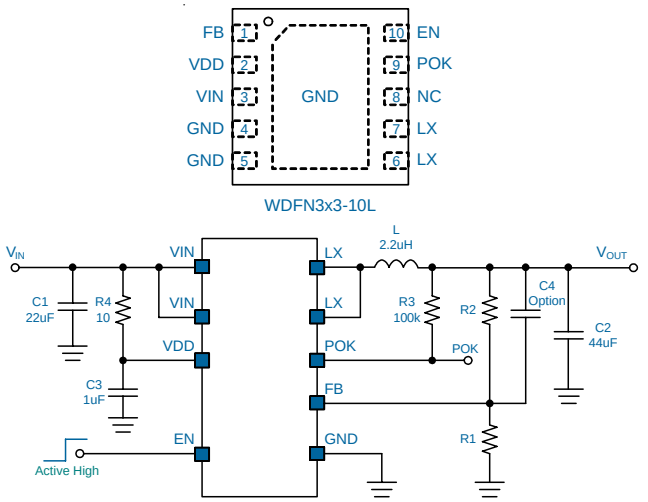


Figure 1. Pin configuration and typical application circuit of uP1727Q

Since power MOSFETs are integrated into the thermally enhanced package, special attention should be paid to the PCB layout for VIN, LX, GND pin/pad to obtain better thermal dissipation performance. Figure 2 shows a layout recommendation of four layers PCB of uP1727Q. The input cap is placed physically close to IC, and across the VIN and GND plane to minimize parasitic components.

The top layer ground (GND) and input (VIN) copper fill area near the IC should be as large as possible. This will aid in thermal dissipation as well as lower conduction losses in the ground return. PCB pattern for LX should be as broad as possible. It is recommended to duplicate the LX plane shape to the inner and bottom layer for current sharing and heat transferring. Broad LX plane helps heat transfer to the inner PCB layer. Use at least one single whole inner plane for GND. The GND pin should connect to the large ground plane and add sufficient number of via to the inner ground layer. The GND pin should also connect to the exposed pad. Larger GND plane also help heat transfer to the inner PCB layer.

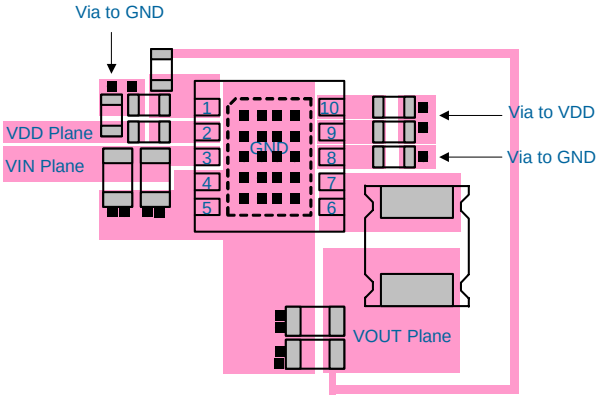


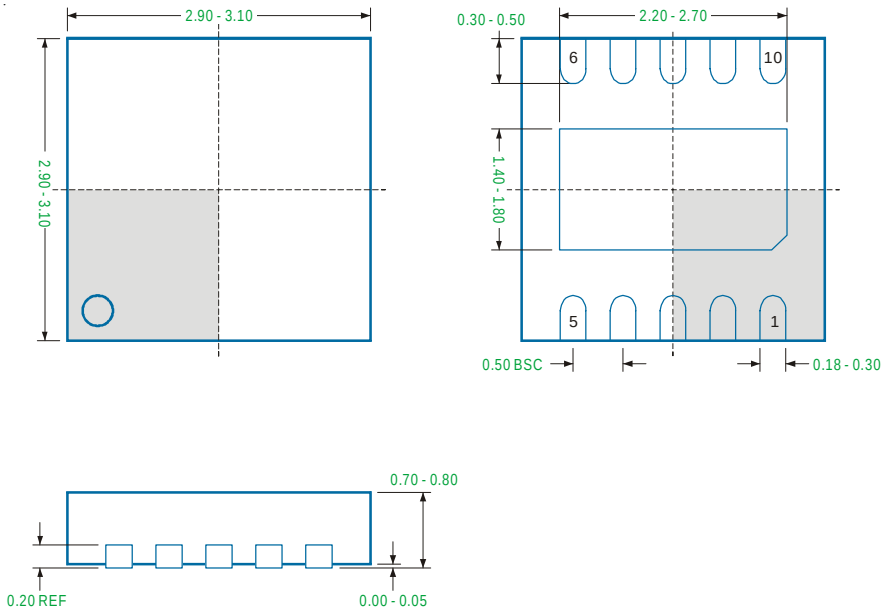
Figure 2. PCB layout recommendation

In addition to the thermally-related layout, there are other layout guidelines for rest of the circuit as show in the following.

- VDD and VIN capacitor should be placed near the device.
- Keep the input switching current loop as small as possible.
- Keep feedback compensation components away from switching node LX.
- Output capacitor should be connected to a broad pattern of the GND.
- Voltage feedback trace should be as short as possible, and preferably with inner ground layer shielding.

Package Information

WDFN3x3-10L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Important Notice

uPI and its subsidiaries reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

uPI products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment. However, no responsibility is assumed by uPI or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of uPI or its subsidiaries.

uPI Semiconductor Corp.
Headquarter
9F.,No.5, Taiyuan 1st St. Zhubei City,
Hsinchu Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888

Sales Branch Office
12F-5, No. 408, Ruiguang Rd. Neihu District,
Taipei Taiwan, R.O.C.
TEL : 886.2.8751.2062 FAX : 886.2.8751.5064