uP1741P-B1

Wide Input Range, 8A, Synchronous-Rectified Buck Converter

General Description

The uP1741P-B1 is a high performance synchronous buck converter. The synchronous buck of the uP1741P-B1 uPI's proprietary robust constant on-time (RCOT™) PWM scheme that features easy-to-use, low external component count, fast transient response and quasi-constant frequency operation over the operation range.

The uP1741P-B1 has complete functions including under voltage protection, over current protection, over voltage protection, power-up sequencing, power OK output, and thermal shutdown. The uP1741P-B1 is available in WQFN4x4-32L package.

Features

- **Wide Input Voltage Range from 4.5V to 26V**
- **Fast Load Transient Response**
- **Output Current Up to 8A**
- **RCOT™ Control Topology**
- **Discharge Output When Disable**
- **Fixed 1.5V, 1.8V Output or Adjustable from 0.75V to 3.3V**
- **POR, OVP, UVP and Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Applications

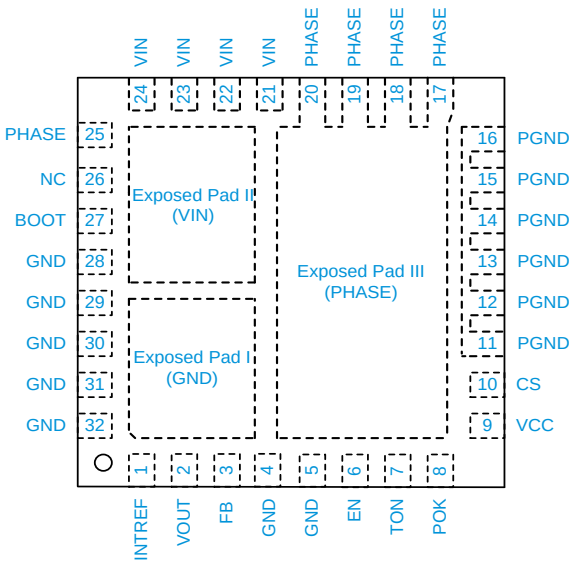
- **Desktop PCs, Notebooks, and Workstations**
- **Microprocessor and Chipset Supplies**

Ordering Information

Order Number	Package Type	Top Marking
uP1741PQMI-B1	WQFN4x4-32L	uP1741P

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



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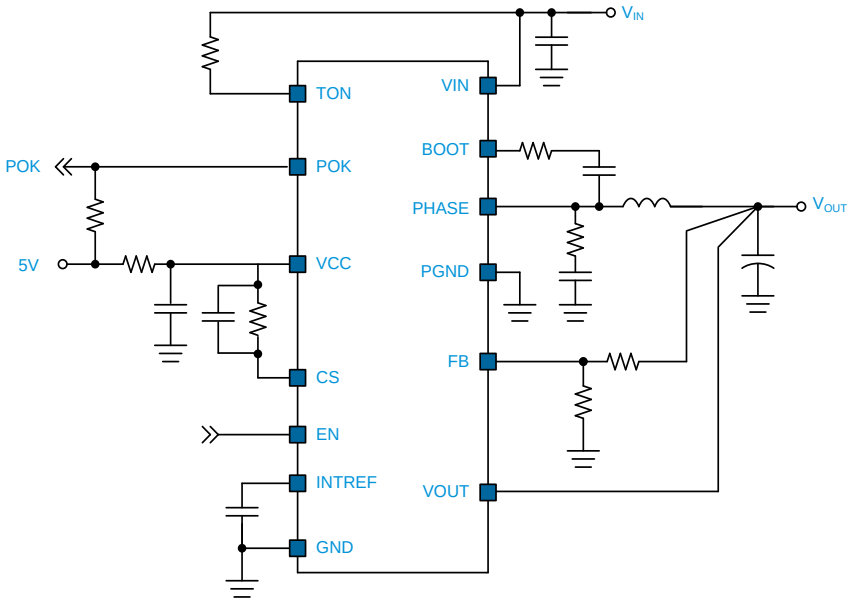
Typical Application Circuit



uP1741P-B1

Functional Pin Description

Pin No.	Name	Pin Function
1	INTREF	**Internal Reference.** Bypass this pin with 0.1uF ceramic capacitor to GND.
2	VOUT	**Output Voltage Sense.** Connect this pin to output point of converter. A discharge resistor is connected when disable.
3	FB	**Voltage Feedback Input.** This pin is the inverting input of the error amplifier. A resistor divider from output to GND is used to set the regulator output voltage. For fixed output voltage application, connect this pin to VCC for fixed output 1.8V, or connect this pin to GND for fixed output 1.5V.
4, 5, 28~32	GND	**Signal Ground for the IC.** All voltage levels are measured with respect to this pin.
6	EN	**EN Enable.** This pin is for the chip enable and disable. Pulling this pin to logic high/low level to enable/disable the IC.
7	TON	**On-Time Setting Pin.** Connect a resistor from this pin to V_{IN} to set the on-time for the upper MOSFET.
8	POK	**Power OK Indication.** POK is the open-drain architecture that indicates the output voltage is ready or not. This pin is set to high impedance when the output voltage is within regulation and the soft-start ends. POK is pulled low immediately when either output is in soft-start, standby, shutdown or fault protection.
9	VCC	**5V Power Supply Input.** This pin provides power for internal circuit. Bypass this pin with a 1uF ceramic capacitor to GND.
10	CS	**CS Current Limit Threshold Setting.** Connect this pin through the setting resistor to VCC for inductor current limit threshold setting.
11~16	PGND	**Power Ground.** This pin is dedicated for lower MOSFET gate driver and should be directly connected to the source of the lower MOSFET with an isolated path.
17~20, 25	PHASE	**Switch Node.** This pin is used as the sink for the upper MOSFET gate driver. This pin is also monitored by the shoot-through protection circuitry to determine when the upper MOSFET has turned off. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET.
21~24	VIN	**Supply Input.** Input voltage that supplies current to the output voltage.
26	NC	**Not Internally Connected.**
27	BOOT	**Bootstrap Supply for the Floating Upper MOSFET Gate Driver.** The bootstrap capacitor provides the charge to turn on the upper MOSFET. Connect this bootstrap capacitor between BOOT pin and the PHASE pin to form a bootstrap circuit.
Exposed Pad I (GND)		**Signal Ground for the IC.** All voltage levels are measured with respect to this pin.
Exposed Pad II (VIN)		**Supply Input.** Input voltage that supplies current to the output voltage.
Exposed Pad III (PHASE)		**Switch Node.** This pin is used as the sink for the upper MOSFET gate driver. This pin is also monitored by the shoot-through protection circuitry to determine when the upper MOSFET has turned off. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET.

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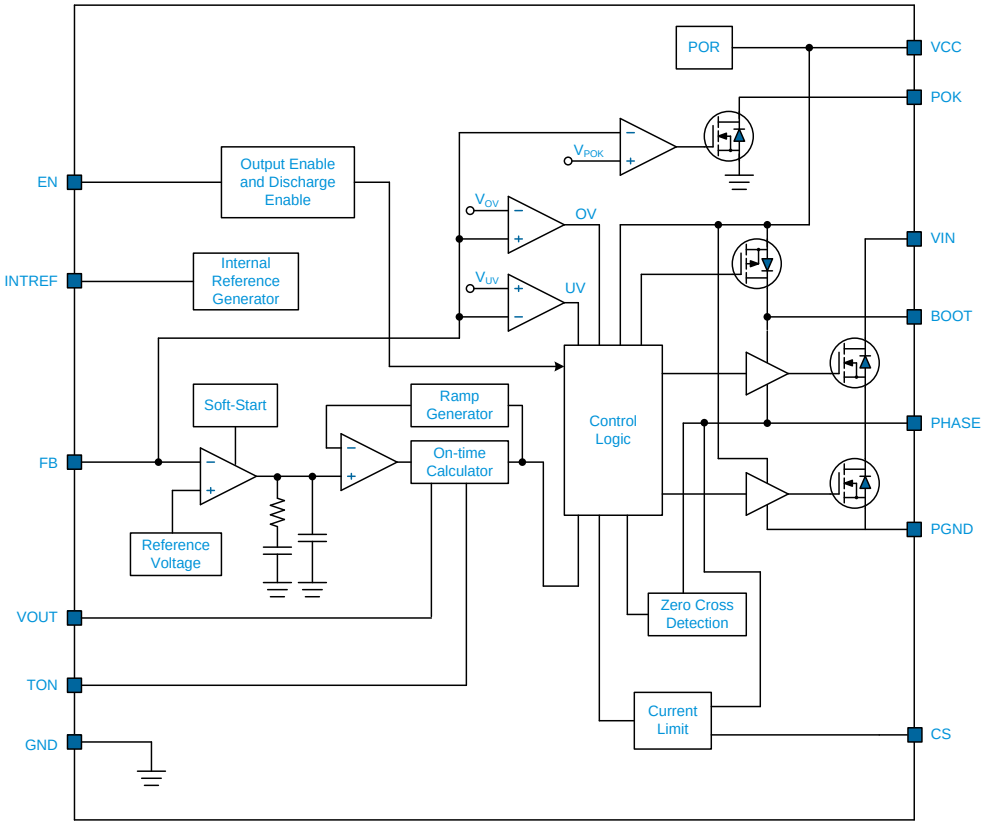
Functional Block Diagram



uP1741P-B1

Functional Description

The uP1741P-B1 is a high performance synchronous buck converter with wide input range.
The buck converter adopts RCOT™ PWM scheme that features easy-to-use, low external component count, fast transient response and quasi-constant frequency operation over the operation range.
The uP1741P-B1 has complete functions including over current protection, over voltage protection, thermal shutdown, power-up sequencing, power OK output, and thermal shutdown. The uP1741P-B1 is available in space-saving WQFN4x4-32L package.

Output Voltage Selection

As shown in Table 1, uP1741P-B1 can support fixed 1.8V/1.5V or adjustable output voltage by connecting resistor divider to the FB pin

Table 1. Output Voltage Selection

FB Connection	VOUT
VCC	1.8V
GND	1.5V
Resistor Divider	Adjustable

The uP1741P-B1 can adjust output voltage by connecting a resistive voltage divider between VOUT and GND as shown in Figure 1. Choose R_{FB2} to be approximately 10kΩ and solve R_{FB1} using the equation as below:

$V_{OUT} = V_{REF} \times (1 + \frac{R_{FB1}}{R_{FB2}})$, where V_{REF} is 0.75V (typ.)

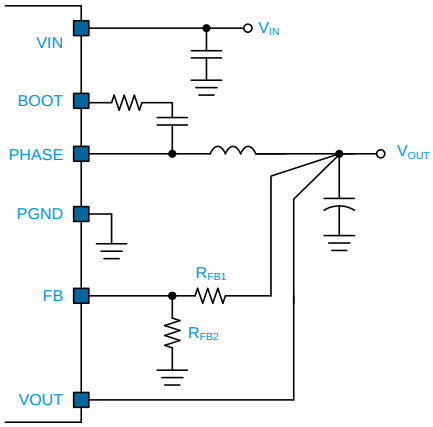


Figure 1. Output Voltage Setting

On-Time Setting

The uP1741P-B1 adopts a compensated constant-on-time control scheme. A resistor R_{TON} connected to TON pin programs the constant on time according to equation:

$T_{ON} = \frac{3.8\times10^{-12}\times VOUT\times R_{TON}}{VIN-0.5V}$,

where R_{TON} is in kΩ, VIN is the supply input voltage and VOUT is the sensed output voltage

Functional Description

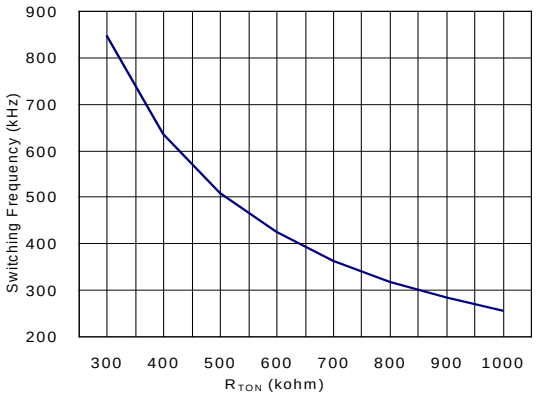


Figure 2. Switching Frequency vs. R_{TON}

Soft Start and POK

The soft-start function of the uP1741P-B1 is achieved by ramping up reference as shown in Figure 3. After EN is set high, the VREF is rising. There is a time delay between VREF ramping up and VOUT rising. After that, the uP1741P-B1 initiates soft-start operation.

The POK is an open-drain output. The uP1741P-B1 asserts POK high impedance output if the output voltage is within regulation with a time delay after soft-start end. Anytime the fault protection is triggered, the POK signal will go low immediately.

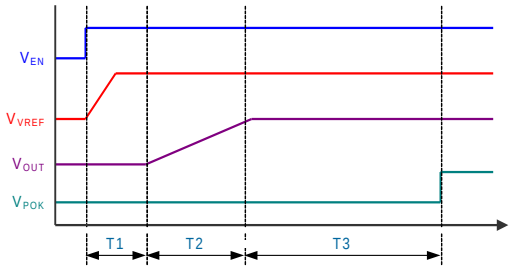


Figure 2. Soft Start and POK Timing

Light Load Operation

The uP1741P-B1 automatically reduces switching frequency at light load to maintain high efficiency. As the output current decreases from heavy-load condition, the inductor current will also be reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the lower MOSFET allows only partial of negative current when the inductor freewheeling current reaches negative. As the load current is further decreased, it takes longer time to discharge the output capacitor to the level than requires the next ON cycle.

Output Discharge Control

The uP1741P-B1 has internal discharge resistor 15Ω, which is connected from VOUT to GND.

Functional Description

Output Current Limit

The synchronous buck output monitors the inductor valley current by lower MOSFET $R_{DS(ON)}$ when it turns on. The over current limit is triggered once the sensing current level is higher than $V_{OCSET.}$ When triggered, the over current limit will keep upper MOSFET off even the voltage loop commands it to turn on. Converter will latch off if CS pin is open during VCC power on or enable.

The output voltage will decrease if the load continuously demands more current than current limit level. Further increase in load current higher than the current limit level will eventually let V_{OUT} decrease to trip UVP to shut down the uP1741P-B1.

The current limit threshold is set by connecting a resistor from CS to VCC. The CS pin will sink a 10uA current source and create a voltage drop across R_{CS} as the V_{OCSET}.

V_{OCSET} = 10uA x R_{CS}

When the voltage drop across the lower MOSFET equals the voltage across the setting resistor, the current limit will be activated.

The current limit level is calculated as:

$$I_{LIM} = \frac{V_{OCSET}}{R_{DS(ON)}} + \frac{I_{RIPPLE}}{2}$$

where I_{RIPPLE} is the peak-to-peak inductor ripple current at steady state.

Over Voltage/Under Voltage Protection

The uP1741P-B1 monitors FB voltage to detect overvoltage and undervoltage condition of output. When the FB voltage becomes higher than 115% of the target voltage, the OVP is triggered. Then, upper MOSFET is off and lower MOSFET is on. When the FB voltage is lower than 70% of the target voltage, the UVP is triggered after 30us fault detection. Then, upper MOSFET and lower MOSFET are latched off. This function is enabled 2ms after EN goes high to ensure startup.

VCC UVLO

The VCC has under voltage lockout protection (UVLO). When the VCC voltage is lower than UVLO threshold voltage, all functions are turned off. This is non-latch protection.

Thermal Protection

The uP1741P-B1 monitors the temperature of itself. If the temperature exceeds typical 150°C, the uP1741P-B1 will be turned off. This is non-latch protection.

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Absolute Maximum Rating

(Note 1)

VCC to GND ---------- -0.3V to +6V

VIN to GND ---------- -0.3V to +30V

BOOT to PHASE ---------- -0.3V to +6V

PHASE to GND

- DC ---------- -0.3V to +30V
- < 50ns -- ---------- -5V to +30V

Other Pins ---------- -0.3V to +6V

Storage Temperature Range ---------- -65℃ to +150℃

Junction Temperature ---------- 150℃

Lead Temperature (Soldering,10 sec) ---------- 260℃

EDS Rating (Note 2)

- HBM (Human Body Mode) ---------- 1kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)

- WQFN4x4-32L $\theta_{JA, controller}$ ---------- 55℃/W
- WQFN4x4-32L $\theta_{JA, HS}$ ---------- 45℃/W
- WQFN4x4-32L $\theta_{JA, LS}$ ---------- 39℃/W
- WQFN4x4-32L $\theta_{JC, controller}$ ---------- 21℃/W
- WQFN4x4-32L $\theta_{JC, HS}$ ---------- 12℃/W
- WQFN4x4-32L $\theta_{JC, LS}$ ---------- 7℃/W

Power Dissipation, P_D @ T_A = 25℃

- WQFN4x4-32L $P_{D, controller}$ ---------- 1.81W
- WQFN4x4-32L $P_{D, HS}$ ---------- 2.22W
- WQFN4x4-32L $P_{D, LS}$ ---------- 2.56W

Recommended Operation Conditions

(Note 4)

Supply Input Voltage, V_{IN} ---------- +4.5V to +26V

Control Voltage, VCC ---------- +4.5V to +5.5V

Operating Junction Temperature Range ---------- -40℃ to +125℃

Operating Ambient Temperature Range ---------- -40℃ to +85℃

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25℃ on a high effective thermal conductivity test board of *JEDEC 51-7* thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions

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Electrical Characteristics

(V_{IN} = 12V, V_{CC} = 5V, T_A = +25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Current						
VCC Current	I_{VCC}	Supply current, EN = 5V, force FB above regulation level (no switching)	--	470	1000	uA
		Shutdown current, EN = 0V	--	1	10	
TON Current	I_{TON}	Operating current, R_{TON} = 1MΩ	--	15	--	uA
		Shutdown current, EN = 0V	--	0.1	5	
Reference Voltage						
FB Reference Voltage	V_{REF}	V_{VCC} = 4.5V to 5.5V	0.742	0.75	0.758	V
		Connect FB pin to VCC	--	1.8	--	
		Connect FB pin to GND	--	1.5	--	
FB Input Bias Current	I_{FB}	V_{FB} = 0.75V	-1	0.1	1	uA
VOUT						
Input Resistance	R_{VOUT}		--	100	--	kΩ
Discharge Resistance	$I_{VOUTDis}$	EN = 0V	--	15	--	Ω
On Time						
On-Time	T_{ON}	R_{TON} = 510kΩ, VOUT = 1.35V	182	228	274	ns
Minimum On-Time	T_{ONMIN}		--	80	--	ns
Minimum Off-Time	T_{OFFMIN}		250	400	550	ns
Power OK						
POK Rising Threshold	V_{THPOKH}	Measured at FB, with respect to reference voltage	87	90	93	%
		Hysteresis	--	5	--	
POK Propagation Delay	T_{POK}	From FB forced below POK falling threshold to POK go low	--	2.5	--	us
POK Leakage Current	I_{LK_POK}	High state, POK = 5V	--	--	1	uA
POK Output Low Voltage	V_{POK_L}	Sink current = 1mA	--	--	0.4	V
Logic Input Threshold						
High Level Input Voltage	V_{IH}	EN high	2	--	--	V
Low Level Input Voltage	V_{IL}	EN low	--	--	0.8	V
Logic Input Leakage Current	V_{INLEAK}	EN = 5V/ 0V	-1	--	1	uA
Internal Bootstrap Switch						
Internal Boost Charging Switch On-Resistance	R_{BOOT}	VCC to BOOT, I_{BOOT} = 5mA	--	--	80	Ω

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Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Power Switches						
Upper Switch Resistance	$R_{UG,DSON}$		--	21.5	26	mΩ
Lower Switch Resistance	$R_{LG,DSON}$		--	9	11	mΩ
Protection: Current Limit						
CS Sink Current	I_{CS}	V_{CS} > 4.5V	9	10	11	uA
CS Current Temp. Coefficient	T_{CICS}	On the basis of 25°C (Note 5)	--	4700	--	ppm/°C
OCP Comparator Offset	V_{OCLoff}	GND – V_{PHASE}, R_{CS} = 5kΩ	-15	--	15	mV
Zero Current Threshold	V_{ZC}	GND – V_{PHASE},	-5	--	10	mV
Protection: UVP and OVP						
OVP Trip Threshold	V_{OVP}	Measured at FB, with respect to reference voltage	110	115	120	%
OVP Propagation Delay	T_{OVPDEL}	Force FB above OVP trip threshold	--	20	--	us
UVP Trip Threshold	V_{UVP}	Measured at FB, with respect to reference voltage	60	70	80	%
UVP Propagation Delay	T_{UVPDEL}	Force FB above UVP trip threshold	--	30	--	us
UVP Enable Delay	T_{UVPEN}	From EN signal go high	--	2	--	ms
Protection: UVLO						
VCC UVLO Threshold	V_{UVLO}	Rising edge	3.9	4.2	4.5	V
		Hysteresis	--	0.12	----	
Protection: Thermal Shutdown						
Thermal Shutdown Threshold	T_{SDN}	Shutdown temperature	--	150	--	°C
		Hysteresis	--	20	--	

Note 5. Guaranteed by design

Application Information

PCB Layout Considerations

High speed switching and relatively large peak currents in a synchronous-rectified buck converter make the PCB layout a very important part of design. Fast current switching from one device to another in a synchronous-rectified buck converter causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise that result in overvoltage stress on devices. Careful component placement layout and printed circuit board design minimizes the voltage spikes induced in the converter.

Follow the layout guidelines for optimal performance of uP1741P-B1.

- Place VIN and VCC decoupling capacitor as near as possible to the device.
- Keep analog and non-switching components away from switching components.
- Keep the snubber loop between the PHASE to PGND be as short as possible.
- Keep the pattern lines for current delivery path broad.
- Keep the PHASE node physically small and short as possible to minimize radiated emissions.
- Do not allow switching current to flow under the device.
- Make a single point connection from the signal ground to power ground.
- Providing sufficient via for VIN, PHASE and PGND.
- Voltage feedback loop should be as short as possible, and preferably with ground shield.

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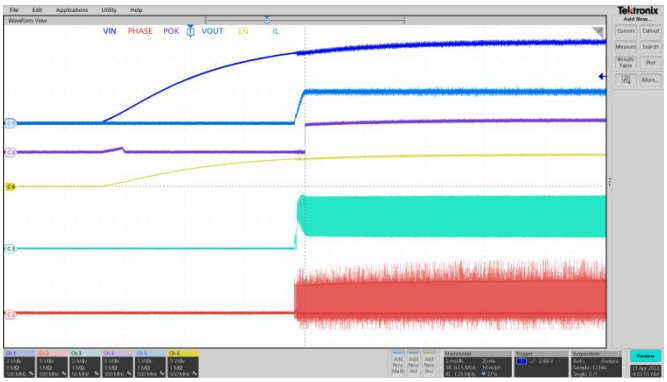
Typical Operation Characteristics

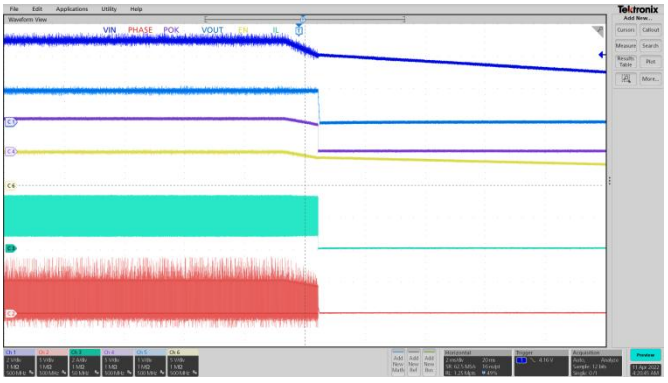
Power On from VIN



Time: 2ms/Div

CH1=VIN(2V/div),CH2=PHASE(5V/div),CH3=IL(2A/div),CH4=POK(5V/div),
CH5=VOUT(1V/div),CH6=EN(5V/div),V_{IN}=V_{EN}=5V ,V_{OUT}=1V ,Load=2A

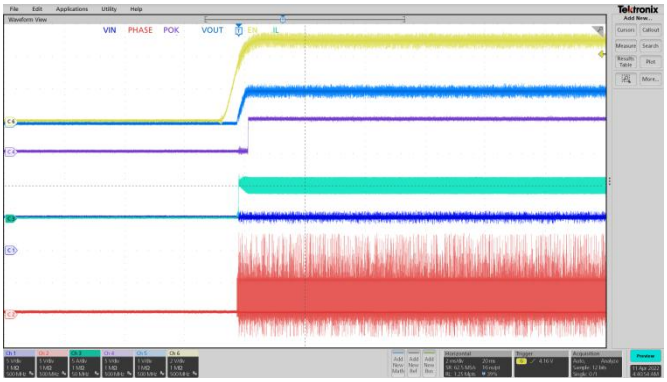
Power Off from VIN



Time:2ms/Div

CH1=VIN(2V/div),CH2=PHASE(5V/div),CH3=IL(2A/div),CH4=POK(5V/div),
CH5=VOUT(1V/div),CH6=EN(5V/div),V_{IN}=V_{EN}=5V ,V_{OUT}=1V ,Load=2A

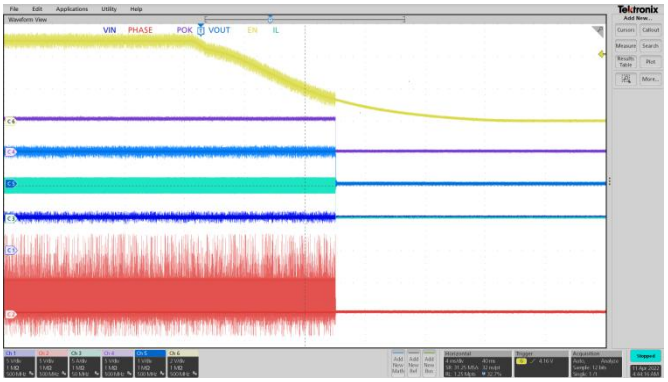
EN On



Time: 2ms/Div

CH1=VIN(5V/div),CH2=PHASE(5V/div),CH3=IL(5A/div),CH4=POK(5V/div)
CH5=VOUT(1V/div),CH6=EN(2V/div),V_{IN}=5V ,V_{OUT}=1V ,Load=5A

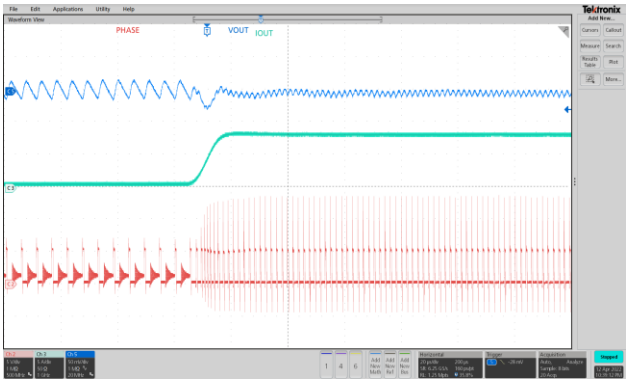
EN Off



Time: 4ms/Div

CH1=VIN(5V/div),CH2=PHASE(5V/div),CH3=IL(5A/div),CH4=POK(5V/div)
CH5=VOUT(1V/div),CH6=EN(2V/div),V_{IN}=5V ,V_{OUT}=1V ,Load=5A

Load Transient

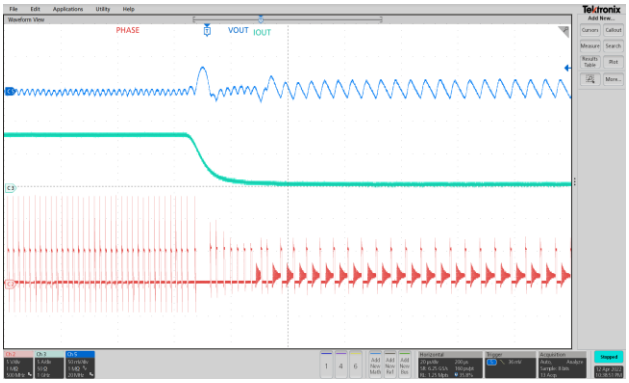


Time: 20us/Div

CH2=PHASE(5V/div), CH3=IOUT(5A/div),CH5=VOUT(50mV/div)

V_{IN}=V_{EN}=5V ,V_{OUT}=1V, Load=0.8A~8A, L=0.68uH

Load Transient



Time: 20us/Div

CH2=PHASE(5V/div), CH3=IOUT(5A/div),CH5=VOUT(50mV/div)

V_{IN}=V_{EN}=5V ,V_{OUT}=1V, Load=8A~0.8A, L=0.68uH

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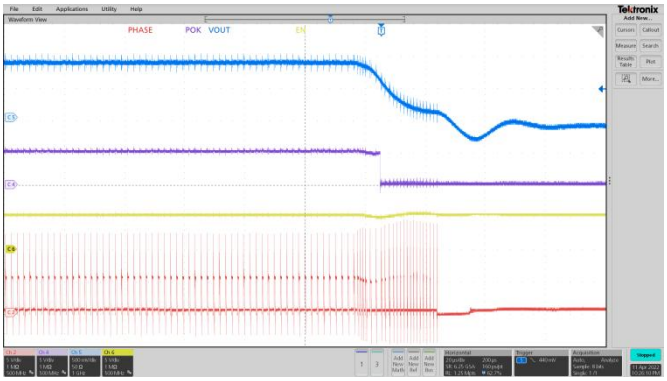
Typical Operation Characteristics

Under Voltage Protection

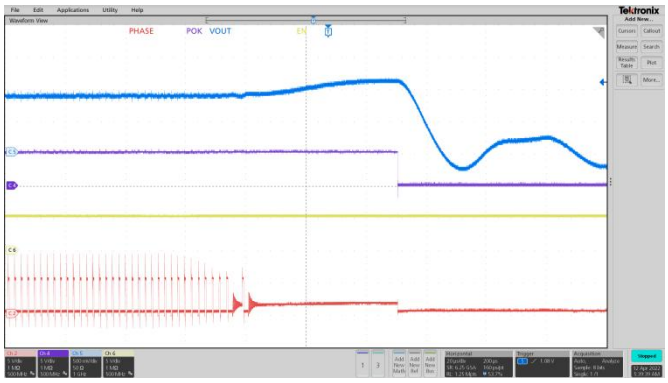


Time: 20us/Div

CH2=PHASE(5V/div),CH4=POK(5V/div),CH5=VOUT(500mV/div),CH6=EN(5V/div)

V_{IN}=5V ,V_{OUT}=1V

Over Voltage Protection

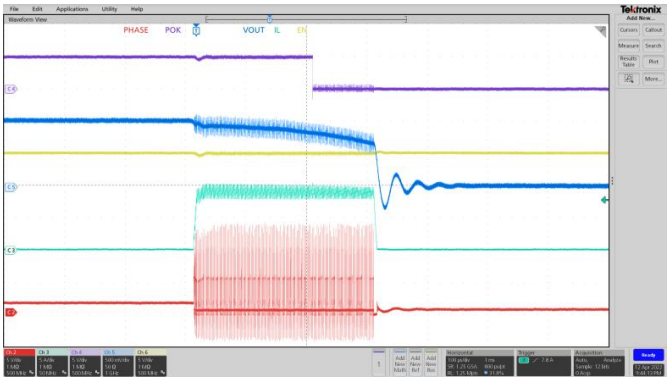


Time:20us/Div

CH2=PHASE(5V/div),CH4=POK(5V/div),CH5=VOUT(500mV/div),CH6=EN(5V/div)

V_{IN}=5V ,V_{OUT}=1V

Over Current Protection



Time: 100us/Div

CH2=PHASE(5V/div),CH3=IL(5A/div),CH4=POK(5V/div)

CH5=VOUT(500mV/div) CH6=EN(5V/div) V_{IN}=5V ,V_{OUT}=1V

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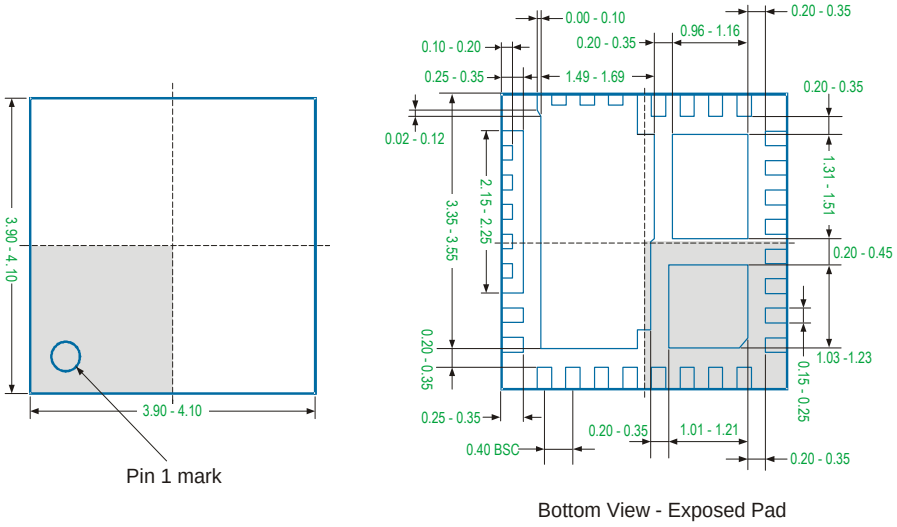
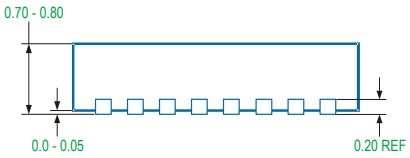
Package Information

WQFN4x4-32L





Note

1. Package Outline Unit Description:
   MIN: Minimum dimension specified.
   NOM: Nominal. Provided as a general value.
   MAX: Maximum dimension specified.
   BSC: Basic. Represents theoretical exact dimension or dimension target.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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