Dual-Phase MOSFET Drivers for DCR current sensing with Phase Extension

General Description

The uP1961S is a high performance gate driver IC with Phase Extension Module (PEM). The PEM interleaves the single PWM input and drives dual-phase synchronous buck power stages. The PEM also extracts and passes the dual-phase current signals to the controller. When operating with uPI's VR controllers with DCR current balance scheme, the uP1961S can double the phase number with perfect phase interleaving and channel current balancing.

Each driver is capable of driving a 5000pF load with 30ns transition time. This device combined with uPI multiphase buck PWM controller forms a complete core voltage regulator for advanced microprocessors.

The uP1961S features adaptive anti-shoot-through protection that prevents cross-conduction of the external MOSFET while maintains minimum deadtime for optimized efficiency.

All gate drivers are turned off by pulling low EN pin or high-impedance at PWM0 pin, preventing rapid output capacitor discharge during system shutdowns. Another feature is supply input under voltage lockout. The uP1961S is available in thermal enhanced WQFN3x3 - 16L package.

Ordering Information

Order Number	Package	Top Marking
uP1961SQDD	WQFN3x3-16L	uP1961S
Note: PWM0 = 3.3V		

Note: uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

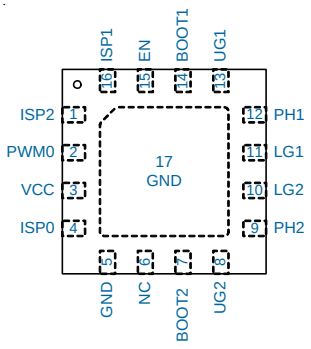
Features

- **Quad MOSFET Drivers for Dual-Phase Buck Converter with Single PWM Input**
- **One PWM Signal Generates Both Drivers**
- **Alternatively Pass DCR Current Signals of Both Phase to Controller for Current Balance**
- **Tri-State PWM Input for Bridge Shutdown**
- **Output Disable Control for Bridge Shutdown**
- **Bootstrapped High-Side Drivers**
- **Adaptive Anti-Shoot-Through Protection Circuit**
- **Supply Input Under Voltage Lockout**
- **Low Power Dissipation**
- **WQFN3x3 - 16L Package**
- **RoHS Compliant and Halogen Free**

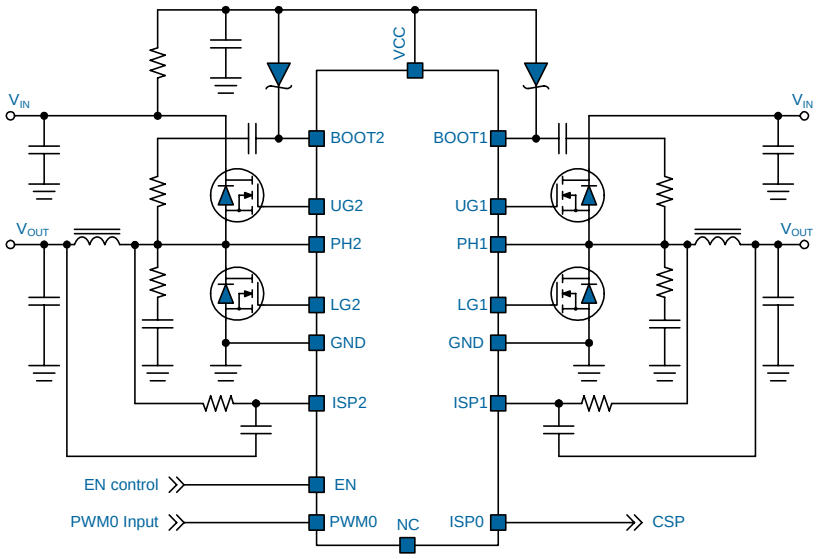
Applications

- **Core Voltage Supplies for Intel and AMD Mobile Microprocessors**
- **High Frequency Low Profile DC/DC Converters**
- **High Current Low Output Voltage DC/DC Converters**
- **High Input Voltage DC/DC Converters**
- **All-in-one Synchronous Buck Drivers**

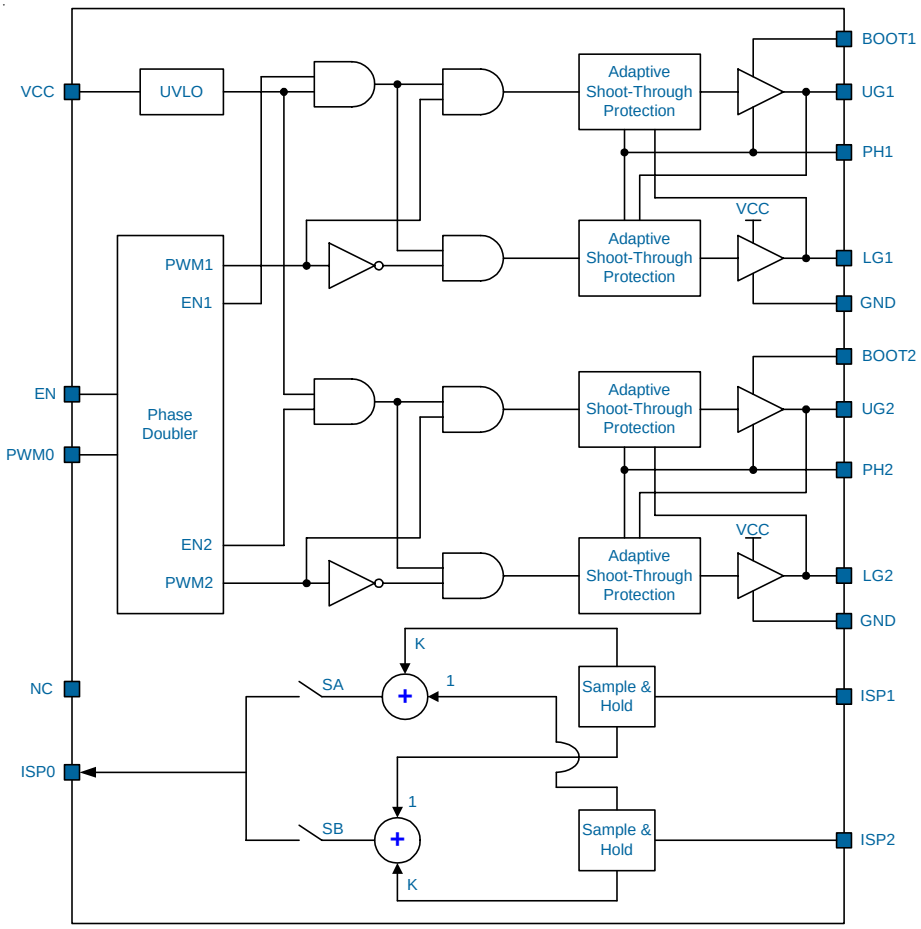
Pin Configuration



Typical Application Circuit



Functional Block Diagram



Functional Pin Description

No.	Name	Pin Function
1	ISP2	**Non-inverting input of the current sensing for phase2.** This pin is used for differentially sensing channel 2 output current. the sensed current is used for channel current blancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor .
2	PWM0	**PWM Input.** This pin receives logic level input and controls the driver outputs. The PWM pin is in high input impedance state if EN input is low. When EN input is high, the PWM pin voltage will be pulled to tri-state by internal circuit. The resistor connected from PWM pin to GND for PWM controller function setting must be greater than 15kΩ.
3	VCC	**Supply Voltage for the IC.** A 2.2 ohm resistor to VCC input with a 0.1uF bypass ceramic capacitor to GND are recommended.
4	ISP0	**current sensing output for ISP1 or ISP2.** ISP0 is connected to either ISP1 or ISP2 according to the internal flip-flop status for DCR current sensing.
5	GND	**Ground for the IC.** All voltage levels are measured with respect to these pins.
6	NC	**Not Internally Connected.**
7	BOOT2	**Bootstrap 2 Supply for the Floating Upper Gate Driver.** Connect the bootstrap resistor (typically 2.2 ohm) and capacitor (typically 0.1uF) between BOOT2 pin and the PH2 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Ensure that C_{BOOT} is placed near the IC.
8	UG2	**Upper Gate2 Driver Output.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
9	PH2	**PHASE2 Switch Node.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UG2 driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. A Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.
10	LG2	**Lower Gate 2 Driver Output.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
11	LG1	**Lower Gate 1 Driver Output.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turn off.
12	PH1	**PHASE1 Switch Node.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UG1driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. A Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.
13	UG1	**Upper Gate1 Driver Output.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
14	BOOT1	**Bootstrap 1 Supply for the floating upper gate driver.** Connect the bootstrap resistor (typically 2.2 ohm) and capacitor (typically 0.1uF) between BOOT1 pin and the PH1 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Ensure that C_{BOOT} is placed near the IC.
15	EN	**Enable Control.** logic low disables normal operation and forces both UGx and LGx off.
16	ISP1	**Non-inverting input of the current sensingr for phas1.** This pin is used for differentially sensing channel 1 output curren. the sensed current is used for channel current blancing and protection. Connect this pin to the node between the RC sense elements surrounding the inductor .
Exposed Pad		**Ground for the IC.** The exposed pad should be well soldered to PCB for effective heat conduction.

Functional Description

The uP1961S is a high performance gate driver IC with Phase Extension Module (PEM). The PEM interleaves the single PWM input and drives dual-phase synchronous buck power stages. It also extracts and passes the dual-phase current signals to the controller. When operating with uPI's VR controllers with DCR current balance scheme, the uP1961S can double the phase number with perfect phase interleaving and channel current balancing.

Each driver is capable of driving a 5000pF load with 30ns transition time. This device combined with uPI's multiphase buck PWM controller forms a complete core voltage regulator for advanced microprocessors.

The uP1961S features adaptive anti-shoot-through protection that prevents cross-conduction of the external MOSFET while maintains minimum deadtime for optimized efficiency.

All gate drivers are turned off by pulling low EN pin or high-impedance at PWM0 pin, preventing rapid output capacitor discharge during system shutdowns. Another feature is supply input under voltage lockout. The uP1961S is available in thermal enhanced WQFN3x3-16L package.

Enable Control, EN

Logic low of EN pin disables the gate driver and keep UGx/LGx low. Logic high of EN pin enables the gate driver after a delay time T_{PDHDEN}. The maximum of this period of delay time is 10uS, and it is between EN go high to UGx/LGx begins to respond to PWM0 input as show in figure 1.

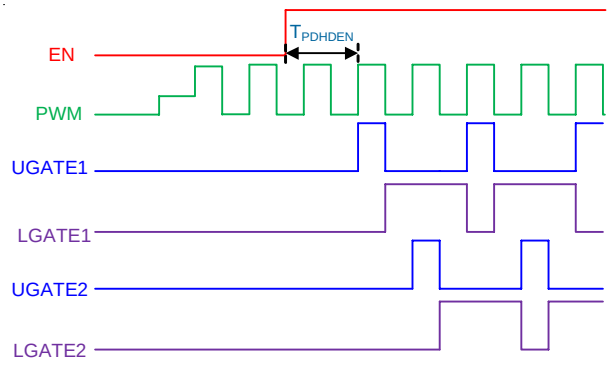


Figure 1. Enable Control, EN

PWM0 Input, PWM0

The PWM0 pin is a tri-state input. High impedance input at PWM0 turns off all gate drivers, logic low at PWM0 turns on the lower gate drivers. Logic high at PWM0 turns on one of the upper drivers and the lower driver of another phase. Once the POR of VCC is granted and EN is kept high, the PEM receives the PWM0 input and alternatively distributes its pulses to turn on the upper MOSFETs as shown in Figure 2. The odd pulses are used to turn on phase 1 while the even pulses are used to turn on phase 2.

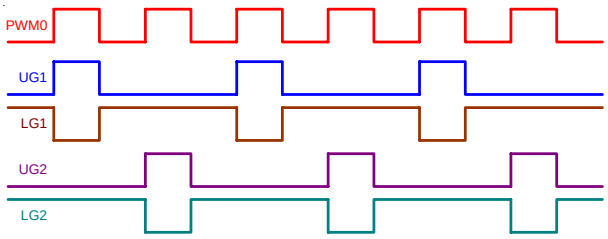


Figure 2. Phase Extension Module

The PWM0 pin voltage is kept around 1.46V by internalbias resistors when floating.

ISP0/1/2

The ISP0 is switched to ISP1 or ISP2 aternatively for DCR current sensing signal. The switching is controlled by the PEM according to the internal flip-flop status. The switching is also synchronized with the PWM distribution. ISP0 is connected to ISP1 when UG2 is turned off, and to ISP2 when UG1 is turned off.

Low Side Driver

The low-side driver is designed to drive a ground-referenced N-Channel MOSFET. The bias to the low-side driver is internally connected to V_{CC} supply and GND. The low-side driver output is out of phase with the PWM0 input when it is enabled. The low side driver is held low if the EN pin is pulled low or high-impedance at PWM0 pin.

High-Side Driver

The high-side driver is designed to drive a floating N-Channel MOSFET. The bias voltage to the high-side driver internally connected to BOOTx and PHx pins. An external bootstrap supply circuit that is connected between BOOTx and PHx pins provides the bias current for the high-side gate driver. The bootstrap capacitor C_{BOOT} is charged to V_{CC} when PHx pin is grounded by turning on the low-side MOSFET. The PHx raises to V_{IN} + V_{CC} when the high-side MOSFET is turned on, forcing the BOOT pin voltage to VIN + VCC that provides voltage to hold the high-side MOSFET on.

The high-side gate driver output is in phase with the PWM0 input when it is enabled. The high-side driver is held low if the EN pin is pulled low or high-impedance at PWM0 pin.

Adaptive Shoot Through Protection

The adaptive shoot-through circuit prevents the high-side and low-side MOSFETs from being ON simultaneously and conducting destructive large current. It is done by turning on one MOSFET only after the other MOSFET is off already with adequately delay time.

At the high-side off edge, UGx and PHx voltages are monitored for anti-shoot- through protection. The uP1961S will not begin to output low-side driver high until both (V_{UGx} -V_{PHx}) and V_{PHx} are lower than 1.2V, making sure the high-side MOSFET is turned off completely.

At the low-side off edge, LGx voltage is monitored for anti-shoot-through protection. The uP1961S will not begin to output high-side driver high until V_{LGx} is lower than 1.2V, making sure the low-side MOSFET is turned off completely.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCC ---------- -0.3V to +15V
BOOTx to PHx ---------- -0.3V to +15V
PHx to GND
- DC ---------- -0.7V to 15V
- < 200ns ---------- -8V to 30V

BOOTx to GND
- DC ---------- -0.3V to VCC + 15V
- < 200ns ---------- -0.3V to 42V

UGx to PHx
- DC ---------- -0.3V to (BOOTx - PHx +0.3V)
- <200ns ---------- -5V to (BOOTx - PHx + 0.3V)

LGx to GND
- DC ---------- -0.3V to + (VCC + 0.3V)
- <200ns ---------- -5V to VCC + 0.3V

PWM0 ---------- -0.3V to +6V
EN ---------- -0.3V to (VCC + 0.3)V
ISP0 to GND, ISP1 to GND, ISP2 to GND ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
- WQFN3x3 - 16L θ_{JA} ---------- 68°C/W
- WQFN3x3 - 16L θ_{JC} ---------- 6°C/W

Power Dissipation, P_D @ T_A = 25°C
- WQFN3x3 - 16L ---------- 1.47W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC} ---------- +10.8V to 13.2V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guarantee by Design.

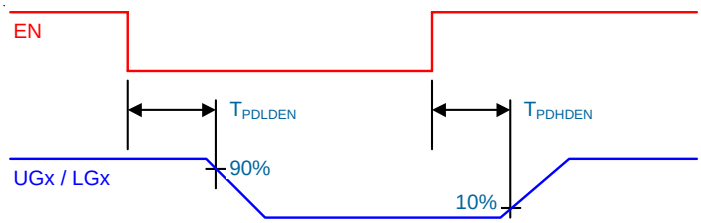
Electrical Characteristics

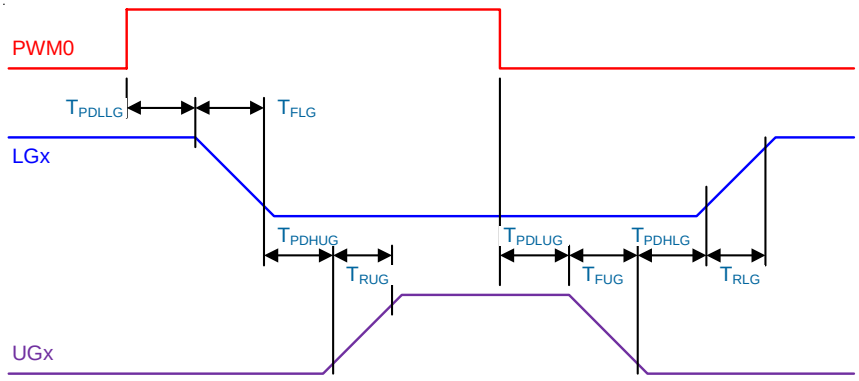
(V_{CC}=12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Input Voltage	V_{CC}		10.8	--	13.2	V
Supply Input Current	I_{CC}	PWM0 = EN = 0V	--	3	5	mA
VCC POR Threshold	V_{CCRTH}	V_{CC} rising	--	4.0	4.4	V
VCC POR Hysteresis	V_{CCHYS}		--	0.2	--	V
PWM0 Input						
Input High Threshold	$PWM0_{RTH}$		2.3	2.5	2.7	V
Input Low Threshold	$PWM0_{FTH}$		0.5	0.7	0.9	V
PWM0 Floating Voltage	$PWM0_{FLT}$		--	1.6	--	V
PWM0 Input Current	I_{PWM}	EN = 12V, PWM0 = 0V	-420	-280	-140	uA
		EN = 12V, PWM0 = 3.3V	--	1	1.5	mA
		EN = 0V, PWM0 = 3.3V	--	--	0.5	uA
Enable Control Input, EN						
Input High	EN_H		2.0	--	--	V
Input Low	EN_L		--	--	0.6	V
EN Input Current	I_{EN}	EN = 0V to 5V	-1	--	1	uA
Propogation Delay Time	T_{PDHDEN}		0.6	--	10	us
	T_{PDLDEN}		--	75	90	ns
High Side Driver						
Output Resistance, Sourcing	R_{H_SRC}	V_{BOOT} - V_{PH} = 12V, I_{UG} = -80mA	–	1.8	3.0	Ω
Output Resistance, Sinking	R_{H_SNK}	V_{BOOT} - V_{PH} = 12V, I_{UG} = 80mA	–	1.0	2.5	Ω
Output Rising Time	T_{RUGA}	V_{BOOT} - V_{PH} = 12V	–	35	45	ns
Output Falling Time	T_{FUG}	V_{BOOT} - V_{PH} = 12V	–	20	30	ns
Propogation Delay Time	T_{PDHUG}	V_{BOOT} - V_{PH} = 12V, C_{LOAD} = 3nF	–	40	65	ns
	T_{PDLUG}	V_{BOOT} - V_{PH} = 12V , C_{LOAD} = 3nF	–	20	35	ns
Low Side Driver						
Output Resistance, Sourcing	R_{L_SRC}	V_{CC} = 12V, I_{LG} = -80mA	–	1.8	3.0	Ω
Output Resistance, Sinking	R_{L_SNK}	V_{CC} = 12V, I_{LG} = 80mA	–	1.0	2.5	Ω
Output Rising Time	T_{RLG}	V_{CC} = 12V	–	35	45	ns
Output Falling Time	T_{FLG}	V_{CC} = 12V	–	20	35	ns
Propogation Delay Time	T_{PDHLG}	V_{CC} = 12V, C_{LOAD} = 3nF	–	40	65	ns
	T_{PDLLG}	V_{CC} = 12V, C_{LOAD} = 3nF	–	20	35	ns

Electrical Characteristics

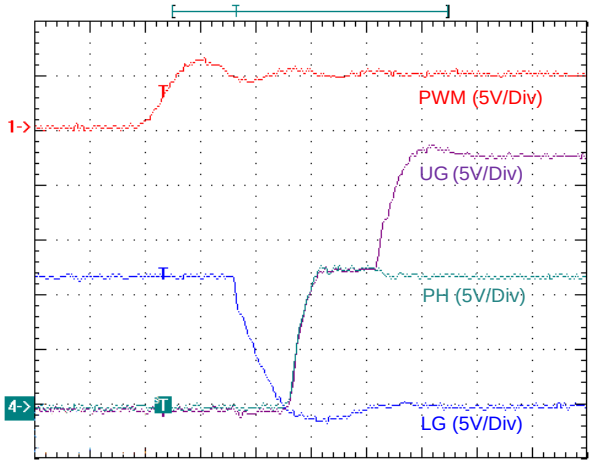
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Analog Switch						
Output Resistance	R_{ISP0_ON}	ISP1/2 Voltage = 0	100	175	250	Ω
Off State Leakage Current	I_{ISP0_SNK}	Output open, $V_{ISP1/2}$ = -0.3V to Vcc+0.3V (Note 5)	-5	0	5	nA
Break-Before-Make Delay	T_{BBM}	(Note 5)	--	15	20	ns
Turn off Time	T_{OFF}		--	100	150	ns
Turn on Time	T_{ON}		--	100	150	ns





Typical Operation Characteristics

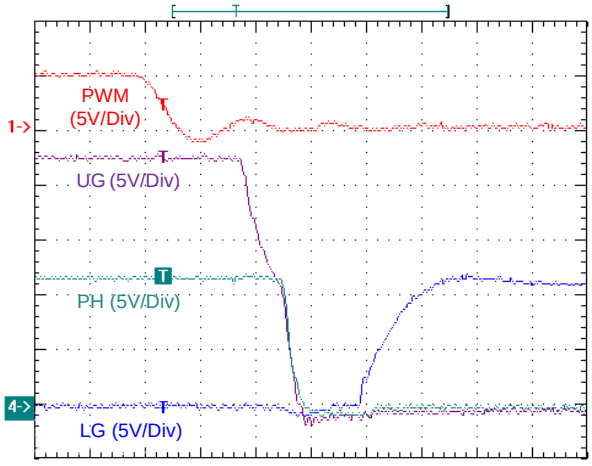
LG Falling to UG Rising Dead Time



Time：20ns/Div

V_{IN} = V_{CC} = 12V, Converter Load = 0A, RC Snubber R = 2.2Ω, C = 3.3nF,HSFET = QM3004*1, LSFET = QM3006*2

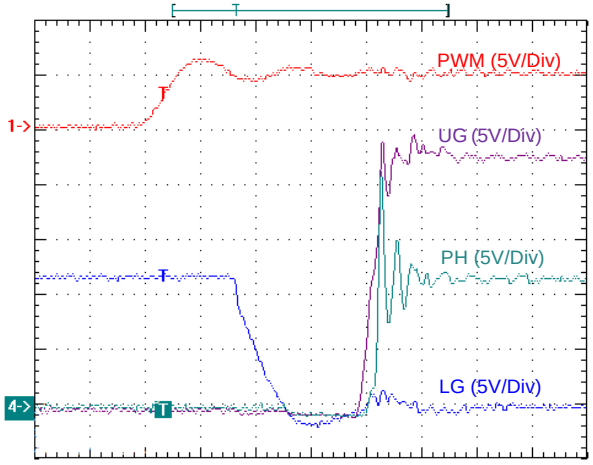
UG Falling to LG Rising Dead Time



Time：20ns/Div

V_{IN} = V_{CC} = 12V, Converter Load = 0A, RC Snubber R = 2.2Ω, C = 3.3nF, HSFET = QM3004*1, LSFET = QM3006*2

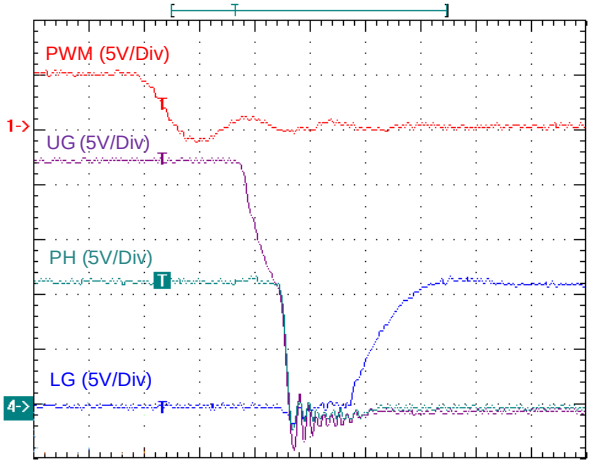
LG Falling to UG Rising Dead Time



Time：20ns/Div

V_{IN} = V_{CC} = 12V, Converter Load = 20A, RC Snubber R = 2.2Ω, C = 3.3nF, HSFET = QM3004*1, LSFET = QM3006*2

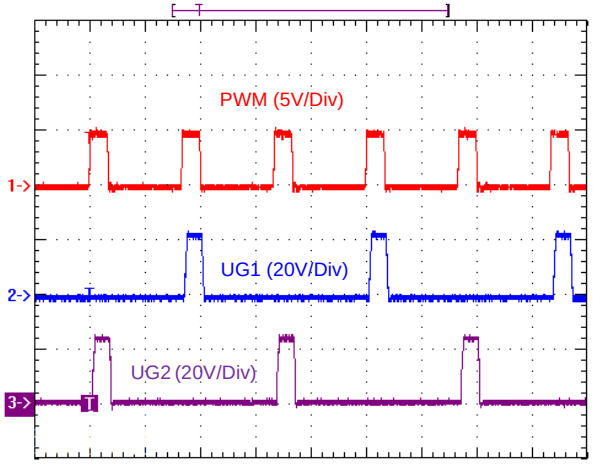
UG Falling to LG Rising Dead Time



Time：20ns/Div

V_{IN} = V_{CC} = 12V, Converter Load = 20A, RC Snubber R = 2.2Ω, C = 3.3nF, HSFET = QM3004*1, LSFET = QM3006*2

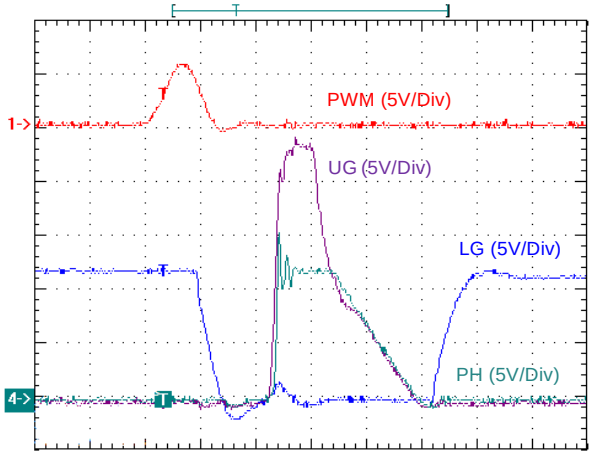
Phase Extension



Time：1us/Div

V_{IN} = V_{CC} = 12V, PWM = 600kHz, duty cycle = 20%, HSFET = QM3004*1, LSFET = QM3006*2

Short Pulse

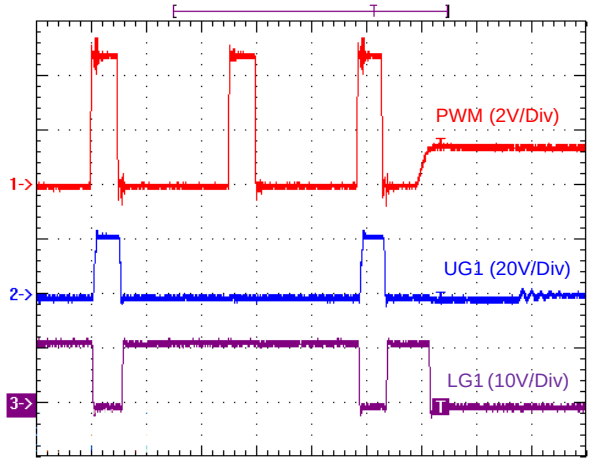


Time：40ns/Div

V_{IN} = V_{CC} = 12V, PWM = 30ns, Converter Load = 0A, HSFET = QM3004*1, LSFET = QM3006*2

Typical Operation Characteristics

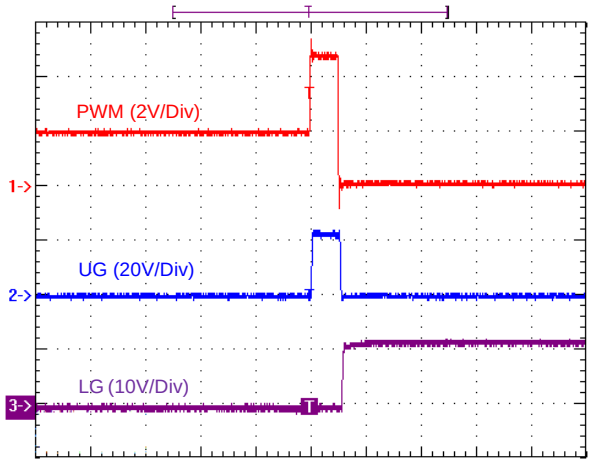
PWM Enter Tristate Operation



Time : 1us/Div

V_{IN} = V_{CC} = 12V, Converter Load = 0A,
HSFET = QM3004*1, LSFET = QM3006*2

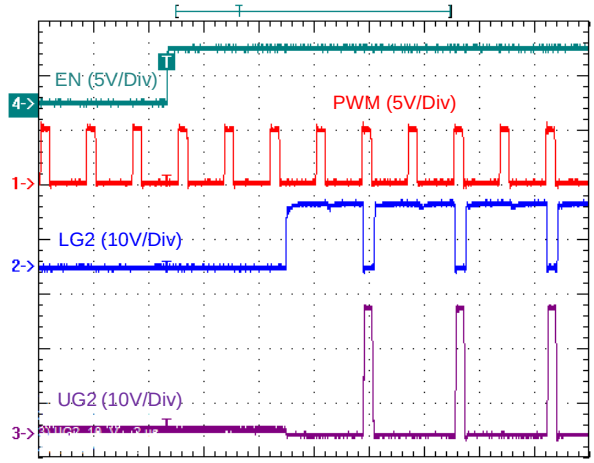
PWM Exit Tristate Operation



Time : 1us/Div

V_{IN} = V_{CC} = 12V, Converter Load = 0A,
HSFET = QM3004*1, LSFET = QM3006*2

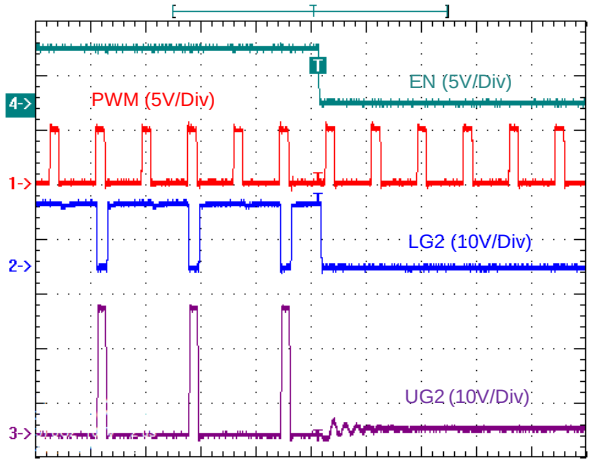
EN Go High Delay



Time : 2us/Div

V_{IN} = V_{CC} = 12V, PWM = 600kHz, duty cycle = 20%,
Converter Load = 5A
HSFET = QM3004*1, LSFET = QM3006*2

EN Go Low Delay

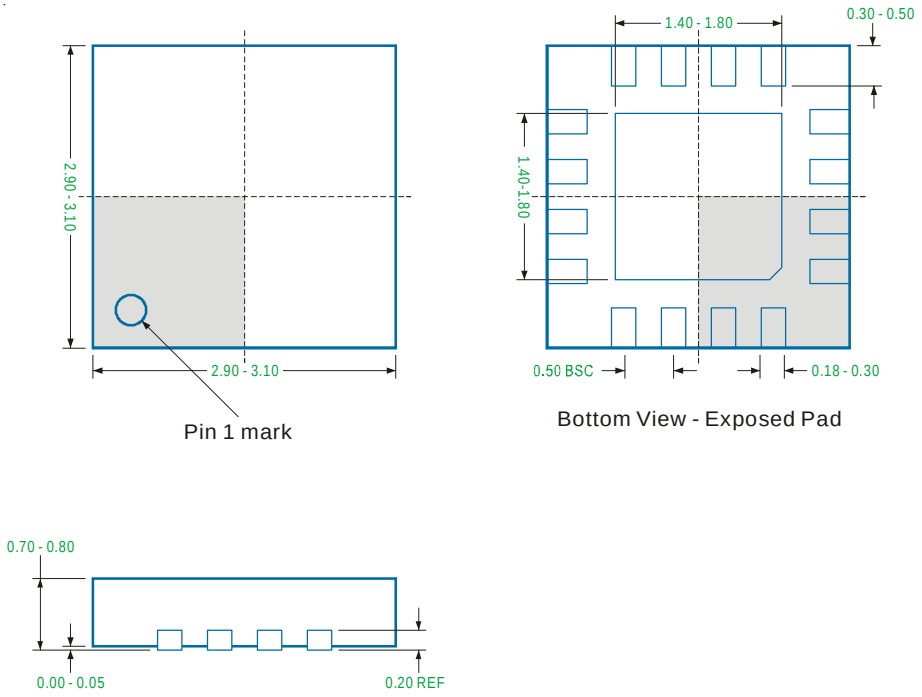


Time : 2us/Div

V_{IN} = V_{CC} = 12V, PWM = 600kHz, duty cycle = 20%,
Converter Load = 5A
HSFET = QM3004*1, LSFET = QM3006*2

Package Information

WQFN3x3 - 16L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Important Notice

uPI and its subsidiaries reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

uPI products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment. However, no responsibility is assumed by uPI or its subsidiaries for its use or application of any product or circuit; nor for any infringements of patents or other rights of third parties which may result from its use or application, including but not limited to any consequential or incidental damages. No uPI components are designed, intended or authorized for use in military, aerospace, automotive applications nor in systems for surgical implantation or life-sustaining. No license is granted by implication or otherwise under any patent or patent rights of uPI or its subsidiaries.

uPI Semiconductor Corp.

Headquarter
9F.,No.5, Taiyuan 1st St. Zhubei City,
Hsinchu Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888

Sales Branch Office
12F-5, No. 408, Ruiguang Rd. Neihu District,
Taipei Taiwan, R.O.C.
TEL : 886.2.8751.2062 FAX : 886.2.8751.5064