

# 12V MOSFET Drivers with Output Disable for Multi-Phase Synchronous-Rectified Buck Converter

## General Description

The uP1988 is a dual, high voltage MOSFET driver optimized for driving two N-channel MOSFETs in a synchronous-rectified buck converter. Each driver is capable of driving a 5000pF capacitive load with 30ns transition time. This device combined with uPI multi-phase buck PWM controller forms a complete core voltage regulator for advanced micro-processors.

The uP1988 features anti-shoot-through protection that prevents cross-conduction of the external MOSFET while maintains minimum deadtime for optimized efficiency.

This part has integrated bootstrap switch to help minimize the external component count. Both gate drives are turned off by pulling low EN pin or high-impedance at PWM pin, preventing rapid output capacitor discharge during system shutdown.

This device also supports supply input under voltage lockout. The uP1988 is available in a thermally enhanced WQFN3x3-16L package.

## Ordering Information

Order Number	Package	Top Marking
uP1988PQDD	WQFN3x3 - 16L	uP1988P

Note:

- (1) Please check the sample/production availability with uPI representatives.
- (2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

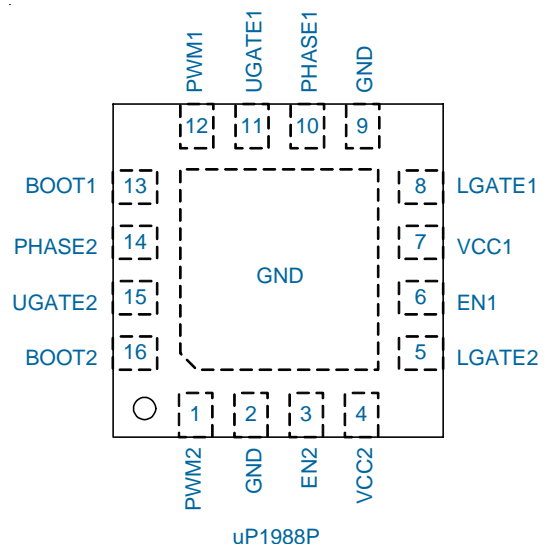
## Features

- All-In-One Synchronous Buck Drivers
- Integrated Bootstrap Switch
- Integrated Gate-to-Source Discharge Resistors
- Anti-Shoot-Through Protection Circuitry
- Tri-State Input for Bridge Shutdown
- Output Disable Control Turns Off both MOSFETs
- Under Voltage Lockout for Supply Input
- High-Side MOSFET Short Power on Protection
- Allow PWM Pin as Multi-Function Setting Application
- WQFN3x3-16L Package
- RoHS Compliant and Halogen Free

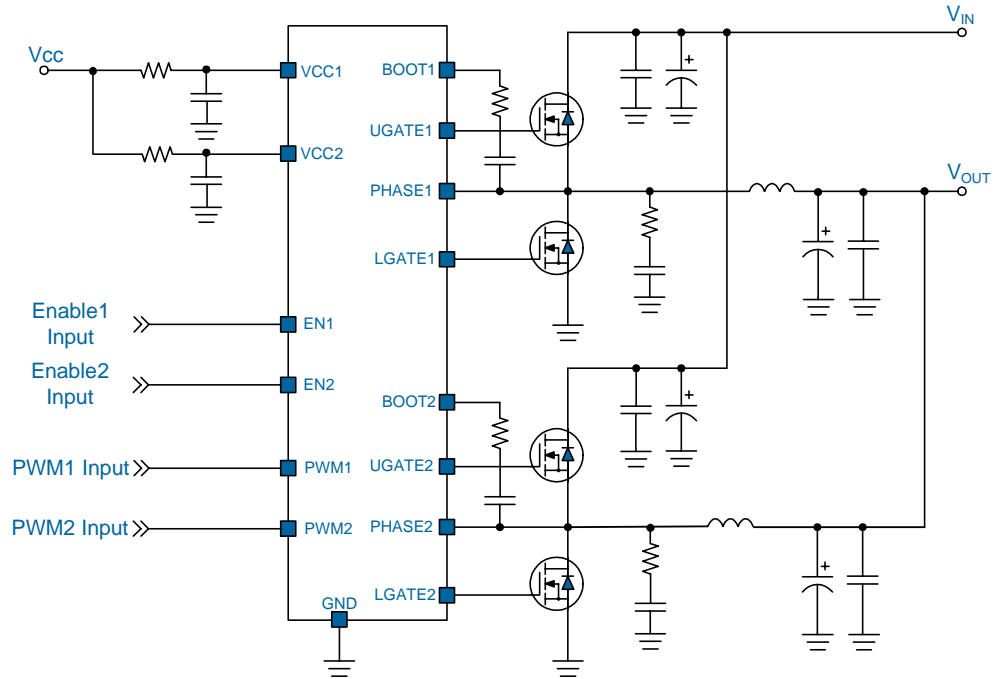
## Applications

- Desktop CPU Core Voltage Regulators
- High Frequency Low Profile DC/DC Converter
- High Current Low Voltage DC/DC Converter

## Pin Configuration



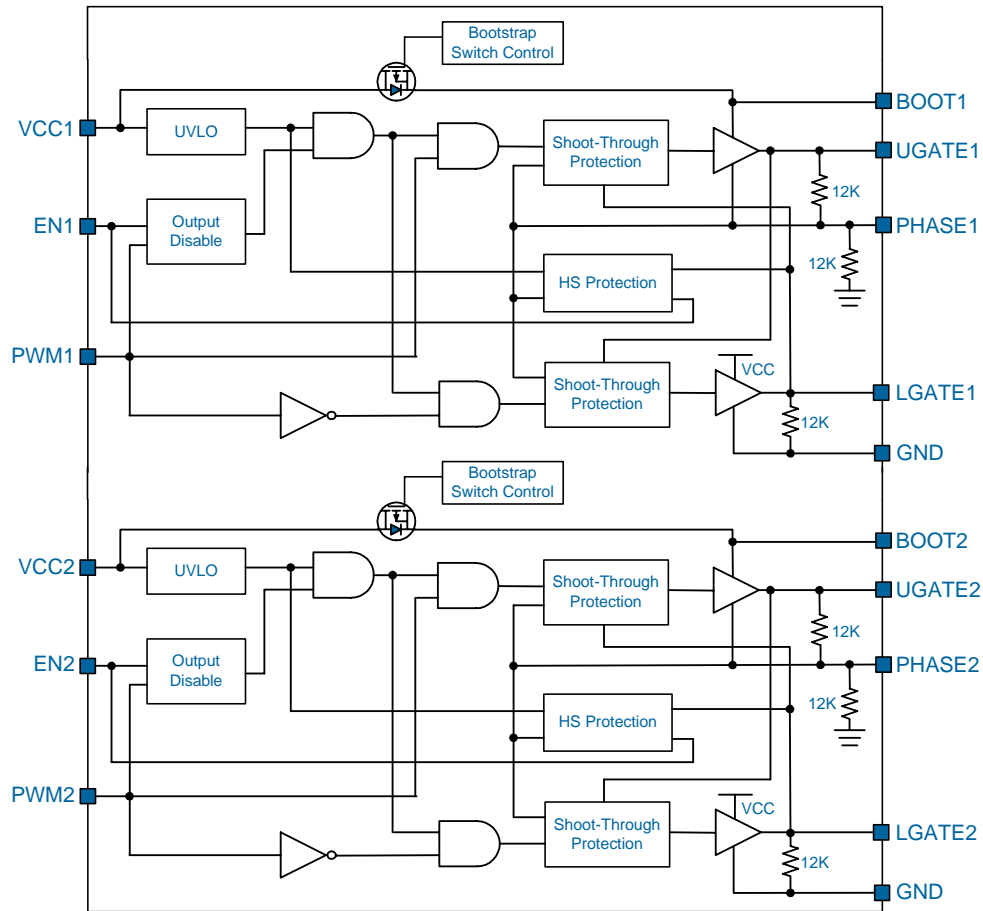
*Typical Application Circuit*



**Functional Pin Description**

Pin No.	Pin Name	Pin Function
1	PMW2	<b>PWMx Input.</b> This pin receives logic level input and controls the driver outputs. The PWMx pin is in high input impedance state if ENx input is low. When ENx input is high, the PWMx pin voltage will be pulled to tri-state by internal circuit. The resistor connected from PWMx pin to GND for PWM controller function setting must be greater than 15kΩ.
12	PMW1	
2,9	GND	<b>Ground for the IC.</b> All voltage levels are measured with respect to this pin.
3	EN2	<b>Enable Control for PWMx.</b> This pin disables normal operation and forces both UGATE <sub>x</sub> and LGATE <sub>x</sub> off when it is pulled low. This pin also controls the state of PWMx pin. When the ENx pin is pulled low, the PWMx pin is in high-input impedance state. There is no internal pull-up or pull-low mechanism to this pin.
6	EN1	
4	VCC2	<b>Supply Input for Embedded MOSFET Driverx.</b> Connect this pin to a 12V voltage source, and bypass this pin to GND with at least 1.0µF MLCC placed very close to the VCC <sub>x</sub> pin. VCC <sub>x</sub> is the supply input for the embedded MOSFET drivers. This pin supplies current for internal gate drivers.
7	VCC1	
5	LGATE2	<b>Lower Gate Driver for Phasex.</b> Connect this pin to the gate of lower MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when the lower MOSFET has been turned off.
8	LGATE1	
10	PHASE1	<b>Switch Node for Phase x.</b> This pin is the return path of upper gate driver for phase x. Connect a capacitor from this pin to BOOT <sub>x</sub> to form a bootstrap circuit for upper gate driver of the phase x.
14	PHASE2	
11	UGATE1	<b>Upper Gate Driver for Phase x.</b> Connect this pin to the gate of phase x upper MOSFET.
15	UGATE2	
13	BOOT1	<b>BOOT for Phase x.</b> Connect a capacitor from this pin to PHASE <sub>x</sub> to form a bootstrap circuit for upper gate driver of the phase x.
16	BOOT2	
Exposed Pad		<b>Ground for the IC.</b> The exposed pad should be well soldered to PCB for effective heat conduction.

**Functional Block Diagram**



**Enable Control**

The EN pin controls PWM pin state and the MOSFET gate driver output state. Logic input low to EN pin disables the gate drivers. Both UGATE and LGATE will be kept low, and PWM pin will be in high input impedance state. Logic input high to EN pin enables the gate drivers after a delay time  $T_{PDH DEN}$  as shown in Figure 1. During this time period the PWM pin stays at high input impedance state, both UGATE and LGATE outputs are kept low, and the internal control circuit does not respond to the PWM input voltage. After  $T_{PDH DEN}$  expires, both UGATE and LGATE begin to respond to the PWM input. This mechanism is specifically designed for uPI's PWM controller, which uses its PWM pin as a multi-functional pin.

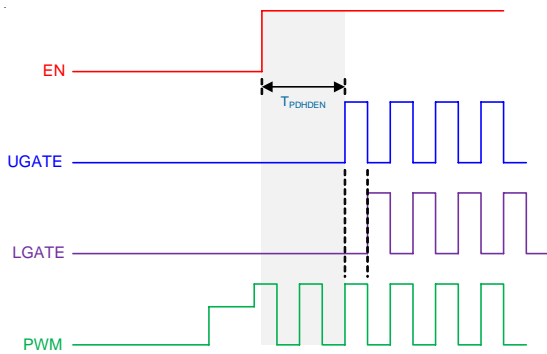


Figure 1. Enable Control, EN

**PWM Input**

The PWM pin is a tri-state input. Logic high turns on the high-side gate driver and turns off the low-side gate driver once the POR of VCC is granted and EN is kept high. Logic low turns off the high-side gate driver and turns on the low-side gate driver. High impedance input at PWM pin will keep both high-side and low-side gate drivers low and turns off both MOSFETs. The PWM pin voltage is kept around 1.6V by internal bias circuit when floating.

Refer to Figure 1, during  $T_{PDH DEN}$ , both UGATE and LGATE are kept low, the PWM pin is in high-input impedance state, and the PWM input will be ignored. For the PWM controller uses its PWM pin as a multi-functional pin, a resistor will be connected from PWM pin to GND to set parameter. Note that this resistor must be greater than 15kΩ. Lower resistor value will cause incorrect PWM voltage level at the PWM pin when the PWM controller output is in tri-state (high-impedance state).

**Low-Side Driver**

The low-side driver is designed to drive a ground referenced N-channel MOSFET. The bias to the low-side driver is internally connected to VCC supply and GND. The low-side driver output is out of phase with the PWM input when it is enabled. The low side driver is held low if the EN pin is pulled low or high-impedance at PWM pin.

**High-Side Driver**

The high-side driver is designed to drive a floating N-channel MOSFET. The bias voltage to the high-side driver is internally connected to BOOT and PHASE pins. An integrated bootstrap switch that is connected between BOOT and VCC pins provides the bias current for the high side gate driver.

The bootstrap capacitor  $C_{BOOT}$  is charged to  $V_{CC}$  when PHASE pin is grounded by turning on the low-side MOSFET. The PHASE rises to  $V_{IN}$  when the high-side MOSFET is turned on, forcing the BOOT pin voltage to  $V_{IN} + V_{CC}$  that provides voltage to hold the high-side MOSFET on.

The high-side gate driver output is in phase with the PWM input when it is enabled. The high-side driver is held low if the EN pin is pulled low or high-impedance at PWM pin.

**Shoot Through Protection**

The shoot-through circuit prevents the high-side and low-side MOSFETs from being turned on simultaneously and conducting destructive large current. It is done by turning on one MOSFET only after the other MOSFET is off already with adequate delay time.

At the high-side off edge, UGATE and PHASE voltages are monitored for anti-shoot-through protection. The low-side driver will not begin to output high until both  $(V_{UGATE} - V_{PHASE})$  and  $V_{PHASE}$  are lower than 1.2V, making sure the high-side MOSFET is turned off completely.

At the low-side off edge, LGATE voltage is monitored for anti-shoot-through protection. The high-side driver will not begin to output high until  $V_{LGATE}$  is lower than 1.2V, making sure the low-side MOSFET is turned off completely.

**HSFET Short Circuit Power on Protection**

The uP1988 provides a protection function to protect the load device of the converter when the converter is powered on with a damaged high-side MOSFET (its drain and source are shorted together). When VCC rises from 0V and across 4.3V, uP1988 starts to detect PHASE voltage. This detection ends when VCC rises above POR 8V (typical value). During this VCC voltage interval, if the PHASE voltage is greater than 2.2V (typical value), LGATE will go high to turn on the low-side MOSFET to pull down the PHASE voltage to protect the load device. The EN pin will be internally pulled low simultaneously to disable the other MOSFET drivers and the PWM controller. This high-side MOSFET short protection is a latch-off function and can only be reset by VCC re-POR.

Figure 2 illustrates the implementation of supply input to VCC if high-side MOSFET short circuit protection function is used. 5VSB and 12V are connected to VCC through a diode. Thus the VCC is supplied by 5VSB before system power on (before 12V is on) and the high-side MOSFET short circuit protection is activated.

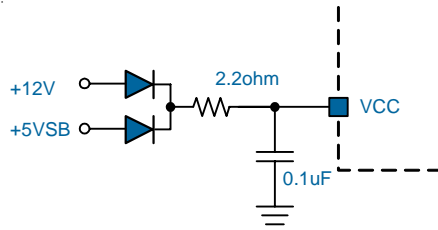


Figure 2. Supply Input to VCC

## Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCCx	-----	-0.3V to +15V
BOOTx to PHASEx	-----	-0.3V to +15V
PHASEx to GND		
DC	-----	-0.7V to +15V
< 200ns	-----	-8V to +30V
BOOTx to GND		
DC	-----	-0.3V to (VCC +15V)
< 200ns	-----	-0.3V to +42V
UGATEx to PHASEx		
DC	-----	-0.3V to (BOOT - PHASE +0.3V)
< 200ns	-----	-5V to (BOOT - PHASE +0.3V)
LGATEx to GND		
DC	-----	-0.3V to (VCC +0.3V)
< 200ns	-----	-5V to (VCC +0.3V)
PWMx	-----	-0.3V to +6V
ENx	-----	-0.3V to (VCC +0.3V)
Storage Temperature Range	-----	-65°C to +150°C
Junction Temperature	-----	150°C
Lead Temperature (Soldering, 10 sec)	-----	260°C
ESD Rating (Note 2)		
HBM (Human Body Mode)	-----	2kV
MM (Machine Mode)	-----	200V

## Thermal Information

Package Thermal Resistance (Note 3)

WQFN3x3 - 16L $\theta_{JA}$	-----	68°C/W
WQFN3x3 - 16L $\theta_{JC}$	-----	6°C/W
Power Dissipation, P <sub>D</sub> @ T <sub>A</sub> = 25°C		
WQFN3x3 - 16L	-----	1.47W

## Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range	-----	-40° to +125°C
Operating Ambient Temperature Range	-----	-40°C to +85°C
Supply Input Voltage, V <sub>CC</sub>	-----	10.8V to 13.2V

**Note 1.** Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.** Devices are ESD sensitive. Handling precaution recommended.

**Note 3.**  $\theta_{JA}$  is measured in the natural convection at T<sub>A</sub> = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Electrical Characteristics**

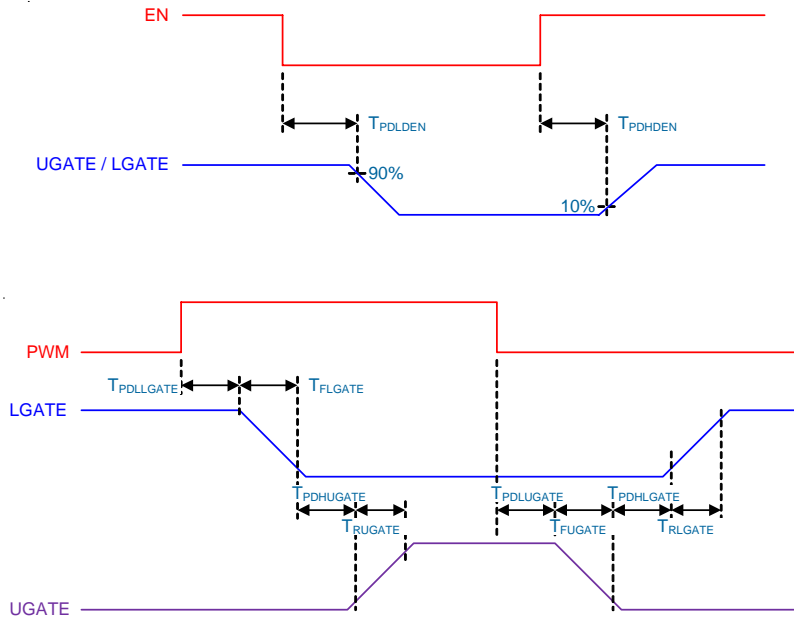
 (VCC = 12V, T<sub>A</sub> = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Supply Input</b>						
Supply Current	I <sub>CC</sub>	EN = 0V	--	1	3	mA
VCC POR Rising Threshold	V <sub>CCRTH</sub>	V <sub>CC</sub> Rising	7	8	9	V
VCC POR Falling Threshold	V <sub>CCHYS</sub>	V <sub>CC</sub> Falling	--	--	4.3	V
<b>PWM Input</b>						
Input High Level	PWM <sub>H</sub>		2.9	--	--	V
Input Low Level	PWM <sub>L</sub>		--	--	0.4	V
PWM Floating Voltage	PWM <sub>FLT</sub>		--	1.6	--	V
PWM Input Current	I <sub>PWM</sub>	PWM = 0V	-520	-280	-200	µA
		PWM = 3.3V	0.5	1	1.6	mA
		PWM = 5V	1	2	2.6	mA
<b>Enable Control</b>						
Input High	EN <sub>H</sub>		2	--	--	V
Input Low	EN <sub>L</sub>		--	--	0.6	V
Propagation Delay Time	T <sub>PDH DEN</sub>		1	2	3	µs
	T <sub>PDL DEN</sub>		60	80	100	ns
<b>Bootstrap Switch</b>						
On Resistance	R <sub>DS(ON)</sub>	Forward bias current = 1mA	--	40	--	Ω
<b>High Side Driver</b>						
Output Resistance, Sourcing	R <sub>H SRC</sub>	V <sub>BOOT</sub> - V <sub>PHASE</sub> = 12V, I <sub>UGATE</sub> = 80mA	--	2	4	Ω
Output Resistance, Sinking	R <sub>H SNK</sub>	V <sub>BOOT</sub> - V <sub>PHASE</sub> = 12V, I <sub>UGATE</sub> = -80mA	--	1	2	Ω
Output Rising Time	T <sub>RUGATE</sub>	V <sub>BOOT</sub> - V <sub>PHASE</sub> = 12V, C <sub>LOAD</sub> = 3nF	--	35	45	ns
Output Falling Time	T <sub>FUGATE</sub>	V <sub>BOOT</sub> - V <sub>PHASE</sub> = 12V, C <sub>LOAD</sub> = 3nF	--	20	30	ns
Propagation Delay Time	T <sub>PDHUG</sub>	V <sub>BOOT</sub> - V <sub>PHASE</sub> = 12V	--	40	65	ns
	T <sub>PDLUG</sub>	V <sub>BOOT</sub> - V <sub>PHASE</sub> = 12V	--	20	35	ns



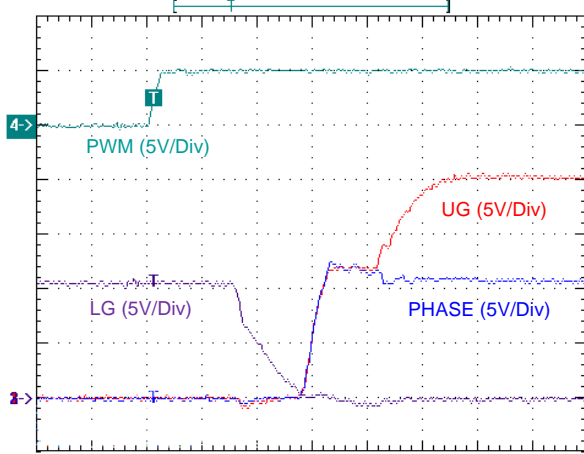
*Electrical Characteristics*

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Low Side Driver</b>						
Output Resistance, Sourcing	$R_{L\_SRC}$	$V_{CC} = 12V, I_{LGATE} = 80mA$	--	2	4	$\Omega$
Output Resistance, Sinking	$R_{L\_SNK}$	$V_{CC} = 12V, I_{LGATE} = -80mA$	--	0.8	1.6	$\Omega$
Output Rising Time	$T_{RLGATE}$	$V_{CC} = 12V, C_{LOAD} = 3nF$	--	35	45	ns
Output Falling Time	$T_{FLGATE}$	$V_{CC} = 12V, C_{LOAD} = 3nF$	--	20	30	ns
Propagation Delay Time	$T_{PDHLG}$	$V_{CC} = 12V$	--	40	65	ns
	$T_{PDLLG}$	$V_{CC} = 12V$	--	20	35	ns
<b>High Side MOSFET Short Protection</b>						
Trigger Level	$V_{HSPT}$	$V_{CC} = 6V, \text{measure PHASE voltage}$	2	2.2	2.4	V



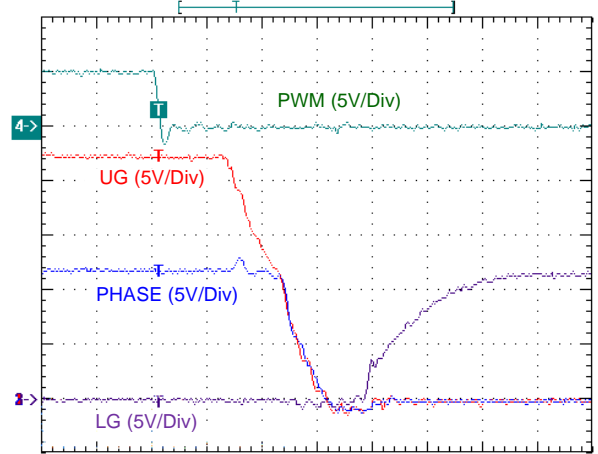
Typical Operation Characteristics

LG Falling to UG Rising Dead Time



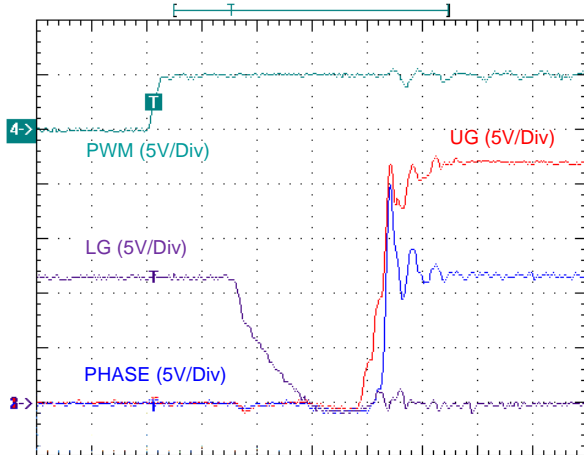
Time : 20ns/Div  
 $V_{IN}=12V, V_{CC}=12V$ , Converter Load = 0A, HSFET = QM3004\*2, LSFET=QM3006\*2, RC Snubber R=2.2Ω, C = 3.3nF

UG Falling to LG Rising Dead Time



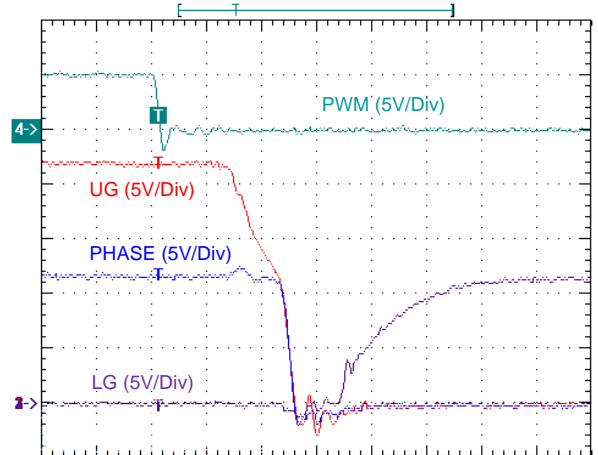
Time : 20ns/Div  
 $V_{IN}=12V, V_{CC}=12V$ , Converter Load = 0A, HSFET = QM3004\*2, LSFET=QM3006\*2, RC Snubber R=2.2Ω, C = 3.3nF

LG Falling to UG Rising Dead Time



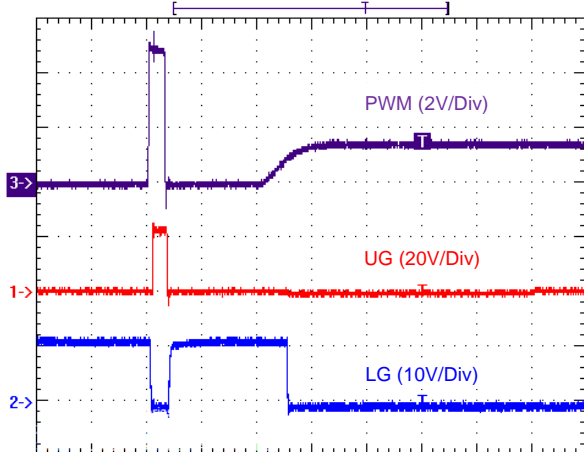
Time : 20ns/Div  
 $V_{IN}=12V, V_{CC}=12V$ , Converter Load = 20A, HSFET = QM3004\*2, LSFET=QM3006\*2, RC Snubber R=2.2Ω, C = 3.3nF

UG Falling to LG Rising Dead Time



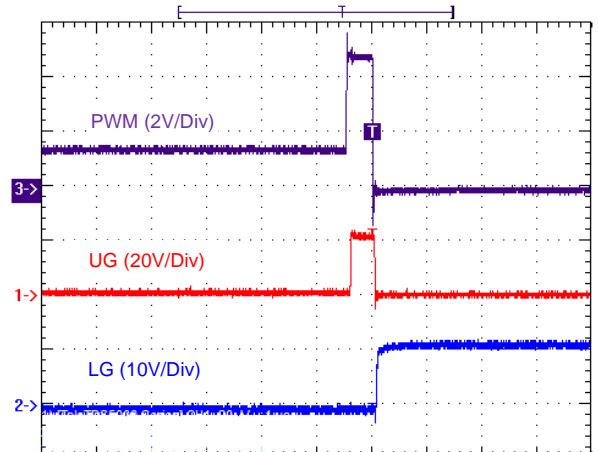
Time : 20ns/Div  
 $V_{IN}=12V, V_{CC}=12V$ , Converter Load = 20A, HSFET = QM3004\*2, LSFET=QM3006\*2, RC Snubber R=2.2Ω, C = 3.3nF

PWM Enter Tristate Operation



Time : 1µs/Div  
 $V_{IN}=12V, V_{CC}=12V$ , Converter Load = 0A, HSFET = QM3004\*2, LSFET=QM3006\*2

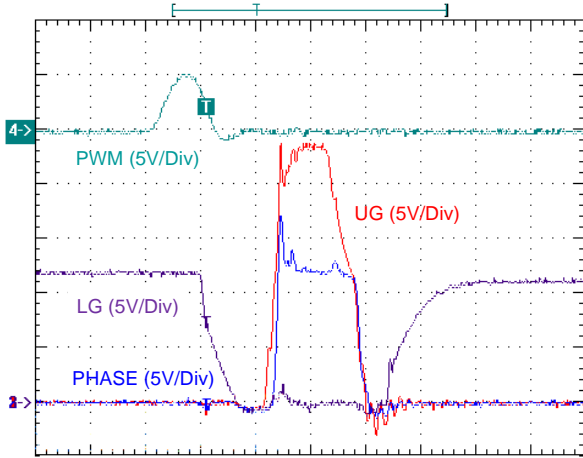
PWM Exit Tristate Operation



Time : 1µs/Div  
 $V_{IN}=12V, V_{CC}=12V$ , Converter Load = 0A, HSFET = QM3004\*2, LSFET=QM3006\*2

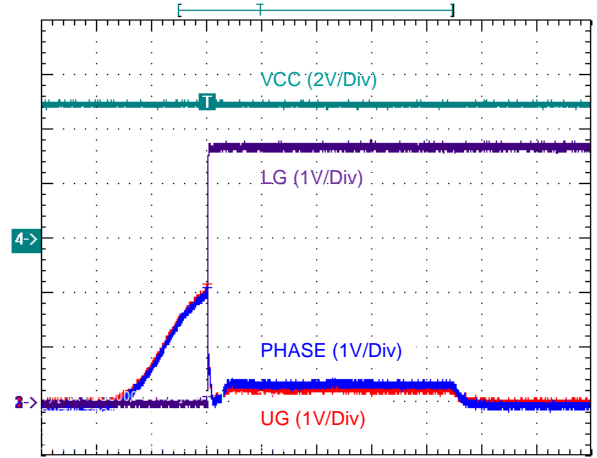
**Typical Operation Characteristics**

**Short Pulse**



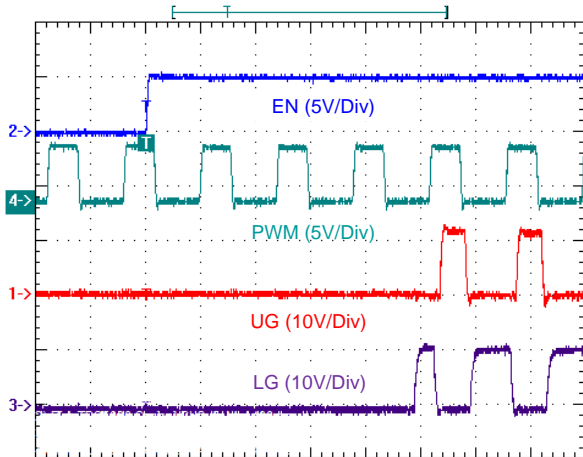
Time : 40ns/Div  
 $V_{IN}=12V, V_{CC}=12V$ , PWM=30ns, Converter Load = 5A,  
 HSFET = QM3004\*2, LSFET=QM3006\*2

**High-side MOSFET Short Protection**



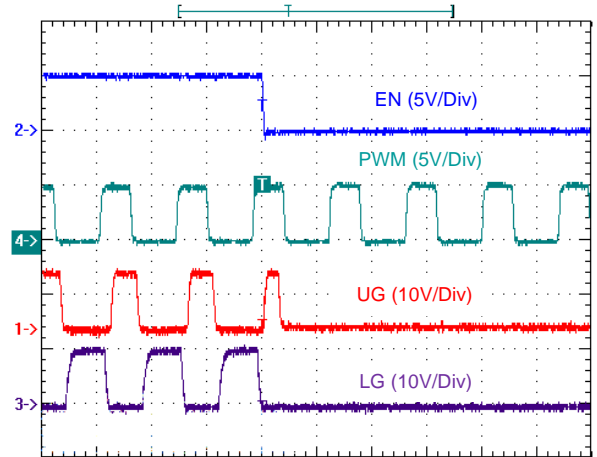
Time : 2ms/Div  
 Use ATX power,  $V_{IN}=12V, V_{CC}=12V$

**EN go High Delay**



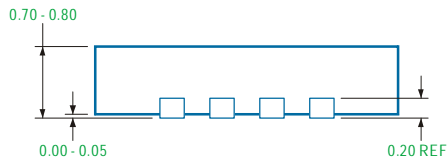
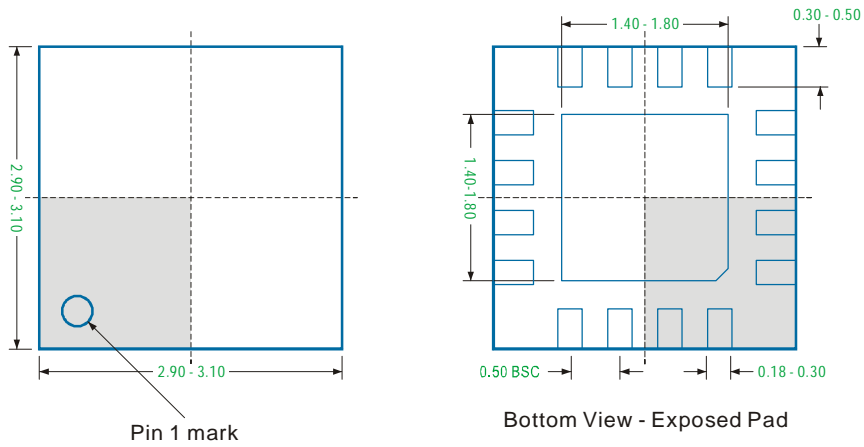
Time : 400ns/Div  
 $V_{CC} = 12V$ , PWM = 1.8MHz, D=40%,  
 HSFET = QM3004\*2, LSFET=QM3006\*2

**EN go Low Delay**



Time : 400ns/Div  
 $V_{CC} = 12V$ , PWM = 1.8MHz, D = 40%  
 HSFET = QM3004\*2, LSFET=QM3006\*2

WQFN3x3 - 16L



Note

1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

TYP: Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

## Important Notice

uPI and its subsidiaries reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

uPI products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment. However, no responsibility is assumed by uPI or its subsidiaries for its use or application of any product or circuit; nor for any infringements of patents or other rights of third parties which may result from its use or application, including but not limited to any consequential or incidental damages. No uPI components are designed, intended or authorized for use in military, aerospace, automotive applications nor in systems for surgical implantation or life-sustaining. No license is granted by implication or otherwise under any patent or patent rights of uPI or its subsidiaries.

COPYRIGHT (c) 2017, UPI SEMICONDUCTOR CORP.

### **uPI Semiconductor Corp.**

Headquarter  
9F., No.5, Taiyuan 1st St. Zhubei City,  
Hsinchu Taiwan, R.O.C.  
TEL : 886.3.560.1666 FAX : 886.3.560.1888

Sales Branch Office  
12F-5, No. 408, Ruiguang Rd. Neihu District,  
Taipei Taiwan, R.O.C.  
TEL : 886.2.8751.2062 FAX : 886.2.8751.5064