3 Phase Synchronous-Rectified Buck Contronller for Next Genenration CPU Core Power

General Description

The uP6207 is a multi-phase synchronous-rectified buck controller specifically designed to deliver high quality output voltage for high-performance microprocessors and graphic processors. The uP6207 integrates a 5V LDO regulator that enables it to work with a single 12V supply voltage. It also integrates bootstrapped drivers that support 12V + 12V driving capability.

The uP6207 provides programmable 2/3-phase operation. It also supports dynamic phase selection by PS1/2 pins that automatically switches to single/two phase operation at light load condition. The uP6207 supports both stand-alone and tracking mode operation. The output voltage is tightly regulated to local or external reference voltages.

The uP6207 extract phase current signals by $R_{DS(ON)}$ of low side switches for phase current balance. It senses the output current by DCR of output inductors for load line slope setting and over current protection. This yields both thermal balance and accurate load line adjustment.

The uP6207 includes programmable no-load offset and droop slope functions to adjust the output voltage as a function of the load current, optimally positioning it for a system transient.

Other features include accurate and reliable short-circuit protection, adjustable over current protection, and a delayed power OK output. This part is available in VQFN5x5 - 32L package.

Applications

- **Desktop PC Core Power Supplies**
- **Middle/High End Graphic Cards**
- **Low Output Voltage, High Power Density DC/DC Converters**
- **Voltage Regulator Modules**

Features

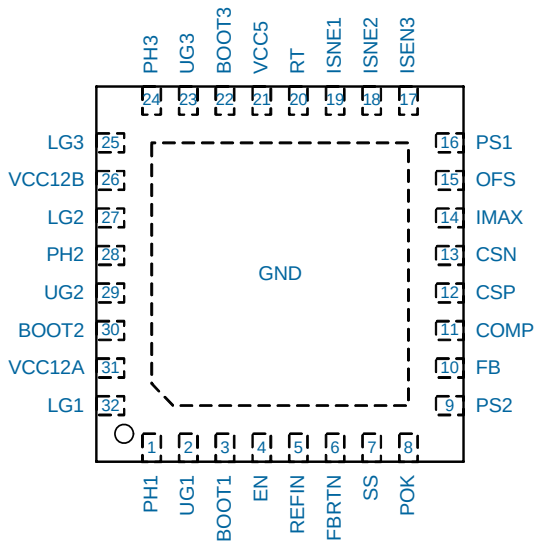
- **Interleaved Two/Three Phase Operation**
- **Programmable Dynamic Power Saving Mode Operation**
- **Simple Single-Loop Voltage-Mode Control**
- **Integrated 12V Bootstrapped Drivers with Internal Bootstrap Diode**
- **Lossless $R_{DS(ON)}$ Current Sensing for Current Balance**
- **Adjustable Operation Frequency form 50kHz to 1MHz Per Phase**
- **External Compensation**
- **Adjustable Over Current Protection**
- **Adjustable Soft Start**
- **VQFN5x5 -32L Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Ordering Information

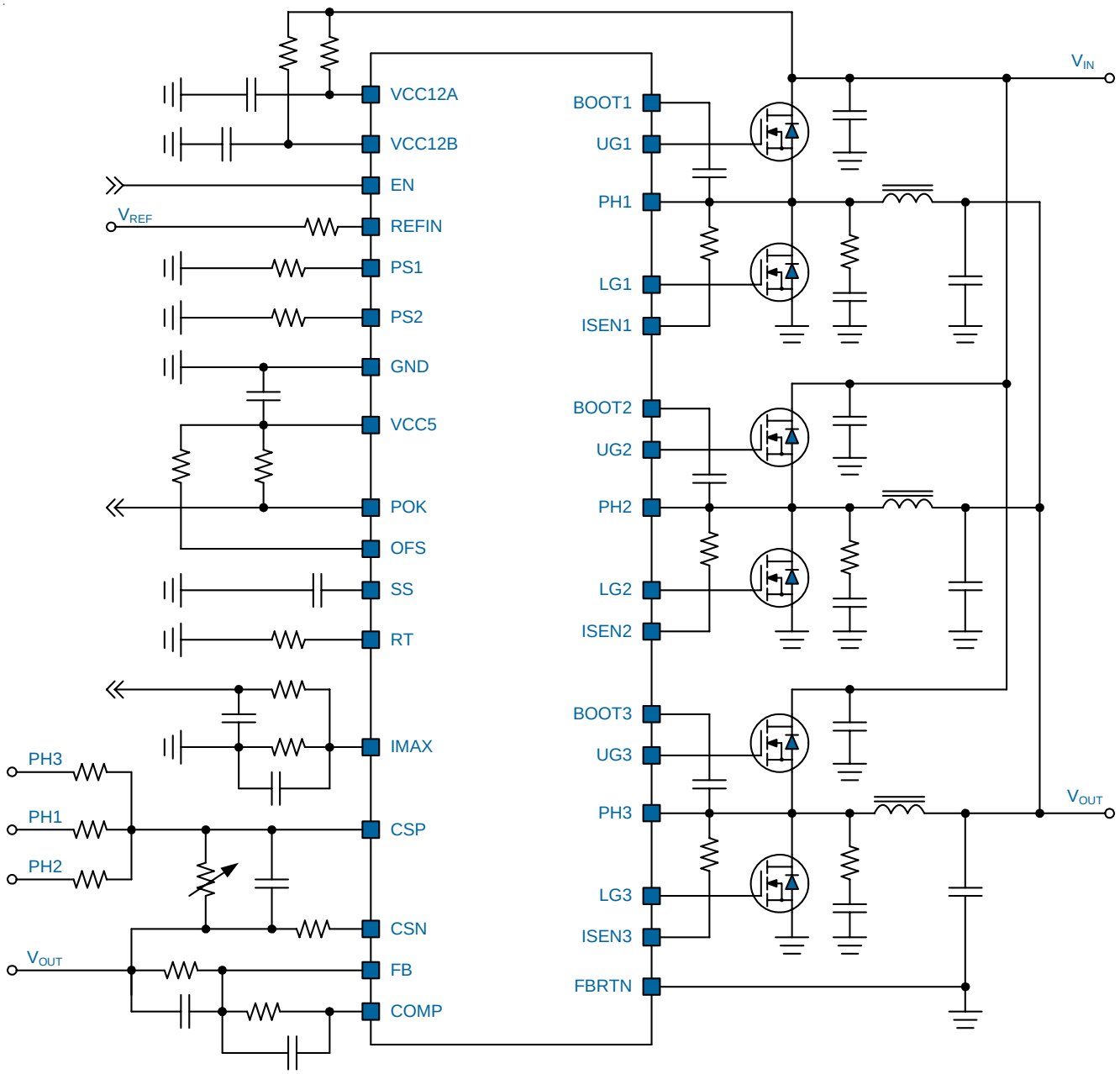
Order Number	Package Type	Remark
uP6207AQAI	VQFN5x5 - 32L	

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 and RoHS requirements. They are 100% matte tin (Sn) plating and suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



Typical Application Circuit



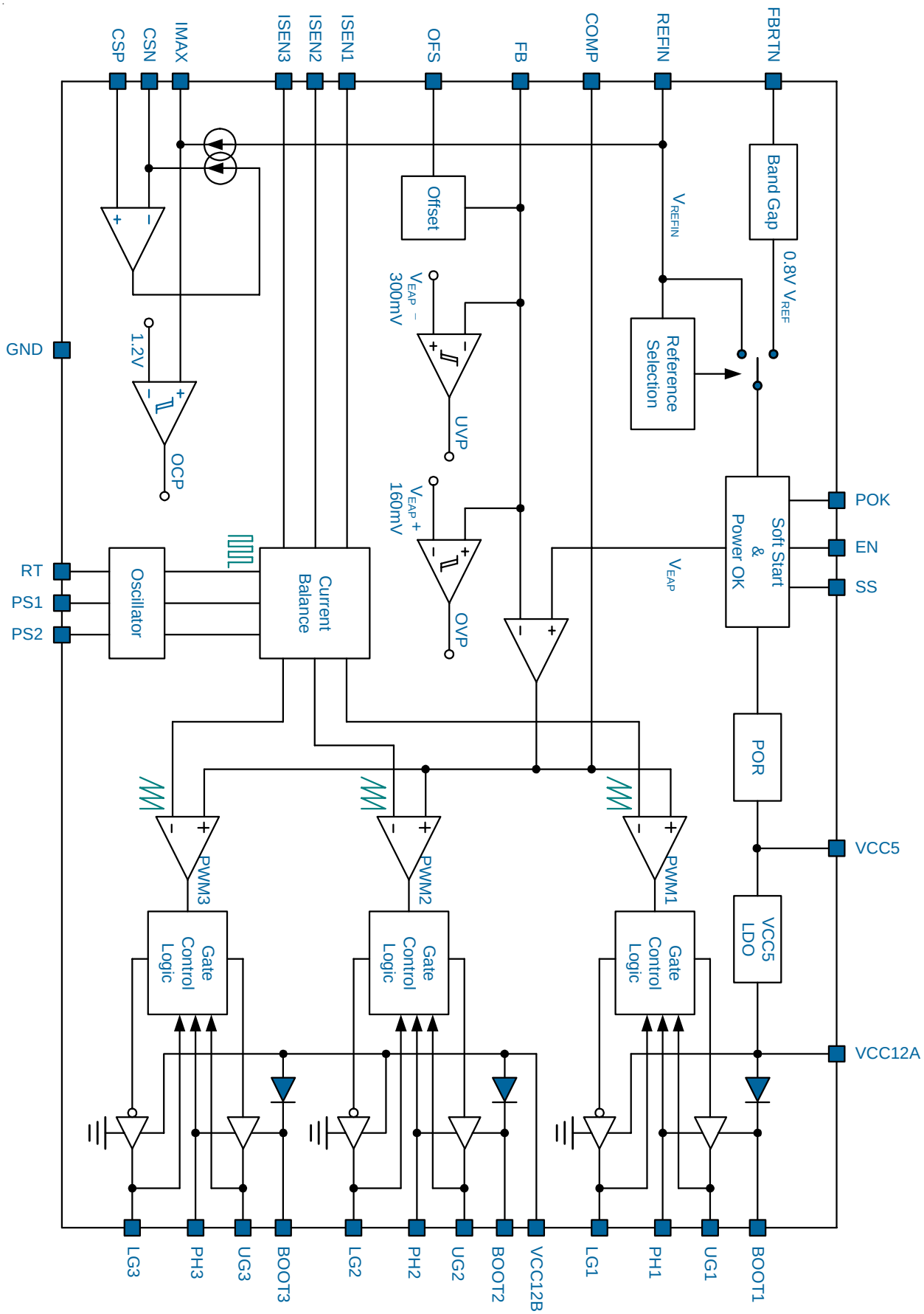
Functional Pin Description

No.	Name	Pin Function
1	PH1	**Phase Pin for Phase 1.** This pin is the return path of upper gate driver for phase 1. Connect a capacitor from this pin to BOOT1 to form a bootstrap circuit for upper gate driver of the phase 1.
2	UG1	**Upper Gate Driver for Phase 1.** Connect this pin the gate of phase 1 upper MOSFET.
3	BOOT1	**BOOT for Phase 1.** Connect a capacitor from this pin to PH1 to form a bootstrap circuit for upper gate driver of the phase 1.
4	EN	**Chip Enable.** Pulling this pin lower than 0.4V shuts down the device**.**
5	REFIN	**External Reference Input.** Connect this pin to an external reference voltage through a resistor. The resistor sets the load line slope.
6	FBRTN	**Return for the Reference Circuit.** Connect this to the ground point where output voltage is to be regulated.
7	SS	**Soft Start.** Connect a capacitor from this pin to GND to set the soft start time.
8	POK	**Power Good Indication.**
9	PS2	**Power Saving Mode Setting Input 2.** Connect a resistor from this pin to GND to set the phase reduction threshold level.
10	FB	**Feedback Pin.** This pin is the inverting input of the error amplifier.
11	COMP	**Compensation Output.** This pin is the output of the error amplifier
12	CSP	**Positive Input of the Current Sensing GM Amplifier.**
13	CSN	**Negative Input of the Current Sensing GM Amplifier.**
14	IMAX	**Output Current Indication.** Connect a resistor from this pin to GND to set the over current protection level.
15	OFS	**Zero Current Offset.** Connect a resistor form this pin to VCC5 or GND to set the output offset voltage.
16	PS1	**Power Saving Mode Setting Input 1.** Connect a resistor from this pin to ground to set the phase reduction threshold level.

Functional Pin Description

No.	Name	Pin Function
17	ISEN3	**Current Sensing for Phase 3.**
18	ISEN2	**Current Sensing for Phase 2.**
19	ISEN1	**Current Sensing for Phase 1.**
20	RT	**Switching Frequency Programming.** Connect a resistor from this pin to GND to set the switching frequency.
21	VCC5	**5V LDO Output.** This pin is the output pin of the internal 5V LDO.
22	BOOT3	**BOOT for Phase 3.** Connect a capacitor from this pin to PH3 to form a bootstrap circuit for upper gate driver of the phase 3.
23	UG3	**Upper Gate Driver for Phase 3.** Connect this pin the gate of phase 3 upper MOSFET.
24	PH3	**Phase Pin for Phase 3.** This pin is the return path of upper gate driver for phase 3. Connect a capacitor from this pin to BOOT3 to form a bootstrap circuit for upper gate driver of the phase 3.
25	LG3	**Lower Gate Driver for Phase 3.** Connect this pin to the gate of phase 3 lower MOSFET.
26	VCC12B	**Supply Input.** This pin supplies current for gate drivers and control circuits.
27	LG2	**Lower Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 lower MOSFET.
28	PH2	**Phase Pin for Phase 2.** This pin is the return path of upper gate driver for phase 2. Connect a capacitor from this pin to BOOT2 to form a bootstrap circuit for upper gate driver of the phase 2.
29	UG2	**Upper Gate Driver for Phase 2.** Connect this pin the gate of phase 2 upper MOSFET.
30	BOOT2	**BOOT for Phase 2.** Connect a capacitor from this pin to PH2 to form a bootstrap circuit for upper gate driver of the phase 2.
31	VCC12A	**Supply Input.** This pin supplies current for gate drivers and control circuits.
32	LG1	**Lower Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 lower MOSFET.
Exposed Pad PGND		**Power Ground.** Tie this pin to the ground island/plane through the lowest impedance connection available.

Functional Block Diagram



Functional Description

The uP6207 is a multi-phase synchronous-rectified buck controller specifically designed to deliver high quality output voltage for high-performance micro processors and graphic processors. The uP6207 integrates a 5V LDO regulator that enables it to work with a single 12V supply voltage. It also integrates bootstrapped drivers that support 12V + 12V driving capability.

The uP6207 provides programmable 2/3-phase operation. It also supports dynamic phase selection by PS1/2 pins that automatically switches to single phase operation at light load condition. The uP6207 supports both stand-alone and tracking mode operation. The output voltage is tightly regulated to local or external reference voltages.

The uP6207 extract phase current signals by $R_{DS(ON)}$ of low side switches for phase current balance. It senses the output current by DCR of output inductors for load line slope setting and over current protection. This yields both thermal balance and accurate load line adjustment.

The uP6207 includes programmable no-load offset and slope functions to adjust the output voltage as a function of the load current, optimally positioning it for a system transient.

Other features include accurate and reliable short-circuit protection, adjustable over current protection, and a delayed power OK output. This part is available in VQFN5x5 - 32L package.

Supply Input and Power on Reset

The uP6207 receives supply input from VCC12A/B pins to provide current to gate drivers. RC filters are required for locally bypassing the supply input pins. Since only the VCC12A pin is monitored for power on reset, **make sure the VCC12A/B pins are connected to the same voltage source externally.**

An internal 5V LDO regulator provides a regulated 5V voltage source to power the internal control circuit. Place a minimum 1uF ceramic capacitor physically near the VCC5 pin for locally bypassing the VCC5 voltage. The VCC5 voltage is continuously monitored for power on reset. The POR level is typical 4.2V at VCC5 rising.

Operation Phase Selection

The uP6207 supports 2/3 phase operation. PS2 status is checked at POR for operation phase selection. 2 phase operation is selected if PS2 < 0.1V at VCC5 POR. When operating at 2 phase, phase 3 is turned off and clock signals of phase1/2 are kept output of phase. When operating at 3 phase, clock signals are kept 120°C difference to each other. Leave gate drivers and ISEN3 floating when operating in 2 phase.

Reference Voltage Selection

The uP6207 supports both stand alone and tracking mode operation. REFIN voltage is checked at VCC5 POR for reference voltage selection as shown in Figure 1. The FB voltage is regulated to internal 0.8V reference voltage if V_{REFIN} is higher than 4V at VCC POR. Otherwise, the FB voltage is regulated to track V_{REFIN}. See the *Voltage Control Loop* section for details.

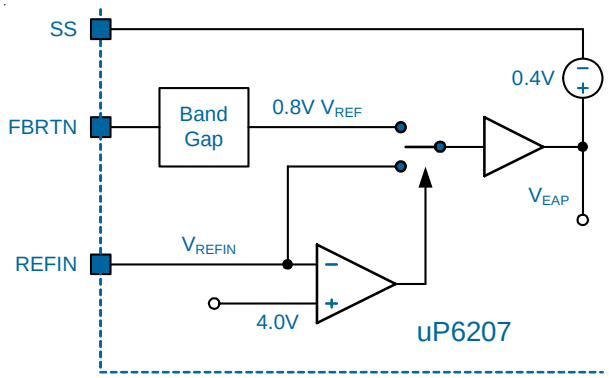


Figure 1. Reference Voltage Selection.

Oscillation Frequency Programming

A resistor R_{RT} connected to RT pin programs the oscillation frequency as:

$$f_{OSC} = \frac{10000}{R_{RT}(k\Omega)} \quad \text{(kHz)}$$

Figure 2 shows the relationship between oscillation frequency and R_{RT}.

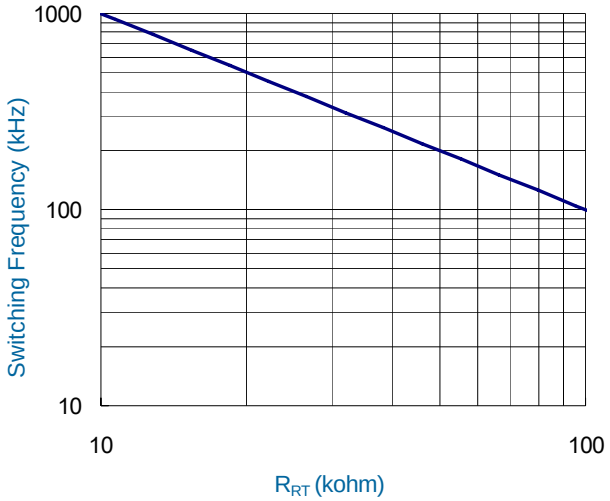


Figure 3. Switching Frequency vs. R_{RT}.

Functional Description

Output Current Sensing

Figure 3 illustrates the output current sensing block of the uP6207. The voltage V_{CS} across the current sensing capacitor C_{CS} can be expressed as:

$V_{CS} = I_{OUT} \times DCR/P$

if the following condition is true.

$P \times L / DCR = R_{CSP} \times C_{CS}$

where P is the phase number of operation (P = 2 for two phase operation, P = 3 for three phase operation), L is the output inductor of the buck converter, DCR is the parasitic resistance of the inductor, R_{CSP} and C_{CS} are the external RC network for current sensing.

The GM amplifier will source a current I_{AVG} to the CSN pin to let its inputs virtually short circuit.

$I_{AVG} \times R_{CSN} = V_{CS}$

Therefore the output current signal I_{AVG} can be expressed as:

$$I_{AVG} = \frac{I_{OUT} \times DCR}{P \times R_{CSN}}$$

The output current signal I_{AVG} is used as droop tuning and output over current protection. *Please see the related section for details.*

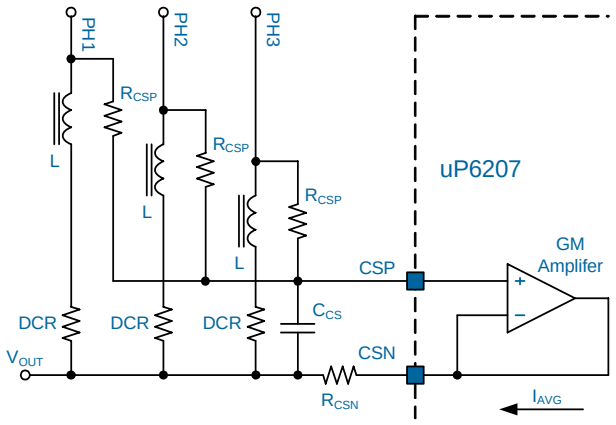


Figure 3. Output Current Sensing of uP6207.

Voltage Control Loop (External Reference Voltage)

Figure 4 illustrates the voltage control loop for external reference voltage of the uP6207. V_{FB} and V_{EAP} are negative and positive inputs of the Error Amplifier respectively. The EAP pin voltage is expressed as:

$V_{EAP} = V_{EXT} - K \times R_{DROOP} \times I_{AVG}$

where V_{EXT} is a slew rate limited voltage source, I_{AVG} is a current source proportional to output current, K a current mirror gain (K = 3 for three phase operation, K = 2 for two phase operation) and R_{DROOP} is an external resistor for adjusting load line slope.

The FB pin voltage V_{FB} is expressed as:

$V_{FB} = V_{OUT} - R_{FB} \times I_{OFS}$

where V_{OUT} is the output voltage, I_{OFS} is a current source for initial offset adjustment, R_{FB} is an external resistor.

The Error Amplifier modulates the COMP voltage V_{COMP} and the duty cycle of buck converter to force FB voltage V_{FB} follows V_{EAP}. Therefore, the output voltage will be:

$V_{OUT} = V_{EXT} - K \times R_{DROOP} \times I_{AVG} + R_{FB} \times I_{OFS}$

$$V_{OUT} = V_{EXT} - \frac{I_{OUT} \times DCR \times R_{DROOP}}{R_{CSN}} + R_{FB} \times I_{OFS}$$

Please see the related section for details.

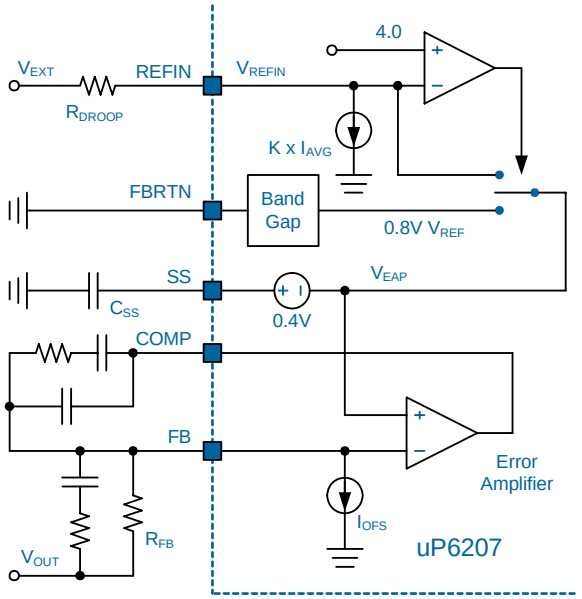


Figure 4. Voltage Control Loop for External Reference.

Please note the external reference voltage V_{EXT} changing slew rate should be limited to a safe level. A large step change of V_{EXT} should be avoid as it may result in large inrush current to charge and discharge the output capacitors and result in false triggering of OCP, UVP and OVP protection functions.

Voltage Control Loop (Internal Reference Voltage)

Figure 5 illustrates the voltage control loop for internal

Functional Description

reference voltage of the uP6207. V_{FB} and V_{EAP} are negative and positive inputs of the Error Amplifier respectively. The Error Amplifier modulates the COMP voltage V_{COMP} and the duty cycle of buck converter to force FB voltage V_{FB} follows V_{EAP}.

V_{EAP} = 0.8V

Note that there is no droop function when internal reference voltage is selected.

$$V_{FB} = \frac{R_{FB2} \times V_{OUT} - I_{OFS} \times R_{FB1} \times R_{RFB2}}{R_{FB1} + R_{FB2}}$$

where V_{OUT} is the output voltage, I_{OFS} is a current source for initial offset adjustment, R_{FB1} and R_{FB2} are external resistor divider for voltage setting.

Therefore, the output voltage will be:

$$V_{OUT} = \frac{0.8V \times (R_{FB1} + R_{FB2}) + I_{OFS} \times R_{FB1} \times R_{FB2}}{R_{FB2}}$$

Please see the related section for details.

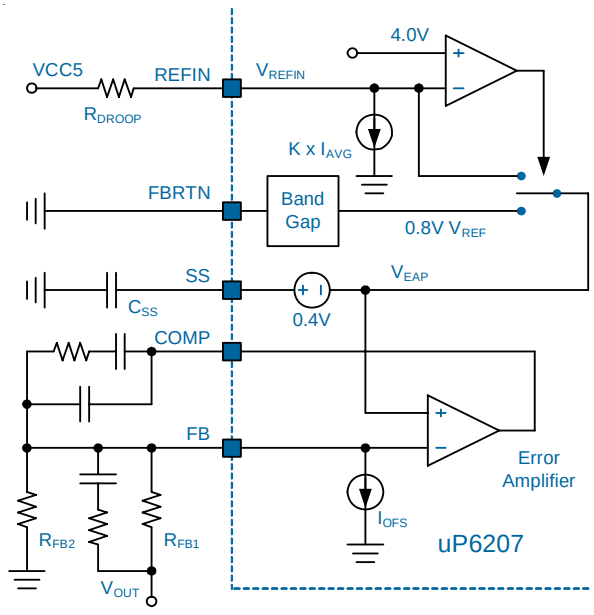


Figure 5. Voltage Control Loop for Internal Reference.

Initial Offset Adjustment

Connect a resistor R_{OFS} from OFS pin to VCC5 or GND to set the initial offset voltage. The OFS voltage V_{OFS} is V_{CC5} - 1.6V or 0.4V when connected to VCC5 or GND respectively. There the current source I_{OFS} can be calculated as:

I_{OFS} = 0.4V / R_{OFS} sourcing, R_{OFS} to GND, positive offset

I_{OFS} = 1.6V / R_{OFS} sinking, R_{OFS} to VCC5, negative offset.

The offset current source I_{OFS} is mirrored and injected to FB pin for initial offset adjustment. Please see the *Voltage Control Loop* section for details.

Soft Start and Power OK

Figure 6 illustrates the soft start cycle of uP6207. A capacitor C_{SS} connected to SS pin is used to adjust the soft start cycle.

A 10uA current source I_{SS} is used to charge/discharge C_{SS} during soft start and V_{REFIN} changes. Since V_{ss} is clamped to 0.4V higher than V_{EAP}, this limit the slew rate of V_{SS} and V_{EAP} during soft start and V_{REFIN} changes. This consequently limits the output voltage ramp up/down slew rate.

The uP6207 is POR and enabled at T0. There is a 800us time delay (T0 ~ T1) before the current source I_{SS} begins charging the C_{SS}. The non-inverting input V_{EAP} and output voltage V_{OUT} is kept zero during (T0 ~ T2). The V_{EAP} and V_{OU}T ramps up to target value during time delay TD2. The uP6207 inserts a time delay TD3 before assertion of power OK. The uP6207 asserts soft start end and set POK to high impedance status at T4.

Time periods are calculated as:

(T2 - T1) = 0.4V x C_{SS} / 10uA

TD1 = T2 - T0 = 800us + 0.4V x C_{SS} / 10uA

TD2 = V_{BOOT} x C_{SS} / 10uA = V_{EAP} x C_{SS} / 10uA

TD3 = (4.1V - V_{EAP}) / 10uA

where V_{BOOT} is the initial boot up reference voltage. V_{BOOT} = 0.8V for internal reference voltage, V_{BOOT} = V_{EXT} for external reference voltage.

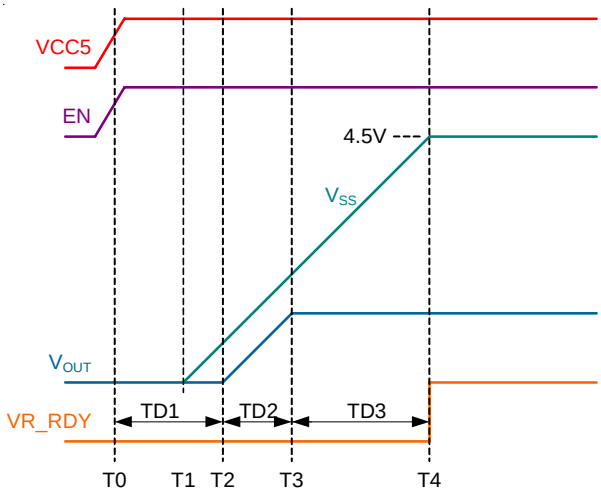


Figure 6. Soft Start Cycle of the uP6207.

Functional Description

Channel Current Sensing

The uP6207 extracts phase currents for current balance and over current protection by parasitic on-resistance of the lower switches when turn on as shown in Figure 7. The ISEN1/2/3 pins sense the corresponding phase current when the low side MOSFETs are turns on.

$I_{SENX} = ((I_{PHX} \times R_{DS(ON)}) + V_{DC}) / R_{SENX}$

where I_{SENX} is the sampled and held phase current signal, I_{PHX} is phase current, $R_{DS(ON)}$ is the on-resistance of the low side MOSFETs, and V_{DC} is an offset voltage for the current balance circuit. The current balance circuit increases the duty cycle of the phase whose phase current is smaller than others and decrease the duty cycle of the phase whose phase current is larger than others.

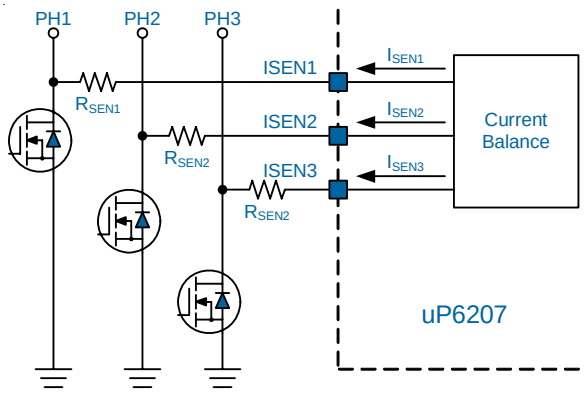


Figure 7. Phase Current Sensing and Current Balance.

Select R_{SEN} to set the current balance gain. A rule of thumb is to keep I_{SENX} = 5uA at rated output current.

Output Over Current Protection

I_{AVG} is mirrored and injected to the IMAX pin and create a voltage V_{IMAX} at IMAX pin.

$V_{IMAX} = K \times R_{IMAX} \times I_{AVG} = R_{IMAX} \times I_{OUT} \times DCR / R_{CSN}$

The over current protection is activated and shuts down the uP6207 if the IMAX voltage is higher than 1.2V.

Output Over Voltage Protection

The OVP is activated and turns on the low side MOSFETs if ($V_{FB} - V_{EAP}$) > 160mV

The over voltage protection is latch-off and can only be reset by POR or toggling the EN pin.

Under Voltage Protection

The under voltage protection is activated if FB voltage V_{FB} is 300mV lower than the V_{EAP}. UVP turns off and latches the uP6207.

Power Saving Mode and Automatic Phase Reduction

The uP6207 sources a 10uA current source out of PS1 and PS2 pins. Connecting resistors R_{PS1} and R_{PS2} at PS1 and PS2 pins creates voltage levels V_{PS1} and V_{PS2} for power saving mode operation.

$V_{PS1} = 10uA \times R_{PS1}$

$V_{PS1} = 10uA \times R_{PS1}$

Table 1 shows the operation phase of uP6207 according to V_{IMAX}, V_{PS1}, V_{PS2}. Take V_{PS1} = 0.2V, V_{PS2} = 0.3V and V_{IMAX} = 0.25V for example, the uP6207 turns off phase 3 and operates the converter in 2-phase. Note that the uP6207 do not reset the clock sequence during dynamic phase reduction. Phase 1 and phase 2 still has 120° phase shift.

The automatic phase reduction reduces the switching and conduction losses at light load condition and enables high efficiency over a wide range of output current.

$R_{PS2} > R_{PS1}$ is recommended when programming the phase-reduction threshold level.

Table 1. Operation Phase Selection.

V_{PS1}	V_{PS2}	Operation Phase
> 0.8V	X	1/2/3
< V_{IMAX}	< 0.1V	1/2
> V_{IMAX}	< 0.1V	1
< V_{IMAX}	< V_{IMAX}	1/2/3
< V_{IMAX}	> V_{IMAX}	1/2
> V_{IMAX}	> V_{IMAX}	1

Absolute Maximum Rating

Supply Input Voltage, VCC12 (Note 1) ---------- -0.3V to +15V
PHx to GND
DC ---------- -1V to 15V
< 200ns ---------- -5V to 30V
BOOTx to PHx ---------- -0.3V to +15V
UGx to PHx ---------- -0.3V to (BOOTx - PHx +0.3V)
LGx ---------- -0.3V to + (VCC12 + 0.3V)
Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
VQFN5x5 - 32L θ_{JA} ---------- TBD
VQFN5x5 - 32L θ_{JC} ---------- TBD
Power Dissipation, P_D @ T_A = 25°C
VQFN5x5 - 32L ---------- TBD

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, $V_{CC12A/B}$ ---------- 10.8V to 13.2V

Electrical Characteristics

(VCC12A/B = 12V, VCC5 = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Input Voltage	V_{CC12}		10.8	--	13.2	V
Supply Current	I_{CC12}	UGx and LGx Open; Switching	--	5	--	mA
VCC12 POR Threshold	$V_{CC12RTH}$	V_{CC12} Rising.	7.0	8.0	9.0	V
VCC12 POR Hysteresis	$V_{CC12HYS}$		--	0.9	--	V
VCC5 Voltage Accuracy	V_{CC5}		5.3	--	5.7	V
VCC5 Maximum Output Current	I_{CC5}		20	--	--	mA
Soft Start						
Soft Start Current	I_{SS}	V_{SS} = 0V	9	10	11	uA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Enable Control						
Logic Low Threshold	V_{IL}		--	--	0.4	V
Logic High Threshold	V_{IH}		0.8	--	--	V
Oscillator						
Switching Frequency	f_{OSC}	R_{RT} = 33kΩ. 3-Phase Operation	270	300	330	kHz
		R_{RT} = 24kΩ. 3-Phase Operation	270	300	330	kHz
Adjustable Frequency Range			50	--	1000	kHz
Ramp Amplitude			--	4	--	V
Maximum Dury		2-Phase Operation	--	87	--	%
		3-Phase Operation	--	90	--	
RT Pin Voltage	V_{RT}		--	1	--	V
Reference Voltage and DAC						
Internal Reference Voltage			0.79	0.80	0.81	V
Output Voltage Accuracy		V_{REFIN} - V_{FB}, V_{REFIN} = 1.2V.	-10	--	10	mV
Reference Selection Threshold Level	V_{IL}	Select Intenal Reference Voltage	4.0	--	V_{CC5}	V
External Reference Voltage Range	V_{REFIN}		0.4	--	3.5	V
OFS Voltage		R_{OFS} = 10kΩ to VCC5. V_{CC5} - V_{OFS}	--	1.6	--	V
		R_{OFS} = 10kΩ to GND.	--	0.4	--	
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by Design	70	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF.	30	--	--	MHz
Slew Rate	SR	Guaranteed by Design	3	6	--	V/us
Trans-conductance	GM	R_{LOAD} = 20kΩ	1200	1600	--	uA/V
Maximum Current (Source & Sink)	I_{COMP}	V_{COMP} = 1.6V	300	360	--	uA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Sense						
Maximum Sourcing Current			100	--	--	uA
Input Offset Voltage			-3	--	3	mV
IMAX Current Mirror Accuracy		I_{IMAX}/I_{AVG} for three phase operation	--	300	--	%
		I_{IMAX}/I_{AVG} for two phase operation	--	200	--	%
Droop Current Mirror Accuracy		I_{DROOP}/I_{AVG} for three phase operation	--	300	--	%
		I_{DROOP}/I_{AVG} for two phase operation	--	200	--	%
Power Saving Mode						
PS1/PS2 Soucing Current	I_{PSX}	$R_{PS1} = R_{PS2} = 47k\Omega$	9	10	11	uA
Gate Drivers						
Upper Gate Source	I_{UG_SRC}	$V_{BOOT} - V_{UGATE} = 6V$	--	-2	--	A
Upper Gate Sink	R_{UG_SNK}	$V_{UGATE} - V_{PHASE} = 1V$	--	1	2	Ω
Lower Gate Source	I_{LG_SRC}	$V_{CC} - V_{LGATE} = 6V$	--	-2	--	A
Lower Gate Sink	R_{LG_SNK}	$V_{LGATE} = 1V$	--	0.8	1.6	Ω
Dead Time	T_{DT}		--	30	--	ns
Protection						
Total Curren Protection Threshold	V_{IMAX}		--	1.2	--	V
FB Over Voltage Protection		$V_{FB} - V_{EAP}$	--	160	--	mV
FB Under Voltage Protection		$V_{FB} - V_{EAP}$	--	-300	--	mV
Over Temperature Protection Threshold			--	160	--	°C
Over Temperature Protection Hysteresis			--	20	--	°C
Power Sequence						
POK Sinking Capability	V_{POK}	$I_{POK} = 4mA$.	--	0.05	0.2	V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

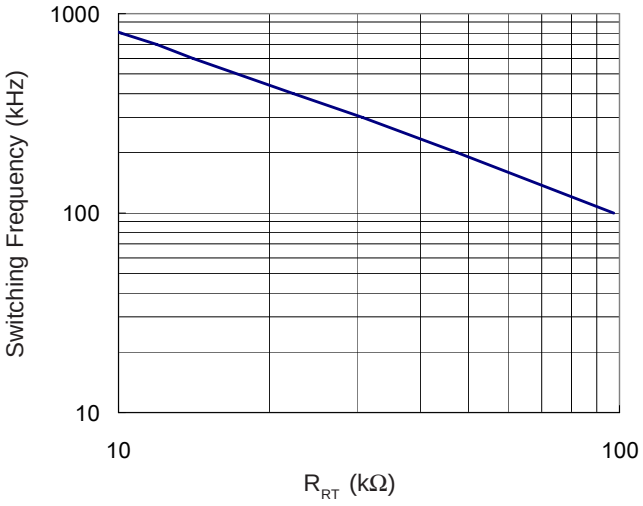
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

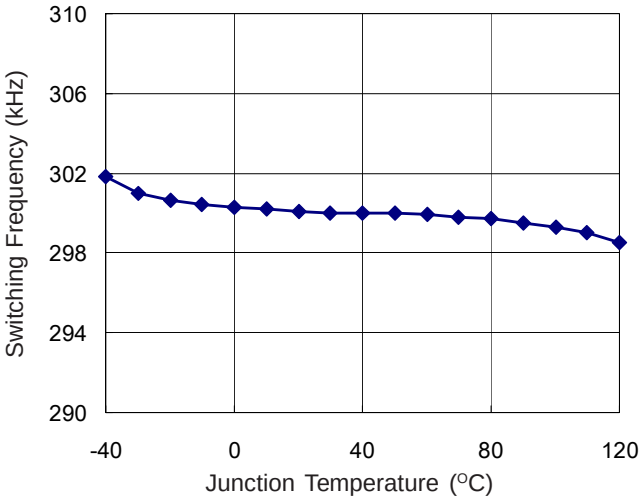
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operation Characteristics

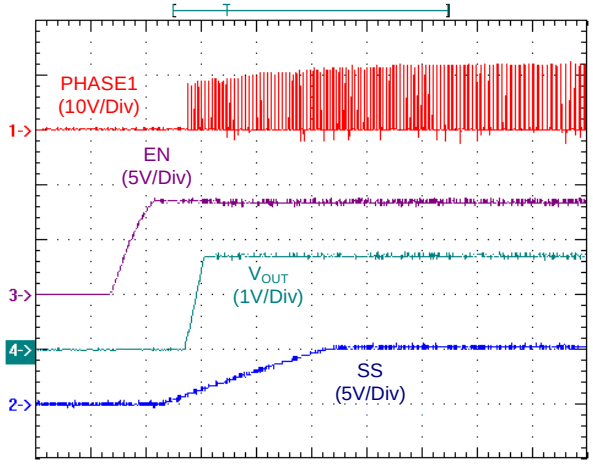
Switching Requency vs. R_{RT}



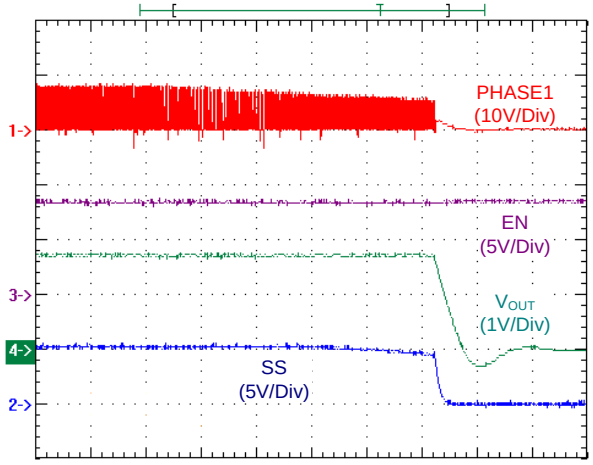
Switching Frequency vs. Temperature



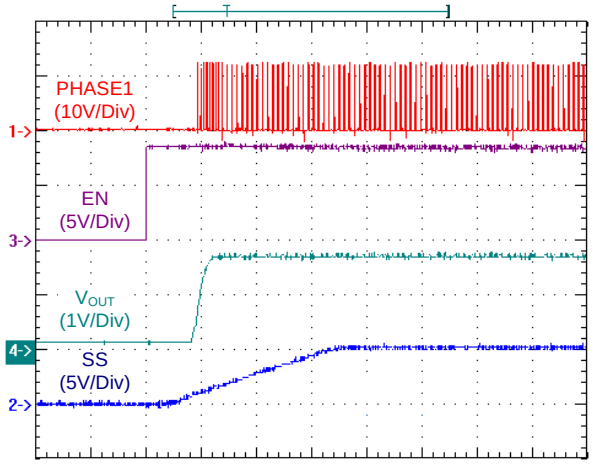
Power On Waveforms



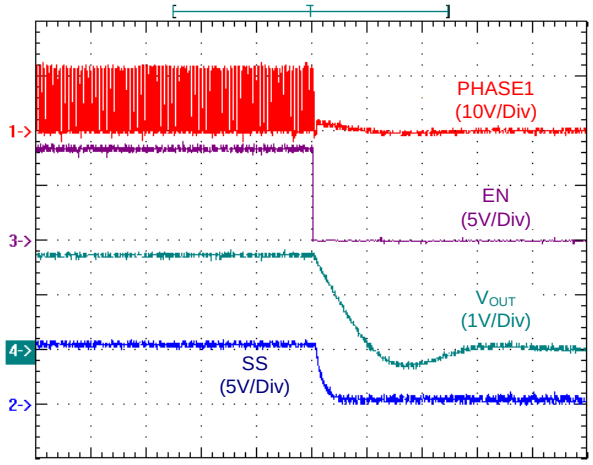
Power Off Waveforms



Turn On Waveforms

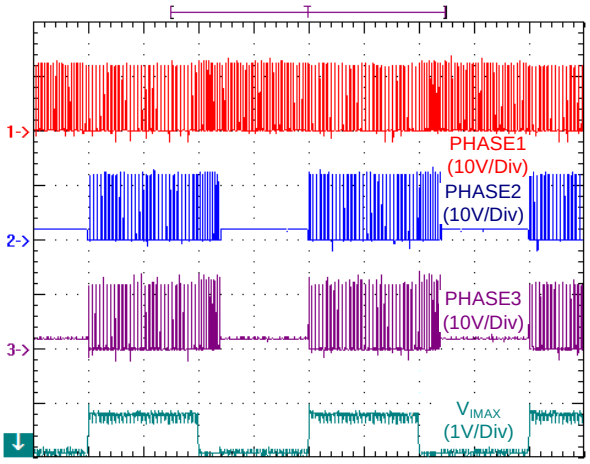


Turn Off Waveforms



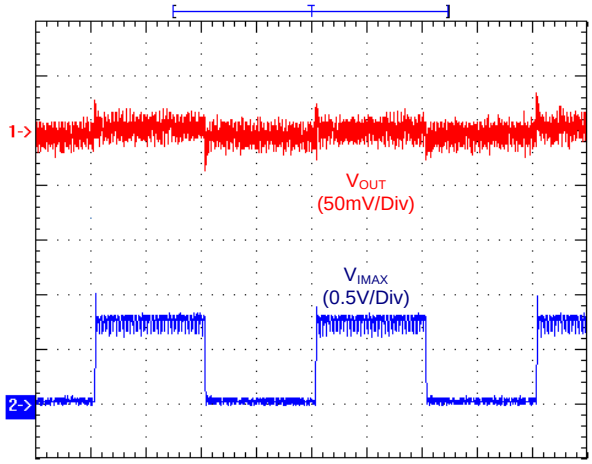
Typical Operation Characteristics

Automatic PSI Operation



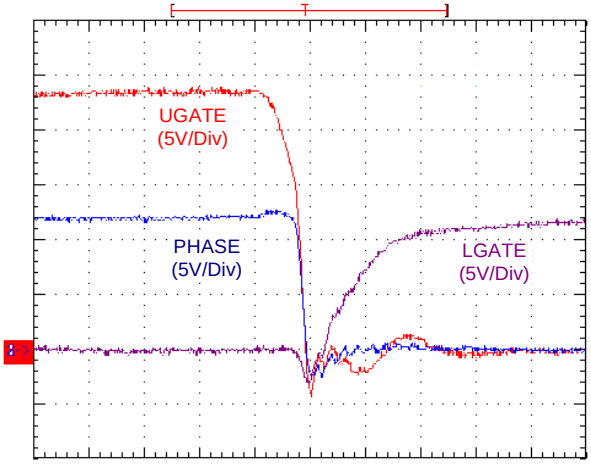
Time (2.5ms/Div)
I_{OUT} = 0A To 60A

Transient Response



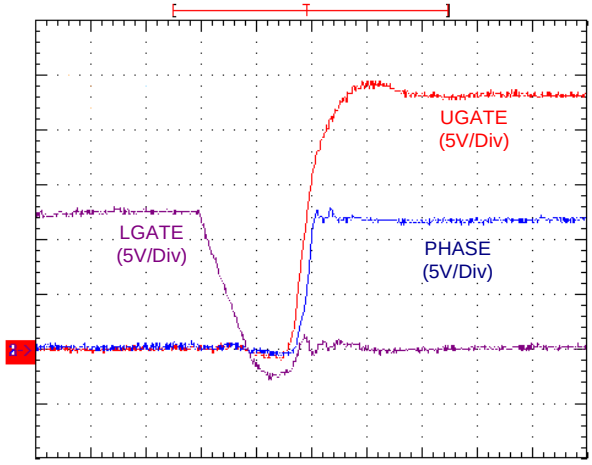
Time (2.5ms/Div)
I_{OUT} = 0A To 60A

Gate Waveforms



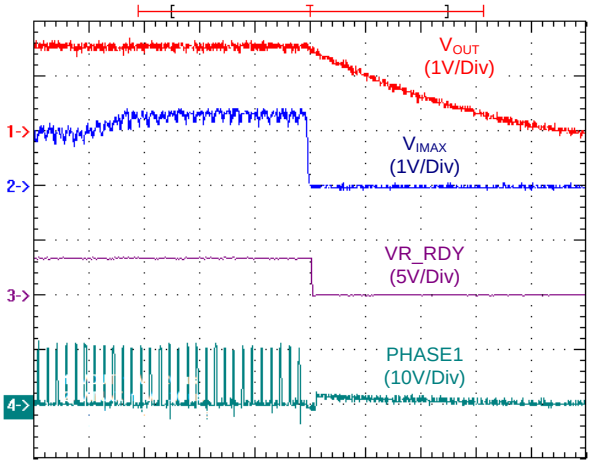
Time (50ns/Div)
I_{OUT} = 60A

Gate Waveforms



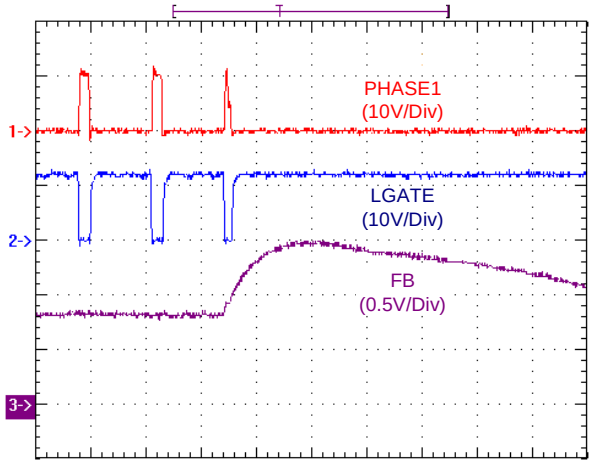
Time (50nus/Div)
I_{OUT} = 60A

Over Current Protection



Time (20us/Div)

Over Voltage Protection



Time (0.5us/Div)
FB Short Circuit to V_{OUT}

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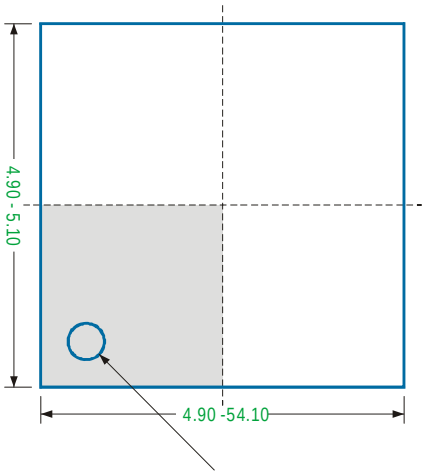
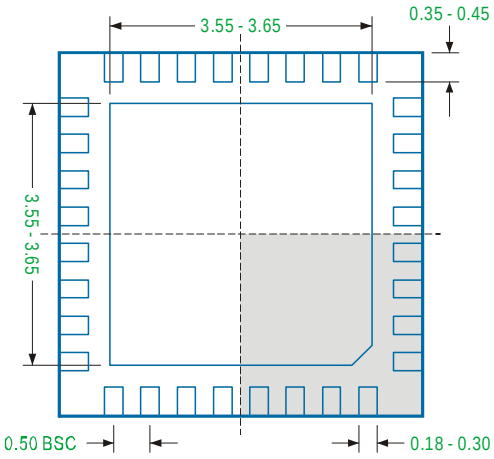
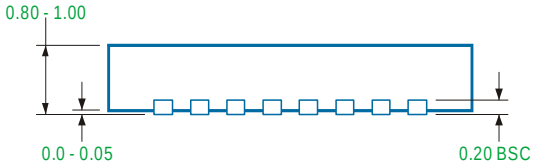
Package Information

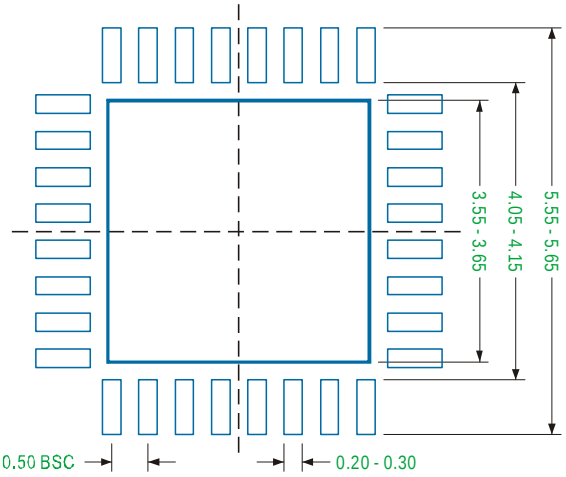
VQFN5x5 - 32L Package





Bottom View - Exposed Pad





Recommended Solder Pad Pitch and Dimensions

Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions no not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.