Smart 5V Dual Controller

General Description

The uP7501 is a power switch controller specifically designed to provide the 5VDUAL voltage for modern motherboards. It controls the switches to power the 5VDUAL plane to comply with ACPI specifications for implementing Sleep States. It switches the ATX/BTX 5VCC output through an NMOS transistor during active states, or switches the ATX/BTX 5VSB through a PMOS transistor for S3 sleep state. A MODE pin controls the power on/shut down of the 5VDUAL rails during the S4/S5 states.

A soft start function is provided to limit inrush current from the 5VSB supply voltage.

This part is packaged in a space saving SOT23-8L package.

Applications

- **ACPI-Compliant Power Regulation for Motherboards**
- **5VDUAL USB/Keyboard/Mouse**

Features

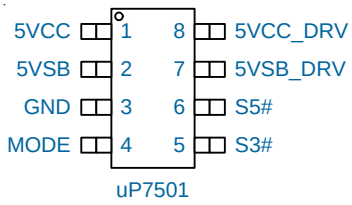
- **Provide ACPI-Compliant 5VDUAL Voltage**
- **Small Size; Low External Component Count**
- **Internal Soft Start**
- **RoHS Compliant and Halogen-Free**

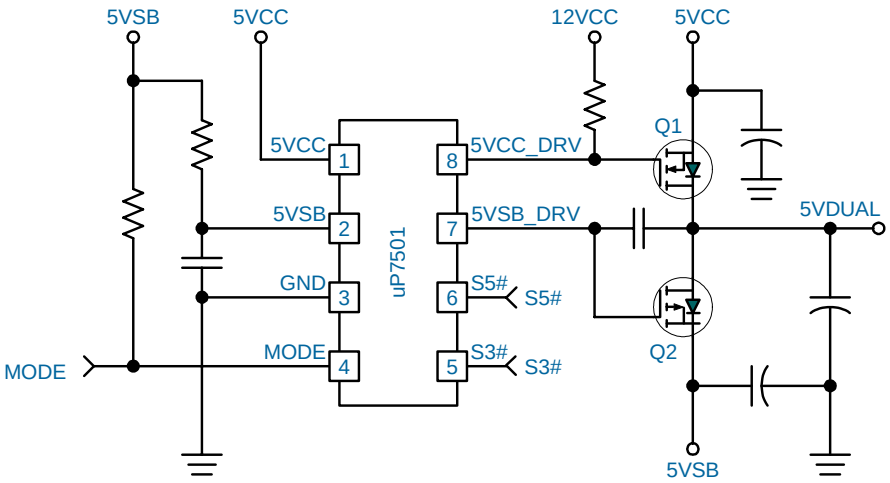
Ordering Information

Order Number	Package Type	Top Marking
uP7501M8	SOT23-8L	S0

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration & Typical Application Circuit

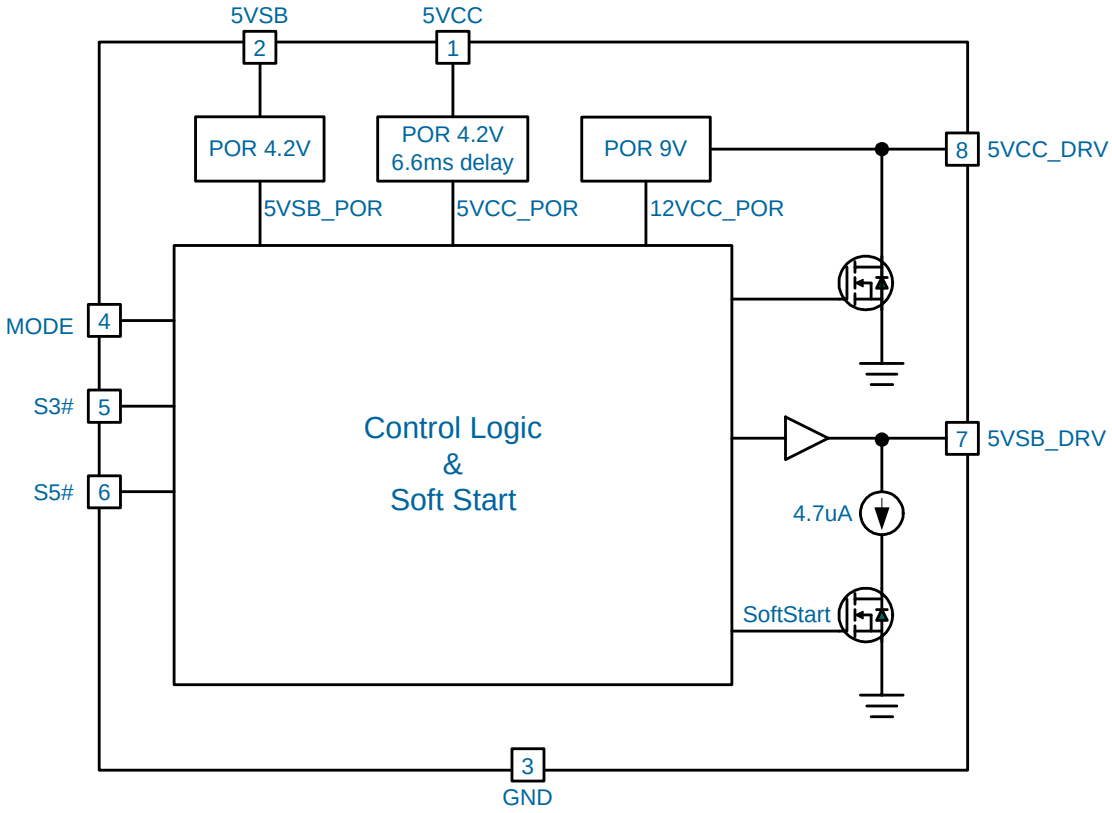




Functional Pin Description

No.	Pin Name	Pin Function
1	5VCC	**5VCC Input.** This pin is continuously monitored for power on reset (POR). The POR threshold level is 4.2V with 0.2V hysteresis. Connect this pin to ATX 5VCC.
2	5VSB	**5VSB Input.** This pin is the power input of the uP7501. This pin is continuously monitored for POR. The POR threshold level is 4.2V with 0.2V hysteresis. Connect this pin to ATX 5VSB with a ceramic decoupling capacitor directly to the GND pin.
3	GND	**Ground.**
4	MODE	**MODE Selection.** This pin programs whether the 5VDUAL output is shut down or stays on during S4/S5 state. Logic low shuts down the 5VDUAL output during S4/S5 state. Logic high powers the 5VDUAL output from ATX 5VSB during S4/S5 state.
5	S3#	**S3# Input.** This pin companied with S5# switches the IC's operating state from active (S0, S1/S2) to S3 and S4/S5 sleep states. This pin is internally pulled down by a 7uA current source. State 0 of S3# is regarded as S3 when S5# is high. Connect this pin to the computer system's SLP_S3 signals.
6	S5#	**S5# Input.** This pin companied with S3# switches the IC's operating state from active (S0, S1/S2) to S3 and S4/S5 sleep states. This pin is internally pulled down by a 7uA current source. State 0 of S5# is regarded as S4/S5 regardless of the S3# state. Connect this pin to the computer system's SLP_S5 signals.
7	5VSB_DRV	**Driver Output for 5VSB.** Connect this pin to the gate of the PMOS transistor. The PMOS transistor is switched on/off according to the status of input of the S3#, S5# and MODE pin.
8	5VCC_DRV	**Driver Output for 5VCC.** Connect this pin to the gate of the NMOS transistor. The transistor is switched on/off according the S5# and S3# pins status. This pin is an open-drain output. A 1k Ω resistor must be connected from this pin to the ATX 12VCC output to drive the gate of the NMOS transistor to switch the ATX 5VCC input into the 5VDUAL output rail. This pin also monitors the 12VCC rail for POR. The POR threshold level is 9V with 1V hysteresis.

Functional Block Diagram



Functional Description

Operation

The uP7501 is a power switch controller specifically designed to provide the 5VDUAL voltage for modern motherboards. It controls the switches to power the 5VDUAL plane to comply with ACPI specifications for implementing Sleep States. It switches the ATX/BTX 5VCC output through an NMOS transistor during active states, or switches the ATX/BTX 5VSB through a PMOS transistor for S3 sleep state. A MODE pin controls the power on/ shut down of the 5VDUAL rails during the S4/S5 states.

Initialization

The uP7501 automatically initializes upon receipt of input power at the 5VSB pin. The Power On Reset (POR) function continually monitors the 5VSB input supply voltage. The threshold of the 5VSB POR at rising edge is typically 4.2V. The uP7501 also monitors the 12VCC and 5VCC rails to insure that the ATX/BTX rails are up before entering into the S0 state even if the S3# and S5# inputs are both high.

5VCC_DRV has an internal 60kΩ pull-down resistor and must be connected to 12VCC through an external pull-up resistor R1 as shown in Figure 1. The voltage of 5VCC_DRV is derived from this resistor divider and drives the external NMOS transistor to switch 5VCC to 5VDUAL for the various power states. During power-up, the uP7501 monitors 5VCC_DRV to determine whether 12VCC is ready. The voltage of 5VCC_DRV must be greater than the POR reference voltage, typically 9V to initialize the uP7501.

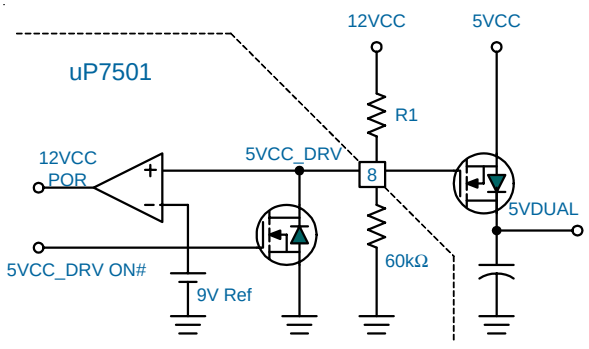


Figure 1. 5VCC_DRV Connection and 12VCC Detection

5VDUAL Output Truth Table

Table 1 describes the truth combinations pertaining to the 5VDUAL outputs. The 5VDUAL output is switched into the ATX/BTX 5VCC output through an NMOS transistor in active states when S3# and S5# are both high. It is switched into the ATX/BTX 5VSB through a PMOS transistor in S3 sleep state when S3# is low and S5# is high. The uP7501 asserts S4/S5 state when S5# is low regardless of the S3# status. The switching between 5VSB and 5VCC is immediate to ensure a seamless 5VDUAL output.

Table 1. 5VDUAL Output Truth Table

S5#	S3#	MODE	5VDUAL	Remarks
1	1	X	5VCC	S0/S1/S2 (Active)
1	0	X	5VSB	S3
0	X	1	5VSB	S4/S5
0	X	0	Shutdown	S4/S5

Note 1: When MODE = L, the 5VDUAL output can only be enabled by 5VCC and 12VCC POR (refer to the related sections for detail).

Note 2: If +12V and +5V are ready, for S5#=1, S3#=1 ,and MODE=X, 5VDUAL is 5VCC. If +12V and +5V aren't ready, for S5#=1, S3#=1 ,and MODE=X, 5VDUAL is 5VSB.

Functional Timing Diagrams

Figure 2 and Figure 3 are timing diagrams for MODE = L and MODE =H. The two figures show the power up/down sequences of all the outputs in response to the status of the sleep-state pins (S3#, S5#), as well as the status of the ATX/BTX power supply outputs (5VSB/5VCC/12VCC).

The S3# and S5# pins have deglitch function to protect false sleep state tripping. Additionally, the uP7501 features a 120us delay in the transition from S0 to S3 states. The transition from the S0 state to S4/S5 state is immediate. The switching between 5VSB and 5VCC is immediately to ensure a seamless 5VDUAL output.

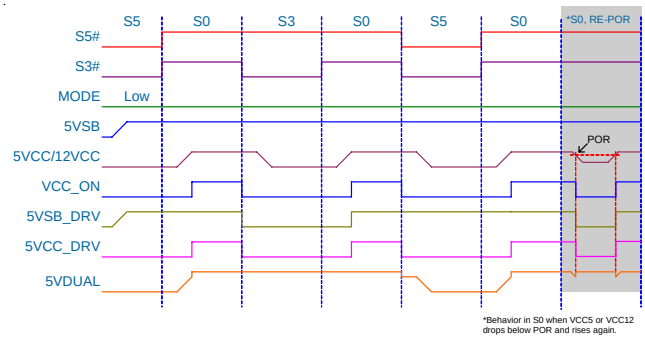


Figure 2. Timing Diagram with MODE = L

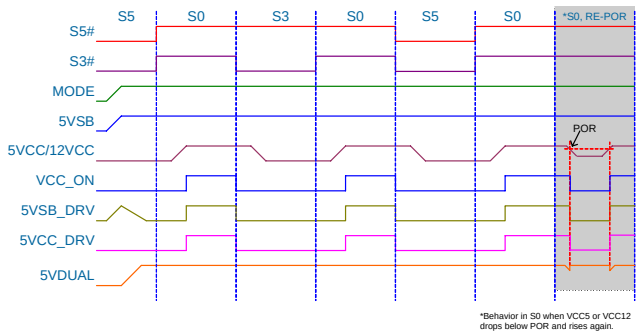


Figure 3. Timing Diagram with MODE = H

G3 to S0 State Transition with MODE = L

Figure 4 shows the start up sequence for the typical application power up from G3 state (mechanical off) to S0 state (active) with MODE = L. At time T0, 5VSB (bias) is applied to the circuit. At time T1, the 5VSB surpasses the POR level. The uP7501 keeps the 5VDUAL output off by turning off both PMOS transistor and NMOS transistor. At time T2, the system has transitioned into S0 state and the ATX/BTX supplies have begun to ramp up. The rising 5VCC charges the 5VDUAL output through the body diode of the NMOS transistor. There is a 0.7V voltage drop between VCC5 and 5VDUAL caused by the body diode. At time T3, 5VCC and 12VCC reach their POR threshold level respectively. At time T4, the uP7501 sets the internal VCC_ON signal high and forces the 5VCC_DRV pin to high impedance state. This allows the gate of the NMOS transistor to be pulled high by the 12VCC divider circuit and turn on NMOS transistor. A 5ms delay is inserted between T3 and T4 to ensure that there is sufficient mains energy stored by the converter to guarantee continuous power operation within specification. There is a voltage jump about 0.7V when uP7501 turns on the NMOS transistor.

It is noted that the 5VDUAL output is ready before ATX/BTX power supplies set high its PWR_OK signal.

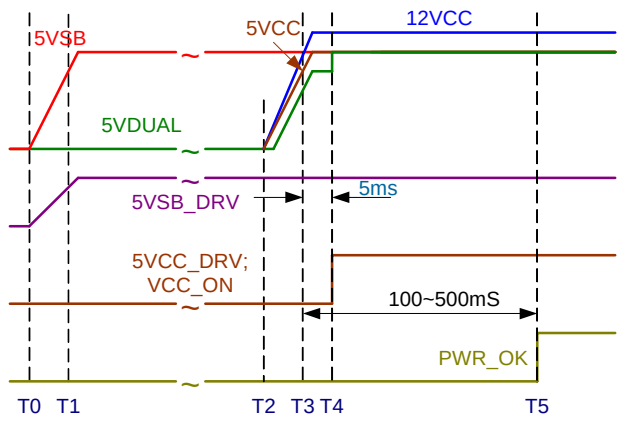


Figure 4. State Transition from G3 to S0 with MODE = L

G3 to S0 State Transition with MODE = H

Figure 5 shows the start up sequence for the typical application power up from G3 state (mechanical off) to S0 state (active) with MODE =H. At time T0, 5VSB (bias) is applied to the circuit. At time T1, the 5VSB surpasses the POR level. The uP7501 will draw 4uA into the 5VSB_DRV for a duration of one soft start period. This current will enhance the PMOS transistor in a controlled manner allowing the 5VDUAL output to ramp up smoothly. At time T2, the system has transitioned into S0 state and the ATX/BTX supplies have begun to ramp up. At time T3, 5VCC and 12VCC reach their POR threshold level respectively. At time T4, the uP7501 sets the internal VCC_ON signal high and forces the 5VCC_DRV pin to a high impedance state. This allows the gate of the NMOS transistor to be pulled high by the 12VCC divider circuit and turn on NMOS transistor. At time T4, 5VSB_DRV is pulled high to turn off the PMOS transistor ensuring a seamless transition for 5VSB to 5VCC. A 5ms delay is inserted between T3 and T4 to insure that there is sufficient mains energy stored by the converter to guarantee continuous power operation within specification.

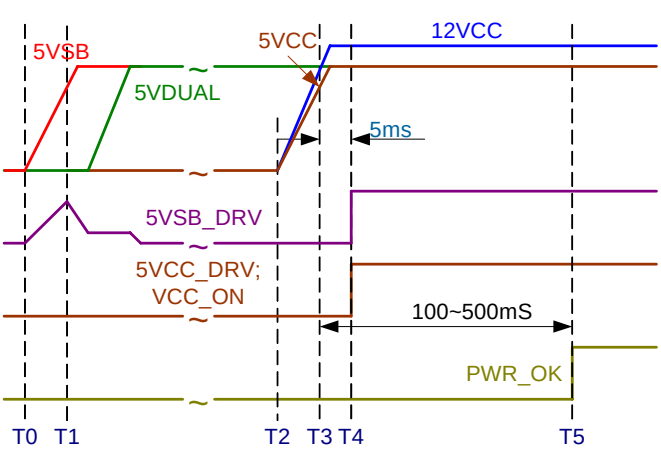


Figure 5. State Transition from G3 to S0 with MODE = H

S5 to S0 State Transition with MODE = L

Figure 6 shows the state transition from S5 to S0 with MODE = L. It is exactly the same as the G3 to S0 transition with MODE = L after T2.

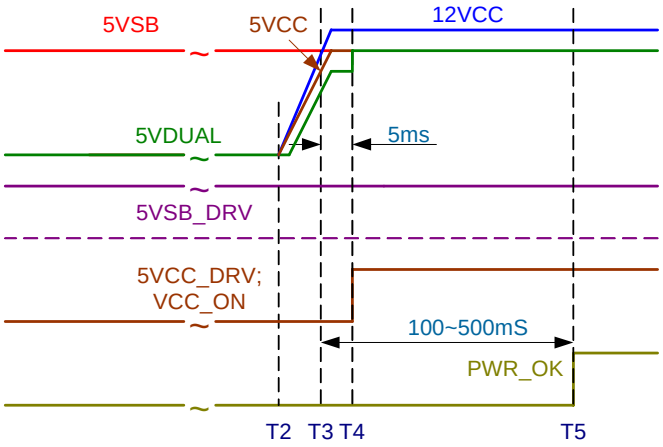


Figure 6. State Transition from S5 to S0 with MODE = L

S5 to S0 State Transition with MODE = H

Figure 7 shows the state transition from S5 to S0 with MODE = H. It is exactly the same as the G3 to S0 transition with MODE = H after T2.

S3 to S0 State Transition with MODE = H/L

This transition is identical to S5 to S0 transition with MODE = H where 5VDUAL is kept on.

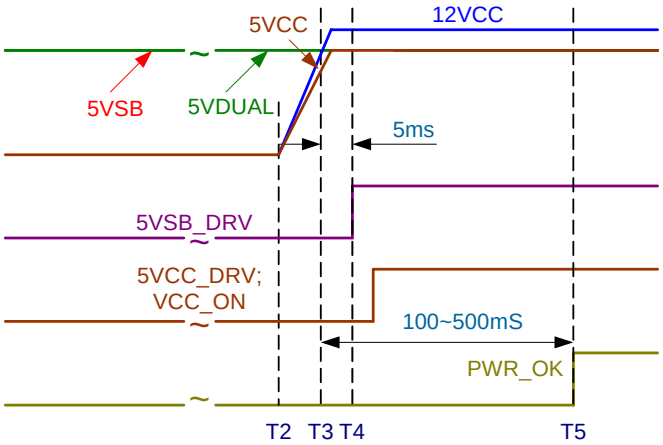


Figure 7. State Transition from S5 to S0 with MODE = H

S0 to S5 State Transition with MODE = H

Figure 8 shows the state transition from S0 to S5 with MODE = H. At time T6, the system has transitioned into S5 state. The uP7501 maintains the 5VDUAL output from 5VSB by pulling 5VSB_DRV low to turn on the PMOS transistor, and pulling 5VCC_DRV low to turn off the NMOS transistor, ensuring a seamless transition. At time T7, the ATX/BTX power supply turns off and 5VCC and 12VCC start to ramp down and reaches 0V at time T8.

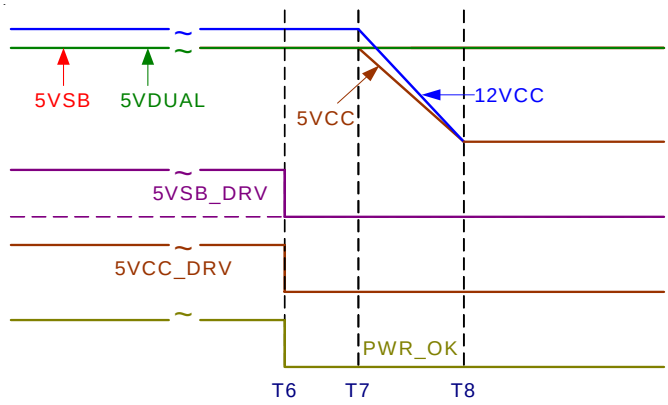


Figure 8. State Transition from S0 to S5 with MODE = H

S0 to S5 State Transition with MODE = L

Figure 9 shows the state transition from S5 to S0 with MODE = L. At time T6, the system is transitioned into S0 state. The uP7501 sets internal VCC_ON low and pulls 5VCC_DRV low to turn off the NMOS transistor. 5VCC/12VCC start ramping down at time T7 when the ATX/BTX power supply turns off and reaches ground at time T8. The 5VDUAL output will follow 5VCC waveforms with a diode bias voltage.

S0 to S3 State Transition with MODE = H/L

This transition is identical to S0 to S5 transition with MODE = H where the 5VDUAL output is kept on.

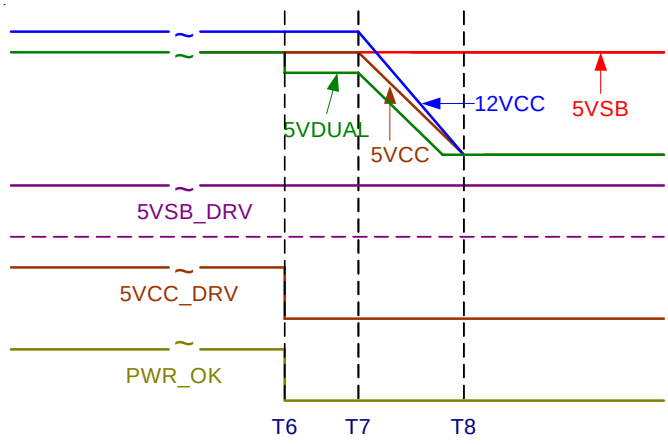


Figure 9. State Transition from S0 to S5 with MODE = L

ATX/BTX Power Supply Timing

Figure 10 illustrates the timing diagram of the ATX/BTX power supplies. The detailed time specifications are illustrated in Table 2. PWR_OK is a power good signal and should be asserted high by the power supply to indicate that the 3.3VCC/5VCC/12VCC outputs are above the undervoltage thresholds of the power supply. A delay time T3 between 95% rising of 3.3VCC/5VCC/12VCC and PWR_OK is specified at 100ms ~ 2000ms to ensure that there is sufficient mains energy stored by the converter to guarantee continuous power operation within specification. Traditional implementation of the 5VDUAL output voltage uses the PWR_OK signal to control the switches as shown in Figure 11. The 5VDUAL output is turned on only when PWR_OK is set high regardless of the sleep state signals S3# and S5#.

Some applications require a large current from the 5VDUAL output during T3. In these cases, the 5VDUAL output driven from 5VSB during T3 cannot provide the current demand and may cause system failure.

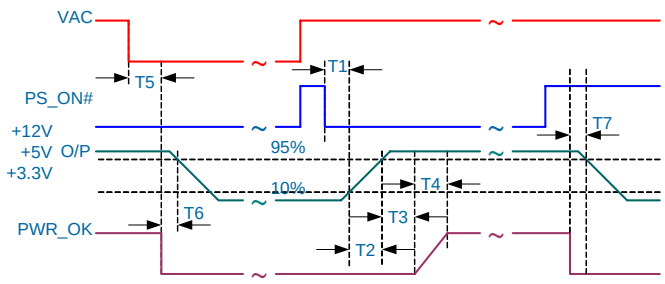


Figure10. Timing Diagram of ATX/BTX Power Supplies

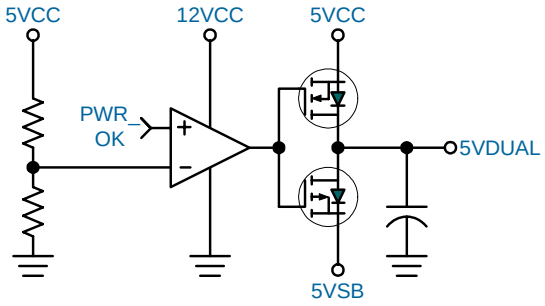


Figure 11. Traditional Implementation of 5VDUAL Output

Table 2. Typical Timing Specification of ATX/BTX Power Supplies

Signal type	+5V TTL compatible
Logic level low	<0.4V while sinking 4mA
Logic level high	Between 2.4V and 5V output while sourcing 200uA
High-state output impedance	1kΩ from output to common
Turn on delay time	T1 < 1s
Voltage ramp up time	2ms < T2 < 200ms
PWR_OK delay time	100ms < T3 < 2000ms
PWR_OK rise time	T4 < 10ms
AC loss to PWR_OK hold-up time	T5 > 16ms
Power-down warning	T6 > 1ms; T7 > 1ms

Absolute Maximum Rating

Supply Input Voltage, 5VSB (Note 1) ---------- -0.3V to +6V
5VCC_DRV Voltage ---------- -0.3V to +13.2V
Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
SOT23-8L θ_{JA} ---------- 250°C/W
SOT23-8L θ_{JC} ---------- 140°C/W
Power Dissipation, P_D @ TA = 25°C
SOT23-8L ---------- 0.4W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{5VSB} ---------- +4.5V to +5.5V

Electrical Characteristics

(V_{5VSB} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Nominal Supply Current	I_{5VSB}		--	0.3	--	mA
Power On Reset						
Rising 5VSB POR Threshold	V_{5VSB_POR}		3.8	4.2	4.5	V
5VSB POR Hysteresis	V_{5VSB_HYS}		--	0.2	--	V
Rising 5VCC_DRV POR Threshold	$V_{5VCCDRV\_POR}$	1kΩ resistor between 5VCC_DRV and 12VCC Rail; 5VCC_DRV rising	--	9.0	10.5	V
5VCC_DRV POR Hysteresis	$V_{5VCCDRV\_HYS}$	1kΩ resistor between 5VCC_DRV and 12VCC Rail; 5VCC_DRV falling	--	1.0	--	V
Rising 5VCC POR Threshold	V_{5VCC_POR}		3.8	4.2	4.5	V
Falling 5VCC POR Threshold	V_{5VCC_HYS}		--	0.2	--	V
5VCC POR Rising Delay Time		From 5VCC rising POR to 5VCC_DRV rising	1	5	10	ms

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Switch Controller						
5VSB_DRV Source Current	I_{5VSB_DRV}	5VSB_DRV = 0V, 5VSB = 5V	20	--	35	mA
5VSB_DRV Sink Current	I_{5VSB_DRV}	5VSB_DRV = 5V, 5VSB = 5V	20	--	35	mA
5VSB_DRV Soft Start Sinking Current	I_{5VSB_DRV}		--	4.0	--	uA
5VCC_DRV Sink Current	I_{5VCC_DRV}	5VCC_DRV = 5V, 5VSB = 5V	20	--	--	mA
Control I/O (S3#, S5#, and MODE)						
High Level Input Threshold			-	-	2.0	V
Low Level Input Threshold			0.8	-	-	V
S3#, S5# Internal Pull Down Current to GND			-	7	-	uA

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

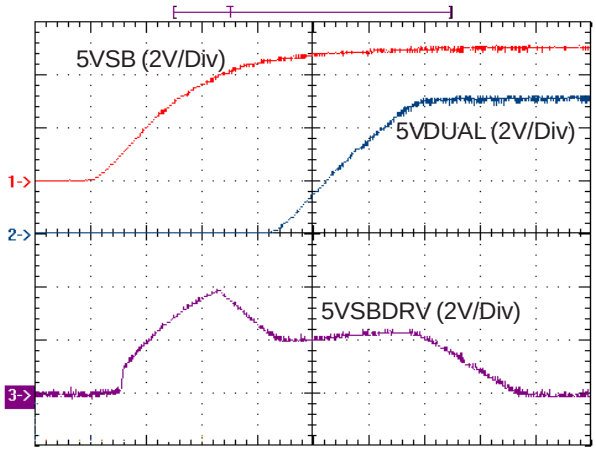
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

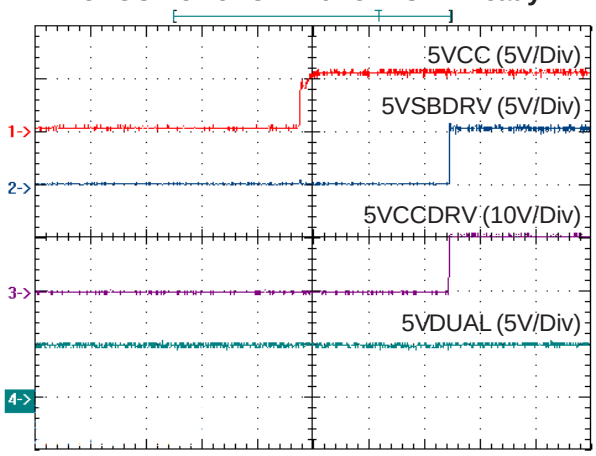
Typical Operation Characteristics

Soft Start for 5VSB



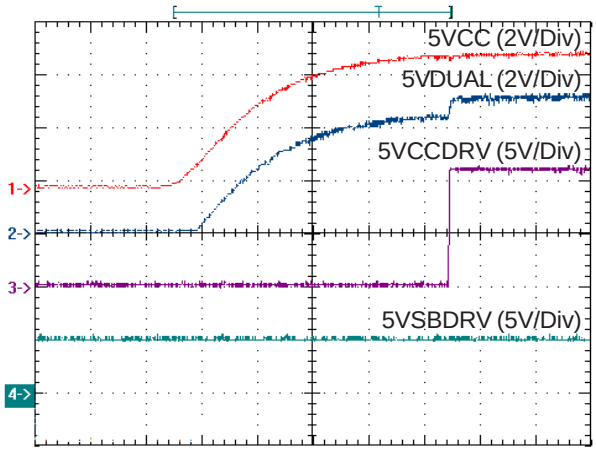
MODE = High; C_{GD} = 3.3nF at PMOS transistor

5VCC Power On with 5VDUAL Ready



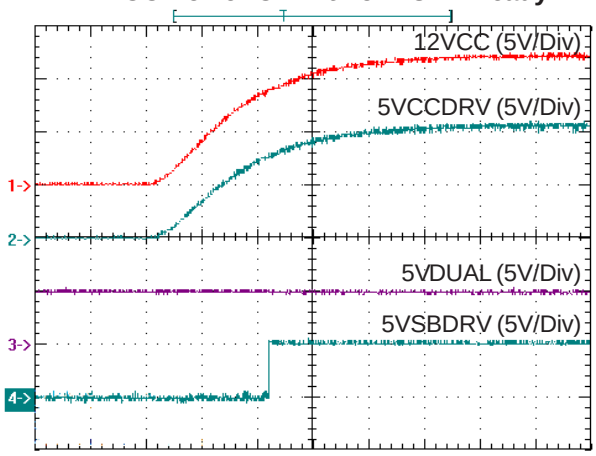
MODE = High; S3/S5 into S0

5VCC Power On with 5VDUAL Off



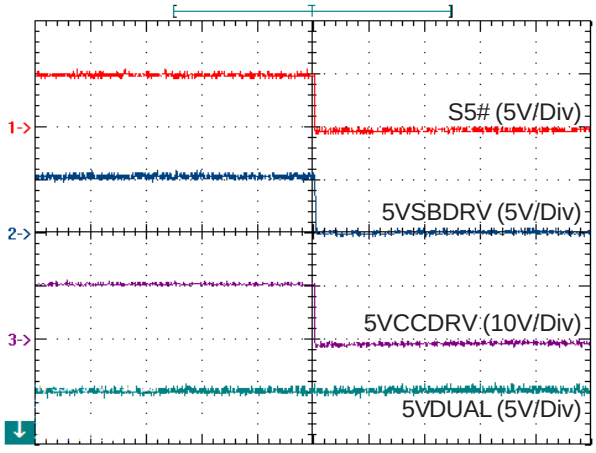
MODE = Low; S5 into S0

12VCC Power On with 5VDUAL Ready



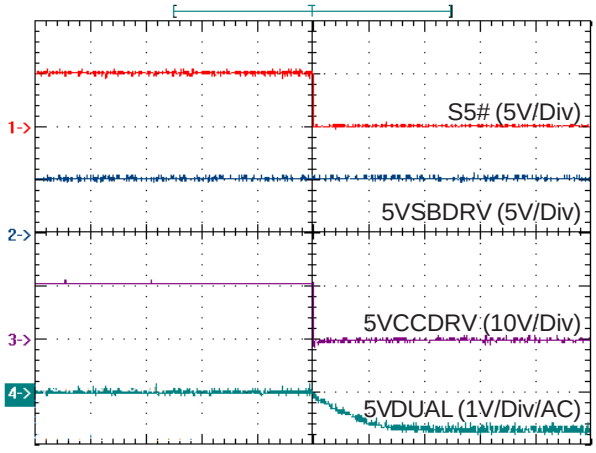
MODE = High; S3/S5 into S0

S0 into S5 with MODE = High



MODE = High; S0 into S5

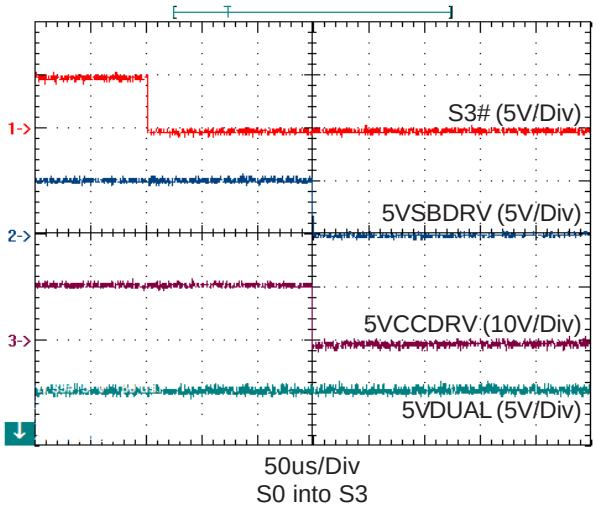
S0 into S5 with MODE = Low



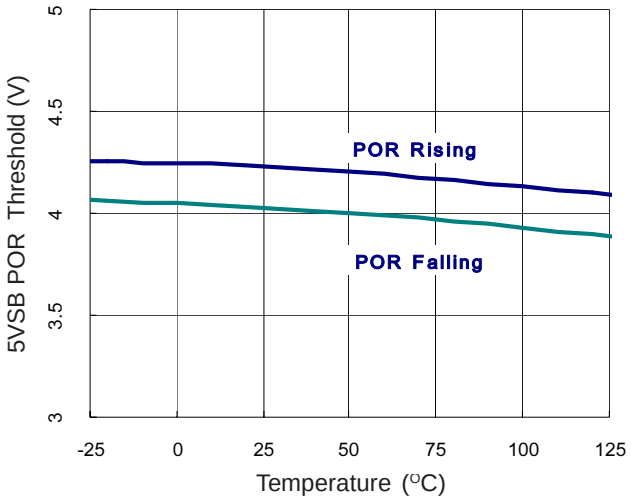
MODE = Low; S0 into S5

Typical Operation Characteristics

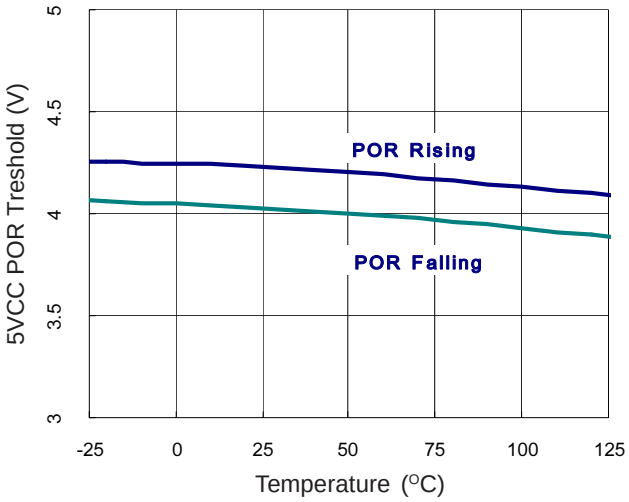
S0 into S3



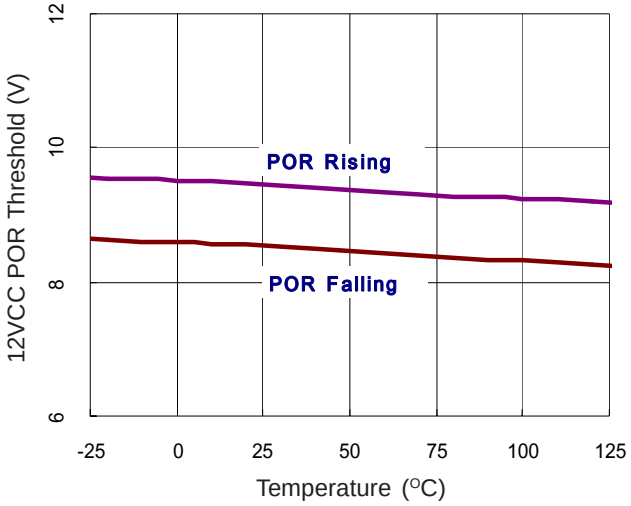
5VSB POR vs. Temperature



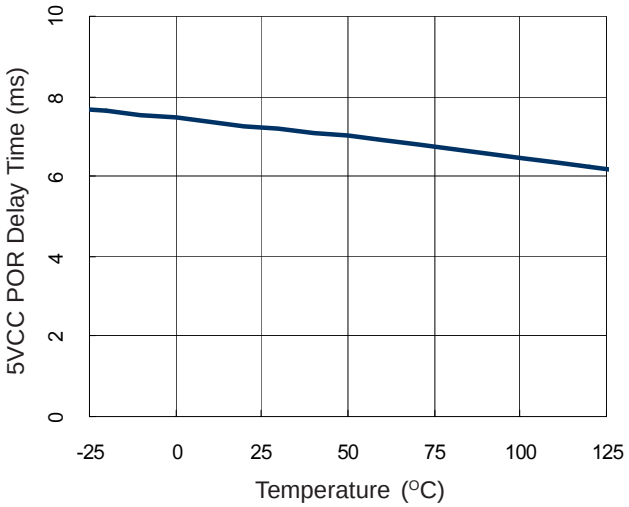
5VCC POR vs. Temperature



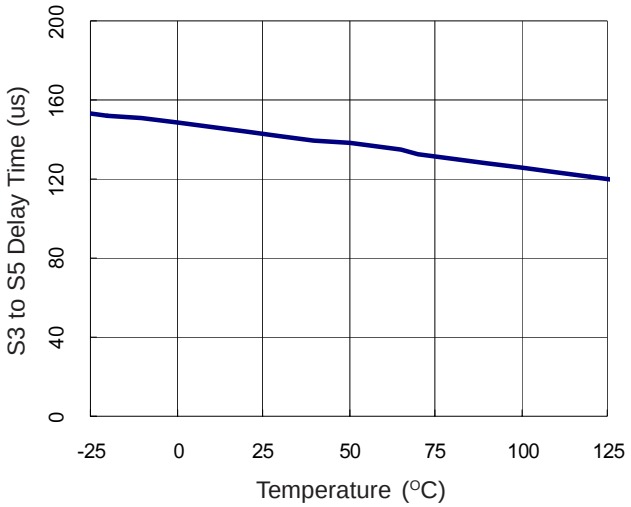
12VCC POR vs. Temperature



5VCC POR Delay vs. Temperature



S0 to S3 Delay vs. Temperature



Component Selection Guidelines

Output Capacitors Selection

The output capacitors should be selected to allow the output voltage to meet the dynamic regulation requirements of active state operation (S0/S1). The load transient for the various microprocessor system's components may require high quality capacitors to supply the high slew rate (di/dt) current demands. Thus, it is recommended that the output capacitors be selected for transient load regulation, paying attention to their parasitic components (ESR, ESL).

Switching on/off of the NMOS transistor and PMOS transistor are simultaneouly. Since it takes a finite time to turn off a MOSFET, there is a small overlapping time where both NMOS transistor and PMOS transistor are both on, ensuring seamless transition between 5VSB and 5VCC. No special concern is required for the voltage drop during the transition that should be taken care in traditional implementation.

Input Capacitors Selection

The input capacitors for an uP7501 application must have a sufficiently low ESR so that the input voltage will not dip excessively when energy is transferred to the output capacitors. If the ATX/BTX supply does not meet required specifications, certain imbalances between the ATX/BTX outputs and the uP7501 regulation levels may result during the brisk transfer of energy from the input capacitors to the supplied outputs. At the transition between active and sleep states, such phenomena could be responsible for the 5VSB voltage drooping excessively and affecting the output regulation. The solution to such a potential problem is using larger input capacitors with a lower total combined ESR.

Transistor Selection/Considerations

The uP7501 usually requires one P-Channel and one N-Channel MOSFETs as shown in the Typical Application Circuit. Both of these MOSFETs are utilized as ON/OFF switching elements. One important criteria for selection of transistors for all the switching elements is package selection for efficient removal of heat. The power dissipated in a switch element while on is:

$$P_D = I_{OUT}^2 \times R_{DS(ON)}$$

Select a package and heatsink that maintains the junction temperature below the rating with the maximum expected ambient temperature.

Q1

This is a P-Channel MOSFET used to switch the 5VSB output of the ATX/BTX supply into the 5VDUAL output during sleep states. The selection criteria of this device, as with the N-Channel MOSFETs, is proper voltage budgeting. The maximum $R_{DS(ON)}$, however, has to be achieved with only 4.5V of gate-to-source voltage, so a true logic level MOSFET needs to be selected.

Q2

This N-Channel MOSFET is used to switch the 5VCC voltage provided by the ATX/BTX supply into the 5VDUAL output while in active (S0, S1) state. The main criteria for the selection of these transistors is output voltage budgeting. The maximum $R_{DS(ON)}$ allowed at highest junction temperature can be expressed with the following equation:

$$R_{DS(ON)\_MAX} = (T_{J\_MAX} - T_A) / \theta_{JA} / I_{OUT}^2$$

, where T_{J_MAX} = maximum allowable junction temperature, θ_{JA} = junction to ambient thermal resistance of the NMOS transistor. Consider the $R_{DS(ON)}$ with gate voltage V_{GS} = 5V.

Softstart Time Control

During G3 to S5 transition with MODE = High, the current sinking capability of 5VSB_DRV is limited to 4uA for softstart. A capacitor connecting gate and drain of the PMOSFET is useful to control the ramp up speed of the 5VDUAL output, thus limiting the inrush current from 5VSB. Figure 12 illustrates the related waveforms. Initially, the 4uA current discharges input capacitor C_{ISS} of the PMOSFET and attached capacitor making the gate voltage ramp down linearly. The PMOSFET starts to conduct current and the 5VDUAL output starts to ramp up after the V_{GS} reaches the threshold. During the ramp up of the 5VDUAL output, the V_{GS} keeps flat due to the Miller Effect even though 4uA current keeps discharging the attahced capacitor.

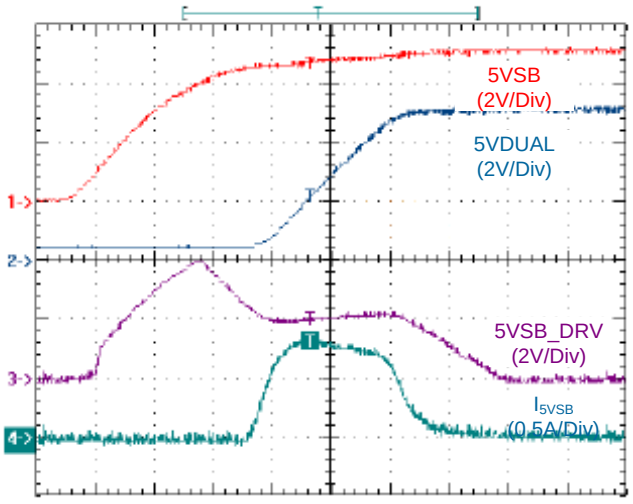


Figure 12. Soft Start of the 5VDUAL Output with a 3.3uF Capacitor Connecting to Gate and Drain of PMOS Transistor

The ramp up time of 5VDUAL can be estimated as:

$$T_{RAMP\_UP} = \frac{5V \times (C_{EXT} + C_{GD})}{4uA}$$

Layout Considerations

The typical application employing an uP7501 is a fairly straight forward implementation as shown in Figure 13. Attention should be paid to sensitive logic inputs (S3# and S5#) and those supplying critical bypass current.

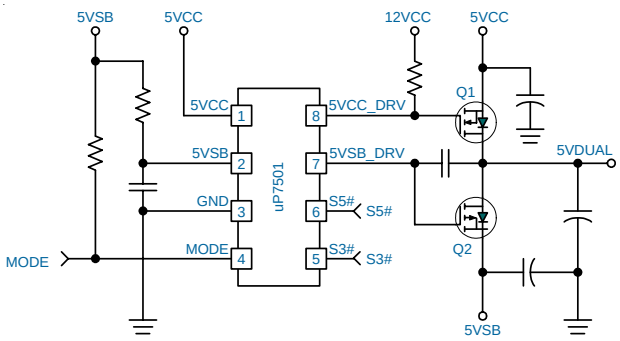


Figure 13. Typical Implementation of 5VDUAL

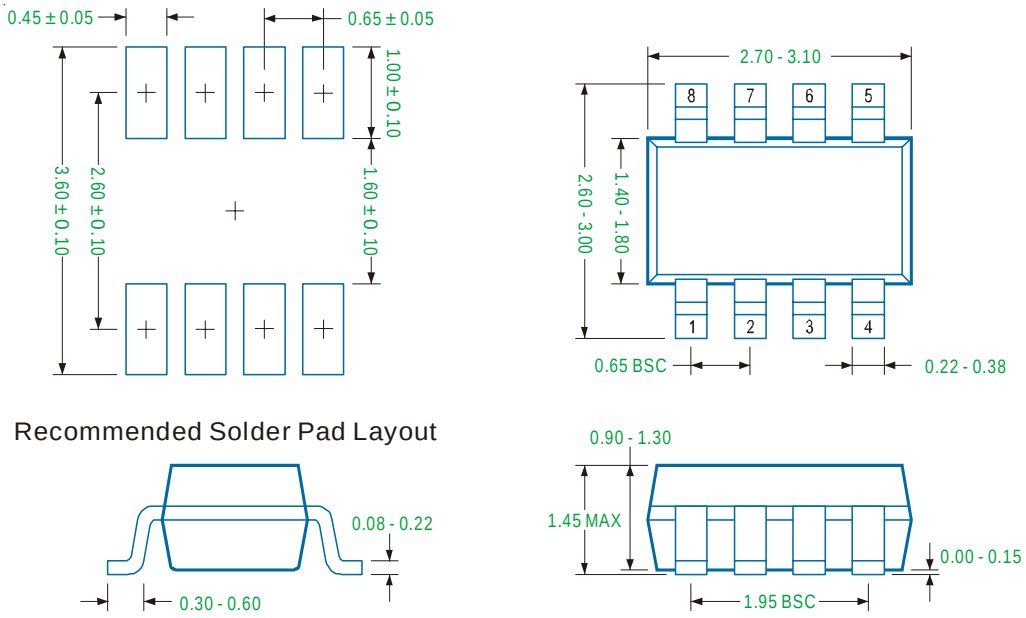
The input bias supply (5VSB) can carry a substantial amount of current. For best results, ensure it is connected to its respected source through an adequately sized trace and is properly decoupled. The pass transistors should be placed on pads capable of heatsinking matching the device power dissipation. Where applicable, multiple via connections to a large internal plane can significantly lower localized device temperature rise.

Placement of the decoupling and bulk capacitors should reflect their purpose. As such, the high-frequency decoupling capacitors should be placed as close as possible to the load they are decoupling; the ones decoupling the controller close to the controller pins, the ones decoupling the load close to the load connector or the load itself (if embedded). Even though bulk capacitance (aluminum electrolytics or tantalum capacitors) placement is not as critical as the high-frequency capacitor placement, having these capacitors close to the load they serve is preferable.

Locate all small signal components close to the respective pins of the control IC, and connect them to ground, if applicable, through a via placed close to the ground pad. A multilayer printed circuit board is recommended.

Package Information

SOT23 - 8L Package



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.

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uPI Semiconductor Corp.
9F.,No.5, Taiyuan 1st St. Zhubei City, Hsinchu, Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888
sales@upi-semi.com