uPI SEMI

uP7567

Ultra-Low $R_{DS(ON)}$ Power Distribution Switch with Adjustable Soft Start, Current Limit, and Current Monitoring

General Description

The uP7567 is a small size, ultra-low $R_{DS(ON)}$, load switch with enable control, adjustable soft start, current limit and current monitoring. The uP7567 contains one internal 12mΩ $R_{DS(ON)}$ N-channel MOSFET which supports a continuous current up to 7A.

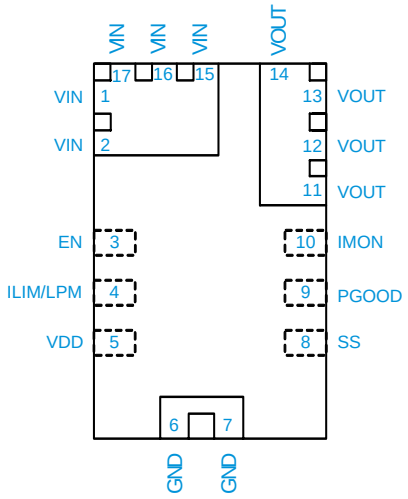
The switch on/off is controlled by EN pin. In uP7567, a 100Ω discharge MOSFET is built in for quick output discharge when switch is turned off. Additionally, the device features adjustable soft start function, adjustable current limit and over temperature protection. The uP7567 is available in UQFN2x3-17L package.

Ordering Information

Order Number	Package Type	Top Marking
uP7567PQSAA	UQFN2x3-17L (Flip-Chip)	uP7567P

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



(Top View)

Features

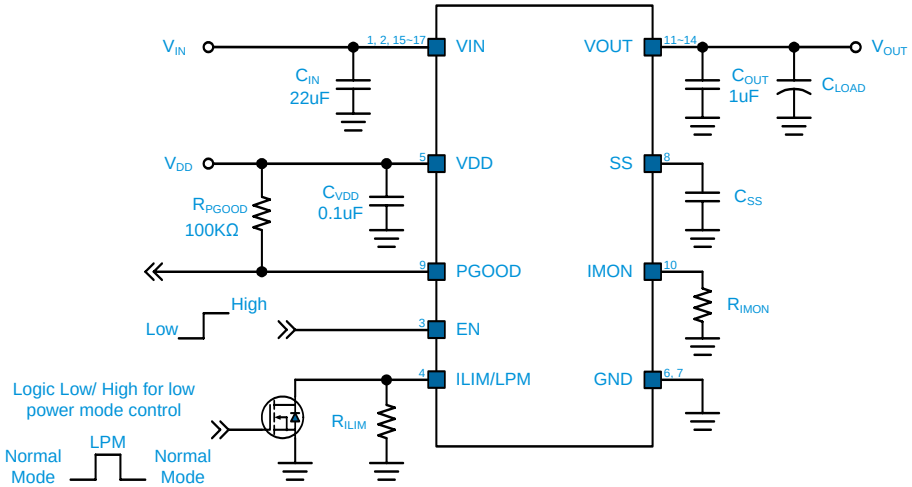
- **Input Voltage Range (V_{IN}): 0.7V~5.5V**
- **Supply Voltage Range (V_{DD}): 3V~5.5V**
- **MOSFET $R_{DS(ON)}$ = 12mΩ at V_{DD}=3.3V**
- **Ultra-Low Quiescent Current: < 50uA**
- **Internal Charge Pump Function for Internal Gate Driver**
- **Adjustable Current Limit Function by ILIM/LPM Multi-Function Pin with 5% Accuracy**
- **Output Short Circuit Protection (SCP)**
- **VOUT Discharge Function**
- **Adjustable Soft Start Function by SS Pin**
- **Low Power Mode Controlled by ILIM/LPM to Support C10 C-State**
- **UVP/OTP/SCP Latch Off Protection**
- **Enable/Shutdown Control by EN Pin**
- **PGOOD for Power Good Indication**
- **Current Monitoring Function by IMON Pin with 5% Report Accuracy**
- **UQFN2x3-17L Package**
- **RoHS Compliant and Halogen Free**

Applications

- **Notebook Computers**
- **Desktop Computers**
- **Consumer Electronics**

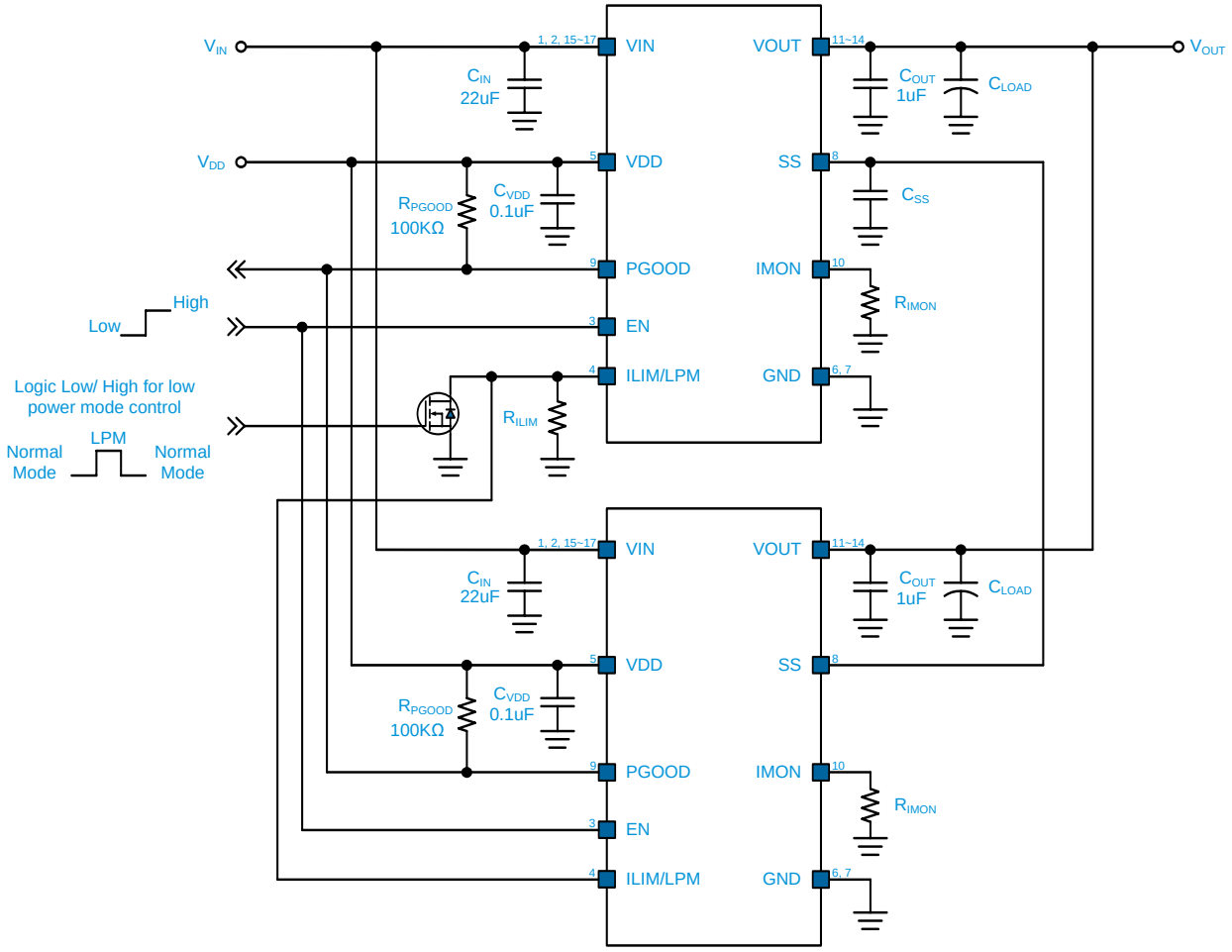
Typical Application Circuit

Standard Configuration



Typical Application Circuit

Paralleled Configuration

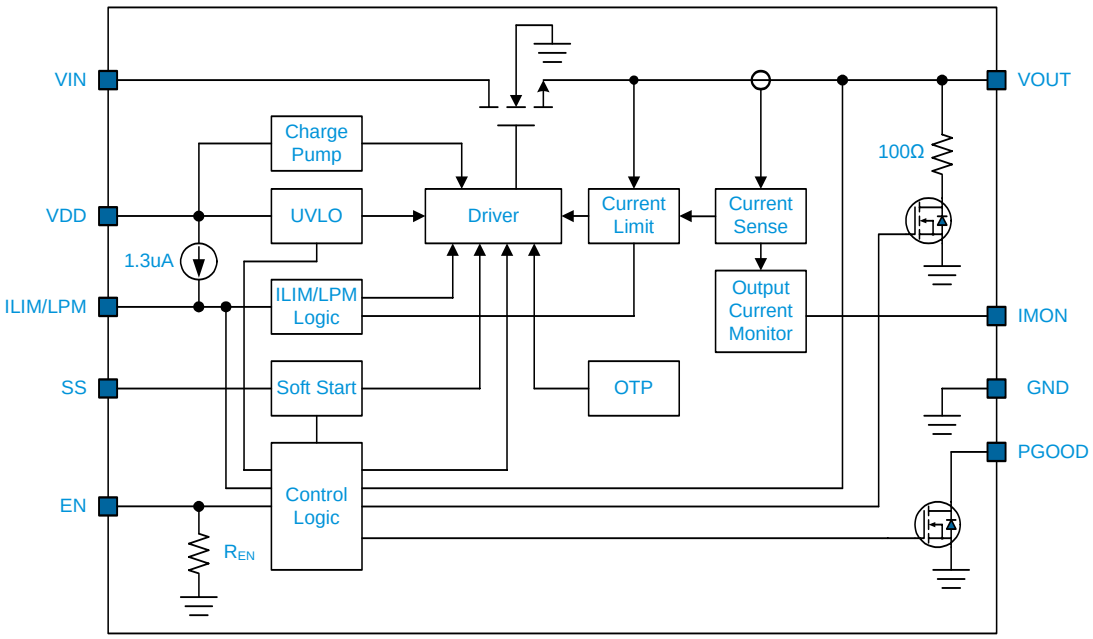


Note:
The input power traces must be short on PCB, and the input capacitance greater than 22uF is recommended in order to avoid voltage overload at power-on. The application of uP7567 in parallel also requires shorter power traces on PCB and larger capacitors to avoid input voltage overshoot.

Functional Pin Description

Pin No.	Pin Name	Pin Function
1,2,15,16,17	VIN	**Power Switch Supply Input.** These pins are the input to the drain of internal MOSFET. It is recommended to connect a 22uF minimum capacitor from this pin to GND.
3	EN	**Enable Input.** This is the enable input to turn the power switch on or off. Logic high input to this pin enables the device, and logic low input to this pin disables the device. There is a pull-down resistor internal to this pin to avoid inadvertent device enable.
4	ILIM/LPM	This pin is a multi-functional pin. It is for current limit threshold selection and also used for low power mode control. **Current Limit Level Selection.** The input voltage level of this pin determines the current limit level of the device. Logic High, floating state and logic low input to this pin denotes three individual current limit levels in a decreasing pattern. Floating state to this pin is allowed since there is a current source internal to this pin. A resistor can be added from this pin to GND to set the current limit level when this pin is floating. See related section for detail. **Low Power Mode Control.** Logic input to this pin controls the operation mode of the device. The device operates in normal mode when logic high input to this pin. Logic low input to this pin enables the low power mode for power saving.
5	VDD	**Supply Input.** This is the input pin to control circuit. Bypass this pin with a 0.1uF minimum capacitor to ground. Note that to make power switch operate normally, V_{DD} voltage should be no lower than V_{IN} voltage.
6,7	GND	**Ground.** These pins are the ground of the device.
8	SS	**Soft Start Control.** Connect an MLCC Css from this pin to GND to set the soft start time of the ouput voltage. It is allowed to leave this pin floating. Refer to Table 2 and Table 3 for Css capacitance selection.
9	PGOOD	**Power Good Indicator.** This pin is an open drain structure. Connect a resistor from this pin to V_{DD}. At the end of soft start, this pin is set to high impedance state (PGOOD=High) to indicate the output voltage is ready if no protection is triggered.
10	IMON	**Output Current Monitoring.** The output current of this pin is proportional to the output current of this device. Connect a resistor from this pin to GND for output current monitoring.
11~14	VOUT	**Output Voltage.** These pins are outputs from N-channel MOSFET source. It is recommended to connect a 1uF minimum capacitor from these pins to GND.

Functional Block Diagram



Functional Description

Power Switch

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from V_{OUT} to V_{IN} and V_{IN} to V_{OUT} when disabled. The power switch is controlled by a logic enable input (active high) and driven by an internal charge pump circuit. When the output load exceeds the current-limit threshold, the uP7567 asserts over current protection and limits the output current to a safe level by driving the power switch into saturation mode.

Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from supply input V_{DD} as low as 3V.

Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise time and fall time of the output voltage.

Chip Enable

The EN pin controls the enable/disable state of the device. Logic high input to the EN pin enables the device, and the output voltage starts to ramp up. Logic low input to the EN pin disables the device, and the output voltage is discharged through a resistor internal to the VOUT pins. Floating state to the EN pin is allowed since there is a resistor internal to the EN pin to prevent the device from inadvertent enable.

Under Voltage Lockout

A voltage sense circuit monitors the V_{DD} supply voltage for power on reset. When the V_{DD} supply input voltage is above 2.4V, the device is ready for operation. If the input voltage below approximately 2.2V, the device is in under voltage lockout state as the V_{DD} input voltage is not high enough for operation.

Output Voltage Discharge When Disabled

The device supports output discharge function. Any time when the logic input to EN is low while V_{DD} is above power on reset (POR) threshold, the device is disabled, and a 100Ω resistor is connected internally to the V_{OUT} to discharge the output capacitor. The output voltage discharge function is used to help decrease the pre-biased output, and to let the output voltage rises from 0V or a low level at next soft start operation.

Output Current Limit

The uP7567 continuous monitors the output current to protect the system power, the power switch, and the load from damage during normal operation or soft start interval. When an overload event is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the MOSFET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load. The device provides three current limit levels to choose from. The ILIM/LPM pin is a multi-function pin, and one of the two functions of this pin is current limit level selection. The voltage to the ILIM/LPM pin determines the current limit level. There is a 1.3uA constant current source internal to the ILIM/LPM pin.

This weak current source allows the pin voltage to be dominated externally. Floating state, 1MΩ to GND, and 0V are recommended input conditions to ILIM/LPM pin for current limit level selection. Note that the current limit level is forced to the highest level during soft start interval regardless of the setting level. This is to ensure a successful soft start operation even if the device is enabled with load current. At the end of soft start, PGOOD goes high if no protection is triggered. The device checks the voltage level right after PGOOD goes high to determine the current limit level. The current limit level is then latched to the selected level. After that, further voltage change at the ILIM/LPM pin does not affect the current limit level. Note that when operating in low V_{IN} (0.75V), to make current limit function operate normally, a capacitor of at least 470pF should be connected to the SS pin.

Over Temperature Protection

The uP7567 continuously monitors the operating temperature of the power switch for over temperature protection. The uP7567 asserts over temperature and turns off the power switch and into latch mode to prevent the device from damage if the junction temperature rises to approximately 140°C due to over current conditions. The switch will turn on when re-POR or re-enable occurs.

Functional Description

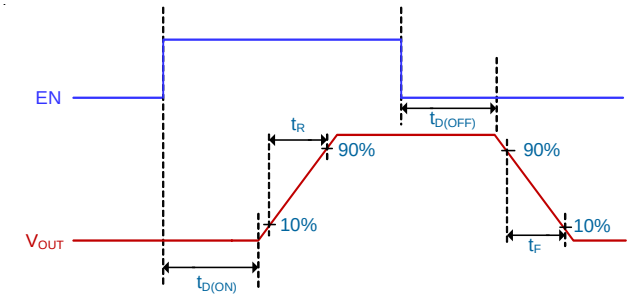
Protection Behavior

Table 1 Protection Behavior

Event	Test Condition	Device Actions	Activated After	Reset
Current Limit	After start-up period, output current > current limit threshold	Clamp output current, PGOOD keeps high	POR and Enable	Current limit event removed
Short Circuit Current	after start up period, output current > 14A (min.)	MOSFET turns off and latches. PGOOD goes low, IMON = V_{DD}	after Soft Start	Re-POR and Re-Enable
Over Temperature Protection	Tj > 140°C	MOSFET turns off and latches. PGOOD goes low. IMON = V_{DD}	POR and Enable	Re-POR and Re-Enable
Under Voltage Protection	V_{OUT} < 40%*V_{IN}	Deglitch time = 20us MOSFET turns off and latches. PGOOD goes low. IMON = V_{DD}	after Soft Start	Re-POR and Re-Enable
Output Discharge	V_{OUT} under voltage protection (V_{OUT}< 40%*V_{IN}), Logic input to EN is low, or V_{DD} supply voltage is below POR	An internal 100Ω resistor is connected to V_{OUT} for output discharge.	POR and Enable	Re-POR and Re-Enable

Soft Start

Figure 1 shows the timing diagram of EN and V_{OUT}. The uP7567 starts the soft start operation to let the output voltage ramp up after EN goes high. The soft start function is used to limit the inrush current from V_{IN} to prevent large voltage sag at V_{IN}. Connect an MLCC Css as a timing capacitor from SS pin to GND to determine the soft start time. After EN goes high, the device waits for a turn on delay time $t_{D(ON)}$ and then the output voltage begins to rise. The output voltage ramps up to the target within a time t_R. Both the rise time (or ramp up time) t_R and the turn on delay time $t_{D(ON)}$ are dependent on the capacitance to SS pin. Table 2 and Table 3 list the recommended soft start capacitor Css and the corresponding output rise time t_R and the turn on delay time t_D.



Notes:

- t_R:Rising Time
- t_F:Falling Time
- $t_{D(ON)}$:Turn On Delay Time
- $t_{D(OFF)}$:Turn Off Delay Time

Figure 1. Enable and Soft Start Timing Diagram

Functional Description

Table 2. Css vs. Soft Start Time

Soft Start Time (us), V_{DD} = 5V, Cout = 10uF/6.3V/X5R/0603							
Css(nF)	V_{IN} = 5V	V_{IN} = 3.3V	V_{IN} = 1.8V	V_{IN} = 1.5V	V_{IN} = 1.2V	V_{IN} = 1.05V	V_{IN} = 0.8V
0 (open circuit)	9	8	7.1	6.8	6.2	5.9	5.6
1	117.8	70.9	38	31.4	25.6	24.2	20.6
2	230	125	71	61.2	50.7	45.5	36
3.3	350	209	113	92.6	74.6	67.6	52.6
4.7	529	297	152	124	103	92	73
10	1324	746	402	346	271	225	185
33	3822	2276	1174	905	772	675	524
47	5234	3000	1562	1322	1068	933	727
100	11530	6968	3350	3184	2132	1932	1534

Table 3. Css vs. Turn On Delay Time

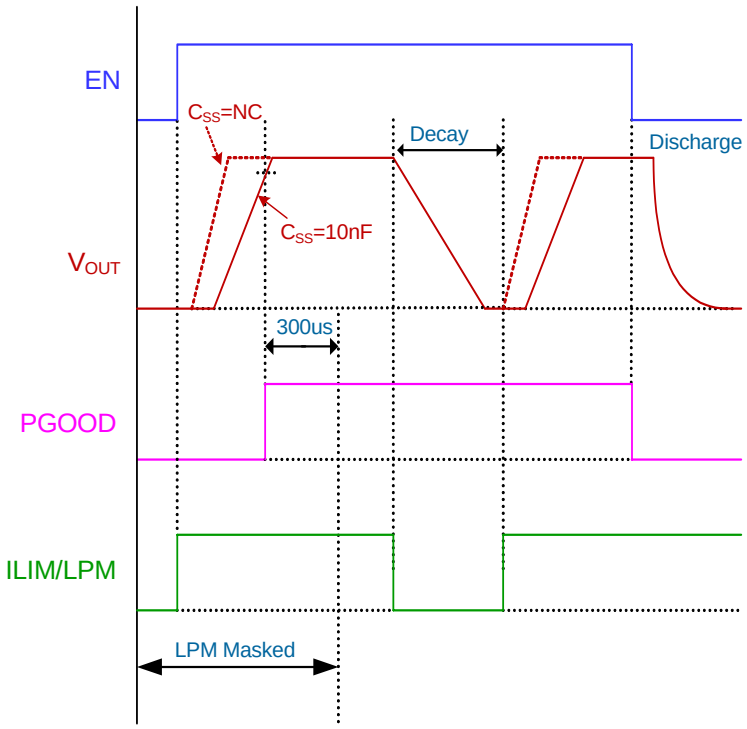
Turn On Delay Time (us), V_{DD} = 5V, Cout = 10uF/6.3V/X5R/0603							
Css(nF)	V_{IN} = 5V	V_{IN} = 3.3V	V_{IN} = 1.8V	V_{IN} = 1.5V	V_{IN} = 1.2V	V_{IN} = 1.05V	V_{IN} = 0.8V
0 (open circuit)	16	16.5	16.7	16.8	17	17.1	17.3
1	29.6	29.9	30	30.2	30.6	30.6	24.3
2	36	37.1	37.7	38	38.5	39	34
3.3	42.6	42.5	44.6	44.7	45	45.2	45.5
4.7	52	54	54.6	55	56.2	56.5	57
10	120	121	124	128	132	133	135
33	250	260	266	270	275	280	282
47	320	330	350	360	372	385	395
100	752	772	800	816	828	836	868

Functional Description

Low Power Mode

The uP7567 supports low power mode (LPM) operation, which is used to further decrease the power consumption of the notebook computer system as the computer system enters C10 state. The enter/exit of LPM is controlled by the logic input to ILIM/LPM pin. Figure 2 shows the timing diagram of LPM operation. The LPM operation is valid only when the highest current limit level is selected (ILIM/LPM pin is floating). The device enters LPM when the ILIM/LPM is pulled low (<0.5V). In LPM, the power switch is turned off, PGOOD is kept high, and the output voltage decays naturally. The output is not discharged when the device is in LPM. The device exit LPM to normal mode when ILIM/LPM is pulled high (>0.5V) or floating. The soft start operation resumes, and the device goes back to normal operation. Note that the initial state of ILIM/LPM must be high, which means the LPM is only allowed once the device works in normal mode. In addition, also note that the LPM has has a 300us mask time, which means the LPM is only entered 300us after PGOOD goes high.

Figure 3 shows the device operation when the highest current limit level is not selected. The device does not respond to the ILIM/LPM input when the highest current limit level is not selected.

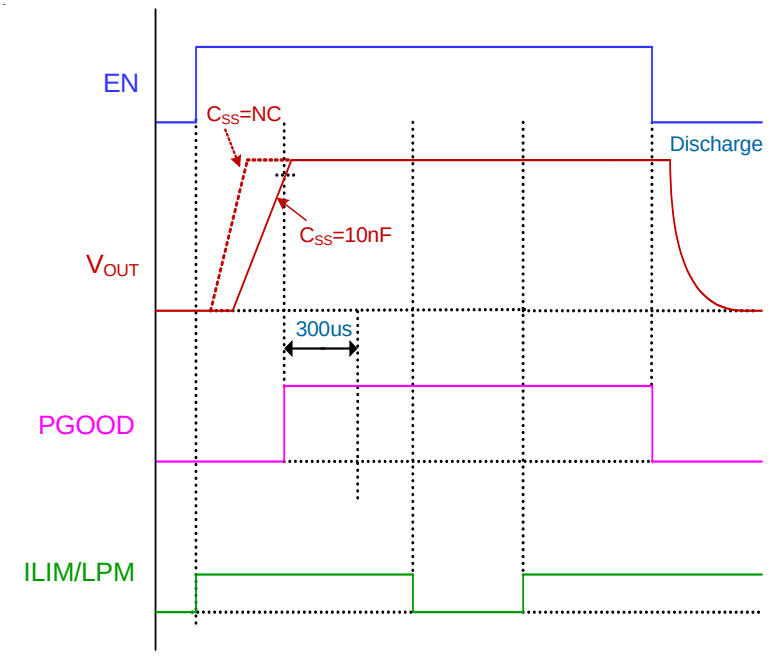


Notes:

- Low power mode is active after PGOOD goes high+300us
- V_{OUT} decays (no discharge) when ILIM/LPM goes low
- PGOOD is kept high during LPM/normaloperation mode change

Figure 2. Low Power Mode Timing Diagram (ILIM/LPM is floating)

Functional Description



Notes:

- The device does not respond to ILIM/LPM input when the highest current limit level is not selected.

Figure 3. Low Power Mode Timing Diagram (ILIM/LPM = 1MΩ)

Absolute Maximum Rating

(Note 1)

Input Voltage, V_{IN} ---------- -0.3V to +6V
Supply Voltage, V_{DD} ---------- -0.3V to +6V
Output Voltage, V_{OUT} to GND ---------- -0.3V to +6V
Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV

Thermal Information

Package Thermal Resistance (Note 3)
UQFN2x3-17L θ_{JA} ---------- 137°C/W
UQFN2x3-17L θ_{JC} ---------- 10.6°C/W
Power Dissipation, P_D @ T_A = 25°C
UQFN2x3-17L P_D ---------- 0.73W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{DD} ---------- +3.0V to +5.5V
Supply Input Voltage, V_{IN} ---------- +0.7V to V_{DD}

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guarantee by design.

Electrical Characteristics

(V_{IN} = V_{DD} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Input Voltage	V_{IN}		0.7	--	5.5	V
Supply Voltage	V_{DD}		3.0	--	5.5	V
VDD Supply Current	I_{VDD}	No load	--	30	50	uA
VDD Supply Current at Shutdown	I_{VDDSD}	V_{DD} = 5V, V_{EN} = 0V , no load	--	--	1	uA
VIN Supply Current	I_{VIN}	No load	--	10	20	uA
VIN Supply Current at Shutdown	I_{VIN_OFF}	V_{DD} = V_{IN} = 5V, V_{EN} = 0V, no load	--	0.1	8	uA
		V_{DD} = 5V, V_{IN} = 3V, V_{EN} = 0V, no load	--	0.1	3	
		V_{DD} = 5V, V_{IN} = 1.8V, V_{EN} = 0V, no load	--	0.1	2	
		V_{DD} = 5V, V_{IN} = 0.7V, V_{EN} = 0V, no load	--	0.1	1	
VOUT Leakage Current		V_{OUT} = 5.5V, V_{IN} = 5V, EN goes low	--	--	1	uA
Power On Reset (POR)						
Rising VDD POR Voltage	V_{DD_POR}	V_{DD} rising	2.1	2.4	2.7	V
VDD UVLO Hysteresis	V_{DD_HYS}	V_{DD} = 3V to 5.5V	--	0.2	--	V
EN Input Voltage						
Input Logic High		V_{DD} = 3V to 5V	1.7	--	--	V
Input Logic Low		V_{DD} = 3V to 5V	--	--	0.8	V
Pull Down Resistance		V_{DD} = 5V	--	6	--	MΩ
Turn On Delay Time	$T_{D(ON)}$	From Enable to V_{OUT} rising, Css = 0pF (open circuit)	10	--	30	us
Turn Off Delay Time	$T_{D(OFF)}$	From Disable to V_{OUT} falling, Css = 0pF (open circuit)	--	6	--	us
Power Switch Resistance						
Power Switch On Resistance	$R_{DS(ON)}$	V_{DD}=5V & 3.3V, I_{OUT} = 6A, T_A = 25°C	--	12	15	mΩ
		V_{DD}=5V & 3.3V, I_{OUT} = 6A, T_A = -40°C to 125°C	--	--	20	
VOUT Discharge Resistance	R_{DIS}	V_{OUT} forced at 1V, V_{EN}=0V	--	100	150	Ω
Thermal Protection						
Shutdown Level Threshold(Note 1)			--	140	150	°C

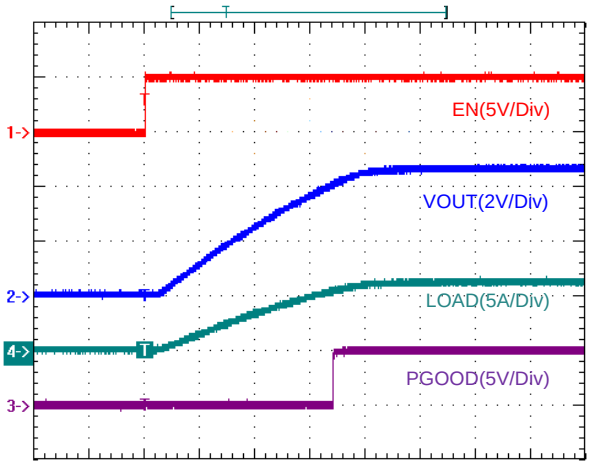
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Current Limit						
Current Limit Threshold	I_{LIM}	ILIM connected to GND	3	--	3.3	A
		Accuracy	-5	--	5	%
		ILIM connected to 1MΩ resistor to GND	5	--	5.5	A
		Accuracy	-5	--	5	%
		ILIM floating (Note 2)	8	--	8.8	A
		Accuracy	-5	--	5	%
Power Good Indicator						
PGOOD High Threshold		PGOOD goes high, measure V_{OUT}	80	85	90	$\%V_{IN}$
PGOOD Low Threshold		PGOOD goes low, measure V_{OUT}	35	40	45	$\%V_{IN}$
PGOOD Pull Low Voltage		PGOOD sinks to 5mA	--	0.25	--	V
PGOOD Debounce Time(Note 1)		High to low	--	20	--	us
Short Circuit Current Threshold						
Short Circuit Current Trip Threshold(Note 1)	I_{SCP}		14	--	--	A
Response Time of Short Circuit Current(Note 1)	T_{SCP}		--	--	1	us
Current Monitor Parameter						
IOUT Current to IMON Current Gain		I_{OUT}/I_{IMON}	--	5400	--	A/A
IMON Current Accuracy (with Gain Error)	I_{IMON}	I_{OUT} = 0.5A	-20	--	20	%
		I_{OUT} = 3A	-7.5	--	7.5	%
		I_{OUT} = 6A	-5	--	5	%

Note 1: Guaranteed by design
Note 2: The current limit level is forced to the higher level during soft start interval.

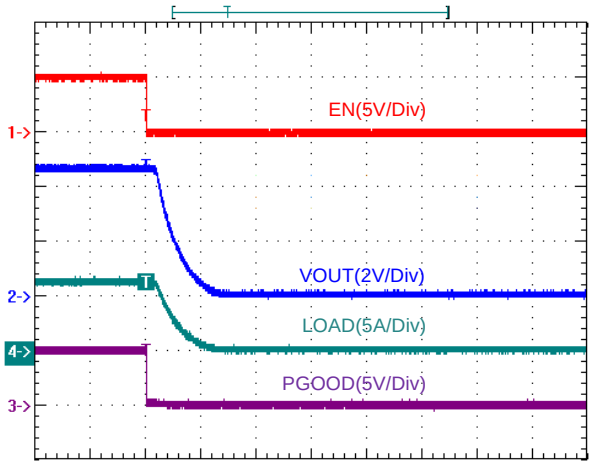
Typical Operation Characteristics

Power On from EN



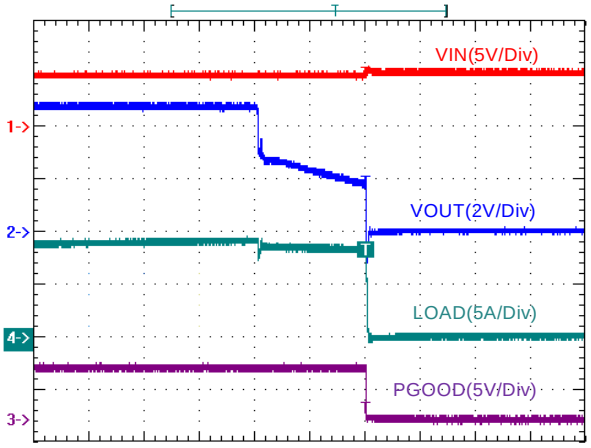
Time: 400us/Div
V_{IN}=5V, R_{ILIM} = NC, C_{SS}=10nF, Load=0.8Ω

Power Off from EN



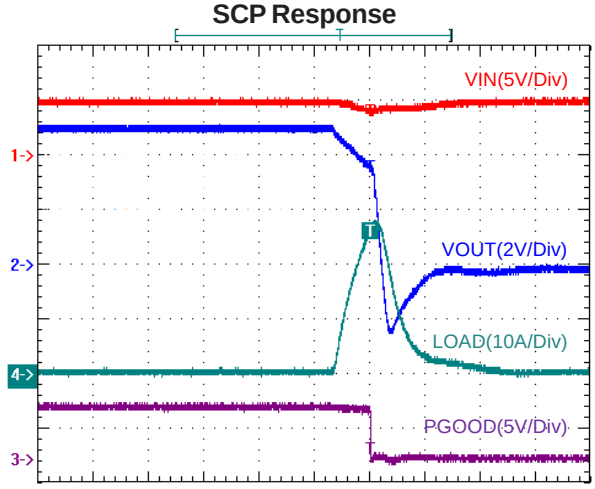
Time: 400us/Div
V_{IN}=5V, R_{ILIM} = NC, C_{SS}=10nF, Load=0.8Ω

Current Limit Response



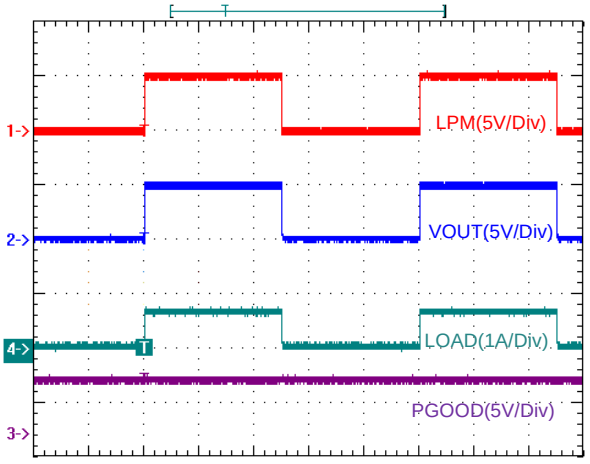
Time: 200us/Div
V_{IN}=5V, R_{ILIM} = NC, C_{SS}=NC

SCP Response



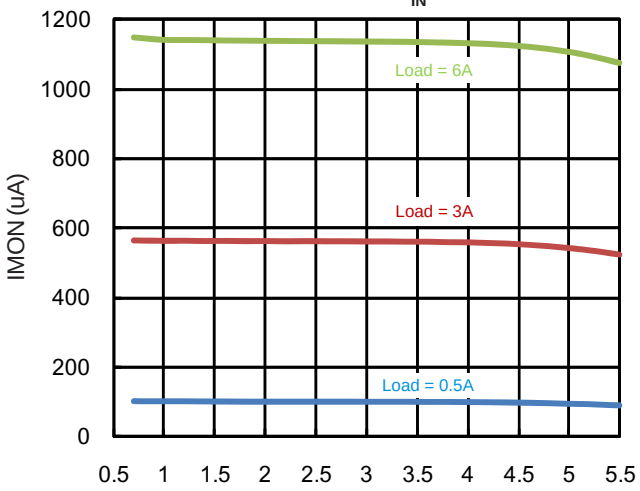
Time: 2us/Div
V_{IN}=5V, R_{ILIM} = NC, C_{SS}=NC

LPM Response



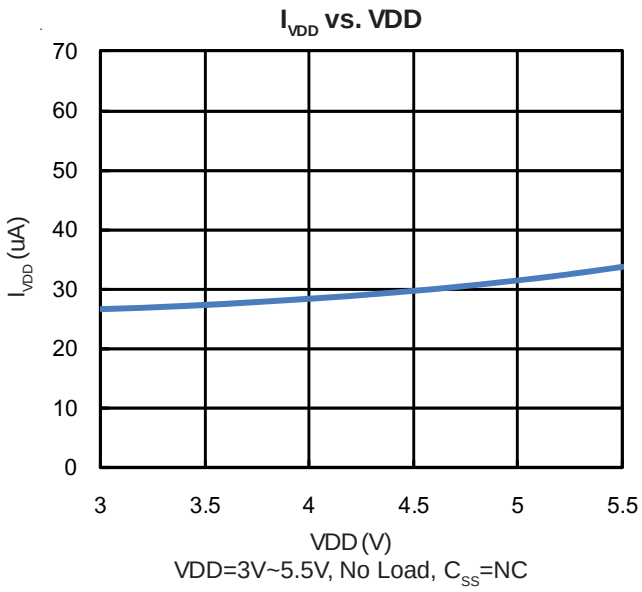
Time: 20ms/Div
V_{IN} =5V, Load=8Ω, C_{SS}=NC

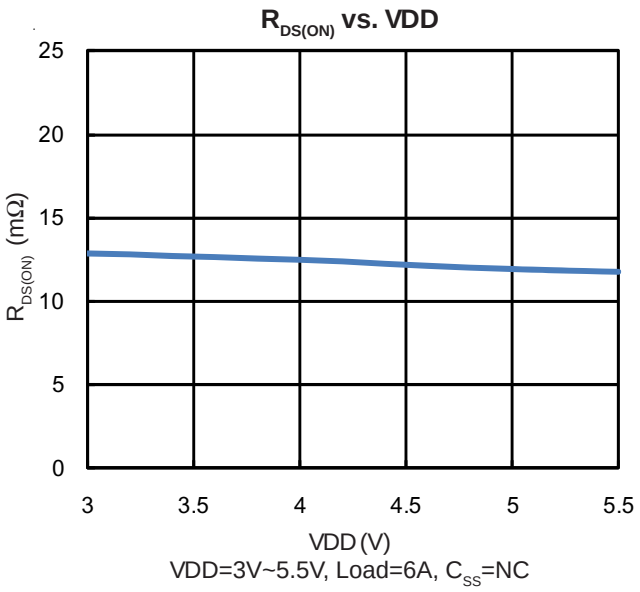
IMON vs. V_{IN}



VDD=5V, R_{ILIM} = NC, C_{SS}=NC

Typical Operation Characteristics





Application Information

Supply Input Filtering

VIN pins supply power to the power switch and internal circuit. Both of them should be connect to upstream power supply with short and wide trace on the PCB. Events such as hot-plug/unplug, output short circuit and over temperature result in step change of input current with sharp edges, which in turn causes voltage transient at supply input due to di/dt effect of parasitic inductance on the current path. A 22uF ceramic capacitor from V_{IN} to GND, physically located near the device is strongly recommended to control the supply input transient. Minimizing the parasitic inductance along the current path also alleviate the voltage transient at the supply input.

Output Voltage Filtering

Bypassing the output voltage with a 1uF ceramic capacitor improves the immunity of the device against output short circuit and hot plug/unplug of load. A lower ESR capacitor results in lower voltage drop against a step load change. A large electrolytic capacitor from V_{OUT} to GND is also recommended. This capacitor reduces power supply transient that may cause ringing on the input. USB supports dynamic attachment (hot plug-in) of peripherals. A current surge is caused by the input capacitance of downstream device. Ferrite beads are recommended in series with all power and ground connector pins. Ferrite beads reduce EMI and limit the inrush current during hot-attachment by filtering high-frequency signals. The DC resistance of the ferrite bead should be specially taken care to reduce the voltage drop.

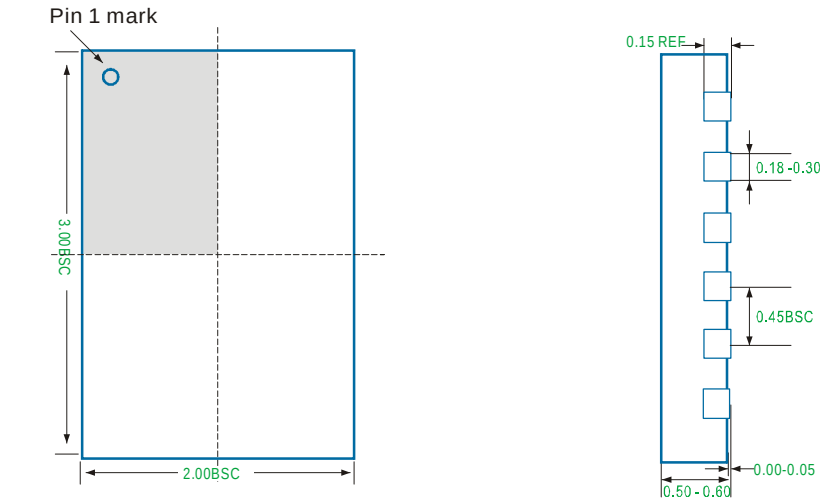
Layout Consideration

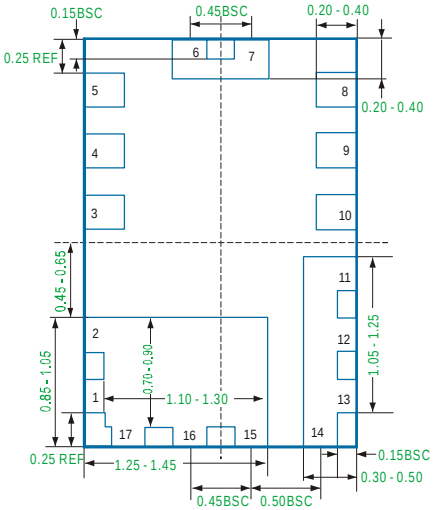
The power circuitry of USB printed circuit boards requires a customized layout to maximize thermal dissipation and to minimized voltage drop and EMI

- Place the device physically as close to the USB port as possible. Keep all traces wide, short and direct to minimized the parasitic inductance.This optimizes the switch response time to output short circuit conditions.
- Place both input and output bypass capacitors near to the device.
- All VOUT pins should be connected together on the PCB. All VIN pins should be connected together on the PCB.

Package Information

UQFN2x3-17L



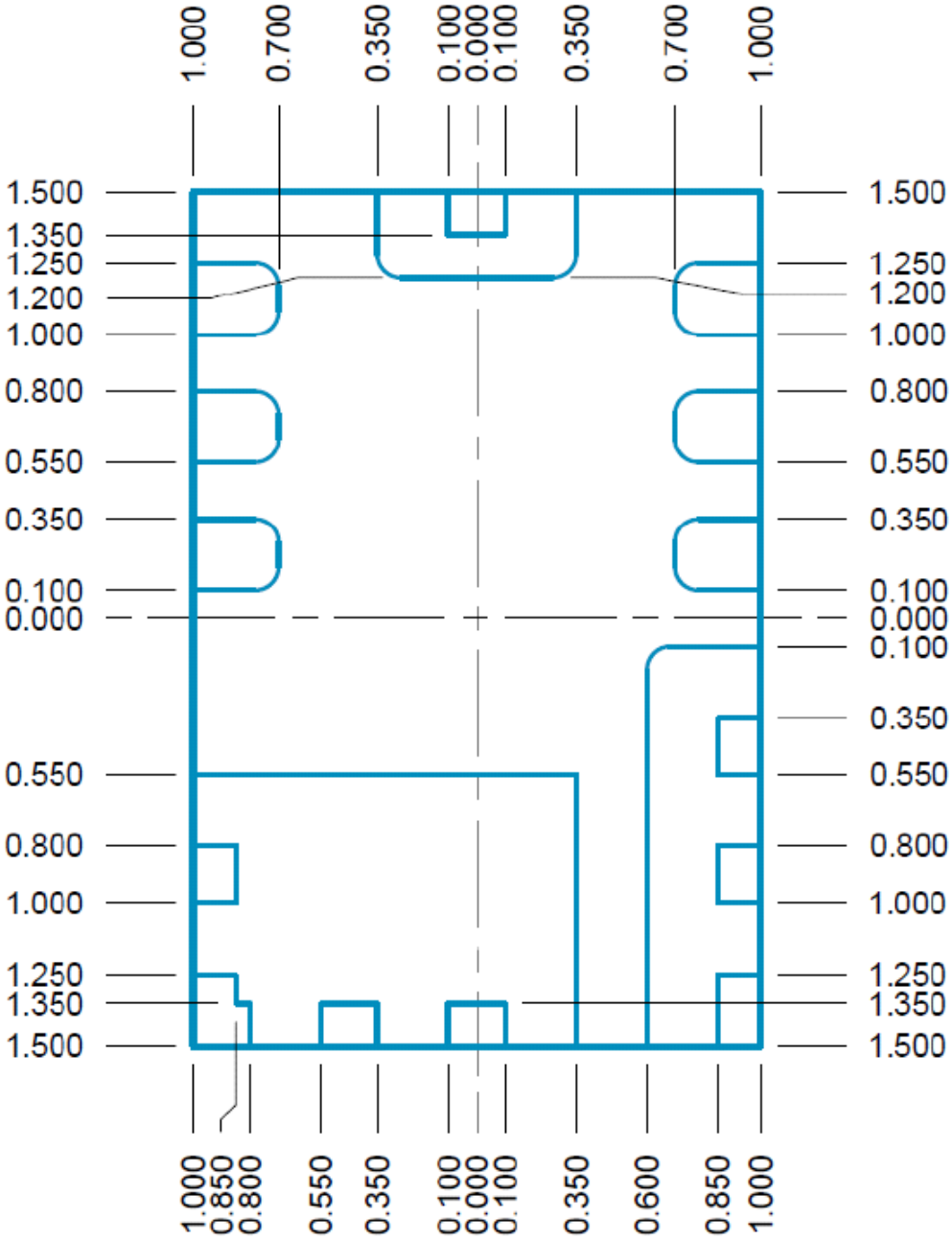


Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Package Information

Reference Dimension



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