2A Ultra Low Dropout Linear Regulator

General Description

The uP7704 is a 2A ultra low dropout linear regulator specifically designed for motherboard, notebook and graphic card applications. This device works with dual supplies, a control input for the control circuitry and a power input as low as 1.2V for providing current to output. The uP7704 delivers high-current and ultra-low-drop output voltage as low as 0.8V for applications where V_{OUT} is very close to V_{IN}.

The uP7704 features comprehensive control and protection functions: a power on reset (POR) circuit for monitoring both control and power inputs for proper operation; an EN input for enabling or disabling the device, a power OK with time delay for indicating the output voltage status, a foldback current limit function, and a thermal shutdown function.

The uP7704 is available in PSOP-8 or WDFN3x3-10L packages with very low thermal resistance.

Applications

- ☐ Desktop PCs, Notebooks, and Workstations
- ☐ Graphic Cards
- ☐ Low Voltage Logic Supplies
- ☐ Microprocessor and Chipset Supplies
- ☐ Split Plane Microprocessor Supplies
- ☐ Advanced Graphics Cards Supplies
- ☐ SoundCards and Auxiliary Power Supplies
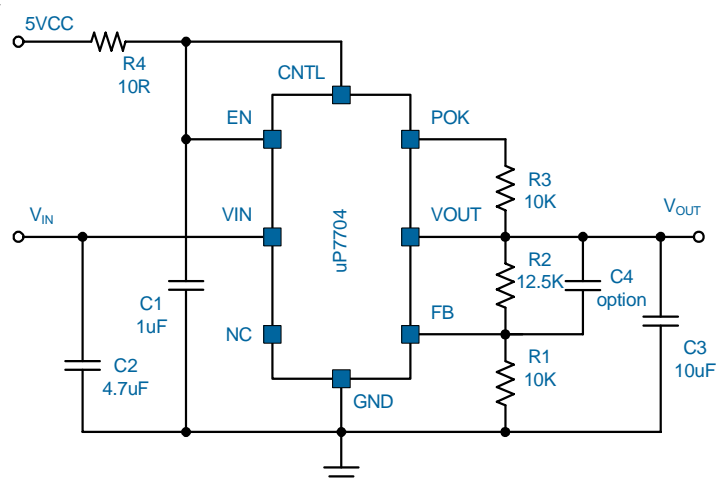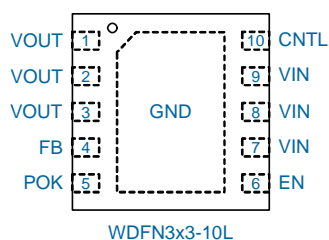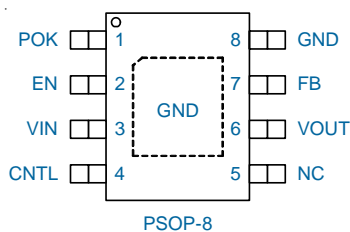- ☐ SMPS Post Regulators

Features

- ☐ Works with 1.2V~5.5V V_{IN}
  - ■ Adjustable Output Voltage, Down to 0.8V
  - ■ 1.5% Initial Accuracy
  - ■ Excellent Line and Load Regulation
- ☐ 2A Guaranteed Output Current
  - ■ 300mV @ 2A Dropout Voltage
- ☐ Very Low On-Resistance
  - ■ 150mΩ typical
- ☐ V_{OUT} Pull Low Resistance when Disabled
- ☐ V_{OUT} Power OK Signal
- ☐ Fast Transient Response
- ☐ Low External Component Count
- ☐ Low Cost and Easy to Use
- ☐ Enable Pin
- ☐ Over Current and Over Temperature Protection

Ordering Information

Order Number	Package Type	Remark
uP7704U8	PSOP-8	
uP7704ADDA	WDFN3x3-10L	

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 and RoHS requirements. They are 100% matte tin (Sn) plating and suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration & Typical Application Circuit

PSOP-8

WDFN3x3-10L

Functional Pin Description

Pin No.		Name	Pin Function
PSOP	**WDFN**		
1	5	POK	**Power OK Indication.** This pin is an open-drain output and is set high impedance once V_{OUT} reaches 90% of its rating voltage.
2	6	EN	**Enable Input.** Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value.
3	7, 8, 9	VIN	**Input Voltage.** This is the drain input to the power device that supplies current to the output pin. Large bulk capacitors with low ESR should be placed physically close to this pin o prevent the input rail from dropping during large load transient. A 4.7uF ceramic capacitor is recommended at this pin. V_{IN} cannot be forced higher than V_{CNTL} otherwise the current limit function may be false triggered and disable the output voltage.
4	10	CNTL	**Supply Input for Control Circuit.** This pin provides bias voltage to the control circuitry and driver for the pass transistor.The driving capability of output current is proportioned to the V_{CNTL}. For the device to regulate, the voltage on this pin must be at least 1.5V greater than the output voltage, and no less than V_{CNTL_MIN}.
5	X	NC	**Not Internally Connected**
6	1, 2, 3	VOUT	**Output Voltage.** This pin is power output of the device. A pull low resistance exists when the device is disabled by pulling low the EN pin. To maintain adequate transient response to large load change, typical value of 1000uF Al electrolytic capacitor with 10uF ceramic capacitors are recommended to reduce the effects of current transients on VOUT.
7	4	FB	**Feedback Voltage.** This pin is the inverting input to the error amplifier. A resistor divider from the output to GND is used to set the regulation voltage as $V_{OUT} = 0.8 \times (R1+R2)/R1$ (V)
8	X	GND	**Ground.**
Exposed Pad		GND	**Ground.** The exposed pad acts the dominant power dissipation path and should be soldered to well designed PCB pads as described in the *Application Informations Chapter.*

Functional Block Diagram
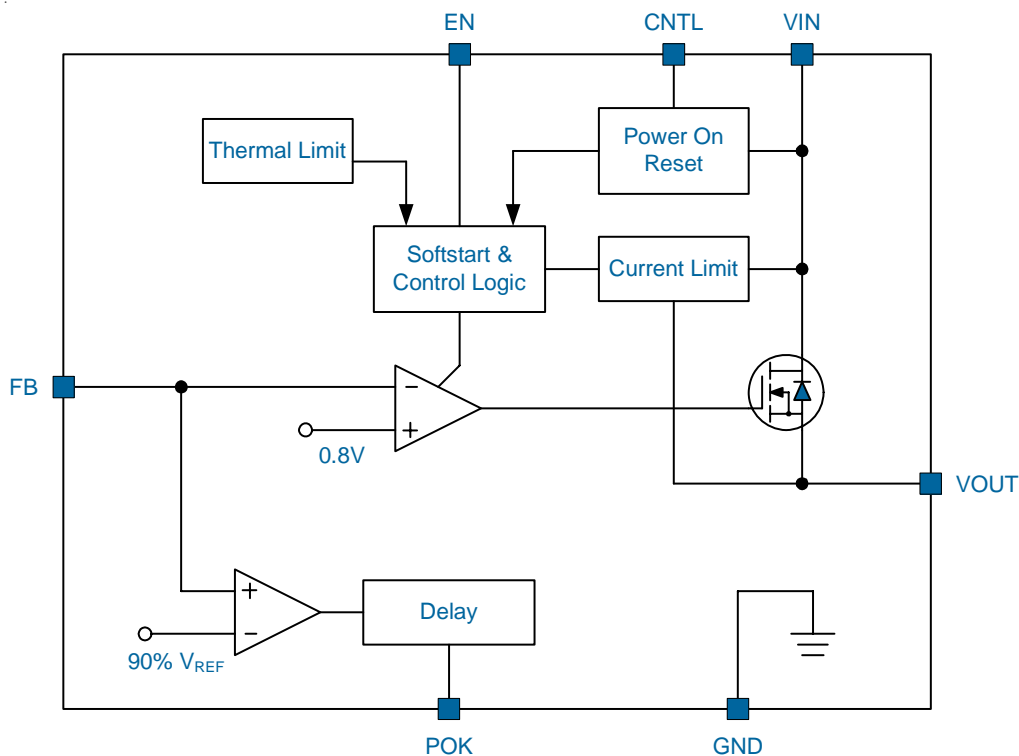
Definitions

Some important terminologies for LDO are specified below.

Dropout Voltage

The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 2% below its nominal value. Dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Load Regulation

The change in output voltage for a change in load current at constant chip temperature. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Maximum Power Dissipation

The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Bias Current

Current which is used to operate the regulator chip and is not delivered to the load.

The quiescent current I_Q is defined as the supply current used by the regulator itself that does not pass into the load. It typically includes all bias currents required by the LDO and any drive current for the pass transistor.

Initialization

The uP7704 automatically initiates upon the receipt of supply voltage and power voltage. A power on reset circuit continuously monitors VIN and CNTL pins voltages with rising threshold levels of 0.6V and 2.7V respectively.

Chip Enable and Soft Start

The uP7704 features an enable pin for enable/disable control of the chip. Pulling V_{EN} lower than 0.4V disables the chip and reduces its quiescent current down to 25uA. When disabled, an internal MOSFET of 50Ω $R_{DS(ON)}$ turns on to pull output voltage to ground. Pulling V_{EN} higher than 1.4V enables the output voltage, providing POR is recognized. The uP7704 features soft start function that limits inrush current for charging the output capacitors. The soft start time is typically 4ms.

Output Voltage Programming

Figure 1 shows a typical application of 2.5V to 1.8V conversion with a 5.0V control supply. The output voltage is sensed through a voltage divider and regulated to internal reference voltage V_{REF}. The output voltage is programmed as:

$$V_{OUT} = V_{REF} \times (R_1 + R_2) / R_1 = 0.8V \times (22.5k/10k) = 1.8V$$

It's recommended to maintain 50-100uA through the output divider network for a tight load and line regulation. The internal voltage reference is $V_{REF} = 0.8V$ with 1.5% initial accuracy. This commands the use of 0.5% or better accuracy resistors to build a precision power supply.
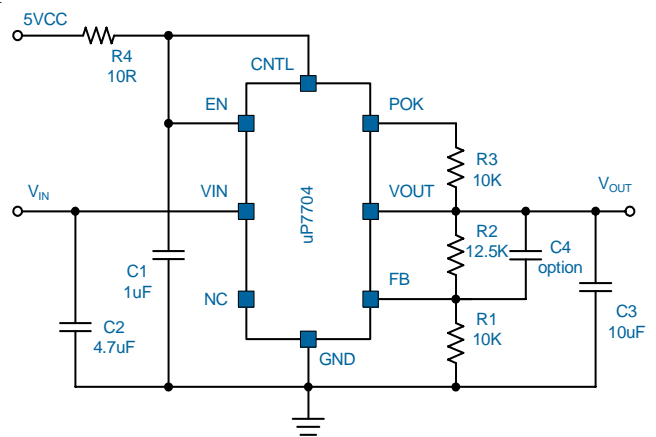

Figure 1. Typical application of 2.5V to 1.8V conversion with a 5.0V control supply

Over Current and Short Circuit Protection

The uP7704 features a foldback over current protection function as shown in Figure 2. The current limit threshold level is proportional to V_{OUT}/V_{NOM} and is typically 2.5A when $V_{OUT} = V_{NOM}$, where V_{NOM} is the target output voltage. If the output continuously demands more current than the maximum current, output voltage will eventually drops below its nominal value. This, in turns, will lower its OCP threshold level. This will limit power dissipation in the device when over current limit happens.

When output short circuit occurs, the uP7704 will try to rebuild the output voltage with maximum allowable current as shown if Figure 3. The duty cycle is about 20% and the averaged short circuit current is about 400mA.
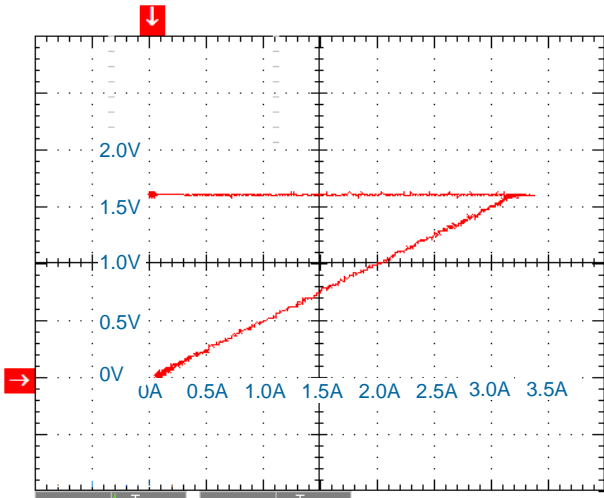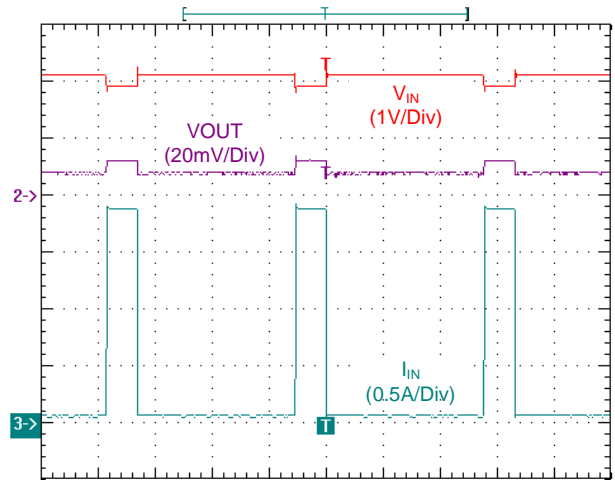
Figure 2. Current Limit Behavior

Figure 3. Output Short Circuit Protection

Absolute Maximum Rating

Control Input Voltage V_{CNTL} (Note 1) -- -0.3V to +7V
Power Input Voltage V_{IN} --- -0.3V to +7V
Other Pins --- -0.3V to (V_{CNTL} + 0.3V)
Storage Temperature Range --- -65°C to +150°C
Junction Temperature --- 150°C
Lead Temperature (Soldering, 10 sec) --- 260°C
ESD Rating (Note 2)
    HBM (Human Body Mode) --- 2kV
    MM (Machine Mode) -- 200V

Thermal Information

Package Thermal Resistance (Note 3)
    PSOP-8 θ_{JA} --- 52°C/W
    PSOP-8 θ_{JC} --- 5°C/W
    WDFN3x3-10L θ_{JA} -- 60°C/W
    WDFN3x3-10L θ_{JC} --- 5°C/W
Power Dissipation, P_D @ T_A = 25°C
    PSOP-8 -- 1.9W
    WDFN3x3-10L θ_{JA} --- 1.67W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) -- -40°C to +125°C
Operating Ambient Temperature Range -- -40°C to +85°C
Supply Input Voltage, V_{CNTL} -- +3.0V to +5.5V
Power Input Voltage, V_{IN} --- +1.0V to V_{CNTL}

Electrical Characteristics

(V_{CNTL} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input Voltage						
Control Input Voltage	V_{CNTL}	$V_{OUT} = V_{REF}$	2.9	--	6	V
POR Threshold	$V_{CNTLRTH}$		2.5	2.7	2.9	V
POR Hysteresis	$V_{CNTLHYS}$		0.1	0.2	--	V
Power Input Voltage	V_{IN}	$V_{OUT} = V_{REF}$	1.0	--	V_{CNTL}	V
Control Input Current in Shutdown	I_{CNTL_SD}	$V_{CNTL} = V_{IN} = 5.0V$, $I_{OUT} = 0A$, $V_{EN} = 0V$	--	20	30	uA
Control Input Current	I_{CNTL}	$V_{CNTL} = V_{IN} = V_{EN} = 5.0V$, $I_{OUT} = 0A$, $V_{OUT} = V_{REF}$	--	0.3	0.6	mA
Quiescent Current	I_Q	$V_{CNTL} = V_{IN} = V_{EN} = 5.0V$, $I_{OUT} = 0A$, $V_{OUT} = V_{REF}$	--	0.3	0.6	mA
Feedback Voltage						
Reference Voltage	V_{REF}	$V_{CNTL} = V_{IN} = V_{EN} = 5.0V$, $I_{OUT} = 0A$. $V_{OUT} = V_{REF}$	0.788	0.8	0.812	V
Feedback Input Current	I_{FB}		--	20	--	nA
V_{IN} Line Regulation	$V_{REF(LINE)}$	$1.2V < V_{IN} < 5.0V$, $V_{CNTL} = V_{EN} = 5.0V$, $I_{OUT} = 0A$. $V_{OUT} = V_{REF}$	--	0.01	0.1	%/V
V_{CNTL} Line Regulation	$V_{REF(CNTL)}$	$3.0V < V_{CNTL} < 5.0V$, $V_{IN} = 1.2V$, $I_{OUT} = 0A$. $V_{OUT} = V_{REF}$	--	0.01	0.1	%/V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Feedback Voltage						
Load Regulation	$V_{REF(LOAD)}$	0mA < I_{OUT} < 2.0A, V_{CNTL} = V_{IN} = V_{EN} = 5.0V, V_{OUT} = V_{REF}	--	0.1	0.5	%/A
Load Regulation over Temperature	$V_{REF(TOTAL)}$	0mA < I_{OUT} < 2.0A, V_{CNTL} = V_{IN} = V_{EN} = 5.0V, V_{OUT} = V_{REF}, -40°C < T_J < 125°C, by design	--	0.5	3	%
On Resistance	$R_{DS(ON)}$	I_{OUT} = 100mA, V_{CNTL} = V_{EN} = 5.0V, V_{OUT} = 1.6V	--	150	250	mΩ
Dropout Voltage	V_{DROP}	I_{OUT} = 2.0A, V_{CNTL} = V_{EN} = 5.0V, V_{OUT} = 1.6V, by design	--	300	500	mV
V_{OUT} Pull Low Resistance		V_{CNTL} = V_{IN} = 5.0V, V_{EN} = 0V,	--	50	--	Ω
Enable						
Enable High Level	V_{EN}		1.4	--	--	V
Disable Low Level	V_{SD}		--	--	0.4	V
EN Source Current	I_{EN}	V_{EN} = 0V, V_{CNTL} = 5.0V	--	10	20	uA
EN Input Impedance	Z_{EN}		--	65	--	KΩ
Output Voltage Ramp Up Time			1.5	3.0	4.5	ms
PWROK						
FB Power OK Threshold	V_{POKTH}	I_{OUT} = 0A, V_{CNTL} = V_{IN} = V_{EN} = 5.0V, V_{OUT} = V_{REF}	--	92	--	%
Power OK Hysteresis	V_{POKHYS}	I_{OUT} = 0A, V_{CNTL} = V_{IN} = V_{EN} = 5.0V, V_{OUT} = V_{REF}	--	8	--	%
POK Delay Time		From V_{OUT} > 92% V_{NOM} to POK rising	2	4	6	ms
Overcurrent Protection						
OCP Threshold Level	I_{OCP}	V_{CNTL} = V_{IN} = V_{EN} = 5.0V, V_{OUT} = V_{REF}	2.5	2.8	--	A
Averaged Output Short Circuit Current	I_{SC}	V_{CNTL} = V_{IN} = V_{EN} = 5.0V, V_{OUT} = 0V	100	400	--	mA
Thermal Protection						
Thermal Shutdown Temperature	T_{SD}	I_{OUT} = 0A, V_{CNTL} = V_{IN} = V_{EN} = 5.0V, V_{OUT} = V_{REF}	--	170	--	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	I_{OUT} = 0A, V_{CNTL} = V_{IN} = V_{EN} = 5.0V, V_{OUT} = V_{REF}	--	30	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

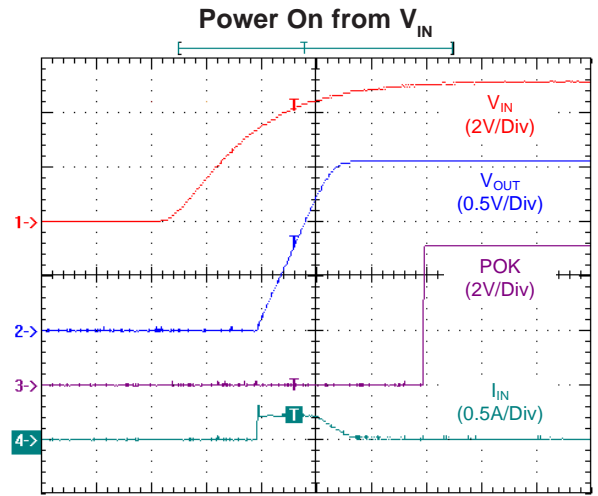**Note 2.** Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

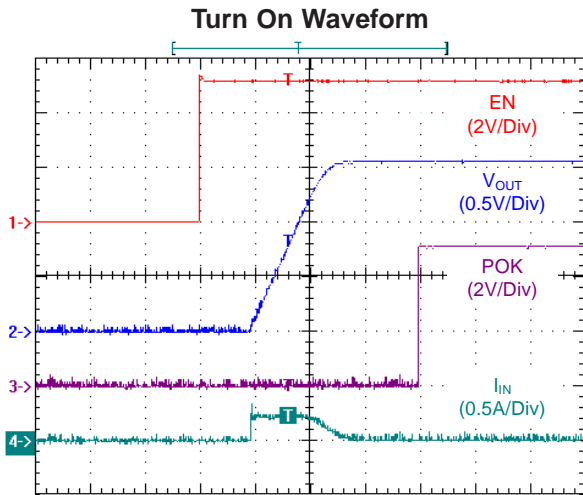**Note 4.** The device is not guaranteed to function outside its operating conditions.
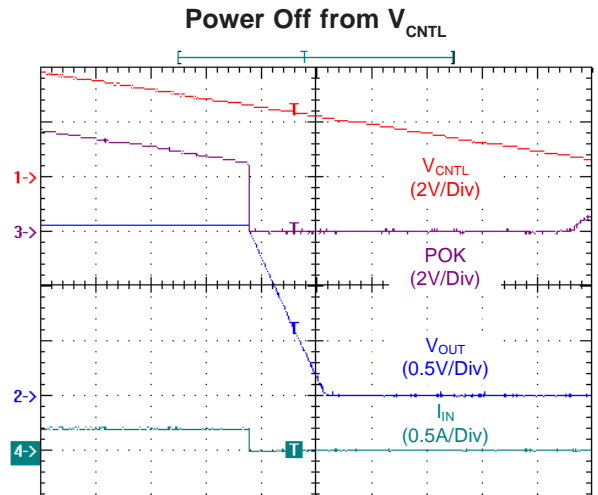
Typical Operation Characteristics
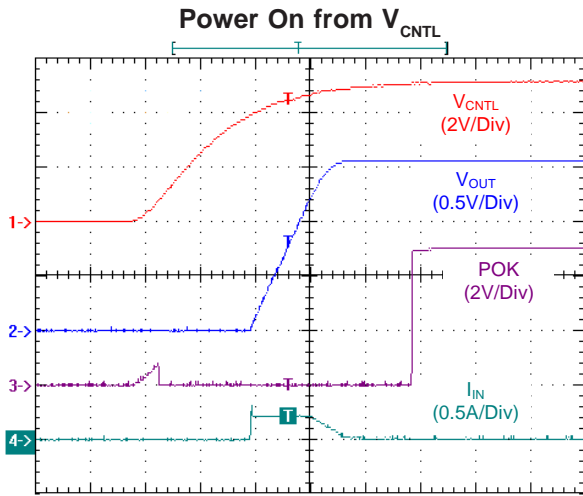
Power On from V$_{CNTL}$

2.5ms/Div
V$_{CNTL}$ = V$_{IN}$ = 5V, C$_{OUT}$ = 470uF, No Load.

Power On from V$_{IN}$

2.5ms/Div
V$_{CNTL}$ = V$_{IN}$ = 5V, C$_{OUT}$ = 470uF, No Load.

Turn On Waveform

2.5ms/Div
V$_{CNTL}$ = V$_{IN}$ = 5V, C$_{OUT}$ = 470uF, No Load.

Power Off from V$_{CNTL}$

2.5ms/Div
V$_{IN}$ = 5V, C$_{OUT}$ = 470uF, I$_{OUT}$ = 0.2A.

Power Off from V$_{IN}$
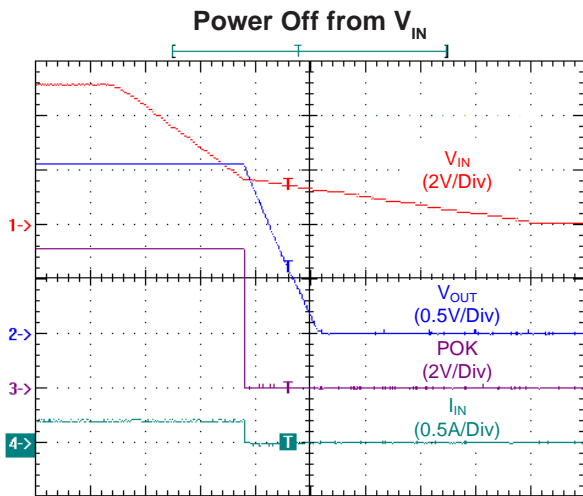
2.5ms/Div
V$_{CNTL}$ = 5V, C$_{OUT}$ = 470uF, I$_{OUT}$ = 0.2A.

Turn Off Waveforms
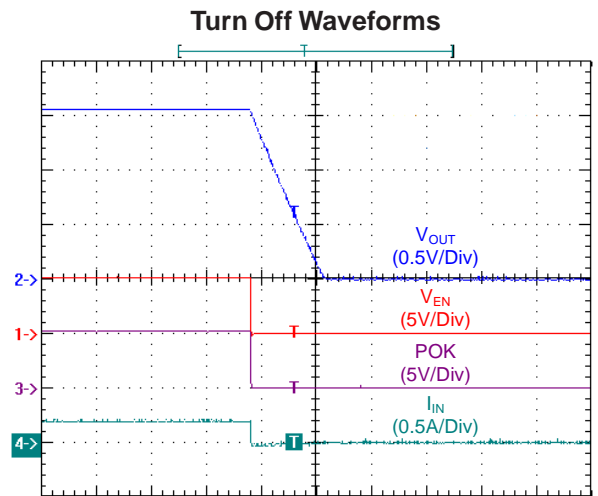
2.5ms/Div
V$_{CNTL}$ = V$_{IN}$ = 5V, C$_{OUT}$ = 470uF, I$_{OUT}$ = 0.2A.

Typical Operation Characteristics

Load Transient Response
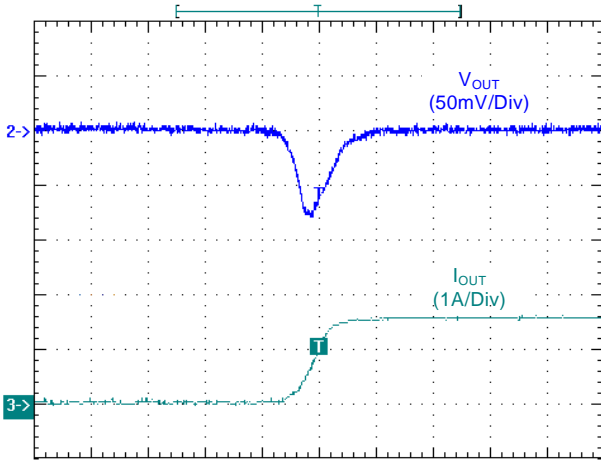
2.5us/Div

$V_{CNTL} = 5V$, $C_{OUT} = 4.7uF$, $I_{OUT} = 0A$ to $1.6A$

Dropout Voltage vs. Output Current
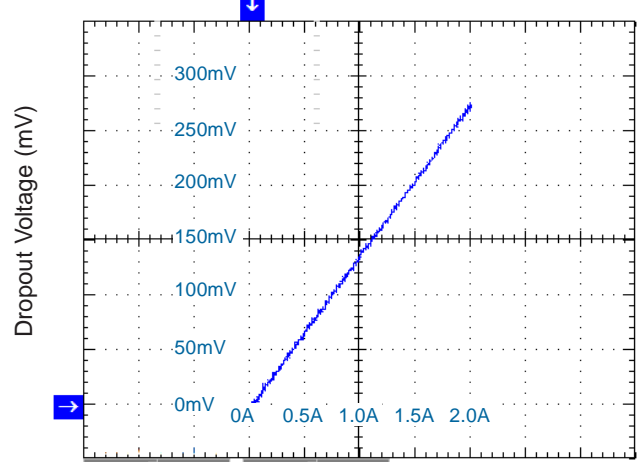
Output Current (A)

Quiescent Current vs. Input Voltage
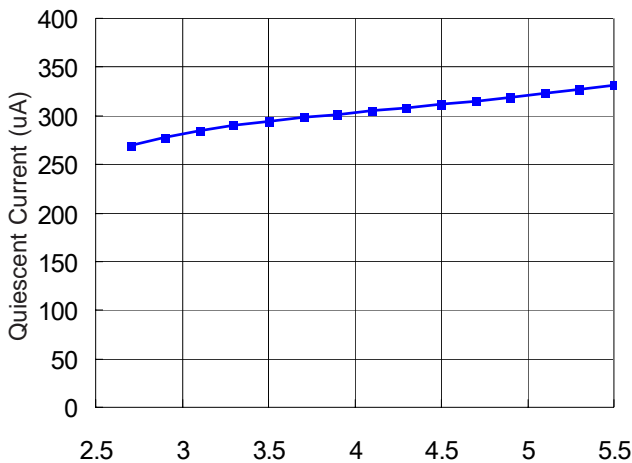
$V_{IN} = V_{CNTL}$ (V)
$V_{OUT} = V_{REF}$

Enable/Disable Threshold vs. Input Voltage
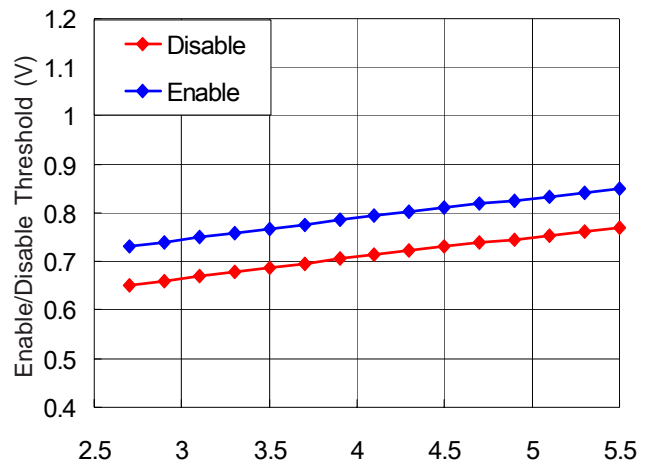
$V_{IN} = V_{CNTL}$ (V)
$V_{OUT} = V_{REF}$

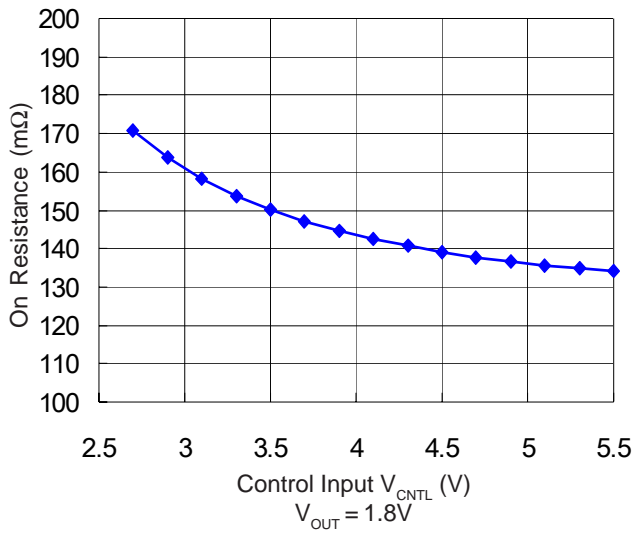### Output Voltage Line Regulation
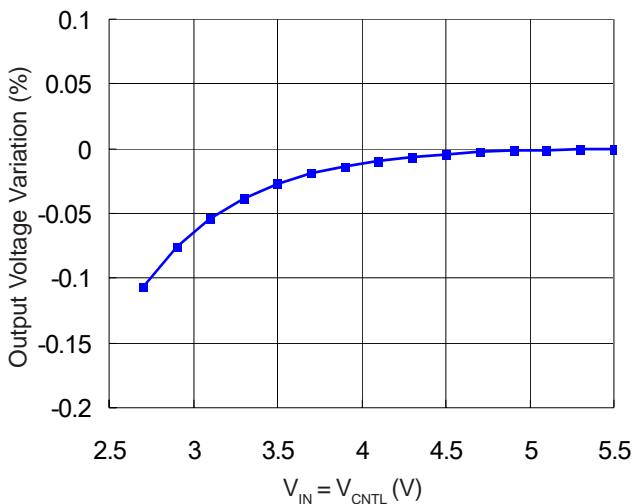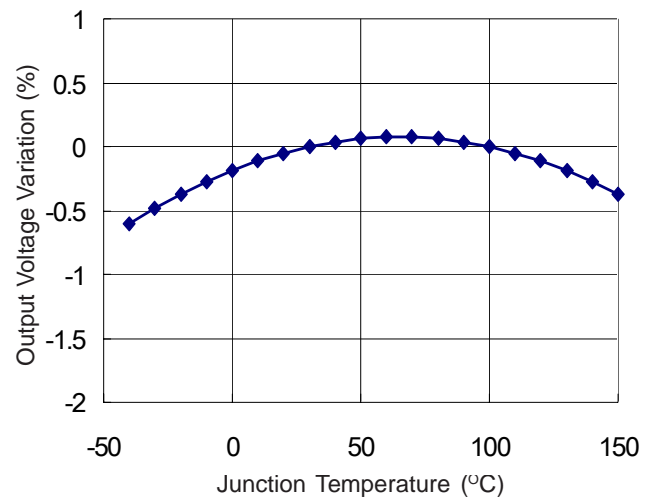

$V_{IN} = V_{CNTL}$ (V)

Output Voltage Load Regulation
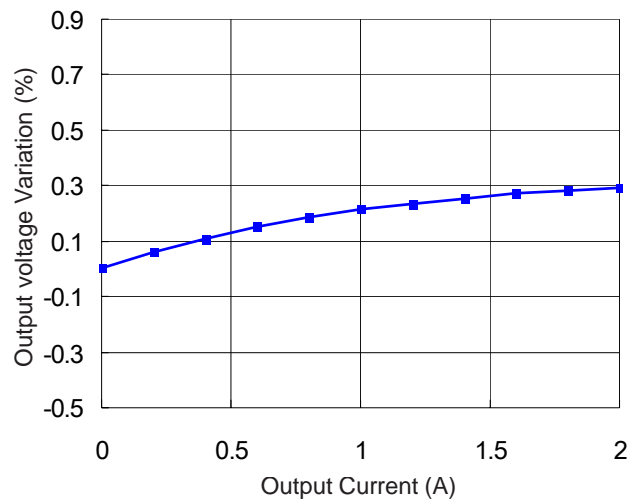
Output Current (A)

Typical Operation Characteristics

On Resistance vs. Input Voltage

On Resistance (mΩ) vs. Control Input V_{CNTL} (V), $V_{OUT} = 1.8V$

Output Voltage vs. Temperature

Output Voltage Variation (%) vs. Junction Temperature (°C)

Current Limit
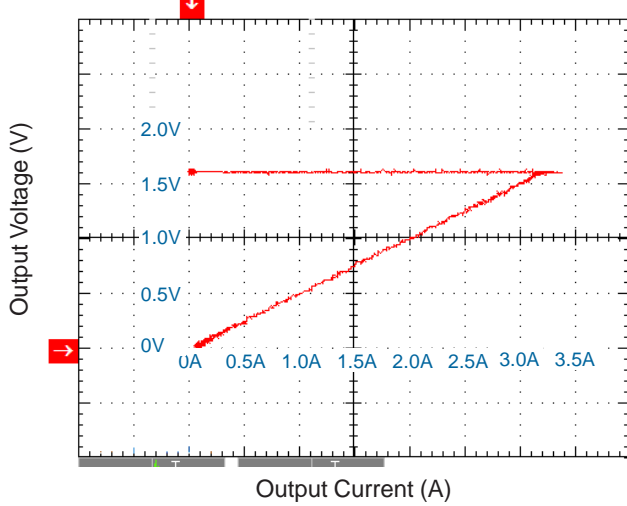
Output Voltage (V) vs. Output Current (A)

The uP7704 is a high performance linear regulator specifically designed to deliver up to 2A output current with very low input voltage and ultra low dropout voltage. With dual-supply configuration, the uP7704 operates with a wide input voltage V_{IN} range from 1.2V to 5.5V and is ideal for applications where V_{OUT} is very close to V_{IN}.

Supply Voltage for Control Circuit V_{CNTL}

Unlike other linear regulators that use a P-Channel MOSFET as the pass transistor, the uP7704 uses an N-Channel as the pass transistor. N-Channel MOSFET provides lower on-resistance and better stability meeting stringent requirements of current generation microprocessors and other sensitive electronic devices. The drain of N-Channel MOSFET is connected to VIN and the source is connected to VOUT. This requires that the supply voltage V_{CNTL} for control circuit is at least 1.5V higher than the output voltage to provide enough overdrive capability for the pass transistor thus to achieve low dropout and fast transient response. It is highly recommended to bias the device with 5V voltage source if available.

Use a minimum 1uF ceramic capacitor plus a 10Ω resistor to locally bypass the control voltage.

Input/Output Capacitor Selection

The uP7704 has a fast transient response that allows it to handle large load changes associated with high current applications. Proper selection of the output capacitor and its ESR value determines stable operation and optimizes performance. The typical application circuit shown in Figure 1 was tested with a wide range of different capacitors. The circuit was found to be unconditionally stable with capacitor values from 10uF to 1000uF and ESR ranging from 0.5mΩ to greater then 75mΩ.
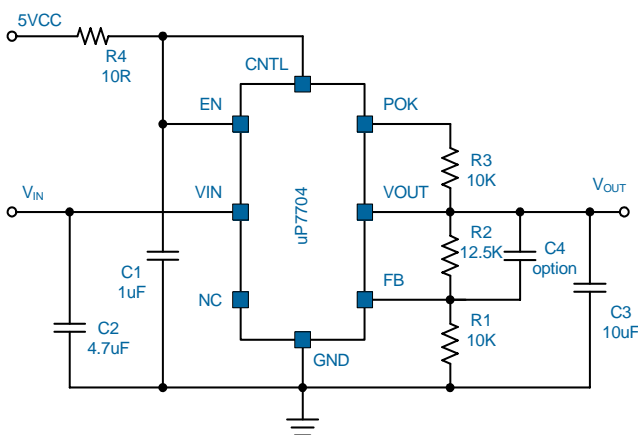

Figure 1. Typical Application Circuit

Input capacitor: A minimum of 4.7uF ceramic capacitor is recommended to be placed directly next to the VIN pin.

This allows for the device being some distance from any bulk capacitance on the rail. Additionally, bulk capacitance may be added closely to the input supply pin of the uP7704 to ensure that V_{IN} does not sag, improving load transient response.

Output capacitor: A minimum bulk capacitance of 10uF, along with a 0.1uF ceramic decoupling capacitor is recommended. Increasing the bulk capacitance will improve the overall transient response. The use of multiple lower value ceramic capacitors in parallel to achieve the desired bulk capacitance will not cause stability issues. Although designed for use with ceramic output capacitors, the uP7704 is extremely tolerant of output capacitor ESR values and thus will also work comfortably with tantalum output capacitors.

Thermal Consideration

The uP7704 integrates internal thermal limiting function to protect the device from damage during fault conditions. However, continuously keeping the junction near the thermal shutdown temperature may remain possibility to affect device reliability. It is highly recommended to keep the junction temperature below the recommended operation condition 125°C for maximum reliability.

Power dissipation in the device is calculated as:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{CNTL} \times I_{CNTL}$$

It is adequate to neglect power loss with respective to control circuit $V_{CNTL} \times I_{CNTL}$ when considering thermal management in uP7704 Take the following moderate operation condition as an example: V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{OUT} = 1A, the power dissipation is:

$$P_D = (3.3V - 1.5V) \times 1A = 1.8W$$

This power dissipation is conducted through the package into the ambient environment, and, in the process, the temperature of the die (T_J) rises above ambient. Large power dissipation may cause considerable temperature raise in the regulator in large dropout applications. The geometry of the package and of the printed circuit board (PCB) greatly influences how quickly the heat is transferred to the PCB and away from the chip. The most commonly used thermal metrics for IC packages are thermal resistance from the chip junction to the ambient air surrounding the package (θ_{JA}):

$$\theta_{JA} = (T_J - T_A) / P_D$$

θ_{JA} specified in the *Thermal Information* section is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard. The case point of

θ_{JC} is on the exposed pad for PSOP-8 package.

Given power dissipation P_D, ambient temperature and thermal resistance θ_{JA}, the junction temperature is calculated as:

$$T_J = T_A + \Delta T_{JA} = T_A + P_D \times \theta_{JA}$$

To limit the junction temperature within its maximum rating, the allowable maximum power dissipation is calculated as:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. θ_{JA} of PSOP-8 packages is 75°C/W on JEDEC 51-7 (4 layers, 2S2P) thermal test board with minimum copper area. The maximum power dissipation at $T_A = 25$°C can be calculated as:

$$P_{D(MAX)} = (125°C - 25°C) / 75°C/W = 1.33W$$

The thermal resistance θ_{JA} highly depends on the PCB design. Copper plane under the exposed pad is an effective heatsink and is useful for improving thermal conductivity. Figure 3 show the relationship between thermal resistance θ_{JA} vs. copper area on a standard JEDEC 51-7 (4 layers, 2S2P) thermal test board at $T_A = 25$°C. A 50mm² copper plane reduces θ_{JA} from 75°C/W to 52°C/W and increases maximum power dissipation from 1.33W to 1.9W.
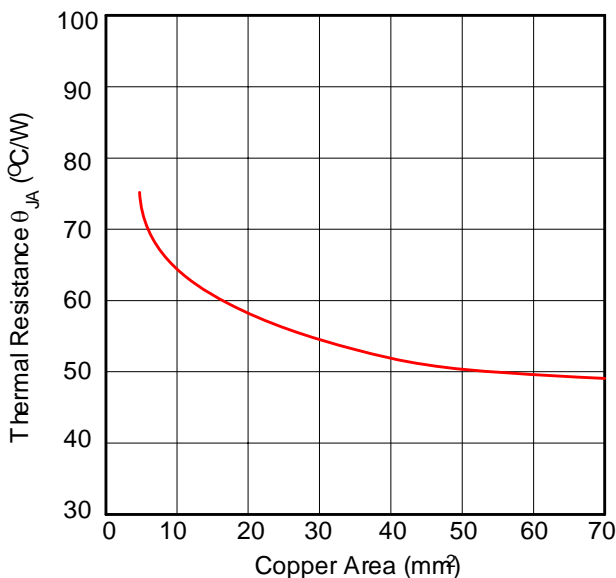

Figure 3. Thermal Resistance θ_{JA} vs. Copper Area
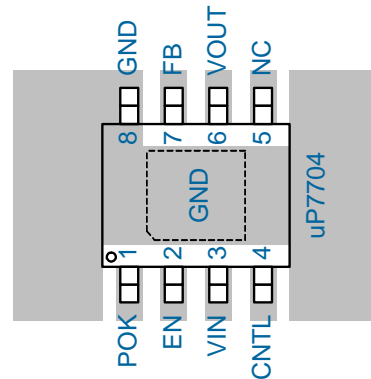
Figure 4 illustrated the recommended PCB layout for best thermal performance.

Figure 4. Recommended PCB Layout.

Layout Consideration

1. Place a local bypass capacitor as closed as possible to the VIN pin. Use short and wide traces to minimize parasitic resistance and inductance.

2. The exposed pad should be soldered on GND plane with maximum area and with multiple vias to inner layer of ground place for improving thermal performance.

3. Connect voltage divider directly to the point where regulation is required. Place voltage divider close to the device.

PSOP-8 Package
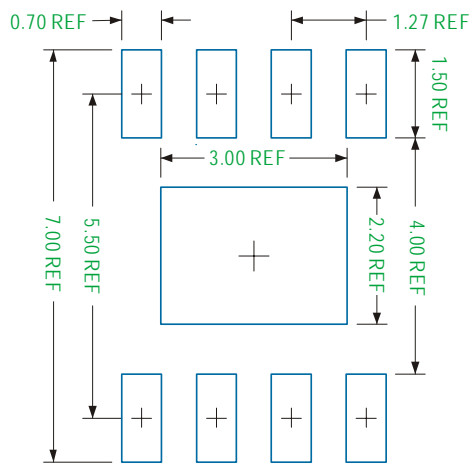
Recommended Solder Pad Layout
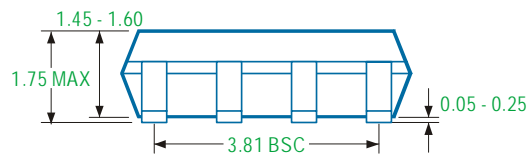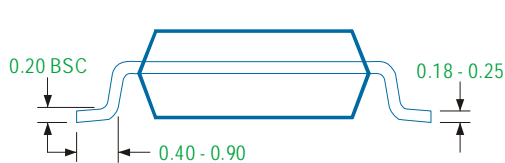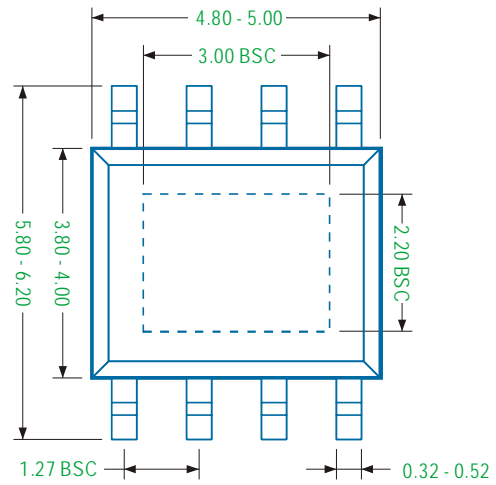
Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
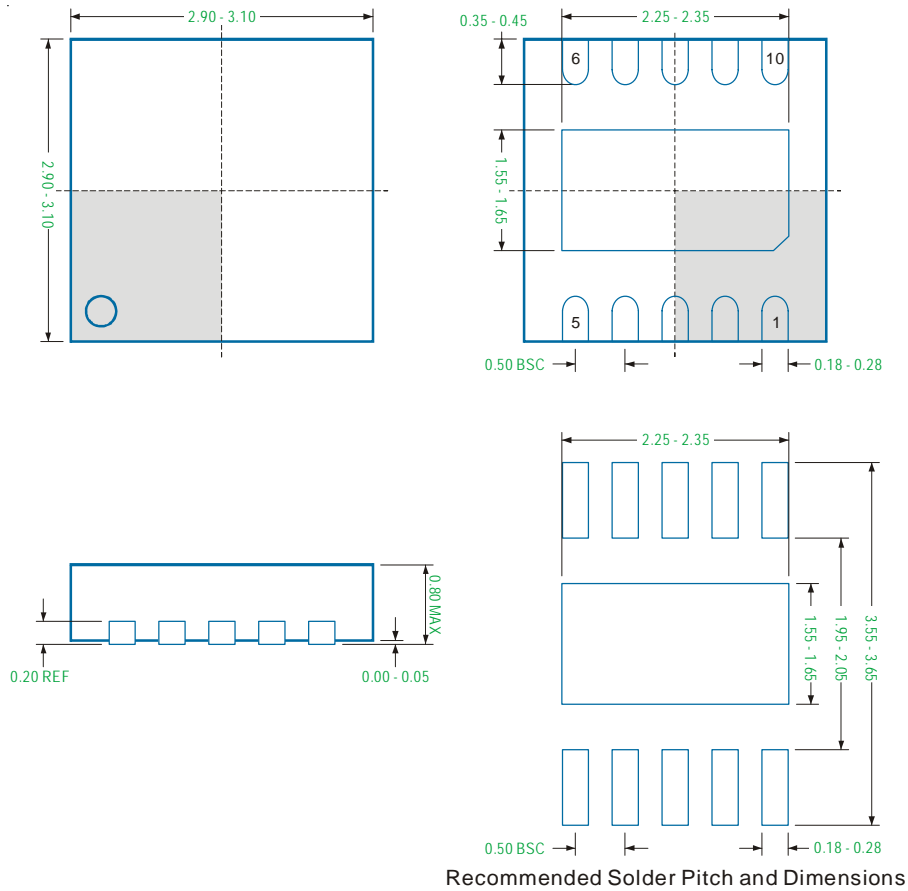   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions no not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.

WDFN3x3-10L Package

Recommended Solder Pitch and Dimensions

Note
1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions no not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.