

## 2A Ultra Low Dropout Linear Regulator for DDR4 Memory VTT Termination

### General Description

The uP8817Q is an ultra low dropout regulator for Double Data Rate (DDR) termination system. It is specifically designed for low input voltage and low external component count systems. The uP8817Q is capable of sinking/sourcing up to 2A output current, providing fast load transient and only requires a minimum 3x10uF ceramic output capacitor. The uP8817Q supports all power requirements for DDR VTT bus termination, DDR4 especially. Other features include thermal protection, bi-directional current limit protection. The uP8817Q is available in a PSOP-8L package.

### Ordering Information

Order Number	Package	Top Marking
uP8817QSW8	PSOP-8L	uP8817Q

Note:

(1) Please check the sample/production availability with uPI representatives.

(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

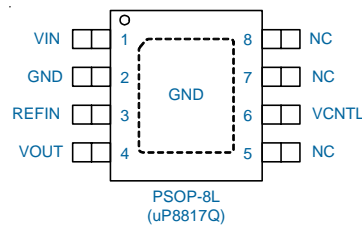
### Features

- ❑ VIN Input Voltage Range: 1V to 3.6V
- ❑ VCNTL Input Voltage: 2.9V to 5.5V
- ❑ Low External Component Count
- ❑ Enable/Disable Control from REFIN
- ❑ Discharge MOSFET at VOUT Shutdown
- ❑ Up to 2A Source/Sink Current
- ❑ Support DDR3 and Low Power DDR3/DDR4
- ❑ Stable with Pure MLCC as Output Cap
- ❑ RoHS Compliant and Halogen Free

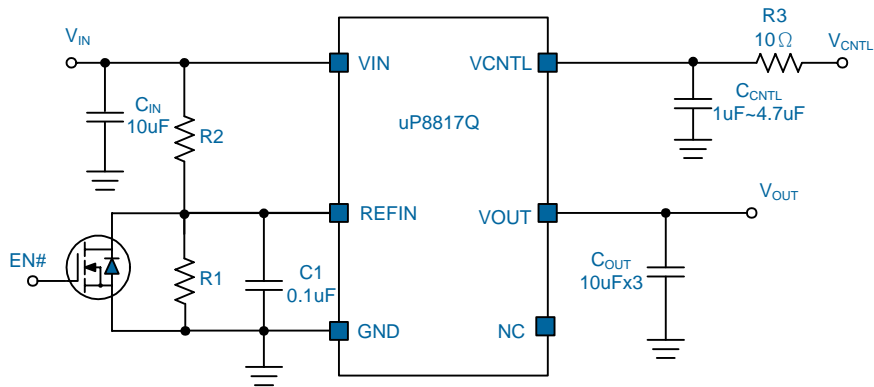
### Applications

- ❑ DDR Memory Termination
- ❑ Desktop PCs, Notebook Computers, and Server

### Pin Configuration



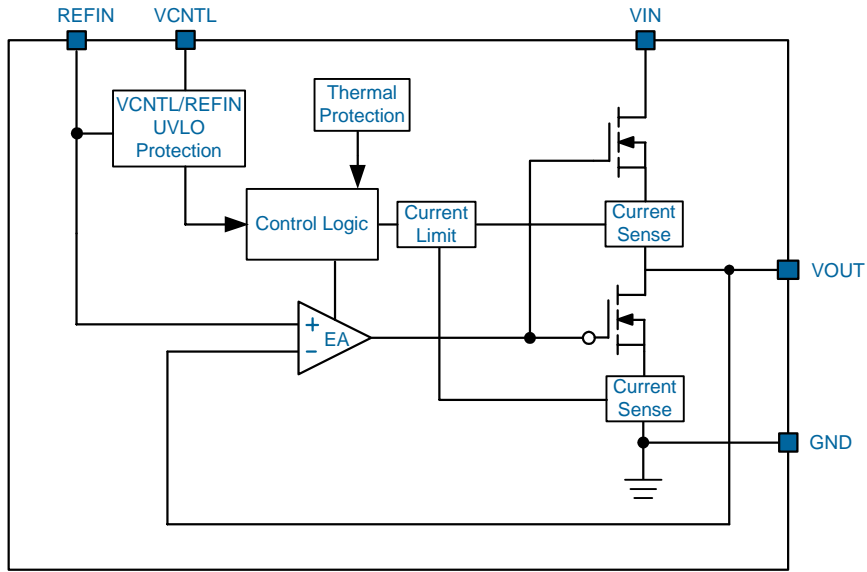
*Typical Application Circuit*



**Functional Pin Description**

Pin No.	Name	Pin Function
1	VIN	<b>Input Voltage.</b> This is the drain input to the power device that supplies current to the output pin. Use a ceramic capacitor of at least 10uF on the uP8817Q Input for stability and improving transient response.
2	GND	<b>Ground.</b>
3	REFIN	<b>Reference Input.</b> The input to REFIN also controls enable/disable state of this device.
4	VOUT	<b>Output Voltage.</b> This pin is the power output of the device. A minimum capacitance of 10uFx3 output capacitor is recommended. And the maximum is 50uF capacitor.
5	NC	<b>No Internal Connection.</b>
6	VCNTL	<b>Supply Input for Control Circuit.</b> This pin provides bias voltage to the control circuitry and driver for the pass transistor. The driving capability of output current is proportioned to the $V_{CNTL}$ . For the device to regulate, the voltage on this pin must be at least 1.5V greater than the output voltage, and no less than $V_{CNTL\_MIN}$ .
7	NC	<b>No Internal Connection.</b>
8	NC	<b>No Internal Connection.</b>
Exposed Pad		<b>Ground.</b> The exposed pad is the ground of the IC, and it must be soldered to a large PCB and connect to GND for power dissipation.

*Functional Block Diagram*



**Source/Sink Current Limit**

The uP8817Q monitor sourcing and sinking output currents and it has a constant over current limit by reducing power MOSFET gate voltage. Note that the current limit level will be reduced to short circuit current limit level when the output voltage is short to ground. This current limit function is a non-latch protection.

**VCNTL UVLO Protection**

This device provides UVLO function by monitoring the input voltage to VCNTL pin. If  $V_{CNTL}$  is less than the UVLO threshold voltage,  $V_{OUT}$  regulator is powered off.

**REFIN**

The REFIN also provides UVLO protection. And It can be set by external voltage divider connected to the memory supply bus (VDDQ). When the REFIN voltage is below shutdown threshold, the regulator is turned off.

## Absolute Maximum Rating

(Note 1)

Control Input Voltage, $V_{CNTL}$	
DC	-0.3V to +6.5V
<200ns	-0.3V to +7.0V
Power Input Voltage, $V_{IN}$	
DC	-0.3V to +6.5V
<200ns	-0.3V to +7.0V
Other Pins	-0.3V to ( $V_{CNTL} + 0.3V$ )
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C
ESD Rating (Note 2)	
HBM (Human Body Mode)	2kV
MM (Machine Mode)	200V

## Thermal Information

Package Thermal Resistance (Note 3)

PSOP-8L $\theta_{JA}$	47°C/W
PSOP-8L $\theta_{JC}$	17.9°C/W
Power Dissipation, $P_D$ @ $T_A = 25^\circ\text{C}$	
PSOP-8L	2.13W

## Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range	-40°C to +125°C
Operating Ambient Temperature Range	-40°C to +85°C
Supply Input Voltage, $V_{IN}$	+1V to +3.6V
Supply Input Voltage, $V_{CNTL}$	+2.9V to +5.5V

**Note 1.** Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.** Devices are ESD sensitive. Handling precaution recommended.

**Note 3.**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ\text{C}$  on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

**Note 4.** The case temp location for measuring  $\theta_{JC}$  is on the top of the package.

**Note 5.** The device is not guaranteed to function outside its operating conditions.

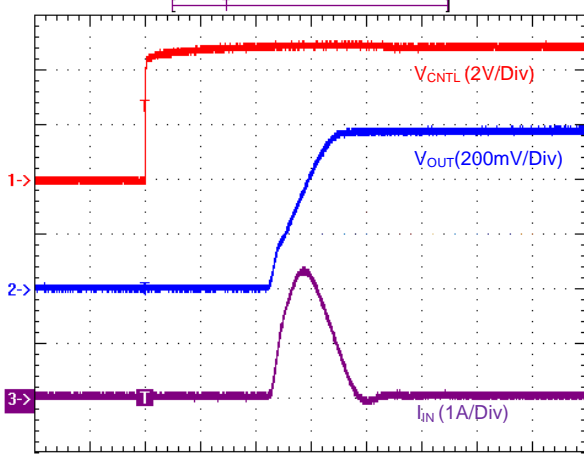
**Electrical Characteristics**

( $V_{CNTL} = 5V$ ,  $C_{OUT} = 10\mu F \times 3$ ,  $T_A = 25^\circ C$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>VCNTL Supply Input</b>						
VCNTL POR Threshold	$V_{CNTLRTH}$	$V_{CNTLRTH}$ rising	2.5	2.7	2.85	V
VCNTL POR Hysteresis	$V_{CNTLHYS}$	$V_{CNTLRTH}$ falling	--	0.2	--	V
VCNTL Shutdown Current	$I_{SD\_VCNTL}$	$V_{REFIN} = 0V$ , $I_{OUT} = 0A$	--	65	80	$\mu A$
VCNTL Input Current	$I_{VCNTL}$	$V_{CNTL} = 5V$ , $I_{OUT} = 0A$ , $V_{REFIN} > 0.4V$	--	0.7	1	mA
<b>VIN Supply Input</b>						
VIN Supply Current	$I_{VIN}$	$V_{CNTL} = 5V$ , $I_{OUT} = 0A$ , $V_{REFIN} > 0.4V$	--	1	50	$\mu A$
VIN Shutdown Current	$I_{SHDN\_VIN}$	$V_{REFIN} = 0V$ , No Load	--	0.1	50	$\mu A$
<b>Output Voltage</b>						
Output Voltage	$V_{OUT}$	$V_{IN} = 1.5V$ , $V_{REFIN} = 0.75V$ ; $I_{OUT} = 0A$	0.735	0.75	0.765	V
		$V_{IN} = 1.35V$ , $V_{REFIN} = 0.675V$ ; $I_{OUT} = 0A$	0.66	0.675	0.69	
		$V_{IN} = 1.2V$ , $V_{REFIN} = 0.6V$ ; $I_{OUT} = 0A$	0.585	0.6	0.615	
VOUT Voltage Offset to REFIN	$V_{OUT\_OS}$	$I_{OUT} = \pm 2A$ , $V_{IN} = 1.5V$ , $V_{REFIN} = 0.75V$	-25	--	25	mV
		$I_{OUT} = \pm 2A$ , $V_{IN} = 1.35V$ , $V_{REFIN} = 0.675V$	-25	--	25	
		$I_{OUT} = \pm 2A$ , $V_{IN} = 1.2V$ , $V_{REFIN} = 0.6V$	-25	--	25	
Load Regulation	$\Delta V_{LOAD}$	$-1A < I_{OUT} < 1A$	-20	--	20	mV
VOUT Discharge Resistance	$R_{DISCHARGE}$	$V_{REFIN} = 0V$ , $V_{OUT} = 0.3V$	--	18	25	$\Omega$
VOUT Source Current Limit	$I_{LIM\_VOUT\_SR}$		3.5	4.5	5.5	A
VOUT Sink Current Limit	$I_{LIM\_VOUT\_SK}$		3.5	4.5	5.5	A
<b>REFIN</b>						
REFIN Logic High Threshold	$V_{ENH}$	REFIN rising to enable the device	360	390	420	mV
REFIN Hysteresis	$V_{HYS}$		--	20	--	mV
REFIN Input Current	$I_{REFIN}$		--	--	1	$\mu A$
REFIN Voltage Range	$V_{REFIN}$		0.5	--	1.8	V
<b>Soft Start</b>						
Soft Start Time	$T_{SS}$	$V_{IN} = 1.2V$ , $V_{OUT} = 0.6V$	--	--	35	$\mu s$
<b>Thermal Protection</b>						
Thermal Shutdown Temperature	$T_{SD}$		--	160	--	$^\circ C$
Thermal Shutdown Hysteresis	$T_{SDH\_HYS}$		--	30	--	$^\circ C$

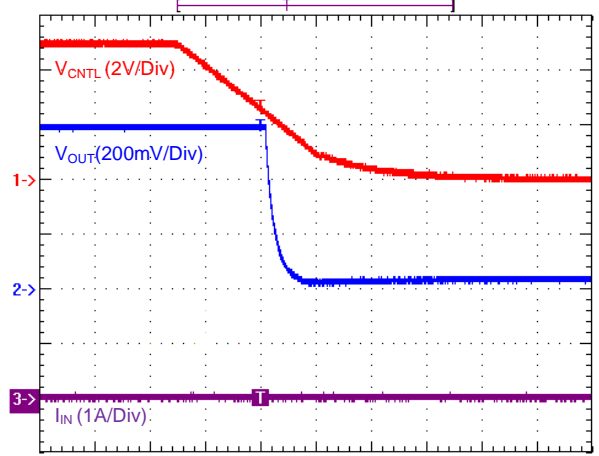
Typical Operation Characteristics

Power On from VCNTL



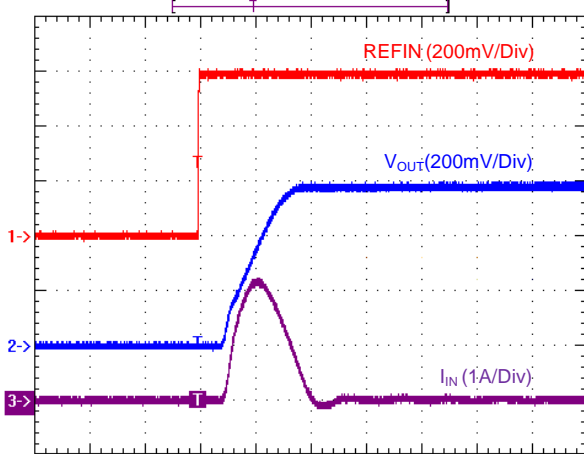
Time: 10us/Div  
 $V_{IN}=1.2V, V_{REFIN}=0.6V, C_{OUT}=10\mu F \times 3$

Power Off from VCNTL



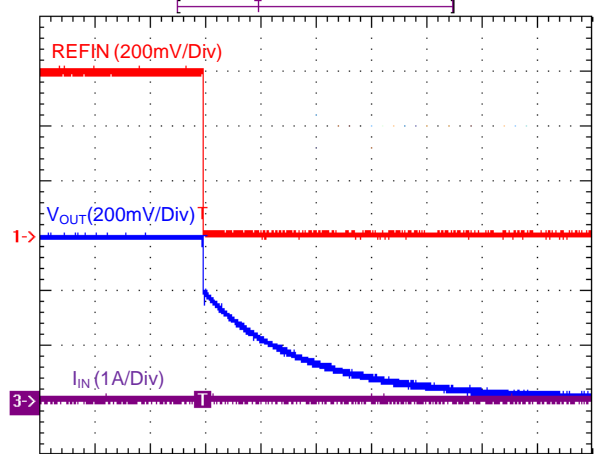
Time: 4ms/Div  
 $V_{IN}=1.2V, V_{REFIN}=0.6V, C_{OUT}=10\mu F \times 3$

Power On from REFIN



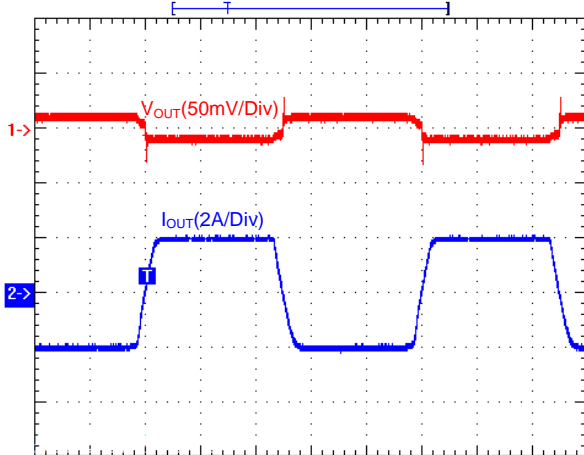
Time: 10us/Div  
 $V_{IN}=1.2V, V_{REFIN}=0.6V, C_{OUT}=10\mu F \times 3$

Power Off from REFIN



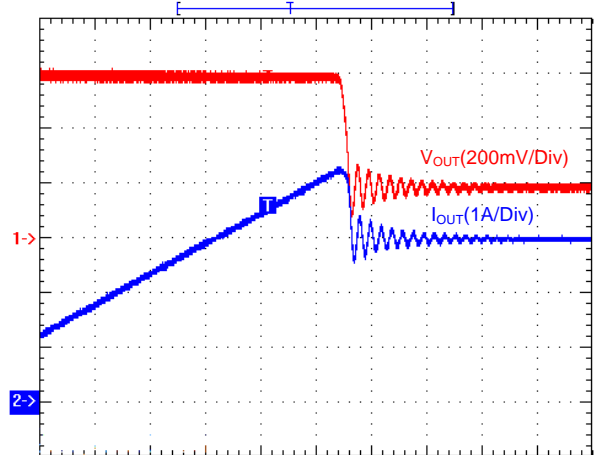
Time: 200us/Div  
 $V_{IN}=1.2V, V_{REFIN}=0.6V, C_{OUT}=10\mu F \times 3$

Load Transient



Time: 200us/Div  
 $V_{IN}=1.2V, V_{REFIN}=0.6V, I_{OUT}=-2A \text{ to } 2A, C_{OUT}=10\mu F \times 3$

Sourcing Current Limit

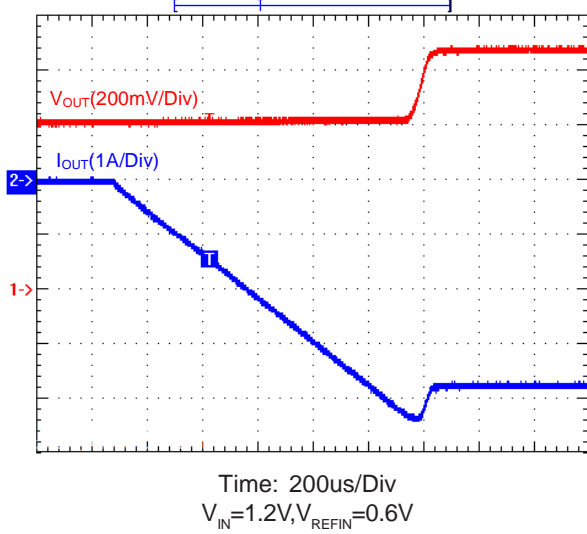


Time: 200us/Div  
 $V_{IN}=1.2V, V_{REFIN}=0.6V$

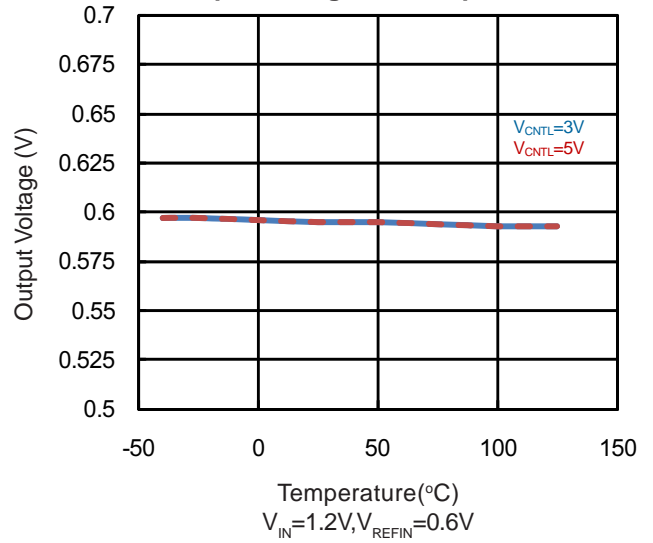


## Typical Operation Characteristics

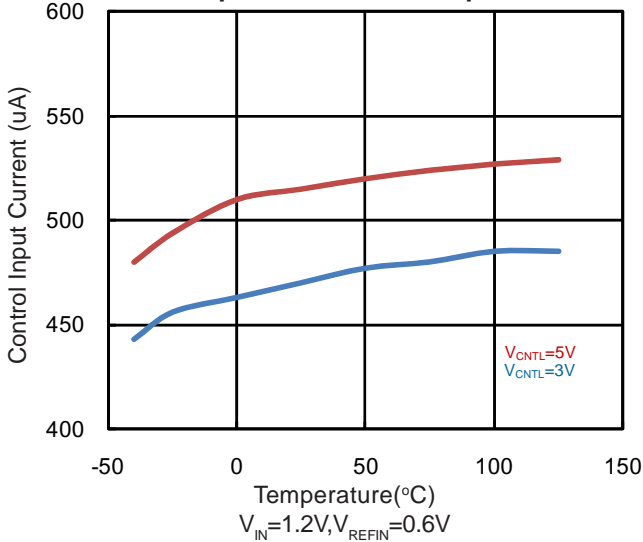
### Sinking Current Limit



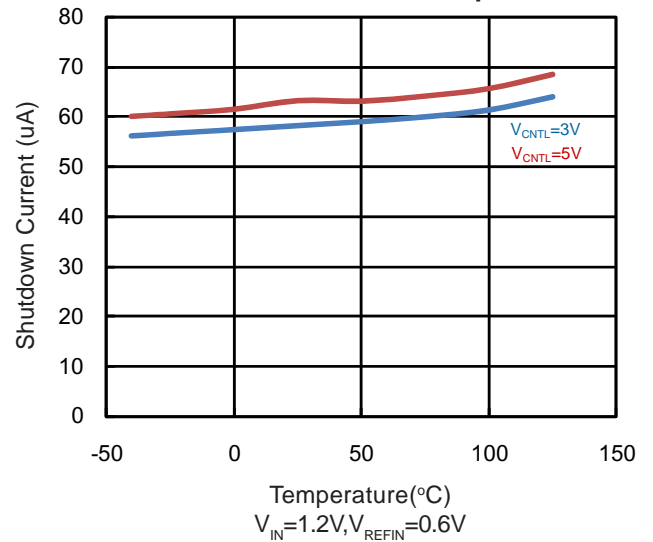
### Output Voltage vs. Temperature



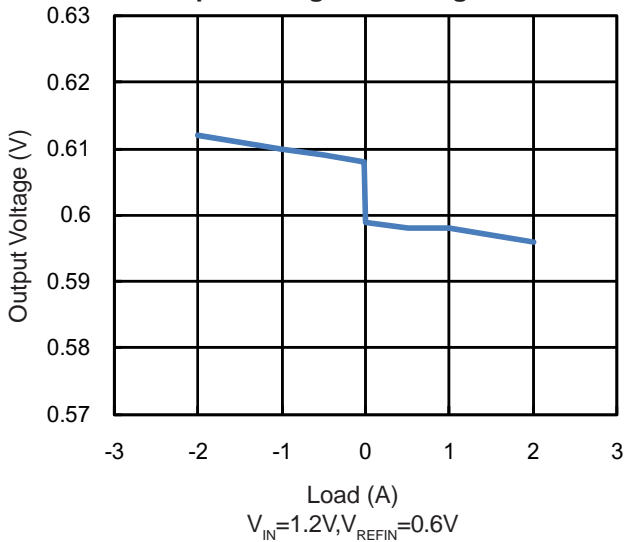
### Control Input Current vs. Temperature



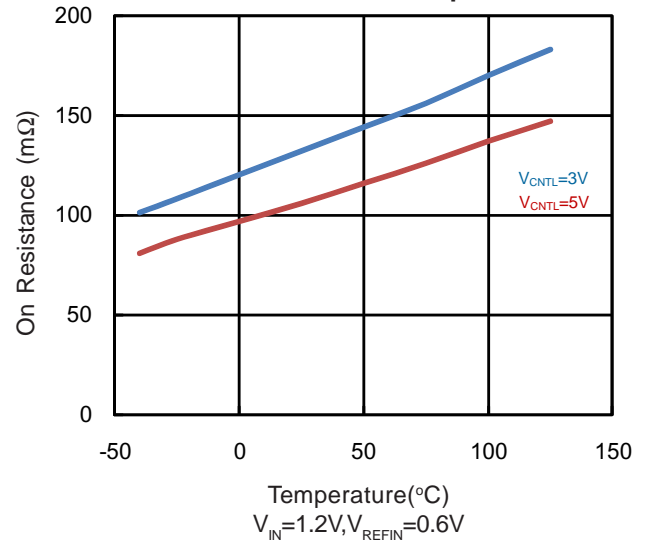
### Shutdown Current vs. Temperature



### Output Voltage Load Regulation



### On Resistance vs. Temperature



## Application Information

The uP8817Q is an ultra low dropout linear regulator specifically designed to provide termination voltage for DDR memory system. Designed with low on-resistance NMOSFETs, this device is capable of sinking/sourcing up to 2A output current. The output voltage is tightly regulated to track reference voltage input with fast to line/load transient.

### Supply Voltage for Control Circuit VCNTL

This uP8817Q works with dual supplies, a control input for the control circuitry and a power input as low as 1.0V for providing current to output. The control input provides bias current for control circuit and gate voltage for turning on and off the NMOSFETs. It is highly recommended to keep the control input 1.5V higher than the output voltage for optimal performance. The control voltage should be locally bypassed by a minimum 1uF ceramic capacitor plus a 10Ω resistor.

### Power Input Capacitor (C<sub>IN</sub>) and Control Input Capacitor (C<sub>CNTL</sub>)

The VIN pin supplies current to output when the upper MOSFET turns on. The uP8817Q is designed to work with minimum 10uF ceramic input capacitor. When work with large output capacitor, the uP8817Q may demand large input current during soft start. Make sure the power input is capable of delivering up to 2A.

Table 1 Component Recommended Value

Component	Recommended Value
C <sub>CNTL</sub>	1uF ~ 4.7uF Ceramic Capacitor
C <sub>IN</sub>	10uF or greater Ceramic Capacitor

### Reference Input

The output voltage is regulated to track the reference input at REFIN pin. The reference input can be obtained from power input by voltage divider or from an independent voltage reference. A ceramic capacitor physically near the IC is required to filter the reference voltage.

### Output Voltage and Output Capacitor, C<sub>OUT</sub>

The uP8817Q is designed to work with low ESR ceramic capacitors. Attach three, 10-uF ceramic capacitors in parallel to minimize the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL).

### Thermal Consideration

The uP8817Q integrates internal thermal limiting function to protect the device from damage during fault conditions. However, continuously keeping the junction near the thermal shutdown temperature may remain possibility to affect device reliability. It is highly recommended to keep the junction temperature below the recommended operation condition 125°C for maximum reliability. Power dissipation in the device is calculated as:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{CNTL} \times I_{CNTL}$$

It is adequate to neglect power loss with respect to control circuit  $V_{CNTL} \times I_{CNTL}$  when considering thermal management in uP8817Q. This power dissipation is conducted through the package into the ambient environment, and, in the process, the temperature of the die ( $T_J$ ) rises above ambient. Large power dissipation may cause considerable temperature raise in the regulator in large dropout applications. The geometry of the package and of the printed circuit board (PCB) greatly influence how quickly the heat is transferred to the PCB and away from the chip. The most commonly used thermal metrics for IC packages are thermal resistance from the chip junction to the ambient air surrounding the package ( $\Delta T_{JA}$ ):

$$\theta_{JA} = (T_J - T_A) / P_D$$

$\theta_{JA}$  specified in the Thermal Information section is measured in the natural convection at  $T_A = 25^\circ\text{C}$  on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-5 thermal measurement standard. Given power dissipation  $P_D$ , ambient temperature and thermal resistance  $\theta_{JA}$ , the junction temperature is calculated as:

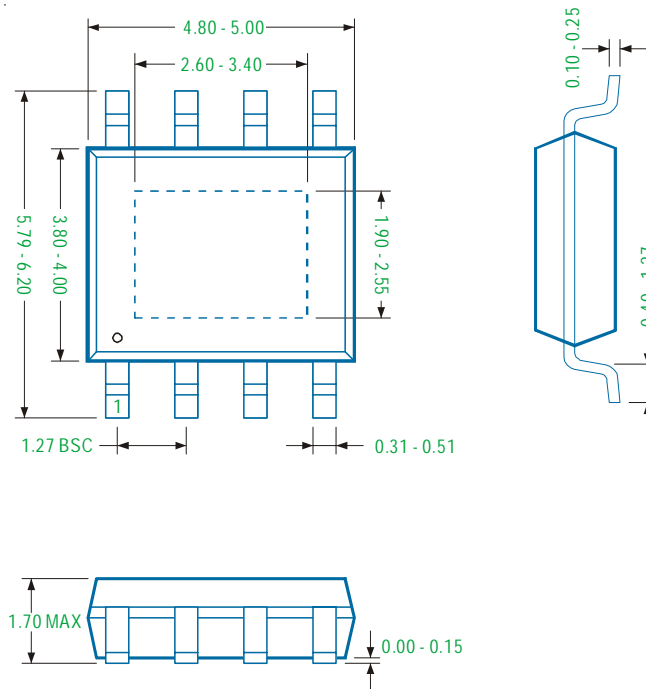
$$T_J = T_A + \Delta T_{JA} = T_A + P_D \times \theta_{JA}$$

To limit the junction temperature within its maximum rating, the allowable maximum power dissipation is calculated as:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where  $T_{J(MAX)}$  is the maximum operation junction temperature 125°C,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance.

PSOP - 8L



Note

1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

TYP: Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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