uPI SEMI

# uP9303

## 5V/12V Synchronous-Rectified Buck Controller

## General Description

The uP9303 is a compact synchronous-rectified buck controller specifically designed to operate with single 12V supply voltage and to deliver high quality output voltage. It adopts external compensated, voltage mode control to tightly regulate the feedback voltage to internal 0.6V reference voltage. The switching frequency is programmable from 50kHz to 500kHz, providing an optimal level of integration to reduce size and cost of the power supply.

The uP9303 integrates MOSFET drivers that support 12V+12V bootstrapped voltage for high efficiency power conversion.

The uP9303B features clock output that enables synchronized operation of two buck converters, reducing stress at input capacitors and EMI interference between converters.

Other features include under voltage lockout (UVLO), under-voltage protection, over-voltage protection and user programmable over-current protection. With aforementioned functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solutions. This part is available in SOP-14L package.

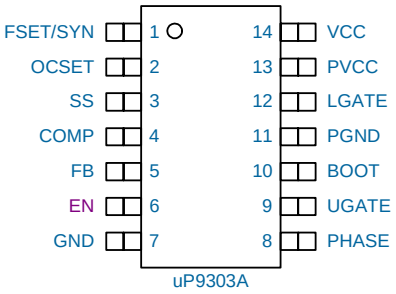
## Features

- **Operate with Single 12V Supply Voltage**
  - **0.6V $V_{REF}$ with 1.0% Accuracy**
  - **Up to 30A High Output Current**
- **Lossless, Programmable Overcurrent Protection**
  - **Uses Upper MOSFET $R_{DS(ON)}$**
- **Adjustable Soft Start**
- **Support Synchronized Operation**
  - **Clock Output (uP9303B)**
- **Simple Voltage-Mode PWM Control Design**
  - **Adjustable Switching Frequency**
  - **External Compensation**
  - **Fast Transient Response**
  - **Minimum off time 300ns**
  - **Adaptive Shoot-Through Protection**
- **Over/Under Voltage Protection**
- **RoHS Compliant and Halogen Free**

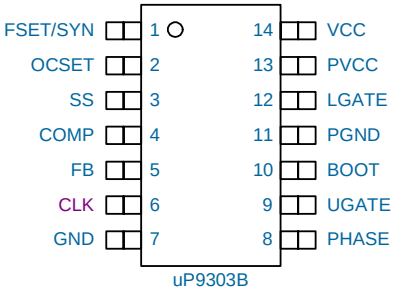
## Applications

- **Cable Modems, Set Top Boxes, and xDSL Modems**
- **ATX Power Supplies**
- **Power Supplies for Microprocessors or Subsystem Power Supplies**
- **Industrial Power Supplies; General Purpose Supplies**
- **5V or 12V Input DC-DC Regulators**
- **Low Voltage Distributed Power Supplies**

## Pin Configuration



uP9303A



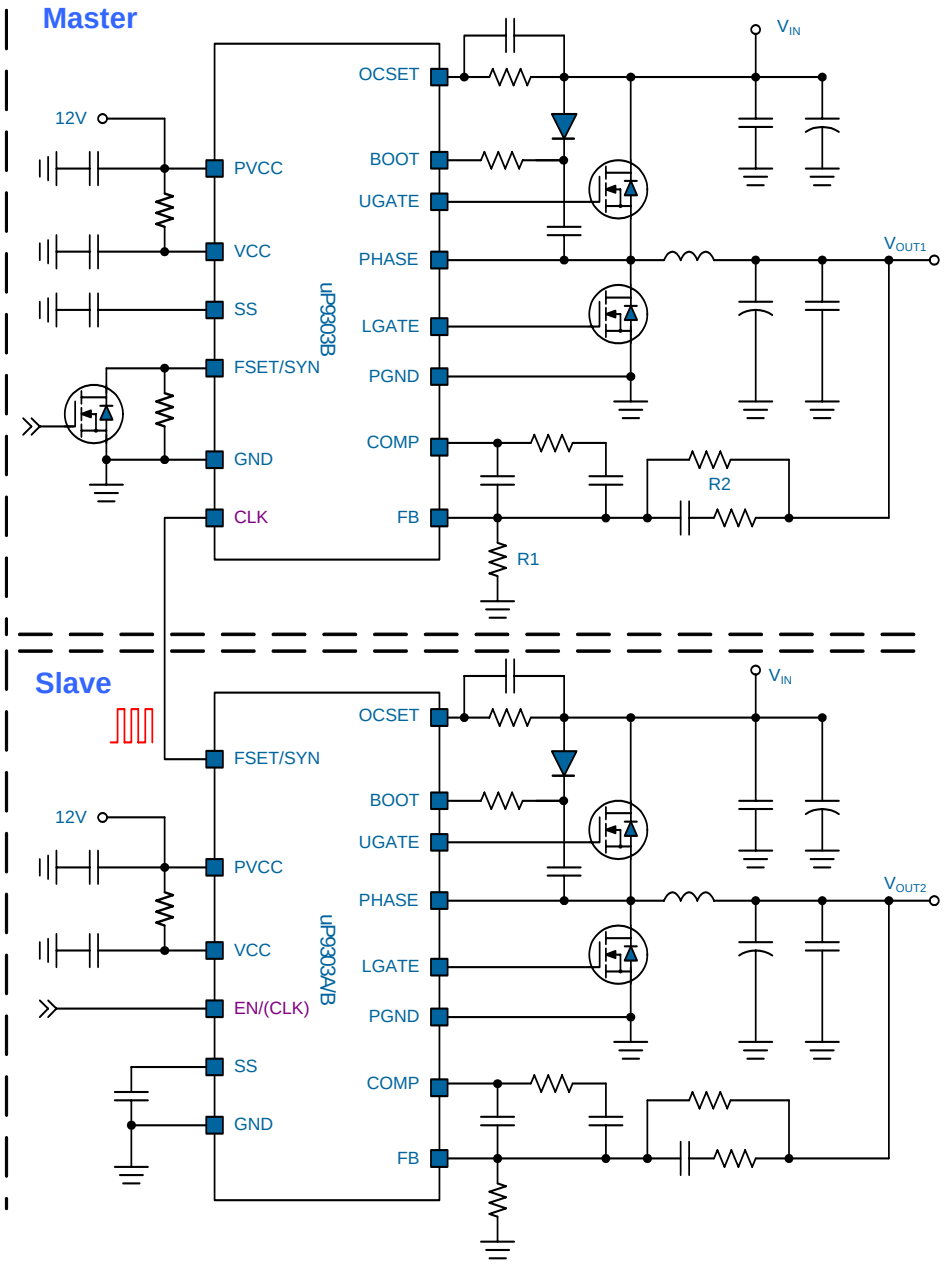
uP9303B

## Ordering Information

| Order Number | Package Type | Top Marking |
|---|---|---|
| uP9303ASAC | SOP-14L | uP9303A |
| uP9303BSAC | SOP-14L | uP9303B |

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

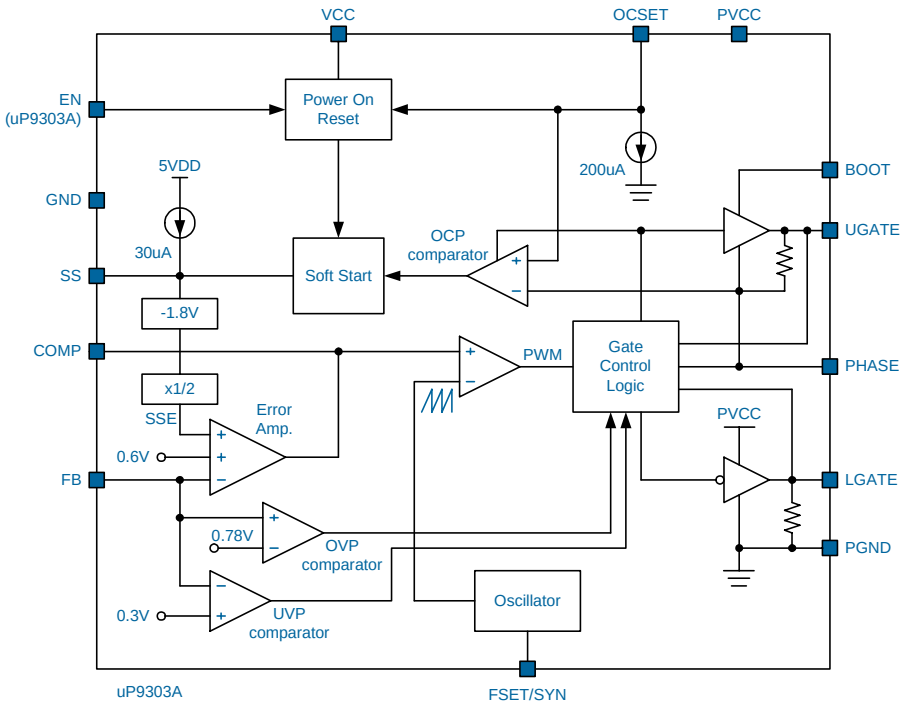
## Typical Application Circuit

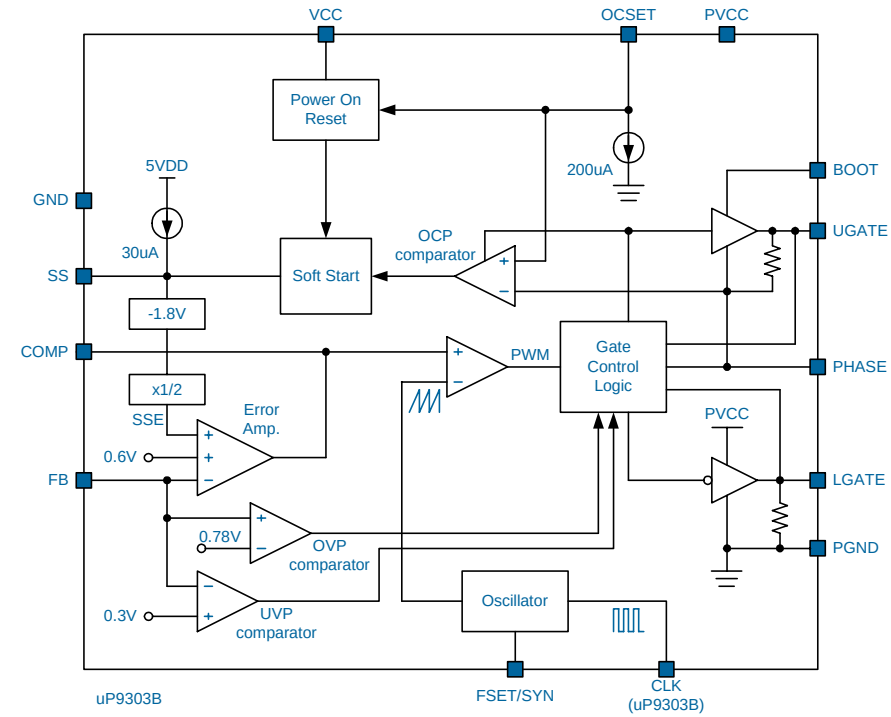


## Functional Pin Description

| No. | Pin Name | Pin Function |
|---|---|---|
| 1 | FSET/SYN | **Frequency Setting and Synchronization Input.** Connect a resistor from this pin to GND to set the switching frequency. The switching frequency can also be synchronized to external clock applied to this pin. Pulling this pin lower than 0.4V also disables the chip. |
| 2 | OCSET | **OCP Level Setting.** Connect a resistor to supply input of power stage to set the over current protection threshold level. A capacitor in parallel with the resistor helps to filter out the switching noise. |
| 3 | SS | **Soft Start Setting.** Connect a capacitor from this pin to GND to set the ramp-up time of ouptut voltage. |
| 4 | COMP | **Compensation Output.** This pin is the output of error amplifier and input of the PWM comparator. Connect an RC network to FB pin to compensate the voltage control loop. |
| 5 | FB | **Output Voltage Feedback Input.** This pin is the inverting input of the error amplifier. Connect a voltage divider to set the output voltage. |
| 6 | EN | **Chip Enable (uP9303A only).** Logic low of this pin disables the uP9303A. |
| | CLK | **Clock Output (uP9303B only).** This pin output a clock that is 180$^{o}$ output of phase with the internal switching clock. The uP9303B can operate in master mode when connect this pin to the FSET/SYN pin of another uP9303 that operates in slave mode. |
| 7 | GND | **Analog Ground.** |
| 8 | PHASE | **PHASE Switch Node.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE driver and is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. |
| 9 | UGATE | **Upper Gate Driver Output.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. |
| 10 | BOOT | **Bootstrap Supply** for the upper gate driver. Connect the bootstrap capacitor $C_{BOOT}$ between BOOT and PHASE pins to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. |
| 11 | PGND | **Power Ground for the IC.** This pin is the return of the lower gate driver. Tie this pin to the source of lower MOSFET with wide and short trace. |
| 12 | LGATE | **Lower Gate Driver Output.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off. |
| 13 | PVCC | **Supply Voltage for Gate Drivers.** This pin provide supply voltage for the gate drivers. Decouple this pin with a low ESR ceramic capacitor. |
| 14 | VCC | **Supply Voltage for Control Circuit.** This pin provides supply voltage for the internal control circuit. The supply voltage is internally regulated to 5VDD for internal control circuit. Connect a well-decoupled 10.8V to 13.2V supply voltage to this pin. Ensure that a decoupling capacitor is placed near the IC. |

## Functional Block Diagram



## Functional Description

The uP9303 is a compact synchronous-rectified buck controller specifically designed to operate with single 12V supply voltage and to deliver high quality output voltage. It adopts external compensated, voltage mode control to tightly regulate the feedback voltage to internal 0.6V reference voltage. The switching frequency is programmable from 50kHz to 500kHz, providing an optimal level of integration to reduce size and cost of the power supply.

The uP9303 integrates MOSFET drivers that support 12V+12V bootstrapped voltage for high efficiency power conversion.

The uP9303B features clock output that enables synchronized operation of two buck converters, reducing stress at input capacitors and EMI interference between converters.

Other features include under voltage lockout (UVLO), under-voltage protection, over-voltage protection and user programmable over-current protection. With aforementioned functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solutions. This part is available in SOP-14 package.

### Supply Voltage

The uP9303 features two supply input pins: VCC and PVCC for control circuit and gate drivers respectively. In real application, connect VCC and PVCC to a well-decoupled 10.8V to 13.2V supply voltage as shown in the *Typical Application Circuit*. A minimum 1uF ceramic capacitor physically near the supply input pins are required for locally bypassing the supply voltages.

An internal linear regulator regulates VCC supply voltage into a 5.0V voltage 5VDD for internal control logic circuit. No external bypass capacitor is required for filtering the 5VDD voltage.

The uP9303 integrates MOSFET gate drives that are powered from the PVCC pin and support 12V+12V driving capability. Converters that consist of uP9303 feature high efficiency without special consideration on the selection of MOSFETs.

### Power On Reset and Chip Enable

The uP9303 continuously monitors 1.) VCC pin voltage, 2.) EN pin voltage, 3.) OCSET pin voltage and 4.) FSET/SYN pin voltage for power on reset. The uP9303 is enabled only when all the POR is released. The POR threshold voltage are 9.5V, 1.3V, 1.3V and 0.4V at VCC, EN, OCSET, and FSET/SYN rising respectively. Before POR is released, the uP9303 is disabled, SS pin is pulled low to ground and both gate drivers are turned off.

Because the PVCC voltage is not monitored by POR circuitry, it must be connected to VCC pin externally to ensure PVCC is ready when POR is released.

### Soft Start

A capacitor $C_{SS}$ connected to SS pin controls the soft start behavior of output voltage as shown in Figure 1.

Before POR is released, the SS pin is internally pulled low to ground. When POR is released, an internal 30uA current source starts to charge $C_{SS}$, resulting in a linearly ramping-up voltage $V_{SS}$:

$$V_{SS} = \frac{30uA}{C_{SS}} \times T$$

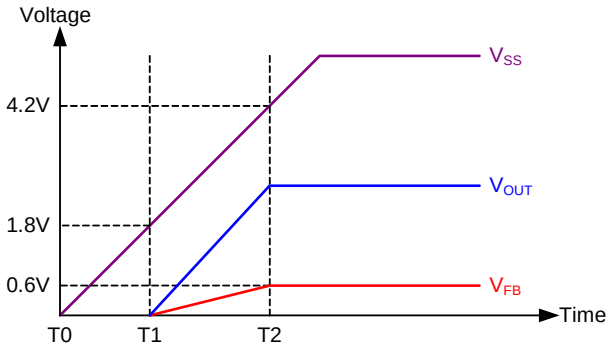



Figure 1. Softstart Behavior.

The error amplifier is a three-input device (referring to the Functional Block Diagram). Reference voltage $V_{REF}$ or the soft start voltage $V_{SSE}$ whichever is smaller dominates the behavior of the non-inverting input of the error amplifier. The SSE voltage is clamped as:

$$V_{SSE} = \frac{V_{SS} - 1.8V}{4} = \frac{30uA \times T / C_{SS} - 1.8V}{4}$$

Consequently, when $V_{SS}$ is lower than 1.8V, the feedback voltage $V_{FB}$ is kept at zero. When $V_{SS}$ is between 1.8V and 4.2V, the feedback voltage $V_{FB}$ ramps up linearly from 0V to 0.6V. When $V_{SS}$ is higher than 4.2V, the internal 0.6V reference takes over the control of error amplifier and the feedback voltage is regulated to $V_{REF}$. At the same time, the uP9303 asserts soft start end and enables the under voltage protection.

The output voltage ramp-up time can be calculated as:

$$T_{SS} = T2 - T1 = \frac{(4.2V - 1.8V) \times C_{SS}}{I_{SS}} = \frac{2.4V \times C_{SS}}{30uA}$$

### Switching Frequency Setting

The uP9303 features adjustable switching frequency by a resistor connected to the FSET/SYN pin. When the FSET/SYN pin is floating, the uP9303 operates at a free-running

## Functional Description

200kHz switching frequency. When a resistor is connected from FSET/SYN to ground, the uP9303 operates at a frequency higher than 200kHz. When a resistor is connected from FSET/SYN to VCC, the uP9303 operates at a frequency lower than 200kHz. The Figure 2 shows the relationship between switching frequency and the external resistance.

$R_{FSET}$ to GND : $R_{FSET} = \frac{9600}{(F_{SW} - 200)} (k\Omega)$

$R_{FSET}$ to VCC : $R_{FSET} = \frac{48000}{(200 - F_{SW})} (k\Omega)$

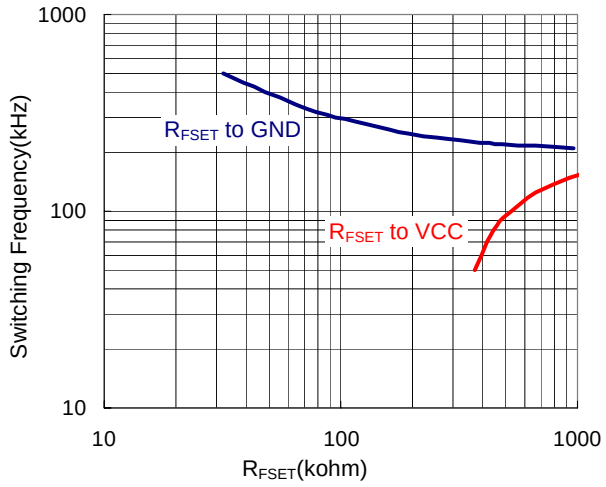



Figure 2. Switching Frequency vs. FSET/SYN Resistance

The switching frequency can also be synchronized to external clock from 50kHz to 500kHz applied to FSET/SYN pin.

Figure 4 depicts the clock logic of uP9303. When a resistor $R_{FSET}$ is connected from FSET/SYN to GND, its voltage $V_{FSET/SYN}$ is clamped to 2.4V. If the $V_{FSET/SYN}$ stays between 2.0V and 3.0V for 30us, the internal clock is selected for operation (Local Clock Mode, LCM).

A Schmitt trigger circuit receives the $V_{FSET/SYN}$ and generates an inverse squarewave that is synchronized to the $V_{FSET/SYN}$ when an external clock or internal clock is applied. The uP9303 works with synchronization mode if the squarewave frequency is higher than 50kHz (Remote Clock Mode RCM). The $V_{IH}$ and $V_{IL}$ of the Schmitt trigger circuit are 2/3 and 1/3 of 5V(=5VDD,Internal 5V) respectively.

If the $V_{FSET}$ stays below 1/3 of 5VDD or above 2/3 of 5VDD for 30us, the uP9303 asserts clock off and turns off the converter (Clock Off Mode COM).

The transitions from LCM to COM, COM to RCM or LCM to RCM are allowable. However, the transitions from COM to LCM, RCM to COM or RCM to LCM are regarded as fatal faults and not allowed. The uP9303 shuts down and latches off when forbidden mode transitions occur and can only be reset by POR of $V_{CC}$.

The uP9303B outputs a clock signal at CLK pin that is 180° out of phase with the operation clock. This clock can be used as synchronization for other uPI controller that features FSET/SYN pin.

### Output Voltage Setting

The output voltage can be programmed by a resistive divider connected to the FB pin as shown in the Typical Application Circuit:

$$V_{OUT} = 0.6V \times \frac{R1 + R2}{R1}$$

### Overcurrent Protection (OCP)

The uP9303 monitors the voltage drop across the upper MOSFET for over current protection (OCP). A resistor connected between OCSET pin and the drain of the upper MOSFET programs the OCP threshold level as shown in the Figrue 3. An internal 200uA current source flows through the $R_{OCSET}$, creating a voltage $V_{OCSET}$ at OCSET as:

$$V_{OCSET} = V_{IN} - 200uA \times R_{OCSET}$$

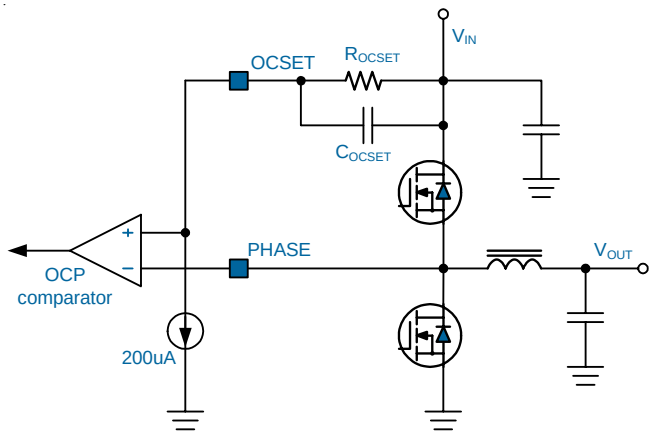



Figure 3. OCP Level Programming.

The OCP comparator compares the $V_{OCSET}$ and $V_{PHASE}$ for over current protection when the upper MOSFET turns on. If $V_{PHASE}$ is lower than $V_{OCSET}$, an OCP is triggered.

The OCP threshold level is given by:

$$I_{OCP} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}} = \frac{200uA \times R_{OCSET}}{R_{DS(ON)}}$$

## Functional Description

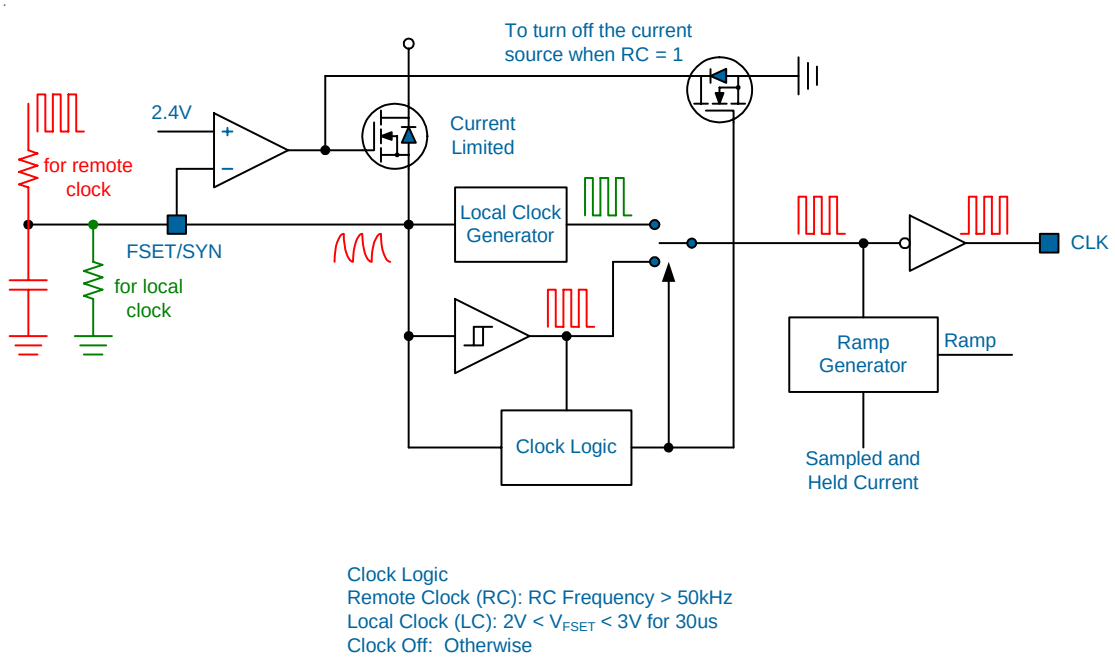



Figure 4. Clock Logic of uP9303

An OCP will shut down the device and discharge the $C_{SS}$ with a 30uA sinking current source. When the $C_{SS}$ is discharged completely, another soft start cycle is initiated.

If the over current condition is not removed during the soft start cycle, the uP9303 will shut down immediately when another OCP is triggered. However, the $V_{SS}$ keeps rising to 4V to complete the soft start cycle before the internal 30uA current source discharges the $C_{SS}$. If the over current conditon is not removed, the re-soft-start cycle will repeat 3 times and then latch off uP9303.

To avoid false trigger of OCP, variations of all parameters in above equation should be well considered, including:

1.) The $R_{DS(ON)}$ of MOSFET varies with temperature and the gate to source voltage. Consider the highest operation temperature and lowest gate to source voltage.

2.) Consider the minimum $I_{OCSET}$ (~180uA) and minimum $R_{OCSET}$.

3.) Consider the inductor ripple current.

### Under Voltage Protection (UVP)

The FB voltage is monitored for undervoltage protection after soft start end is asserted. If the FB voltage is lower than 0.3V (50% of 0.6V reference voltage), the UVP is triggered and shuts down the uP9303 with about 2us time delay. The uP9303 turns off both upper and lower MOSFETs when UVP is triggered. The UVP is a latch-off type protection and can only be reset by POR of the device.

### Over Voltage Protection (OVP)

The FB voltage is monitored for overvoltage protection. If the FB voltage is higher than 0.78V (130% of 0.6V reference voltage), the OVP is triggered and shuts down the uP9303 with about 25us time delay. The uP9303 turns off the upper and lower MOSFET when OVP is triggered. The OVP is a latch-off type protection and can only be reset by POR of the device.

## Absolute Maximum Rating

(Note 1)

Supply Input Voltage, $V_{CC}$ ---------- -0.3V to +16V

BOOT to PHASE

DC ---------- -0.3V to +16V

PHASE to GND

DC ---------- -0.7V to +16V

<200ns ---------- -8V to +30V

BOOT to GND

DC ---------- -0.3V to ($V_{CC}$ +16V)

<200ns ---------- -0.3V to 42V

UGATE to PHASE

DC ---------- -0.3V to (BOOT - PHASE + 0.3V)

<200ns ---------- -5V to (BOOT - PHASE + 0.3V)

LGATE to GND

DC ---------- -0.3V to ($V_{CC}$ + 0.3V)

<200ns ---------- -5V to ($V_{CC}$ + 0.3V)

FB to GND

DC ---------- -0.3V to +7V

<2ms ---------- -0.7V

FSET/SYN,OCSET to GND ---------- -0.3V to ($V_{CC}$ + 0.3V)

COMP to GND ---------- -0.3V to +7V

EN to GND ---------- -0.3V to +16V

CLK,SS to GND ---------- -0.3V to +6V

PGND to GND ---------- -0.3V to +0.3V

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- 150°C

Lead Temperature (Soldering, 10 sec) ---------- 260°C

ESD Rating (Note 2)

HBM (Human Body Mode) ---------- 2kV

MM (Machine Mode) ---------- 200V

## Thermal Information

Package Thermal Resistance (Note 3)

SOP-14L $\theta_{JA}$ ---------- 120°C/W

SOP-14L $\theta_{JC}$ ---------- 32°C/W

Power Dissipation, $P_D$ @ $T_A$ = 25°C

SOP-14L ---------- 0.83W

## Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C

Operating Ambient Temperature Range ---------- -40°C to +85°C

Supply Input Voltage, $V_{CC}$ ---------- +10.8V to 13.2V

## Electrical Characteristics

($V_{CC}$ = 12V, $T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply Input** | | | | | | |
| Supply Voltage Range | $V_{CC}$ | | 10.8 | -- | 13.2 | V |
| Supply Input Current | $I_{CC\_Q}$ | UGATE, LGATE Open; switching | -- | 5 | 10 | mA |
| **Power On Reset** | | | | | | |
| VCC POR Rising Threshold | $V_{CCRTH}$ | $V_{CC}$ rising | 9.0 | 9.5 | 10.0 | V |
| VCC POR Falling Threshold | $V_{CCFTH}$ | $V_{CC}$ falling (master ) | 6.5 | 7 | 7.5 | V |
| | | $V_{CC}$ falling (slave ) | 7.5 | 8.0 | 8.5 | V |
| OCSET POR Threshold | | $V_{OCSET}$ rising | -- | 1.3 | -- | V |
| OCSET POR Hysteresis | | $V_{OCSET}$ falling | -- | 0.1 | -- | V |
| EN POR Threshold | | $V_{EN}$ rising | -- | 1.3 | -- | V |
| EN POR Hysteresis | | $V_{EN}$ falling | -- | 0.1 | -- | V |
| **Oscillator** | | | | | | |
| Free Running Frequency | $f_{OSC}$ | FSET = open. | -- | 200 | -- | kHz |
| FSET/SYN Pin Voltage | $V_{FSET/SYN}$ | FSET = open. | -- | 2.4 | -- | V |
| Frequency Accuracy | | | -15 | -- | +15 | % |
| Frequency Adjustment Range | | | 50 | -- | 500 | kHz |
| Freqnency Synchronization Range | | | 50 | -- | 500 | kHz |
| External Clock Duty Ratio Range | | | 10 | -- | 90 | % |
| External Clock Low Voltage | | | -- | -- | 0.8 | V |
| External Clock High Voltage | | | 4.2 | -- | -- | V |
| Ramp Amplitude | $\Delta V_{OSC}$ | | -- | 1.6 | -- | $V_{P-P}$ |
| Minimum off time | | | -- | 300 | -- | ns |
| **Reference Voltage** | | | | | | |
| Reference Voltage Accuracy | $V_{REF}$ | | 0.594 | 0.600 | 0.606 | V |
| **Error Amplifier** | | | | | | |
| Open Loop DC Gain | AO | Guaranteed by Design | 70 | 80 | -- | dB |
| Gain-Bandwidth Product | GBW | Guaranteed by Design | -- | 10 | -- | MHz |
| Slew Rate | SR | Guaranteed by Design | 3 | 6 | -- | V/us |
| FB Input Current | | $V_{FB}$ = 0.6V | -- | 0.01 | 1 | uA |
| COMP High Voltage | $V_{COMP\_H}$ | | -- | 5.5 | -- | V |
| COMP Low Voltage | $V_{COMP\_L}$ | | -- | 0 | -- | V |
| COMP Source Current | | $V_{COMP}$ = $V_{COMP\_H}$ - 1.6V | -- | 2 | -- | mA |
| COMP Sink Current | | $V_{COMP}$ = 1.6V | -- | 2 | -- | mA |

## Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Clock Output** | | | | | | |
| Output High Level Voltage | | $I_{CLK}$ = 1mA sourcing | 4.5 | -- | -- | V |
| Output Low Level Voltage | | $I_{CLK}$ = 1mA sinking | -- | -- | 0.4 | V |
| Clock Duty Ratio | | FSET/SYN = open | -- | 50 | -- | % |
| **PWM Controller Gate Drivers** | | | | | | |
| Upper Gate Sourcing Current | $I_{UG\_SRC}$ | $V_{BOOT}$ = 12V, $V_{UGATE}$ - $V_{PHASE}$ = 2V | -- | 2.5 | -- | A |
| Upper Gate Sourcing Resistance | $R_{UG\_SRC}$ | $I_{UGATE}$ = 100mA sourcing | -- | 4 | 5 | Ω |
| Upper Gate Sinking Resistance | $R_{UG\_SNK}$ | $I_{UGATE}$ = 100mA sinking | -- | 2 | 3 | Ω |
| Lower Gate Sourcing Current | $I_{LG\_SRC}$ | $V_{PVCC}$ = 12V, $V_{LGATE}$ = 2V | -- | 6.5 | -- | A |
| Lower Gate Sourcing Resistance | $R_{LG\_SRC}$ | $I_{LGATE}$ = 100mA sourcing | -- | 1.5 | 2.5 | Ω |
| Lower Gate Sinking Resistance | $R_{LG\_SNK}$ | $I_{LGATE}$ = 100mA sinking | -- | 1 | 2 | Ω |
| PHASE Falling to LGATE Rising Delay | | $V_{PHASE}$ < 1.2V to $V_{LGATE}$ > 1.2V | -- | 25 | -- | ns |
| LGATE Falling to UGATE Rising Delay | | $V_{LGATE}$ < 1.2V to ($V_{UGATE}$ - $V_{PHASE}$) > 1.2V | -- | 25 | -- | ns |
| **Protection** | | | | | | |
| Soft-Start Charge Current | $I_{SS}$ | $V_{SS}$ = 0V | 24 | 30 | 36 | uA |
| OVP Threshold Level | $V_{OVP}$ | $V_{FB}$ rising. | -- | 0.78 | -- | V |
| OVP Delay Time | | | -- | 25 | -- | us |
| UVP Threshold Level | $V_{UVP}$ | $V_{FB}$ falling | -- | 0.3 | -- | V |
| UVP Delay Time | | | -- | 2 | -- | us |
| OCSET Sink Current Source | $I_{OCSET}$ | $V_{OCSET}$ = $V_{CC}$ - 0.3V. | 180 | 200 | 220 | uA |
| OCP Delay Time | | | -- | 5 | -- | us |

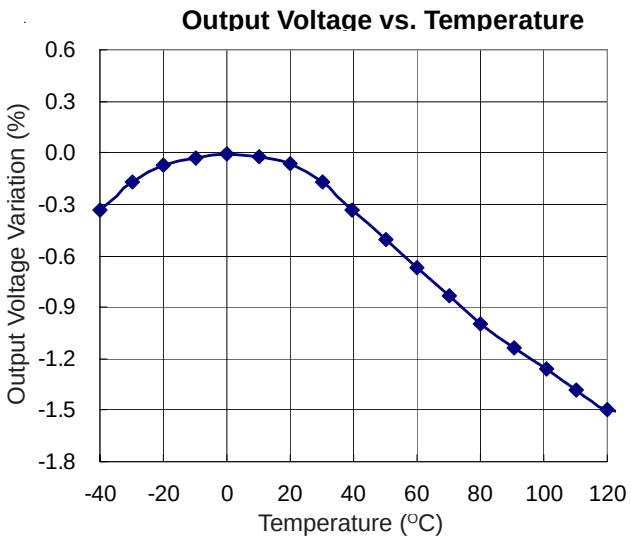
**Note 1.** Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

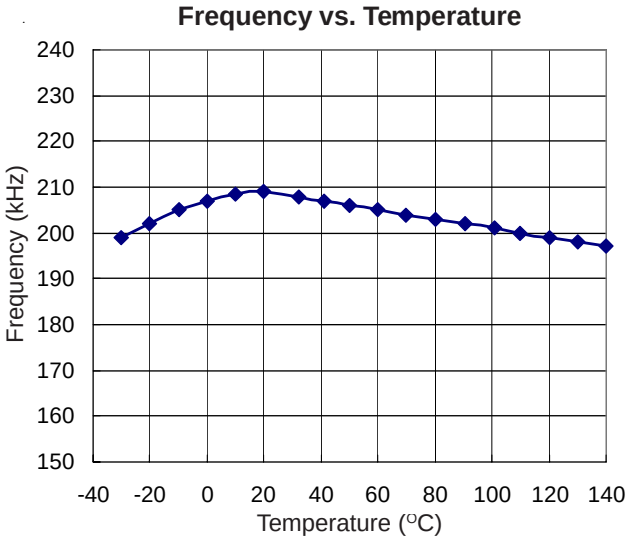
**Note 2.** Devices are ESD sensitive. Handling precaution recommended.

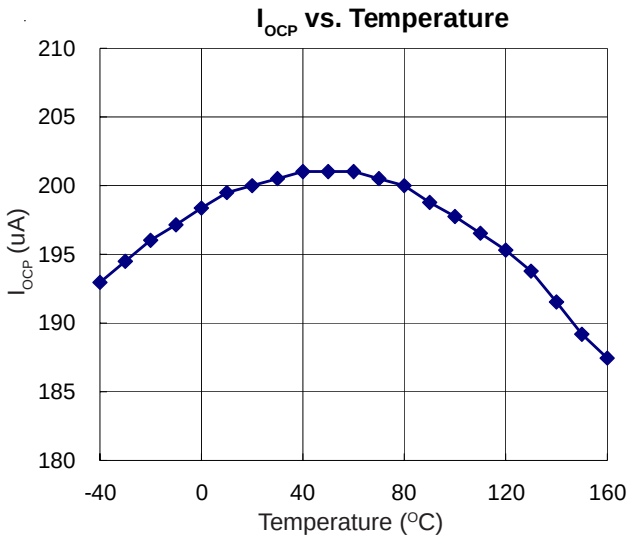
**Note 3.** $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

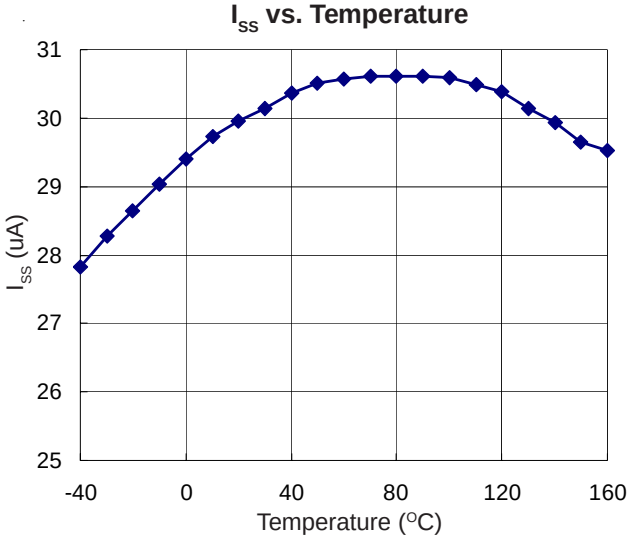
**Note 4.** The device is not guaranteed to function outside its operating conditions.

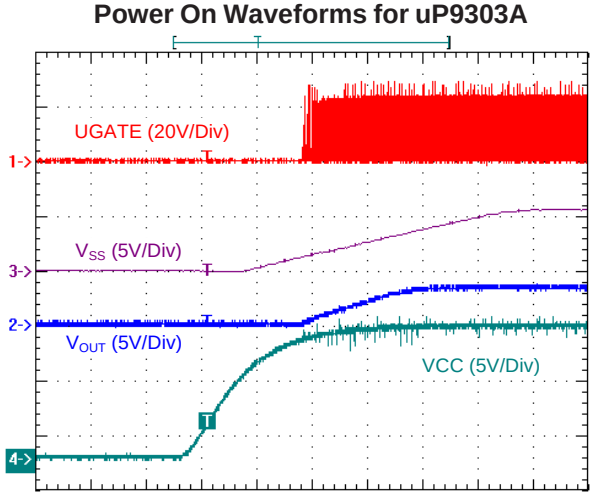
## Typical Operation Characteristics



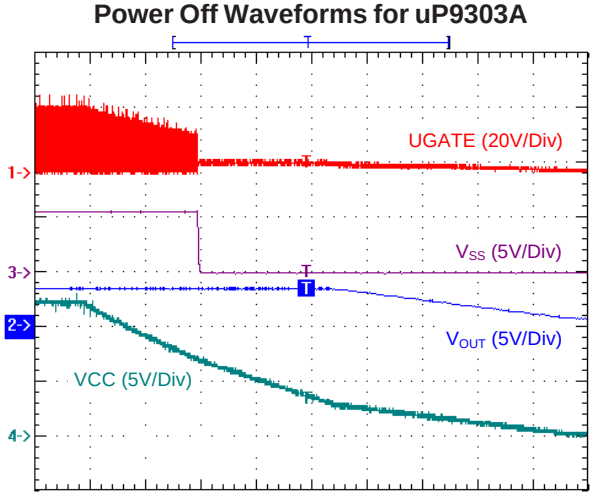



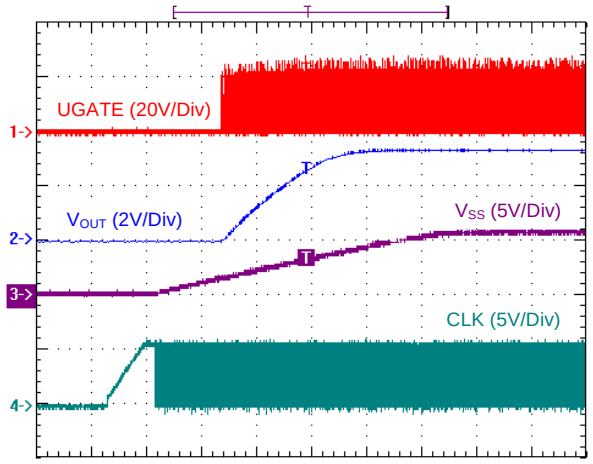

4ms/Div
$V_{IN} = V_{CC} = 12V$, No Load




40ms/Div
$V_{IN} = V_{CC} = 12V$, No Load

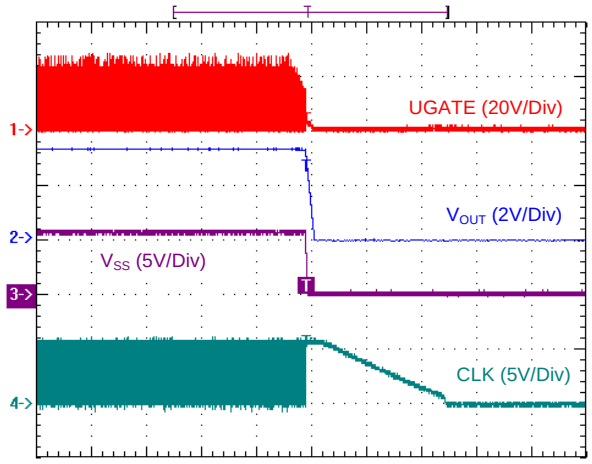
## Typical Operation Characteristics

### Power On Waveforms for uP9303B



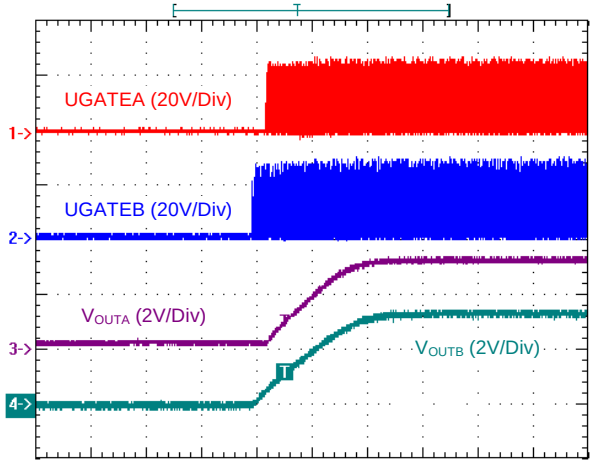

4ms/Div
$V_{IN} = V_{CC} = 12V, I_{LOAD} = 2A$

### Power Off Waveforms for uP9303B



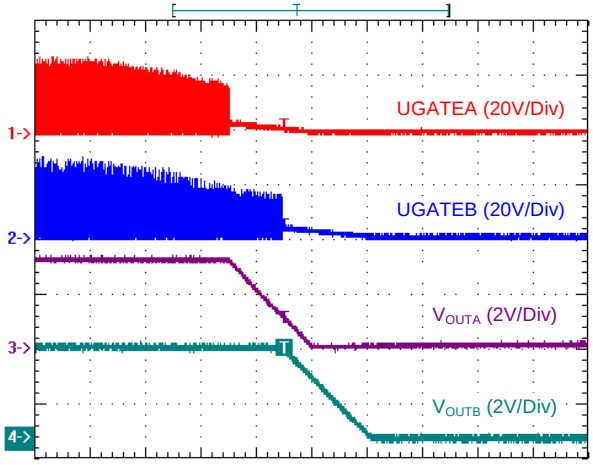

40ms/Div
$V_{IN} = V_{CC} = 12V, I_{LOAD} = 2A$

### Power On Waveforms for uP9303A/B



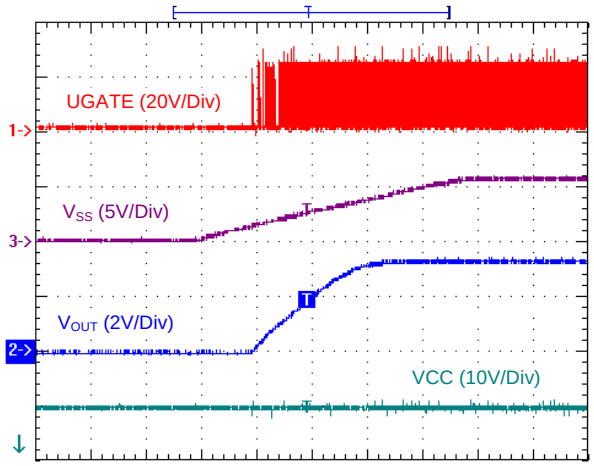

4ms/Div
$V_{IN} = V_{CC} = 12V, I_{LOAD} = 2A$

### Power Off Waveforms for uP9303A/B




4ms/Div
$V_{IN} = V_{CC} = 12V, I_{LOAD} = 2A$

### EN On Waveforms for uP9303B




4ms/Div
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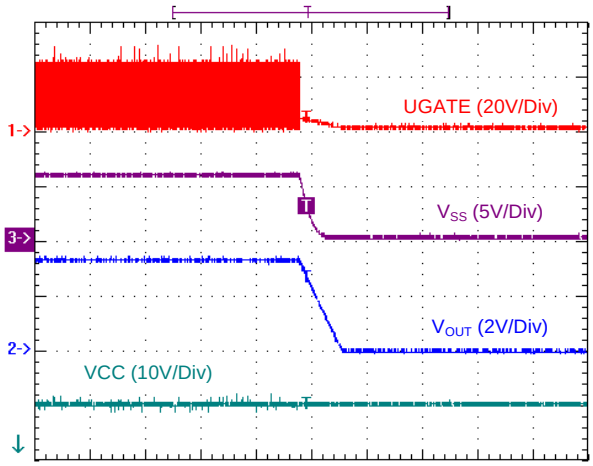
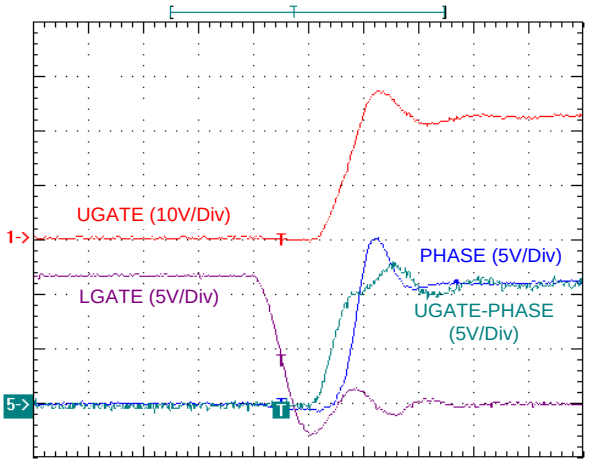
### EN Off Waveforms for uP9303B




4ms/Div
$V_{IN} = V_{CC} = 12V, I_{LOAD} = 2A$

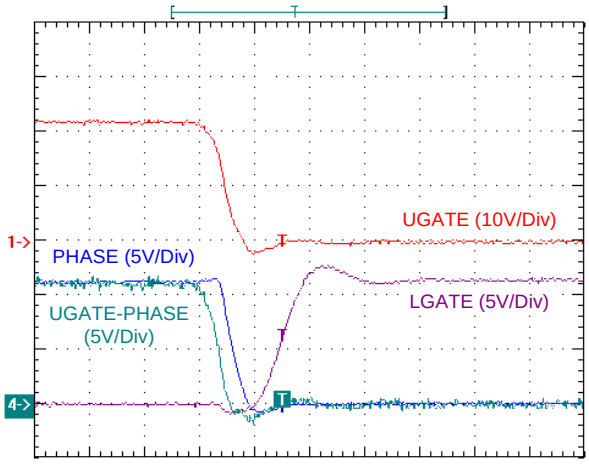
## Typical Operation Characteristics

**Gate waveforms**



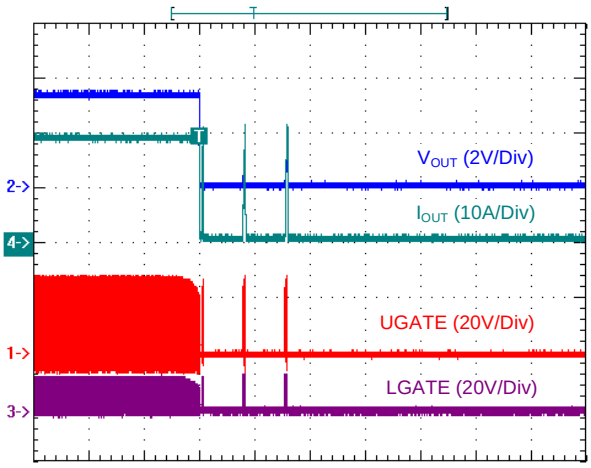

40ns/Div
$V_{IN}$ = $V_{CC}$ = 12V, $I_{LOAD}$ = 10A

**Gate waveforms**



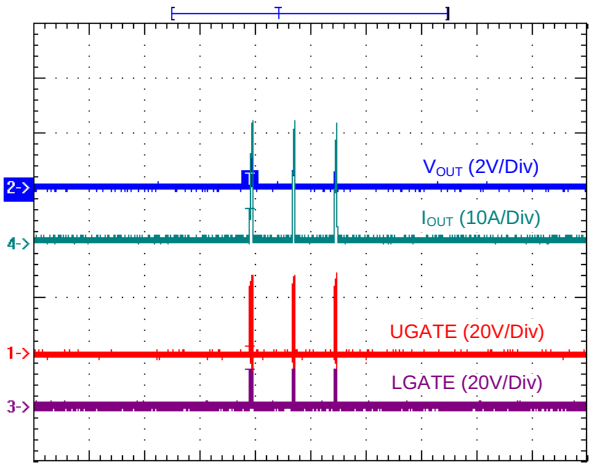

40ns/Div
$V_{IN}$ = $V_{CC}$ = 12V, $I_{LOAD}$ = 10A

**OCP**



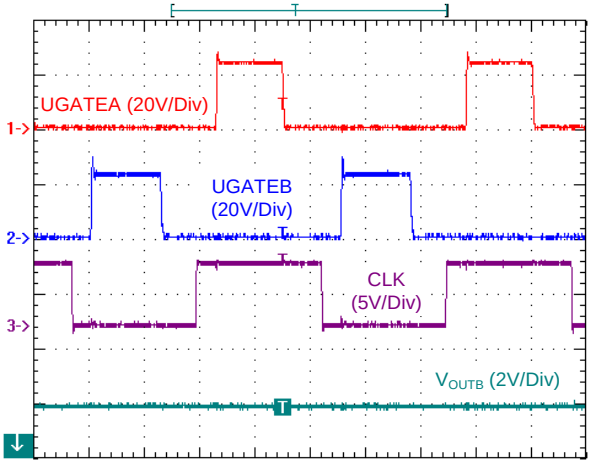

40ms/Div

**SCP**




40ms/Div

**Operation Mode for uP9303A/B**




1us/Div

## Application Information

### Power MOSFET Selection

External component selection is primarily determined by the maximum load current and begins with the selection of power MOSFET switches. The uP9303 requires two external N-channel power MOSFETs for upper (controlled) and lower (synchronous) switches. Important parameters for the power MOSFETs are the breakdown voltage $V_{(BR)DSS}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance $C_{RSS}$, maximum current $I_{DS(MAX)}$, gate supply requirements, and thermal management requirements.

The gate drive voltage is powered by VCC pin that receives 10.8V~13.2V supply voltage. When operating with a 12V power supply for VCC (or down to a minimum supply voltage of 8V), a wide variety of NMOSFETs can be used. Logic-level threshold MOSFET should be used if the input voltage is expected to drop below 8V. Since the upper MOSFET is used as the current sensing element, particular attention must be paid to its on-resistance. Look for $R_{DS(ON)}$ ratings at lowest gate driving voltage.

Special cautions should be exercised on the lower switch exhibiting very low threshold voltage $V_{GS(TH)}$. The shoot-through protection present aboard the uP9303 may be circumvented by these MOSFETs if they have large parasitic impedances and/or capacitances that would inhibit the gate of the MOSFET from being discharged below its threshold level before the complementary MOSFET is turned on. Also avoid MOSFETs with excessive switching times; the circuitry is expecting transitions to occur in under 50 nsec or so.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty cycle. Since the uP9303 is operating in continuous conduction mode, the duty cycles for the MOSFETs are:

$$D_{UP} = \frac{V_{OUT}}{V_{IN}} ; \quad D_{LO} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The resulting power dissipation in the MOSFETs at maximum output current are:

$$P_{UP} = I_{OUT}^2 \times R_{DS(ON)} \times D_{UP} + 0.5 \times I_{OUT} \times V_{IN} \times T_{SW} \times f_{OSC}$$

$$P_{LO} = I_{OUT}^2 \times R_{DS(ON)} \times D_{LO}$$

where $T_{SW}$ is the combined switch ON and OFF time.

Both MOSFETs have $I^2R$ losses and the top MOSFET includes an additional term for switching losses, which are largest at high input voltages. The bottom MOSFET losses are greatest when the bottom duty cycle is near 88%, during a short-circuit or at high input voltage. These equations assume linear voltage current transitions and do not adequately model power loss due the reverse-recovery of the lower MOSFET's body diode. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

The gate-charge losses are dissipated by the uP9303 and don't heat the MOSFETs. However, large gate charge increases the switching interval, $T_{SW}$ that increases the MOSFET switching losses. The gate-charge losses are calculated as:

$$P_G = V_{CC} \times (V_{CC} \times (C_{ISS\_UP} + C_{ISS\_LO}) + V_{IN} \times C_{RSS}) \times f_{OSC}$$

where $C_{ISS\_UP}$ is the input capacitance of the upper MOSFET, $C_{ISS\_LO}$ is the input capacitance of the lower MOSFET, and $C_{RSS\_UP}$ is the reverse transfer capacitance of the upper MOSFET. Make sure that the gate-charge loss will not cause over temperature at uP9303, especially with large gate capacitance and high supply voltage.

### Output Inductor Selection

Output inductor selection usually is based the considerations of inductance, rated current, size requirement, and DC resistance (DC)

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{1}{f_{OSC} \times L_{OUT}} \times V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$.

There is another tradeoff between output ripple current/ voltage and response time to a transient load. Increasing the value of inductance reduces the output ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

## Application Information

Maximum current ratings of the inductor are generally specified in two methods: permissible DC current and saturation current. Permissible DC current is the allowable DC current that causes 40°C temperature raise. The saturation current is the allowable current that causes 10% inductance loss. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current.

The size requirements refer to the area and height requirement for a particular design. For better efficiency, choose a low DC resistance inductor. DCR is usually inversely proportional to size.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements.

**Input Capacitor Selection**

The synchronous-rectified buck converter draws pulsed current with sharp edges from the input capacitor resulting in ripples and spikes at the input supply voltage. Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time upper MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of upper MOSET and the source of lower MOSFET to avoid the stray inductance along the connection trace.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck converter is calculated as:

$$I_{IN(RMS)} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{IN(RMS)} = I_{OUT(RMS)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

For a through-hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can also be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

**Output Capacitor Selection**

An output capacitor is required to filter the output and supply the load transient current. The selection of $C_{OUT}$ is primarily determined by the ESR required to minimize voltage ripple and load step transients. The output ripple $\Delta V_{OUT}$ is approximately bounded by:

$$\Delta V_{OUT} \le \Delta I_L \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}}\right)$$

Since ΔIL increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types.

The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout. Modern components and loads are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

## Application Information

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes.

However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading.

Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

**Bootstrap Capacitor Selection**

An external bootstrap capacitor $C_{BOOT}$ connected to the BOOT pin supplies the gate drive voltage for the upper MOSFET. This capacitor is charged through the internal diode when the PHASE node is low. When the upper MOSFET turns on, the PHASE node rises to $V_{IN}$ and the BOOT pin rises to approximately $V_{IN}$ + $V_{CC}$. The boot capacitor needs to store about 100 times the gate charge required by the upper MOSFET. In most applications 0.1uF to 0.47uF, X5R or X7R dielectric capacitor is adequate.

**PCB Layout Considerations**

High speed switching and relatively large peak currents in a synchronous-rectified buck converter make the PCB layout a very important part of design. Fast current switching from one device to another in a synchronous-rectified buck converter causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise that result in overvoltage stress on devices. Careful component placement layout and printed circuit design minimizes the voltage spikes induced in the converter.

Follow the layout guidelines for optimal performance of uP9303

1 The upper and lower MOSFETs turn on/off and conduct pulsed current alternatively with high slew rate transition. Any inductance in the switched current path generates a large voltage spike during the switching. The interconnecting traces between VIN, MOSFETs and GND conduct pulsed current with sharp transient and should be part of a ground or power plane in a printed circuit board to minimize the voltage spike. Make all the connection the top layer with wide, copper filled areas.

2 Place the power components as physically close as possible.

2.1 Place the input capacitors, especially the high-frequency ceramic decoupling capacitors, directly to the drain of upper MOSFET ad the source of the lower MOSFET. To reduce the ESR replace the single input capacitor with two parallel units

2.2 Place the output capacitor between the converter and load.

3 Place the uP9303 near the upper and lower MOSFETs with pins 8 to 14 facing the power components. Keep the components connected to pins 1 to 7 close to the uP9303 and away from the inductor and other noise sources (noise sensitive components).

4 Use a dedicated grounding plane and use vias to ground all critical components to this layer. The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs. Use an immediate via to connect the components to ground plane including GND of uP9303 Use several bigger vias for power components.

5 Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes to maintain good voltage filtering and to keep power losses low. Also, for higher currents, it is recommended to use a multilayer board to help with heat sinking power components.

6 The PHASE node is subject to very high dV/dt voltages. Stray capacitance between this island and the surrounding circuitry tend to induce current spike and capacitive noise coupling. Keep the sensitive circuit away from the PHASE node and keep the PCB area small to limit the capacitive coupling. However, the PCB area should be kept moderate since it also acts as main heat convection path of the lower MOSFET.

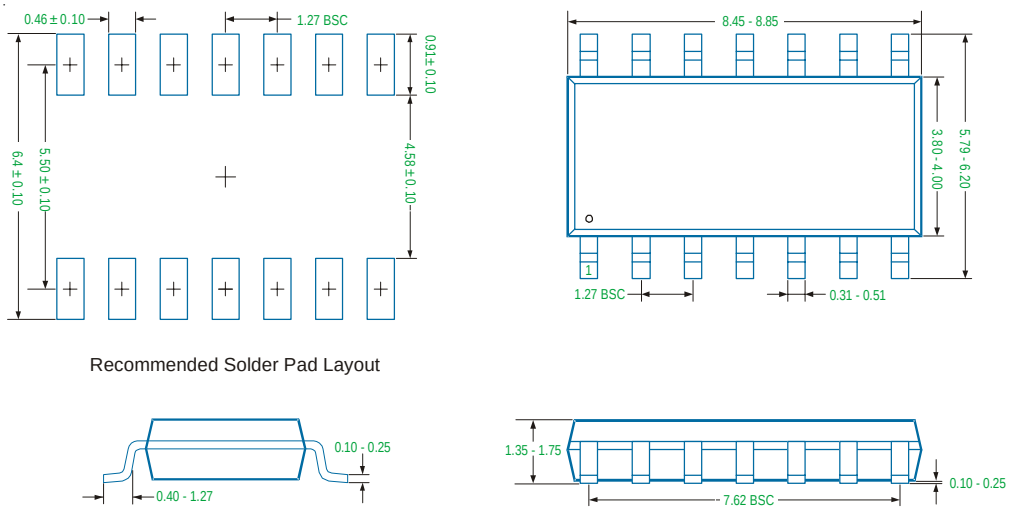
7 uP9303 sources/sinks impulse current to turn on/off the upper and lower MOSFETs. The connecting trace between the controller and gate/source of the MOSFET should be wide and short to minimize the parasitic inductance along the traces.

8 Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component.

9 Provide local VCC decoupling between VCC and GND pins. Locate the capacitor, $C_{BOOT}$ as close as practical to the BOOT and PHASE pins.

## Package Information

SOP-14L Package




Recommended Solder Pad Layout

Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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