3/2/1-Phase Synchronous-Rectified Buck Controller for GPU Power

General Description

The uP9510 is a 3/2/1-phase synchronous-rectified buck controller specifically designed to work with 10.8V ~ 13.2V input voltage and deliver high quality output voltage for high-performance graphic processor power.

The uP9510 adopts proprietary RCOT™ technology, providing flexible selection of output LC filter and excellent transient response to load and line change.

The uP9510 supports NVIDIA Open Voltage Regulator-2+ with PWMVID feature. The PWMVID input is buffered and filtered to generate accurate reference voltage, and the output voltage is precisely regulated to the reference input.

The uP9510 integrates two bootstrapped MOSFET gate drivers and one PWM output achieving optimal balance between cost and flexibility. The uP9510 uses MOSFET $R_{DS(ON)}$ current sensing for channel current balance.

Other features include accurate and reliable over current limit protection, adjustable on-time setting, power saving control input, and power good output. This part is available in VQFN4x4 - 24L package.

Ordering Information

Order Number	Package Type	Top Marking
uP9510PQAG	VQFN4x4 - 24L	uP9510P

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

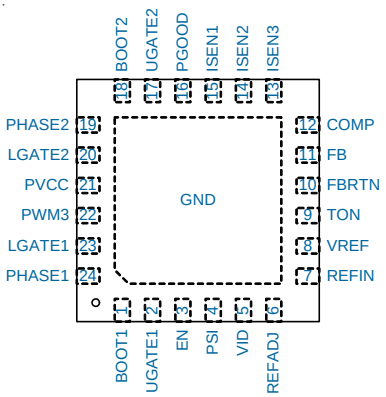
Features

- **Support NVIDIA's Open VReg Type-2+ PWMVID Technology**
- **Input Voltage Range 10.8V ~ 13.2V**
- **Robust Constant On-Time Control**
- **3/2/1 Phase Operation**
- **Two Integrated MOSFET Drivers with Shoot-Through Protection and Internal Bootstrap Schottky Diode**
- **Adjustable Current Balancing by $R_{DS(ON)}$ Current Sensing**
- **Adjustable Operation Frequency**
- **External Compensation**
- **Dynamic Output Voltage Adjustment**
- **Adjustable Per-Phase Over Current Limit**
- **Adjustable Soft-Start Time**
- **Power Good Indication**
- **Over Voltage Protection**
- **Under Voltage Protection**
- **Over Temperature Protection**
- **RoHS Compliant and Halogen Free**

Applications

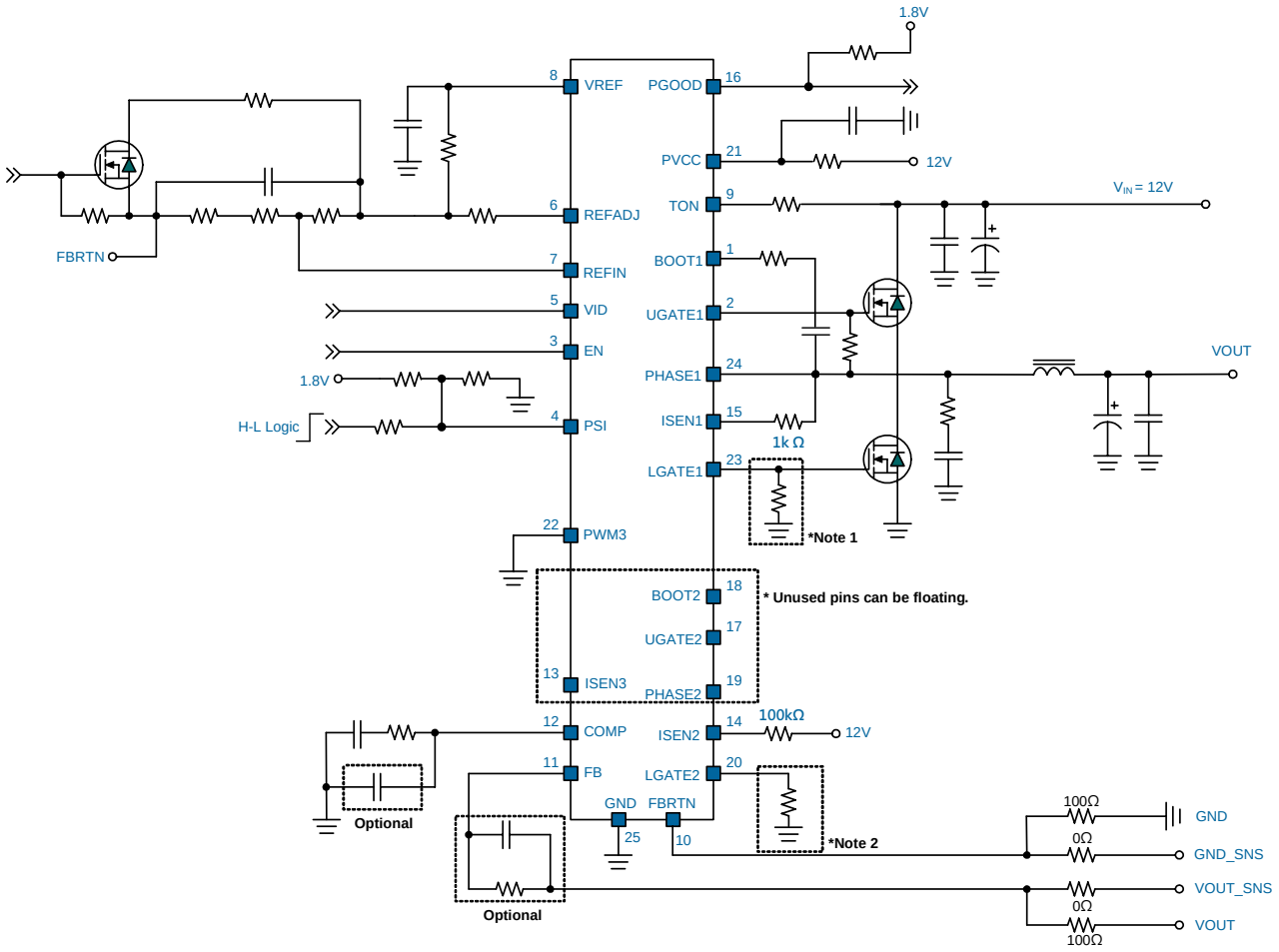
- **Middle-High End GPU Core Power**
- **High End Desktop PC Memory Core Power**
- **Low Output Voltage, High Power Density DC-DC Converters**
- **Voltage Regulator Modules**

Pin Configuration



Typical Application Circuit

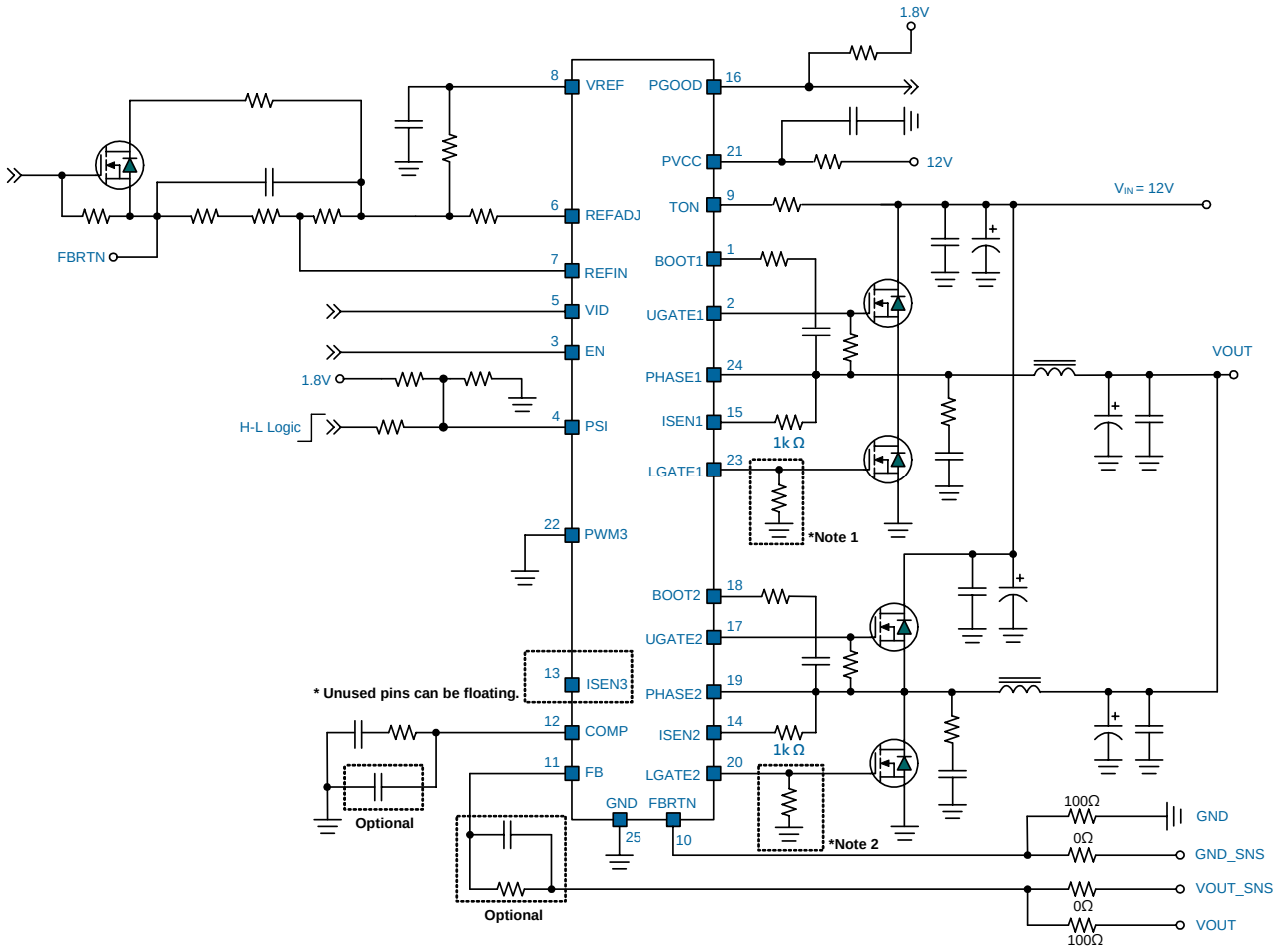
1-Phase Mode



*Note 1 : Programs per-phase over current limit threshold.
*Note 2 : Programs output ramp-up time during power on.

Typical Application Circuit

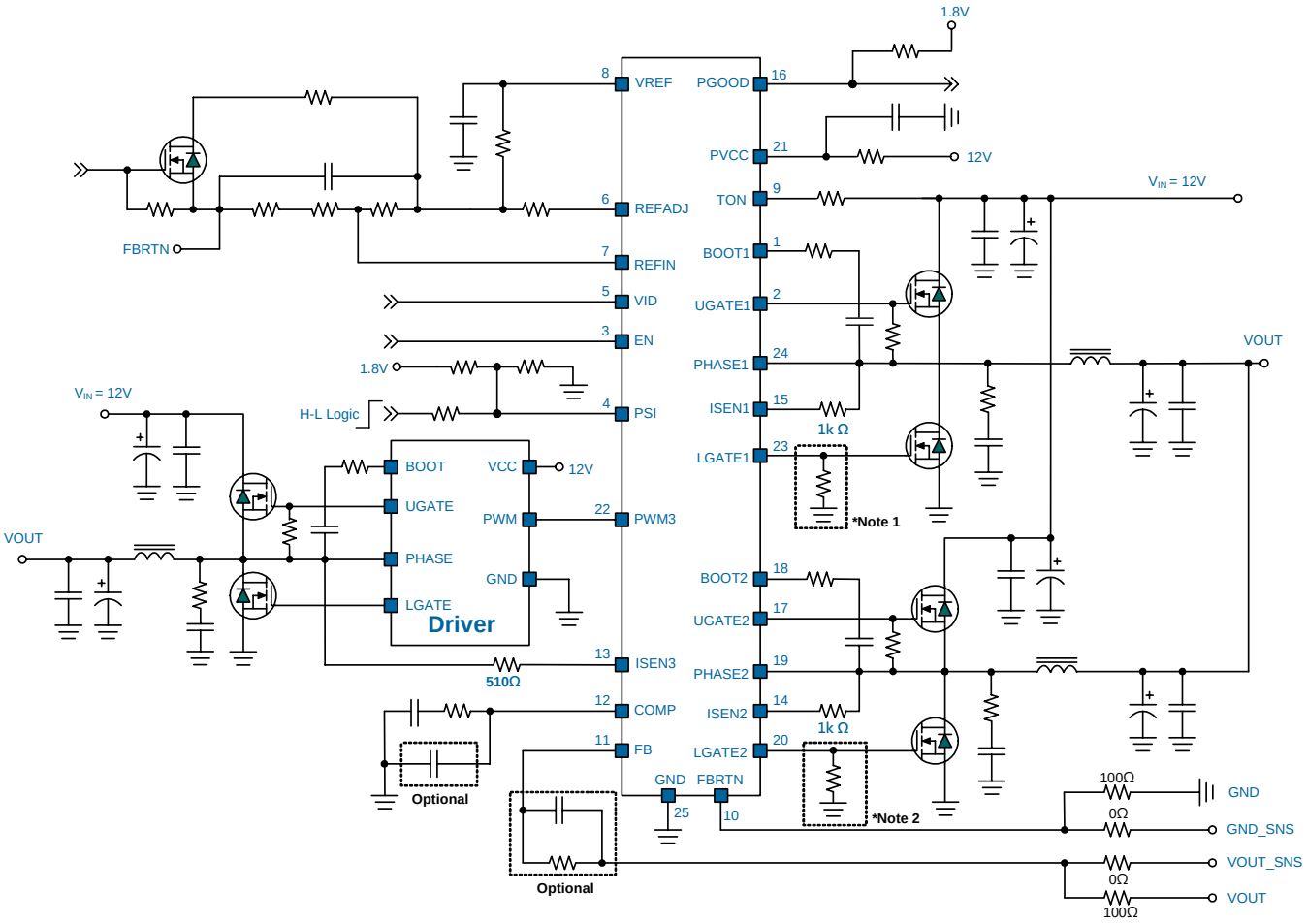
2-Phase Mode



*Note 1 : Programs per-phase over current limit threshold.
*Note 2 : Programs output ramp-up time during power on.

Typical Application Circuit

3-Phase Mode

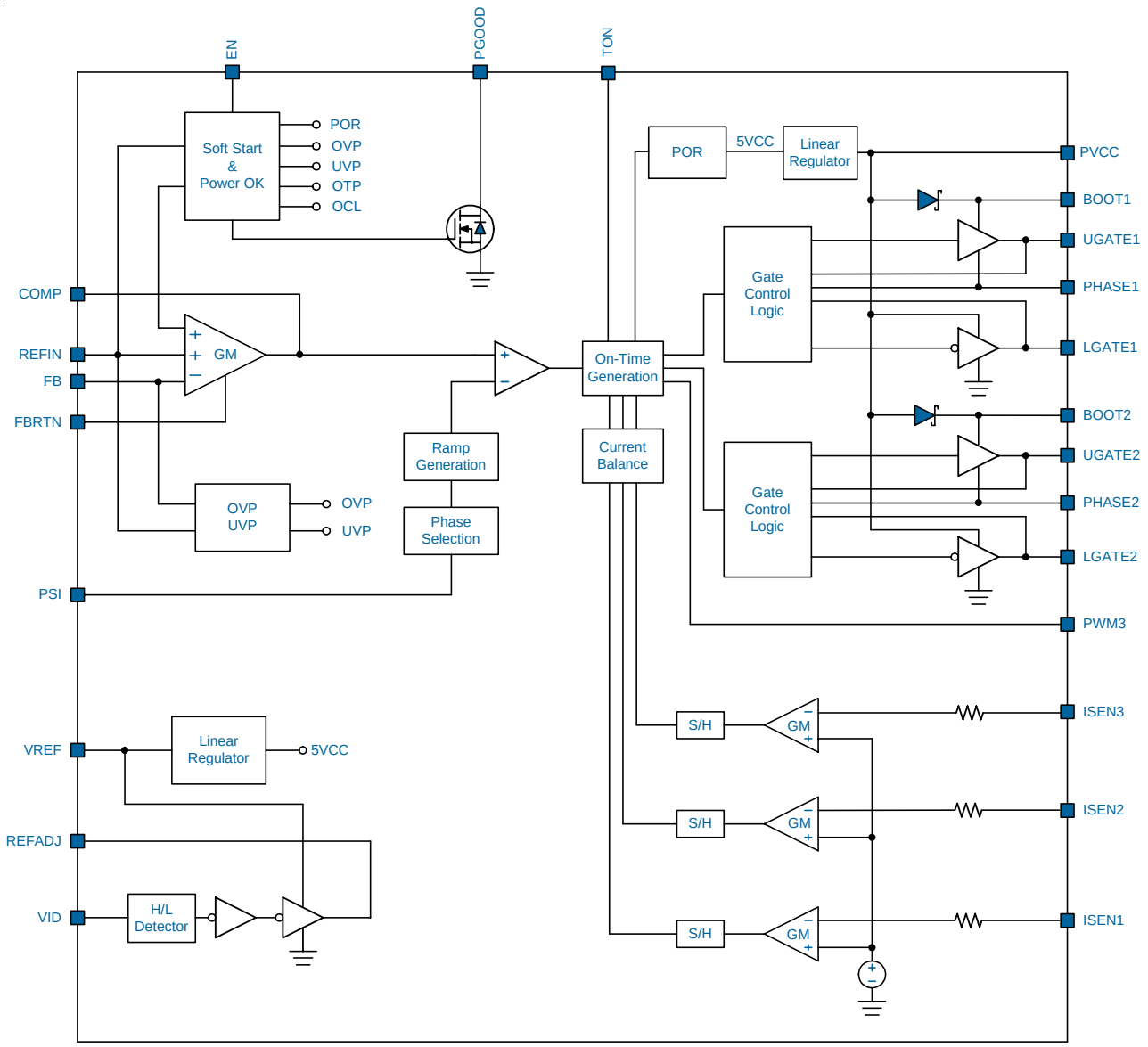


***Note 1 : Programs per-phase over current limit threshold.**
***Note 2 : Programs output ramp-up time during power on.**

Functional Pin Description

No.	Name	Pin Function
1	BOOT1	**BOOT for Phase 1.** Connect a capacitor form this pin to PHASE1 to form a bootstrap circuit for upper gate driver of the phase 1.
2	UGATE1	**Upper Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 upper MOSFET.
3	EN	**Enable.** Chip enable.
4	PSI	**Power Saving Input.** An input pin receiving power saving control signal from GPU. PSI input voltage determines the controller operating mode. Do not leave this pin open.
5	VID	**VID.** PWMVID input pin.
6	REFADJ	**Reference Adjustment.** PWMVID output pin. Connect this pin with an RC integrator to generate REFIN voltage.
7	REFIN	**Reference Input.** Connect this pin to an external reference voltage through a resistor or connect to the output of the REFADJ circuit.
8	VREF	**Reference Voltage.** 2V LDO voltage output pin. Connect an at least 1uF decoupling capacitor between this pin and GND.
9	TON	**On-time Setting Pin.** Connect a resistor from this pin to VIN to set the on-time of the upper MOSFET. Do NOT add any extra capacitor to this pin.
10	FBRTN	**Return for the Reference Circuit.** Connect this pin to the ground point where output voltage is to be regulated.
11	FB	**Feedback Pin.** This pin is the inverting input of the error amplifier.
12	COMP	**Compensation Output.** This pin is the output of the error amplifier. Connect an RC network from this pin to GND to compensate the voltage control loop.
13	ISEN3	**ISEN3.** Connect this pin to the PHASE3 pin ONLY with 510Ω resistor to sense phase 3 output current. **DO NOT use other resistor.**
14	ISEN2	**ISEN2.** Connect this pin to the PHASE2 pin with a resistor to sense phase 2 output current.
15	ISEN1	**ISEN1.** Connect this pin to the PHASE1 pin with a resistor to sense phase 1 output current.
16	PGOOD	**Power Good Indication.** Open-drain structure. Connect this pin to a voltage source with a pull-up resistor.
17	UGATE2	**Upper Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 upper MOSFET.
18	BOOT2	**BOOT for Phase 2.** Connect a capacitor form this pin to PHASE2 to form a bootstrap circuit for upper gate driver of the phase 2.
19	PHASE2	**Phase Pin for Phase 2.** This pin is the return path of upper gate driver for phase 2. Connect a capacitor from this pin to BOOT2 to form a bootstrap circuit for upper gate driver of the phase2.
20	LGATE2	**Lower Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 lower MOSFET.
21	PVCC	**Supply Input for the IC.** Voltage power supply of the IC. Connect this pin to a 12V supply through a 2.2Ω ~ 10Ω resistor and decouple using at least a 1uF ceramic capacitor.
22	PWM3	**PWM Output of Phase 3**. Connect this pin to the PWM input pin of the companion gate driver. Connect this pin to GND to configure this device as a 2-phase controller.
23	LGATE1	**Lower Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 lower MOSFET.
24	PHASE1	**Phase Pin for Phase 1.** This pin is the return path of upper gate driver for phase 1. Connect a capacitor from this pin to BOOT1 to form a bootstrap circuit for upper gate driver of the phase 1.
Exposed Pad		**Ground.** Tie this pin to ground island/plane through the lowest impedance connection available.

Functional Block Diagram



Supply Input and Power On Reset

The uP9510 receives supply input from PVCC pin to provide current to gate drivers and internal control circuit. PVCC is continuously monitored for power on reset. The POR level is typical 9V at rising. The TON pin voltage is used for on-time calculation and should be connected to the supply input of power stage.

The uP9510 integrates floating MOSFET gate driver that are powered from the PVCC pin. A bootstrap Schottky diode is embedded to facilitates PCB design and reduce the total BOM cost. No external Schottky diode is required in real applications.

Phase Number of Operation (Hardware Setting)

The uP9510 supports 3/2/1 phase operation. The maximum phase number of operation is determined by checking the PWM3 and ISEN2 status when POR. Connect PWM3 pin to GND and ISEN3 floating for maximum 2-phase operation. Connect ISEN2 pin to PVCC with 100kΩ resistor and connect PWM3 to GND for maximum 1-phase operation. When configured to 1-phase operation, the components of PHASE2/PHASE3 can be unstuffed. Once selected, the maximum phase number of operation is latched and can only be changed at the next POR.

Table 1. Operation Phase Number Settings

Configuration	Pin Connection, Pull High/Low to Target			
	PWM3	ISEN3	ISEN2	ISEN1
2+1 phase	--	--	--	--
2 phase	GND	Floating	--	--
1 phase	GND	Floating	PVCC	--

Note 1: " -- " denotes normal connection.
Note 2: Use 100kΩ pull up resistor when pull up to PVCC
Note 3: Strictly follow the table for phase disable. Incorrect pin pull up/down connection may cause catastrophic fault during start up.

Constant On-Time Setting

The uP9510 adopts a compensated constant-on-time control scheme. A resistor R_{TON} connected to TON pin programs the constant on time according to the equation:

$$T_{ON}(ns) = \frac{V_{OUT}}{V_{IN}} \times \frac{R_{TON}}{9} \times 100 \quad (ns)$$

where R_{TON} is in kΩ, V_{IN} is the supply input voltage and V_{OUT} is the output voltage.

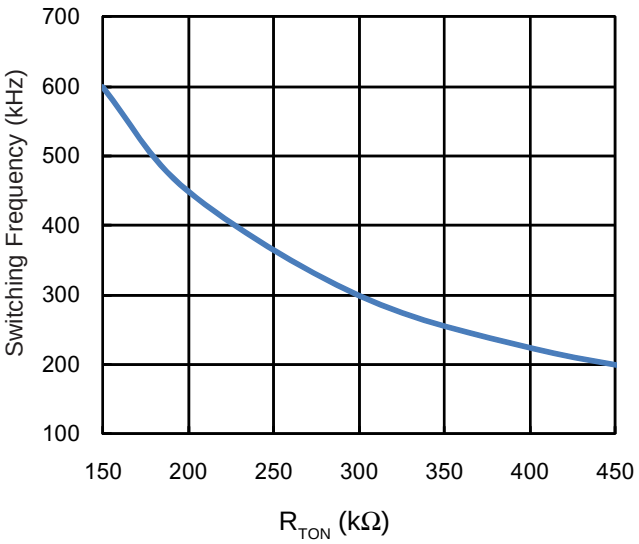


Figure 1. Switching Frequency vs. R_{TON}

Voltage Control Loop and PWMVID Function

Figure 2 illustrates the voltage control loop of the uP9510. FB and REFIN are negative and positive inputs of the Error Amplifier respectively. The Error Amplifier modulates the COMP voltage V_{COMP} of buck converter to force FB voltage V_{FB} follows V_{REFIN}.

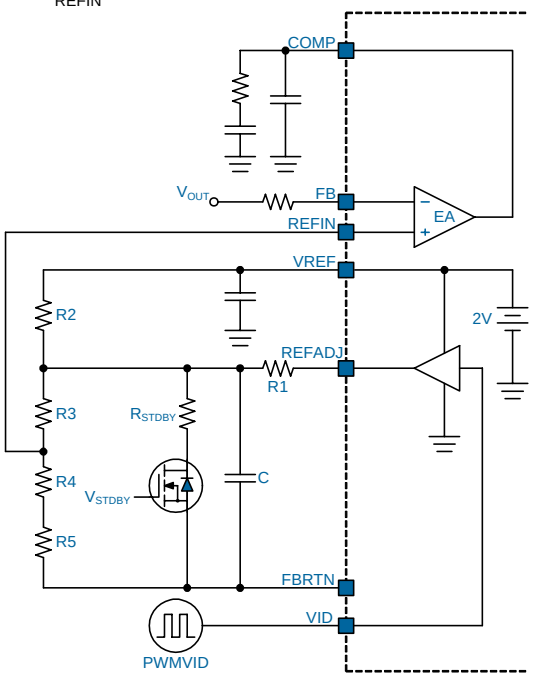


Figure 2. Voltage Control Loop

The PWMVID signal from GPU is applied to the VID pin, which is the input pin of the internal buffer. This buffer plays the role of level shifting, and the output of this buffer is injected into the external RC integrator to generate REFIN voltage, which can be calculated as:

$$V_{REFIN} =$$

$$V_{VREF} \times D \times \frac{R2//(R3+R4+R5)}{R1+R2//(R3+R4+R5)} \times \frac{R4+R5}{R3+R4+R5} +$$

$$V_{VREF} \times \frac{R1//(R3+R4+R5)}{R2+R1//(R3+R4+R5)} \times \frac{R4+R5}{R3+R4+R5}$$

where $V_{REFIN,DC}$ is the DC voltage of REFIN, V_{VREF} is the voltage of VREF (typically 2V), and D is the duty cycle of PWMVID input.

Boot Voltage and Standby Mode

The new generation PWMVID structure includes two operation modes other than normal operation: boot mode and standby mode. During boot mode, the GPU stops sending PWMVID signal and the input of the PWMVID buffer is floating. The REFADJ pin enters high impedance state after the VID pin enters tri-state region, and the REFIN voltage can then be calculated as:

$$V_{REFIN,BOOT} = V_{VREF} \times \frac{R4+R5}{R2+R3+R4+R5}$$

During standby mode, other than GPU stopping the PWMVID transaction, an external system standby signal additionally controls the entry of standby mode. An additional external switch should be connected in parallel with the original PWMVID resistors as shown in Figure 3 to generate the standby mode voltage:

$$V_{REFIN,STDBY} =$$

$$V_{VREF} \times \frac{(R3+R4+R5)//R_{STDBY}}{R2+(R3+R4+R5)//R_{STDBY}} \times \frac{R4+R5}{R3+R4+R5}$$

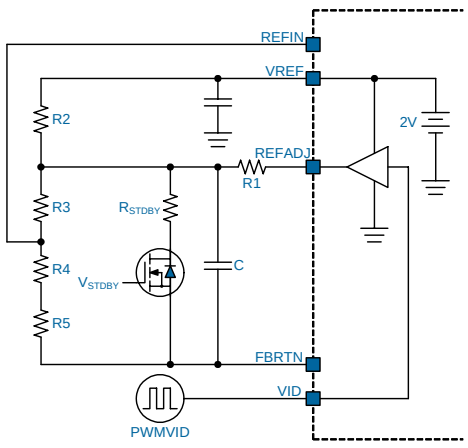


Figure 3. Standby Mode Configuration

Channel Current Balance

The uP9510 senses phase currents for current balance by the means of on-resistance of power stage low-side MOSFET as shown in Figure 4.

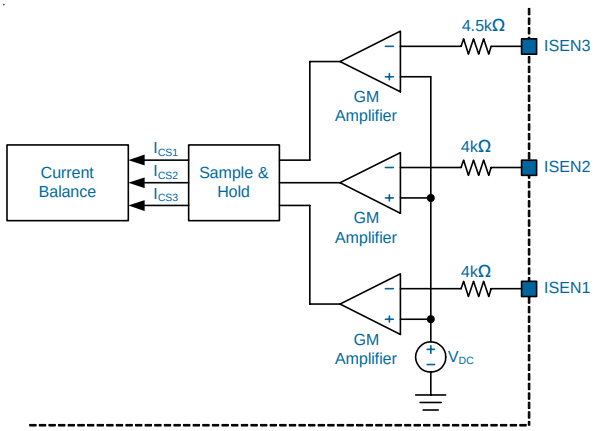


Figure 4. $R_{DS(ON)}$ Current Sensing Scheme

The GM amplifier senses the voltage drop across the low-side MOSFET and converts it into current signal each time it turns on. The sampled and held current is expressed as:

$$I_{CSX} = \frac{(I_{LX} \times R_{DS(ON)} + V_{DC})}{R_{ISENX}}$$

where I_{LX} is the phase N current in Ampere, $R_{DS(ON)}$ is the on-resistance of low-side MOSFET of the power stage in mΩ, V_{DC} is an internal 30mV voltage source, and R_{ISENX} is the external sensing resistor connected at ISENx pins plus the internal resistor to ISENx pins. In this current sense mechanism, the valley of the inductor current is sampled and held. Therefore, the equivalent sensed current can be described by the following equation:

$$I_{LX\_SH} = I_{LX\_AVG} - \frac{1}{2} \times \Delta I_{LX}$$

The sensed current I_{LX_SH} is mirrored to the current balance circuit, comparing between each other, and generating current adjusting signals for each phase. These current adjusting signals are fed to the on-time circuit of the uP9510 to separately adjust each phase on-time for the purpose of adjusting current balance.

The external R_{ISEN} resistor connected at ISEN3 pin should be 510Ω. It can **NOT** use other resistor due to the limitation of Multi-Phase DCM and Phase3 OCL functions. If the phase current unbalance exists in actual application. Fine adjustment of R_{ISEN1} and R_{ISEN2} is allowed for phase current adjustment; however, the resistance of R_{ISEN1} and R_{ISEN2} can **NOT** go lower than 510Ω.

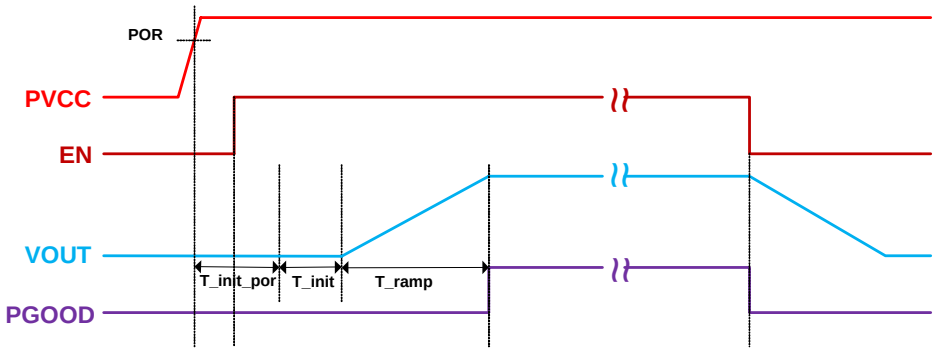
Functional Description

Soft-Start and Power Good

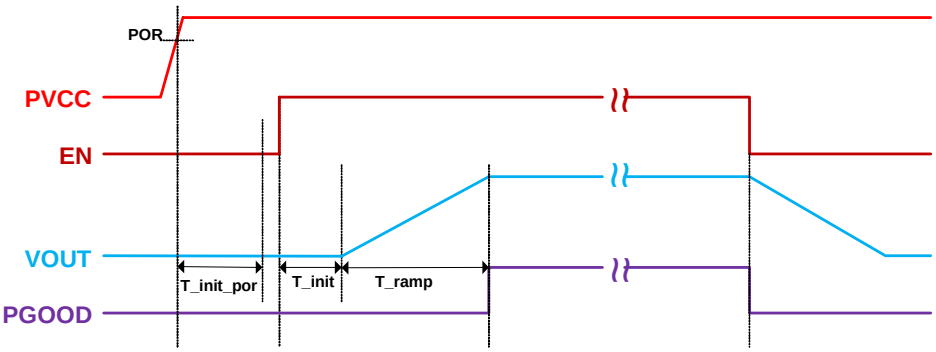
A built-in soft-start is used to prevent surge current from power supply input during turn on. The error amplifier is a three-input device. Reference voltage V_{REFIN} or the internal soft-start voltage SS whichever is smaller dominates the behavior of the non-inverting inputs of the error amplifier. SS internally ramps up to 5VCC with a slew rate determined by V_{REFIN} after the soft start cycle is initiated. Accordingly, the output voltage will follow the SS signal and ramp up smoothly to its target level. The output voltage ramp-up time can be selected through a resistor which is connected from LGATE2 to GND. To keep LGATE2 functional setting work normally, the total capacitance from LGATE2 to GND can **NOT** be larger than 12nF (including C_{ISS} capacitance of Low Side MOSFET). The output ramp-up time selection table is shown as the following table. Figure 5 shows the Soft Start Sequence.

Table 2. Output Ramp Up Time Setting

R_{LG2}	Output Voltage Ramp Up Time (T_ramp)
10kΩ	150us
22kΩ	500us
51kΩ	1ms
Open	1.5ms



Soft Start II



Soft Start I

Figure 5. Soft-Start Sequence

Power Saving Mode

The uP9510 provides power saving features for platform designers to program platform specific power saving configuration. There are four operation modes: multi-phase CCM, multi-phase DCM, single-phase CCM, and single-phase DCM. The uP9510 switches between these four operation modes according to the input voltage level of the PSI pin. Figure 6 shows typical PSI application circuit, and Table 3 shows recommended PSI setting voltage level of four operation modes. In single-phase operation, the uP9510 auto-selects phase 1 to be the operating phase.

DCM operation mode is activated by two conditions:

1. PSI voltage stays at "Single-Phase DCM" or "Multi-Phase DCM" operation mode.
2. After PGOOD goes high, VID pin has received a high or low input signal.

Once the DCM mode is activated, the uP9510 automatically reduces switching frequency at light load to maintain high efficiency. As the load current decreases, the rectifying MOSFET is turned off when zero inductor current is detected, and the converter runs in discontinuous conduction mode.

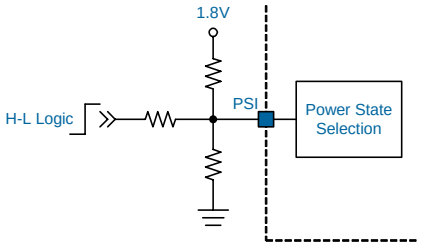


Figure 6. PSI application circuit

Table 3. Recommended PSI Setting

Operation Mode	Recommended Voltage Setting at PSI
Multi-Phase CCM	1.8V
Multi-Phase DCM	1.2V
Single-Phase CCM	0.6V
Single-Phase DCM	GND

Over Current Limit

The uP9510 monitors the inductor valley current by low side MOSFET $R_{DS(ON)}$ when it turns on. The over current limit is triggered once the sensing current level is higher than V_{OC}. When triggered, the over current limit will keep high side MOSFET off even the voltage loop commands it to turn on.

The output voltage will decrease if the load continuously demands more current than current limit level. The current limit threshold is set by connecting a resistor (Roc) from LGATE1 to GND. To keep OCL function work normally, the total capacitance from LGATE1 to GND can **NOT** be larger than 12nF (including C_{ISS} capacitance of Low Side MOSFET).The voltage across PHASE and GND pins is compared with V_{OC} for current limit. The current limit threshold is calculated as:

$$I_{LIM}(A) = \frac{V_{OC}(mV)}{R_{DS(ON)}} + \frac{I_{RIPPLE}}{2}$$

And , R_{OC} resistance can be calculated as:

$$R_{OC}(k\Omega) = \frac{500mV}{\frac{V_{OC}(mV) - 40mV}{360mV} \times \frac{255}{8}(uA) + 5uA}$$

V_{OC} is the per-phase GND-PHASE voltage when the power stage low-side MOSFETs is turned-on; $R_{DS(ON)}$ is the on-resistance of equivalent per-phase power stage low side MOSFET and I_{RIPPLE} is the peak-to-peak inductor ripple current at steady state.

The minimum Voc is 40mV and the maximum V_{OC} is 400mV. Controller will keep the minimum V_{OC} level even if designer sets the V_{OC} level lower than 40mV, and vice versa.

Over Voltage Protection (OVP)

The OVP is triggered if V_{FB} > 1.5xV_{REFIN} sustained 6us. When OVP is activated, the uP9510 turns on all low-side MOSFETs and turns off all high-side MOSFETs. The over voltage protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Under Voltage Protection (UVP)

The under voltage protection is triggered if V_{FB} < 0.5xV_{REFIN} sustained 10us. When UVP is activated, the uP9510 turns off all high-side and low-side MOSFET. The under voltage protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Over Temperature Protection (OTP)

The uP9510 monitors the temperature of itself. If the temperature exceeds typical 150°C, the uP9510 is forced into shutdown mode. The over temperature protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, PVCC ---------- -0.3V to +15V

BOOTx to PHASEx

DC ---------- -0.3V to +15V

PHASEx to GND

DC ---------- -0.7V to +15V

< 100ns ---------- -8V to +30V

BOOTx to GND

DC ---------- -0.3V to 30V

< 100ns ---------- -5V to +42V

UGATEx to PHASEx

DC ---------- -0.3V to 15.3V

< 100ns ---------- -5V to 15.3V

LGATEx to GND

DC ---------- -0.3V to 15.3V

< 100ns ---------- -5V to 15.3V

Other Pins ---------- -0.3V to +6V

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- 150°C

Lead Temperature (Soldering, 10 sec) ---------- 260°C

ESD Rating (Note 2)

HBM (Human Body Mode) ---------- 2kV

MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)

VQFN4x4 - 24L θ_{JA} ---------- 40°C/W

VQFN4x4 - 24L θ_{JC} ---------- 4°C/W

Power Dissipation, P_D @ T_A = 25°C

VQFN4x4 - 24L ---------- 2.5W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40° C to +125°C

Operating Ambient Temperature Range ---------- -40°C to +85°C

Input Voltage, V_{IN} ---------- 10.8V to 13.2V

Control Voltage, V_{PVCC} ---------- 10.8V to 13.2V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(PVCC = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Quiescent Current	I_Q	V_{REFIN} = 0.9V, EN = 1.8V, V_{FB} = 1V, no switching	--	3	--	mA
Shutdown Current	I_{SHDN}	EN = 0V	--	200	--	uA
PVCC POR Threshold	$V_{PVCCRTH}$	V_{PVCC} rising	8	9	10	V
PVCC POR Hysteresis	$V_{PVCCHYS}$		--	1	--	V
VREF Voltage Accuracy	V_{REF}		1.98	2	2.02	V
VREF Sourcing Current	I_{REF}		10	--	--	mA
Control Input: EN						
Logic Low Threshold	V_{EN_L}		--	--	0.6	V
Logic High Threshold	V_{EN_H}		1.2	--	--	V
Internal Pull-down Resistance	R_{EN}		--	150	--	kΩ
Reference Voltage						
REFIN Disable Threshold			--	0.1	--	V
External Rererence Voltage Range	V_{REFIN}		0.2	--	2	V
On Time						
One Shot Width	T_{ON}	V_{IN} = 12V, V_{OUT} = 1.2V, F_{SW} = 300kHz	--	333	--	ns
Minimum Off Time	T_{OFF_MIN}		--	300	--	ns
Minimum On Time	T_{ON_MIN}		--	80	--	ns
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by Design	--	70	--	dB
Gain Bandwidth Product	$G_{BW(EA)}$	Guaranteed by Design	--	10	--	MHz
Offset Voltage	$V_{OS(EA)}$		-1	--	1	mV
Trans-conductance	GM		--	2020	--	uA/V
Maximum Current (Source & Sink)	I_{COMP}		--	300	--	uA
Current Sense Amplifier (Current Balance)						
Input Offset Voltage	V_{OFF_CSA}		-1	--	1	mV
Max Sourcing Current	I_{SRC_CSA}		100	--	--	uA
ISENx Voltage	V_{DC_CSA}		25	30	35	mV
Internal Current Sense Resistance	R_{ISENX_INT}	Internal R_{ISEN1} & R_{ISEN2}	--	4	--	kΩ
		Internal R_{ISEN3}	--	4.5	--	

Electrical Characteristics

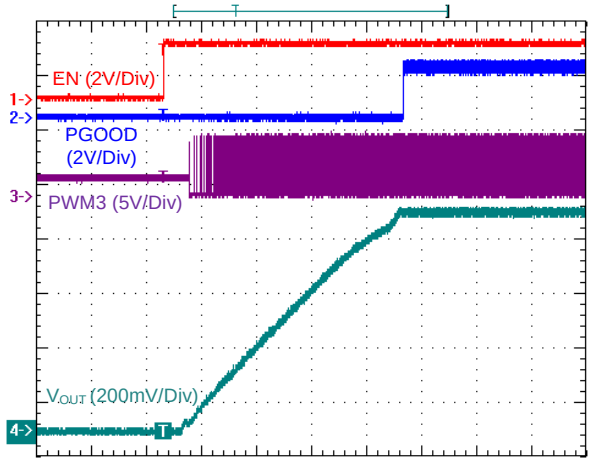
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
FBRTN						
FBRTN Current	I_{FBRTN}	EN = 1.4V, no switching	--	--	500	uA
Soft Start						
Initialization Time at POR	T_init_por	Refer to Figure 5	--	--	350	us
Initialization Time	T_init	Refer to Figure 5	--	--	250	us
Output Voltage Ramp-Up Time	T_ramp	Refer to Figure 5, R_{LG2} = Open	--	1.5	--	ms
PWMVID Buffer						
VID Input Low Level	V_{IL_VID}		--	--	0.6	V
VID Input High Level	V_{IH_VID}		1.2	--	--	V
VID Tri-state Delay	T_{TRI_VID}		--	100	--	ns
REFADJ Source Resistance	R_{BF_SRC}	I_{SRC} = 1mA	--	20	--	Ω
REFADJ Sink Resistance	R_{BF_SNK}	I_{SNK} = 1mA	--	20	--	Ω
PWM3 Output						
Output Low Voltage	V_{PWM_L}	I_{SNK} = 4mA	--	--	0.2	V
Output High Voltage	V_{PWM_H}	I_{SRC} = 4mA	4.7	--	--	V
High Impedance State Leakage		V_{PWM} = 0V	-1	--	0	uA
		V_{PWM} = 5V	0	--	1	uA
PSI						
Power Saving Mode Logic	V_{PSI}	Multi-Phase CCM	1.6	--	--	V
		Multi-Phase DCM	1	--	1.4	V
		Single-Phase CCM	0.4	--	0.8	V
		Single-Phase DCM	--	--	0.2	V
Gate Drivers						
Upper Gate Source	R_{UG_SRC}	I_{UG} = -80mA	--	1	2	Ω
Upper Gate Sink	R_{UG_SNK}	I_{UG} = 80mA	--	0.5	1	Ω
Lower Gate Source	R_{LG_SRC}	I_{LG} = -80mA	--	1	2	Ω
Lower Gate Sink	R_{LG_SNK}	I_{LG} = 80mA	--	0.4	0.8	Ω
Dead Time	T_{DT}		--	30	--	ns
Internal Bootstrap Schottky Diode						
Forward Voltage	V_F	Forward Bias Current = 3.5mA	--	0.33	--	V
Zero Current Detection Threshold						
Zero Current Threshold	V_{ZC}		-0.5	--	0.5	mV

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Protection						
Minimum Over Current Threshold	V_{OC_min}	R_{LG1} = Open, measure GND-V_{PHASE}	--	40	--	mV
Maximum Over Current Threshold	V_{OC_max}	R_{LG1} = 12kΩ, measure GND-V_{PHASE}	--	400	--	mV
Over Voltage Protection Threshold	V_{OVP}	V_{FB}/V_{REFIN}	--	150	--	%
Over Voltage Delay Time	T_{OVP}		--	6	--	us
Under Voltage Protection Threshold	V_{UVP}	V_{FB}/V_{REFIN}	--	50	--	%
Under Voltage Delay Time	T_{UVP}		--	10	--	us
Over Temperature Protection Threshold			--	150	--	°C
Power Good Indicator						
PGOOD Output Low Level		I_{SINK} = 4mA	--	--	0.3	V
PGOOD Leakage Current		V_{PGOOD} = 5V	--	--	0.1	uA

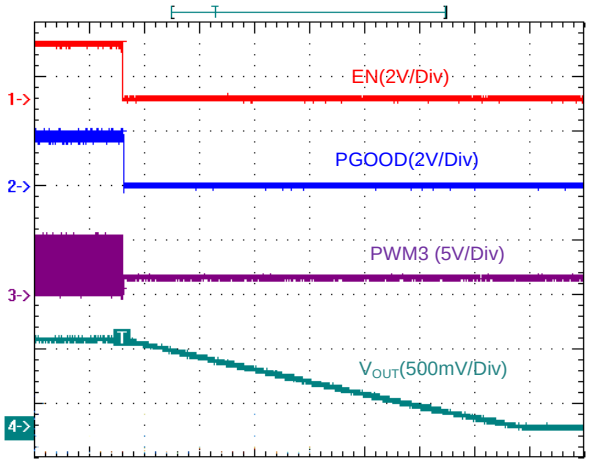
Typical Operation Characteristics

Enable Power On



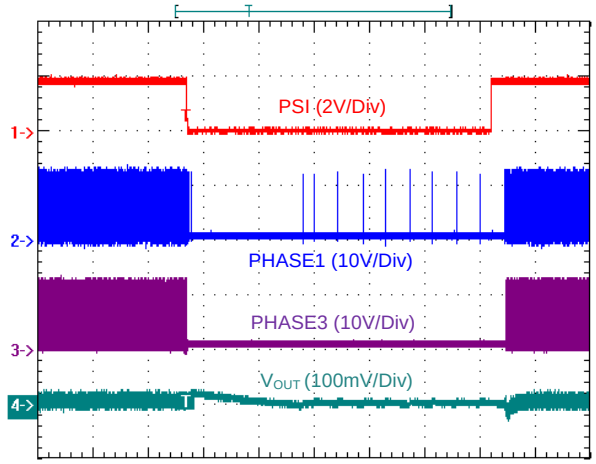
Time：400us/Div
V_{IN} = 12V V_{OUT} = 0.81V, No Load

Enable Power Off



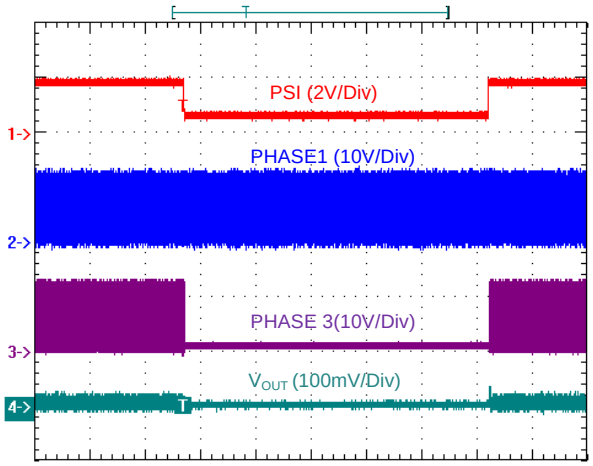
Time：400us/Div
V_{IN} = 12V V_{OUT} = 0.81V, I_{OUT} = 1A

PSI = 1.8V ⇆ 0V



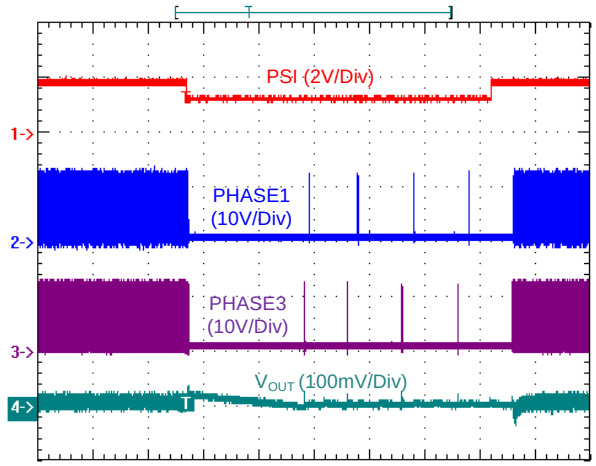
Time：400us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} Offset = 0.81V, I_{OUT} = 0.1A

PSI = 1.8V ⇆ 0.6V



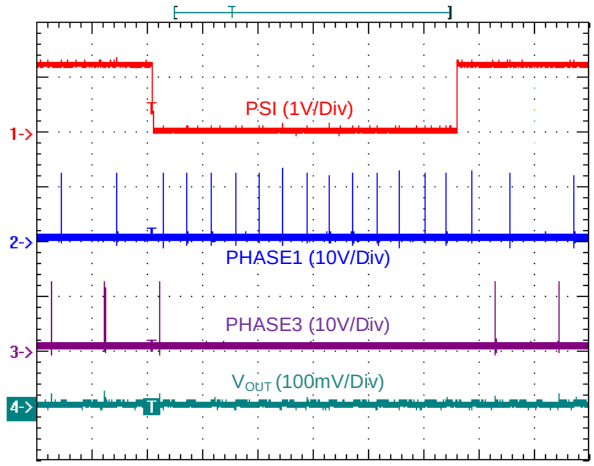
Time：400us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} Offset = 0.81V, I_{OUT} = 0.1A

PSI = 1.8V ⇆ 1.2V



Time：400us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} Offset = 0.81V, I_{OUT} = 0.1A

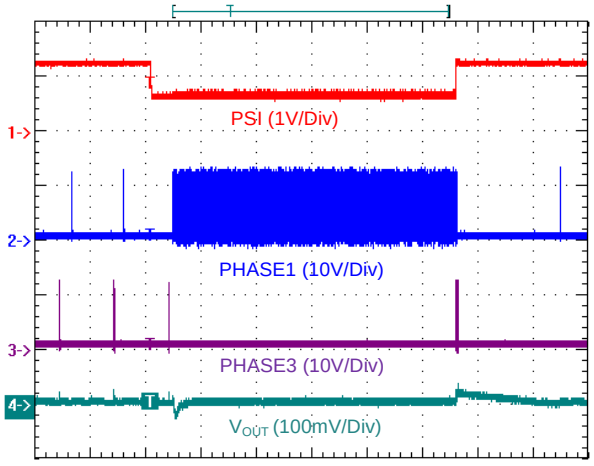
PSI = 1.2V ⇆ 0V



Time：400us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} Offset = 0.81V, I_{OUT} = 0.1A

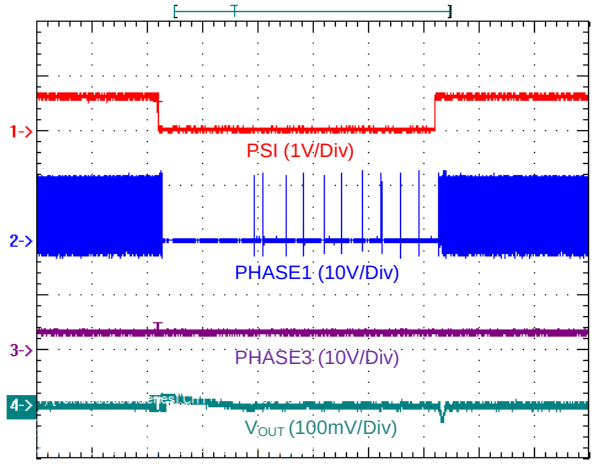
Typical Operation Characteristics

PSI = 1.2V ⇆ 0.6V



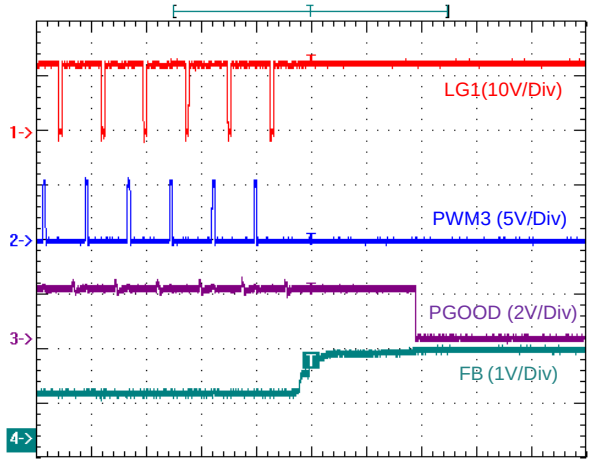
Time：400us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} Offset = 0.81V, I_{OUT} = 0.1A

PSI = 0.6V ⇆ 0V



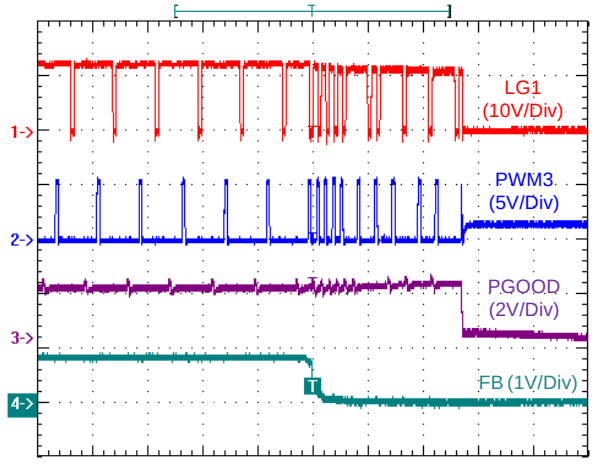
Time：400us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} Offset = 0.81V, I_{OUT} = 0.1A

OVP



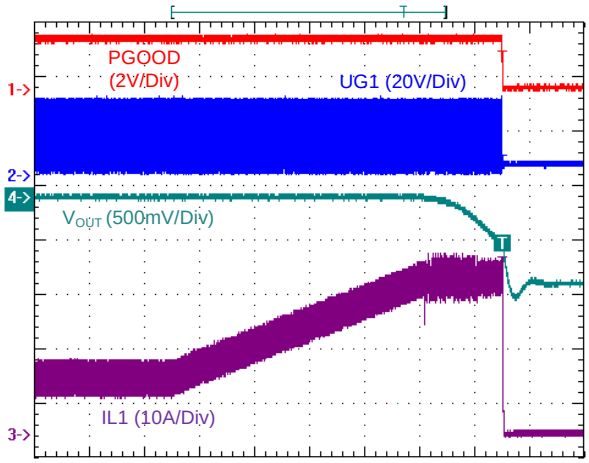
Time：4us/Div
V_{IN} = 12V, No Load

UVP



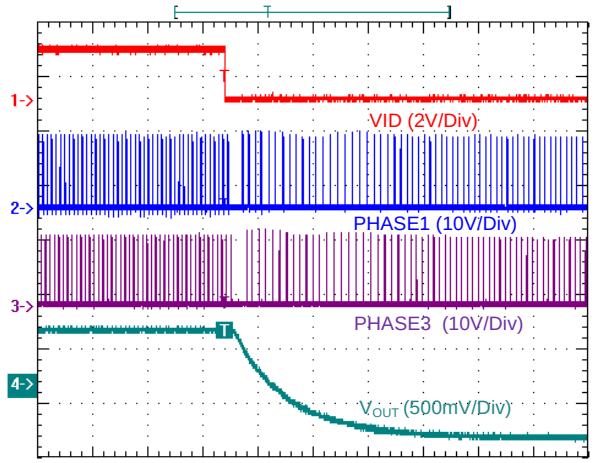
Time：4us/Div
V_{IN} = 12V, No Load

Over Current Limit



Time：400us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} offset = 0.81V,
I_{OUT} = 10A to 70A, R_{LG1} = 91kΩ

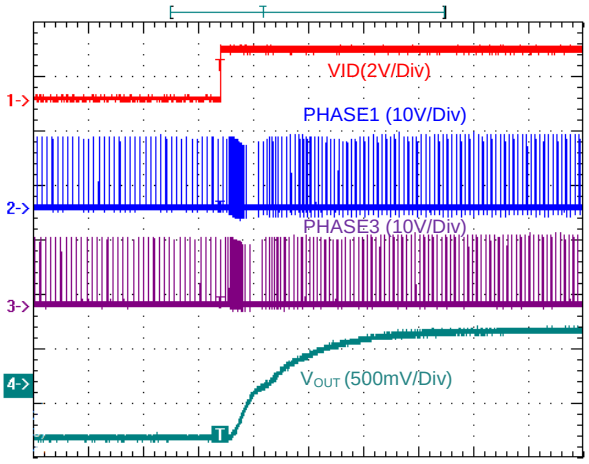
VID Transition: High to Low



Time：40us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} offset = 0.81V, No Load

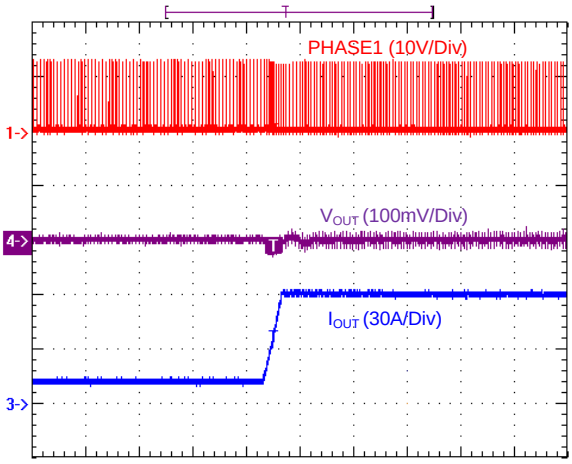
Typical Operation Characteristics

VID Transition: Low to High



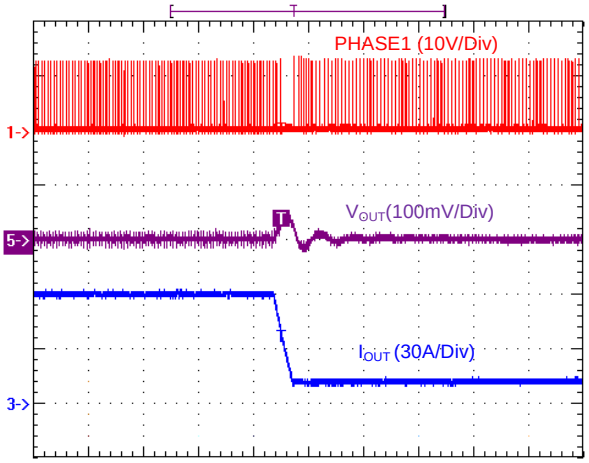
Time：40us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} offset = 0.81V, No Load

Load Transient, Undershoot



Time：40us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} offset = 0.81V,
PSI = 1.8V, I_{OUT} = 14A to 67A

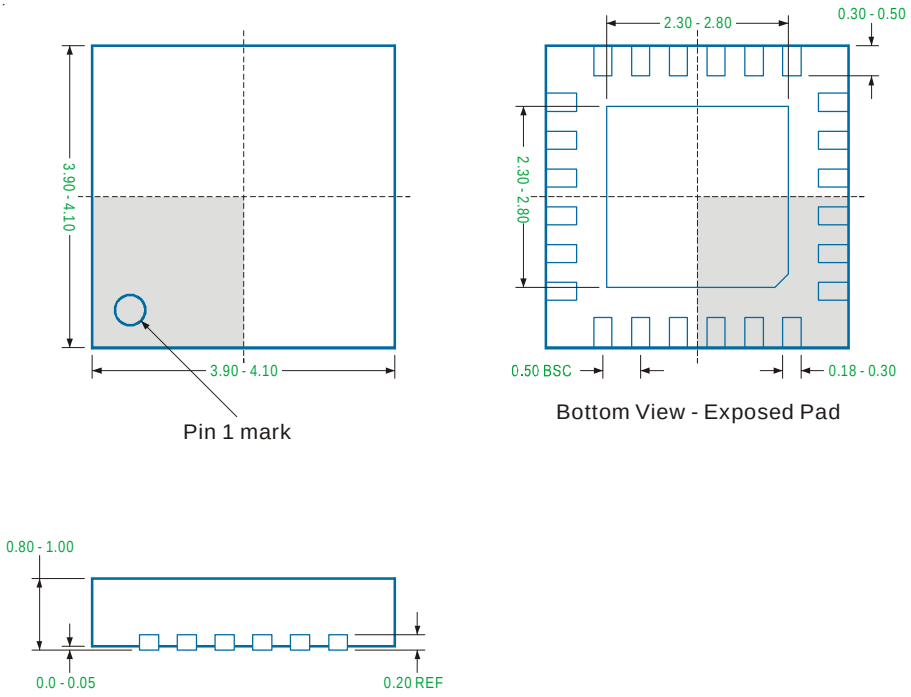
Load Transient, Overshoot



Time：40us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} offset = 0.81V,
PSI = 1.8V, I_{OUT} = 14A to 67A

Package Information

VQFN4x4 - 24L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Important Notice

uPI and its subsidiaries reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

uPI products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment. However, no responsibility is assumed by uPI or its subsidiaries for its use or application of any product or circuit; nor for any infringements of patents or other rights of third parties which may result from its use or application, including but not limited to any consequential or incidental damages. No uPI components are designed, intended or authorized for use in military, aerospace, automotive applications nor in systems for surgical implantation or life-sustaining. No license is granted by implication or otherwise under any patent or patent rights of uPI or its subsidiaries.

uPI Semiconductor Corp.

Headquarter
9F.,No.5, Taiyuan 1st St. Zhubei City,
Hsinchu Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888

Sales Branch Office
12F-5, No. 408, Ruiguang Rd. Neihu District,
Taipei Taiwan, R.O.C.
TEL : 886.2.8751.2062 FAX : 886.2.8751.5064