Wide Input Voltage, High Performance, Single Synchronous Step-Down Converter

General Description

The uP9614 is a high-efficiency, single synchronous buck converter with an internal power switch. With internal low RDS(ON) switches, the high-efficiency buck converter is capable of delivering up to 7A output current for charger interface. The proprietary $RCOT_{TM}$ technology provides fast transient response and high noise immunity. When there is a ripple injection circuit, it can support ceramic and OSCON output capacitors for low ESR application. This combination is ideal for building modern low duty ratio, untra-fast load step response DC-DC converters. The output voltage ranges from 2.9V to12V, and the conversion input voltage ranges is from 10.8V to 30V. The quasi-constant switching frequency is 100kHz. $RCOT_{TM}$ control tracks the 100kHz switching frequency over a wide range of input and output voltages, while it increases the switching frequency at step-up of load.

The strong gate drivers of the uP9614 allow low $R_{DS(ON)}$ FETs for high current applications. It is available in a space saving WQFN4x4-32L package.

Ordering Information

Order Number	Package Type	Top Marking
uP9614PQMI	WQFN4X4-32L	uP9614P
uP9614QQMI	WQFN4X4-32L	uP9614Q

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

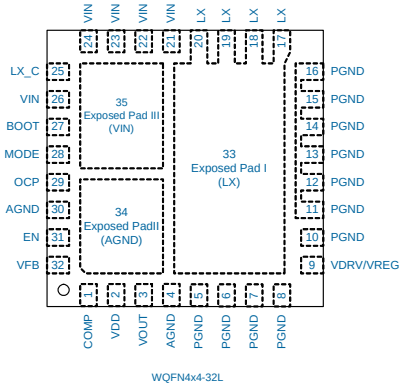
Features

- **Input Voltage Absolute Maximum Rating: 32V**
- **Wide Input Voltage Range: 10.8V to 30V**
- **Input Over Voltage Protection: 32V (typ.)**
- **Output Voltage Range: 2.9V to 12V**
- **Wide Output Load Range: 0A to 7A**
- **Built-In 1% 1V Reference**
- **$RCOT_{TM}$ (Robust Constant On-Time) Control Architecture**
- **Quasi-Constant Switching Frequency Operation: 100kHz**
- **1ms, 2ms, 4ms and 8ms Selectable Output Voltage Soft-Start**
- **Pre-charged Start-up Capability**
- **Built-in Output Discharge**
- **Built-in VIN OVP/VOUT OVP/Output UVP/OCP/OTP**
- **WQFN4x4-32L Package**
- **RoHS Compliant and Halogen Free**

Applications

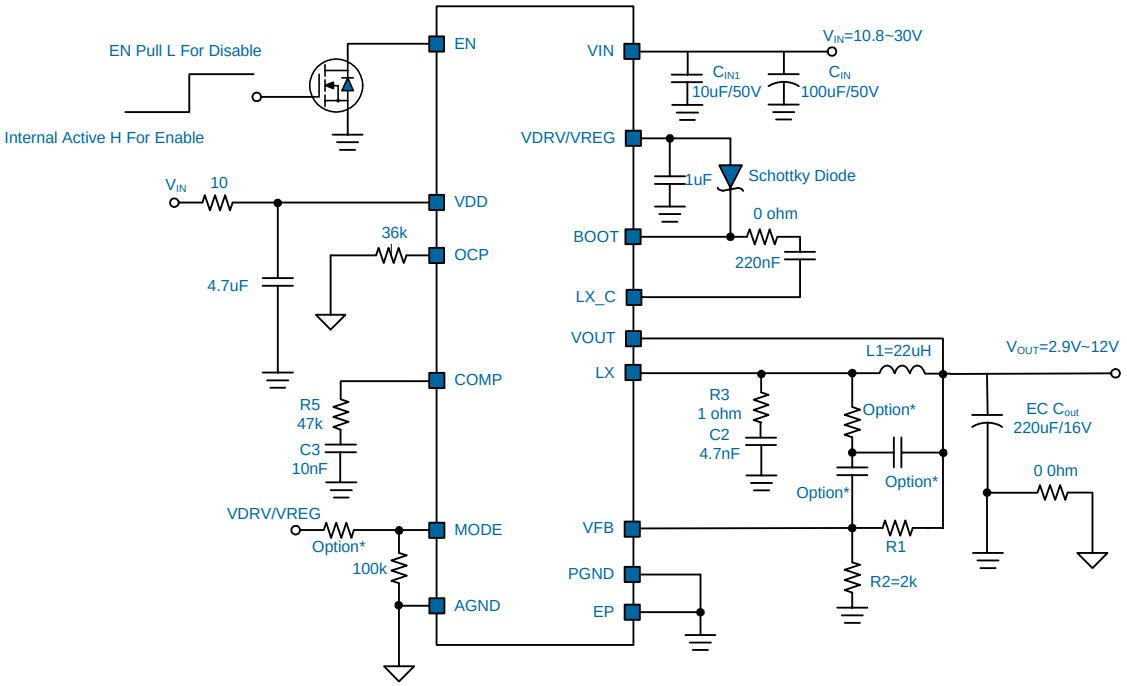
- **Portable Charging Devices**
- **Point-of-Load Systems**
- **Notebook Computers**
- **I/O Supplies**
- **System Power Supplies**

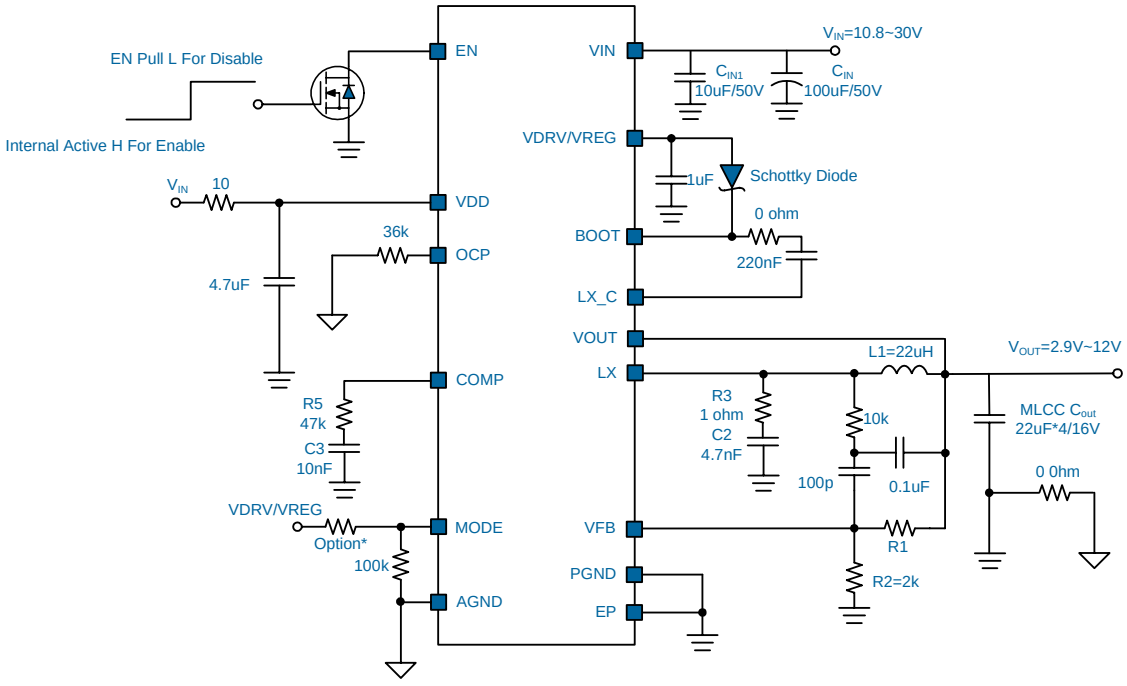
Pin Configuration



WQFN4x4-32L

Typical Application Circuit

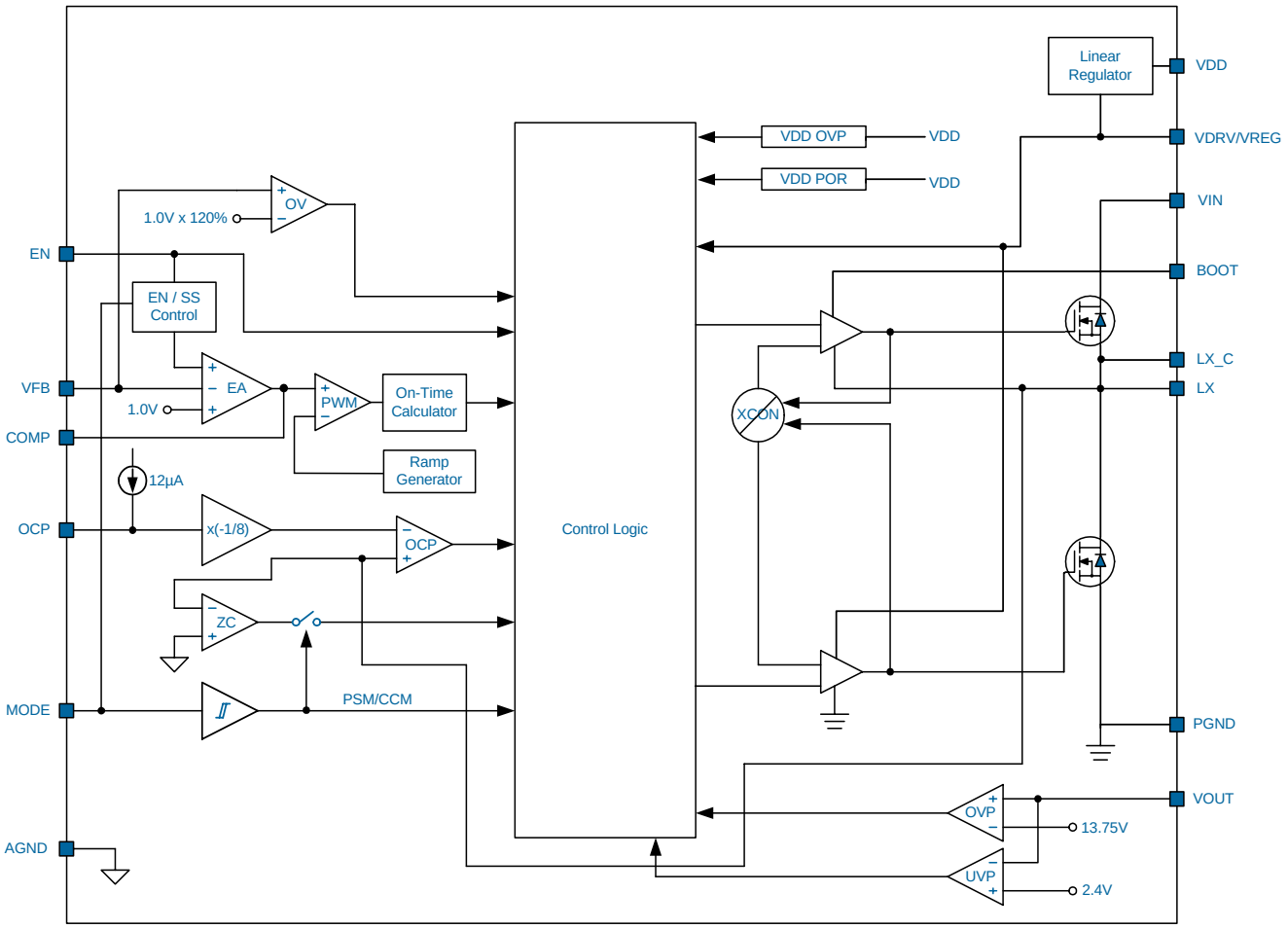




Functional Pin Description

Pin No.	Pin Name	Pin Function
1	COMP	**Error Amplifier Output.** This is the output of the error amplifier and the non-inverting input of the PWM comparator. Use this pin in combination with the FB pin to compensate the voltage-control feedback loop of the converter.
2	VDD	**Converter Power Supply Input.** This pin provides bias voltage for the IC and powers the internal 5V linear regulators. Connect this pin to 10.8V ~ 30V voltage source and bypass it with an R/C filter.
21~24,26	VIN	**Power Supply Input.** Input voltage that supplies current to the output voltage.
3	VOUT	**Output Voltage Feedback.** Connect to output capacitor.
4, 30	AGND	**Signal Ground.**
5~8, 10~16	PGND	**Power Ground.**
9	VDRV / VREG	**5V LDO Output and Gate Drive Supply Voltage Input.**
--	NC	**Not Internally Connected.**
17~20	LX	**Internal Switches Output.** Connect this pin to the output inductor.
25	LX_C	**Internal Switches Output.** Connect the bootstrap capacitor CBOOT to BOOT pin.
27	BOOT	**Bootstrap Supply for the Floating Upper MOSFET Gate Driver.** Connect the bootstrap capacitor C_{BOOT} between BOOT pin and the LX_C pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Ensure that C_{BOOT} is placed near the IC. Externally connected to VREG with a Schottky diode.
28	MODE	**Soft Start and PSM/CCM Selection**. Connect a resistor to select soft-start time and operation mode (Table 1). The soft-start time is detected and stored into internal register during the start-up.
29	OCP	**Over Current Protection Setting.** Connect a resistor from this pin to GND to set the over current protection level. 1The 12uA current is sourced and set Over Current Protection as follows: $V_{OCSET} = 12uA \times R_{OCP.}$ $I_{LIM}=(V_{OCSET}/(8XR_{DS(ON)}))+(I_{RIPPLE}/2)$
31	EN	**Chip Enable**. Internal pull high or short to GND to disable the device.
32	VFB	**Feedback Input.** This pin is the inverting input to the error amplifier. A resistor divider from output to GND is used to set regulator voltage.
33	LX_Exposed Pad I	**Switch Node.** This pin is used as the sink for the upper MOSFET gate driver. This pin is also monitored by the shoot-through protection circuitry to determine when the upper MOSFET has turned off. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET
34	AGND_Exposed Pad II	**Signal Ground**. The exposed pad should be well soldered to PCB with multiple vias to ground plane for optimal thermal performance.
35	VIN_Exposed Pad III	**Power Supply Input.** Input voltage that supplies current to the output voltage.

Functional Block Diagram



Functional Description

The uP9614 implements a unique RCOT$_{TM}$ control topology for the synchronous buck. The RCOT$_{TM}$ supports extremely low ESR output capacitors and makes the design easier and robust. The output voltage ranges from 2.9V to 12V. The conversion input voltage ranges from 10.8V to 30V.

The uP9614 implements adaptive on-time control and it tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

Enable and Soft Start

When the EN pin internal pull high voltage rises above the enable threshold voltage (typically 1.4V), the converter enters its start-up sequence. The internal LDO regulator starts immediately and regulates to 5V at the VREG pin. An internal DAC starts to ramp up the reference voltage from 0V to 1V. Depending on the MODE pin setting, the ramp-up time varies from 1ms to 8ms. Smooth and constant ramp-up of the output voltage is maintained during start-up regardless of load current.

Table 1 Soft-Start and MODE Selection

MODE Selection	Action	Soft-Start Time (ms)	R_{MODE} (kΩ)
Auto Skip	Pull Down to GND	1	39
		2	100
		4	200
		8	475
Forced CCM	Connect to VREG	8	100

PWM On-Time Control

The uP9614 does not have a dedicated oscillator that determines switching frequency. However, the device runs with pseudo-constant frequency by feed-forwarding the input and output voltages into its on-time one-shot timer. The RCOT$_{TM}$ control adjusts the on-time to be inversely proportional to the input voltage and proportional to the output voltage. This makes the switching freuquency fairly constant in steady state conditions over wide input voltage range. The quasi-constant switching frequency is 100kHz.

The off-time is modulated by a PWM comparator. The VFB node voltage (the mid-point of resistor divider) is compared to the internal 1V reference voltage added with a ramp signal. When both signals match, the PWM comparator asserts a set signal to terminate the off-time (turn off the low-side MOSFET and turn on high-side MOSFET). The set signal is valid if the inductor current level is elow the OCP threshold, otherwise the off-time is extended until the current level falls below the threshold.

Light Load Condition in PSM Operation

While the MODE pin is pulled low via RMODE, uP9614 automatically reduces the switching frequency at light load conditions to maintain high efficiency. Detailed operation is described as follows. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The synchronous MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode (DCM). The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage.

The transition point from discontinuous to continuous conduction mode can be calculated as:

$$I_{OUT} = \frac{1}{2 \times f_{OSC} \times L_{OUT}} \times V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Output Discharge Control

When EN is low, the uP9614 discharges the output capacitor using internal MOSFET connected between PHASE and GND while high side and low side MOSFETs are kept off. The current capability of this MOSFET is limited to discharge slowly.

Over Current Limit

the uP9614 monitors the inductor valley current by low side MOSFET $R_{DS(ON)}$ when it turns on. The over current limit is triggered once the sensing current level is higher than V_{OCSET}. When triggered, the over current limit will keep high side MOSFET off even the voltage loop commands it to turn on.

The output voltage will decrease if the load continuously demands more current than current limit level. The current limit level is set at ILIM/2 if the output voltage is lower than 90% of its target level, V_{OUT} decrease faster until UVP occurs and the hiccup cycle time is set by an internal counter .

The current limit threshold is set by connecting a resistor from OCP to GND. The OCP pin will source a 12uA current and create a voltage drop across R_{OCP} as the V_{OCSET}. V_{OCSET} = 12uA x $R_{OCP.}$ When the voltage drop across the low side MOSFET equals the voltage across the setting resistor, the current limit will be activated.

The voltage across LX and GND pins is compared with V_{OCSET} for current limit. The current limit level is calculated as:

$$I_{LIM} = \frac{V_{OCSET}}{8 \times R_{DS(ON)}} + \frac{I_{RIPPLE}}{2}$$

where I_{RIPPLE} is the peak-to-peak inductor ripple current at steady state.

Input Over Voltage Protection

The uP9614 monitors Input voltage VDD to detect Input over voltage protection. When Input voltage becomes higher than 35V of the target voltage, the Input OVP is triggered, then LX stop switching. When the Input OVP condition disappears, the converter will resume normal operation and LX will start switching.

Output Over and Under Voltage Protection

The uP9614 monitors FB voltage to detect over voltage and under voltage. When the FB voltage becomes higher than 120% of the target voltage, the OVP is triggered, The uP9614 provides output short circuit protection function. Once the output loader short-circuits or the output voltage becomes lower than 2.4V, the SCP will be triggered then always hiccup, the hiccup cycle time is set by an internal counter. When the SCP condition disappears, the converter will resume normal operation and the hiccup status will terminate.

UVLO Protection

The uP9614 uses VREG under voltage lockout protection (UVLO). When the VREG voltage is lower than the UVLO threshold voltage,the uP9614 will turn off. This is non-latch protection.

Over Temperature Protection

The uP9614 monitors the temperature of itself. If the temperature exceeds typical 130°C, the uP9614 will be turned off. This is the non-latch protection. It will be recovered once temperature is lower than 110°C.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VIN and VDD ---------- -0.3V to +32V
LX Voltage to GND ---------- -0.3V to (VIN+ -0.3V)
BOOT Pin Voltage ---------- $-V_{LX}$-0.3V to V_{LX}+6V
VDRV/VREG Pin Voltage ---------- -0.3V to +6V
VOUT Pin Voltage ---------- -0.3V to 32V
Other Pins to GND ---------- -0.3V to +6V
Storage Temperature Range ---------- -55°C to +150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
CDM (Charged DeviceMode) ---------- 1kV

Thermal Information

Package Thermal Resistance (Note 3)
WQFN4x4-32L $\theta_{JA, HS}$ ---------- 42°C/W
WQFN4x4-32L $\theta_{JA, LS}$ ---------- 38°C/W
WQFN4x4-32L $\theta_{JC, controller}$ ---------- 21°C/W
WQFN4x4-32L $\theta_{JC, HS}$ ---------- 10°C/W
WQFN4x4-32L $\theta_{JC, LS}$ ---------- 6°C/W
Power Dissipation, P_D @ T_A = 25°C
WQFN4x4-32L $P_{D, controller}$ ---------- 1.85W
WQFN4x4-32L $P_{D, HS}$ ---------- 2.38W
WQFN4x4-32L $P_{D, LS}$ ---------- 2.63W

Recommended Operation Conditions

(Note 4)

Input Voltage, V_{IN} ---------- 10.8V to 30V
Output Voltage, V_{OUT} ---------- 2.9V to 12V
Output Current, I_{OUTmax} ---------- 0A to 7A
Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{IN} = 12V, T_A=25°C, unless otherwise specified)

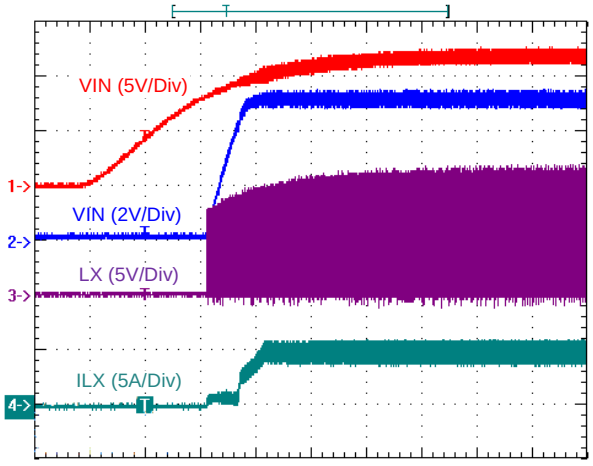
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input Voltage						
Input Voltage Range	V_{IN}		10.8	--	30	V
VDD POR Threshold		VDD Rising	--	--	10.8	V
		VDD Falling	10.3	--	--	
Input OVP Threshold	V_{IN_OVP}	V_{DD_OVP} Rising	--	32	--	V
Supply Current						
VDD Supply Current	I_{VDD}	V_{EN} = 5V, V_{FB} =1.02V, I_{OUT} = No Load	--	420	590	uA
VDD Shutdown Current	I_{VDD_SD}	V_{EN} = 0V, I_{OUT} = No Load,	--	--	20	uA
Internal Reference Voltage						
Feedback Voltage	V_{FB}		0.99	1.00	1.01	V
VFB Input Current	I_{FB}	V_{FB} =1.02V, Skip Mode, T_A = 25°C	--	0.01	--	uA
Error Amplifier Transconductance	GEA	ΔI_C = +10uA	--	200	--	uA/V
Output Voltage Pin		–				
VOUT Discharge Resistor		V_{IN} = 12V. EN = 0V, VOUT = 5.0V	230	320	400	kΩ
Power Switches						
Upper Switch Resistance	$R_{UG,DSON}$	For uP9614P	--	10	13	mΩ
Lower Switch Resistance	$R_{LG,DSON}$	For uP9614P	5.5	6.5	7.5	mΩ
Upper Switch Resistance	$R_{UG,DSON}$	For uP9614Q	--	22	24.5	mΩ
Lower Switch Resistance	$R_{LG,DSON}$	For uP9614Q	5	6.5	9	mΩ
Duty and Frequency Control						
Minimum Off-ime	T_{OFF_MIN}		250	400	600	ns
Soft Start						
Soft Start Time	T_{SS}	From VOUT = 0% to 100%, R_{MODE} = 39kΩ	--	1	--	ms
		From VOUT = 0% to 100%, R_{MODE} = 100kΩ	--	2	--	
		From VOUT = 0% to 100%, R_{MODE} = 200kΩ	--	4	--	
		From VOUT = 0% to 100%, R_{MODE} = 470kΩ	--	8	--	
Logic Threshold and Setting Conditions						
EN Pin Threshold Voltage	V_{EN}	Enable	1.8	--	--	V
		Disable	--	--	0.5	
EN Pull H Source Current	I_{EN}	VEN = 0V	3.2	4	5	uA
Switching Frequency	F_{LX}	V_{IN} = 12V, V_{OUT} = 5V, at CCM	80	100	120	kHz
Protection: Current Sense						
OCP Source Current	I_{CS}		10.88	12	13.2	uA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Protection: OVP and UVP						
Output OVP Threshold Voltage	V_{OVP}	Measured at FB, with respect to reference voltage	115	120	125	%
VOUT OVP Threshold Voltage	V_{OUT_OVP}	Measured at VOUT, with respect to OVP threshold voltage	--	13.75	--	V
VOUT UVP Threshold Voltage	V_{OUT}	Measured at VOUT, with respect to UVP threshold voltage	--	2.4	--	V
VREG LDO Voltage						
VREG UVLO Threshold	$V_{UVLOVREG}$	Rising	3.8	4.0	4.2	V
		Hysteresis	0.27	0.30	0.33	
LDO Output Voltage	V_{REG}		4.95	5.0	5.15	V
LDO Output Current	I_{REG}		--	--	50	mA
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SDN}	Shutdown Temperature	--	130	--	°C
		Hysteresis	--	20	--	

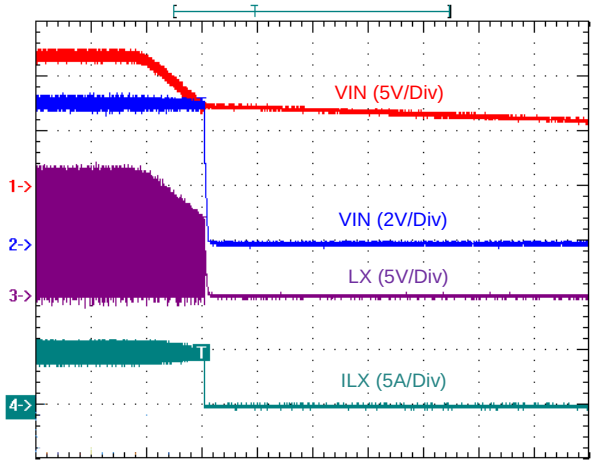
Typical Operation Characteristics

Power On Waveforms



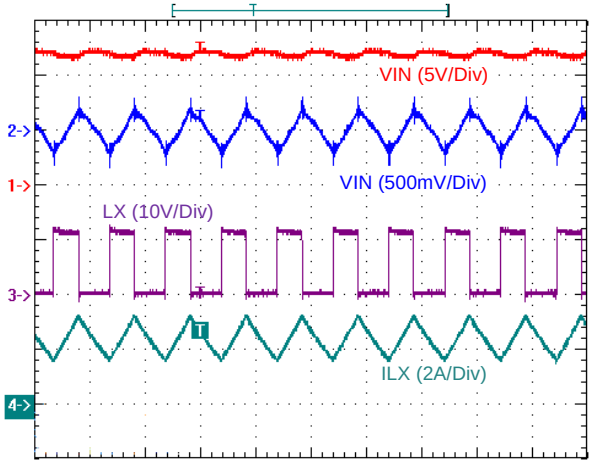
Time：2ms/Div
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 4.8A

Power Off Waveforms



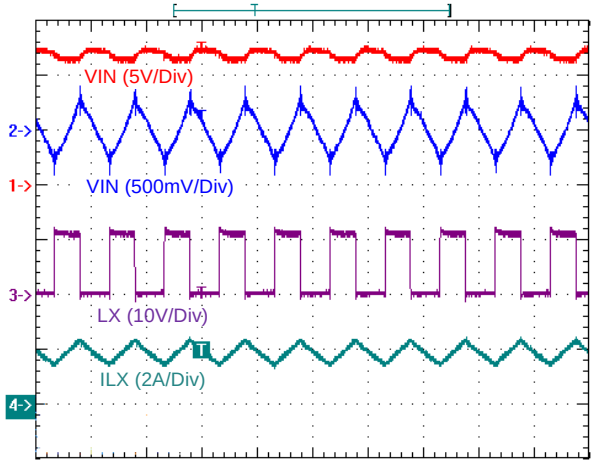
Time：2ms/Div
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 4.8A

Steady State Waveforms



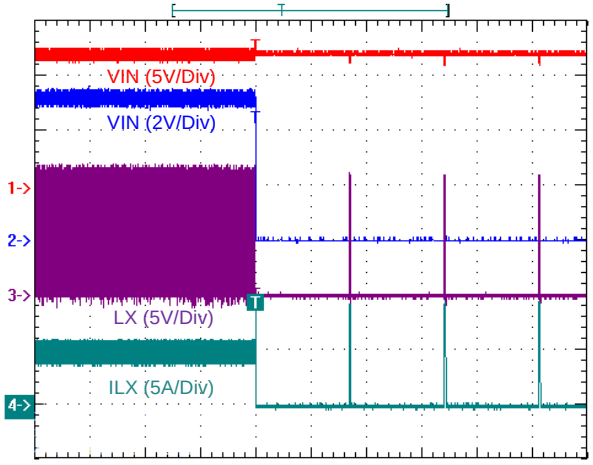
Time：10us/Div
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2.4A

Steady State Waveforms



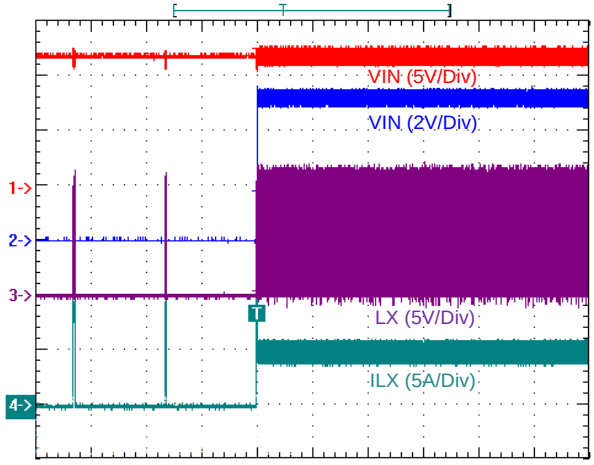
Time：10us/Div
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 4.8A

Short Circuit Protection Waveforms



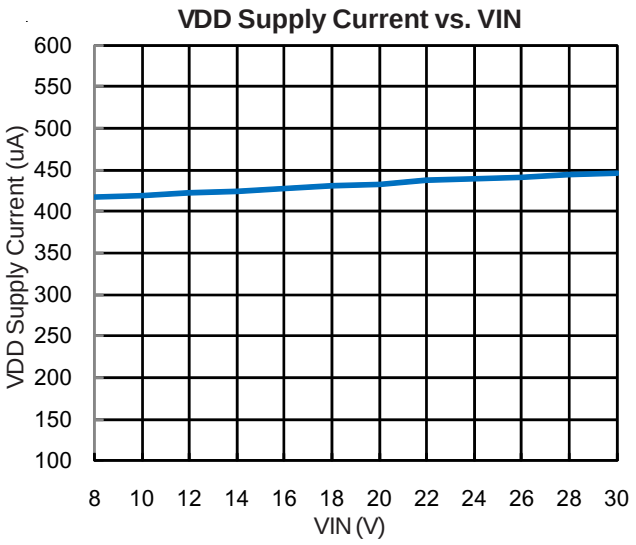
Time：100ms/Div
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 4.8A

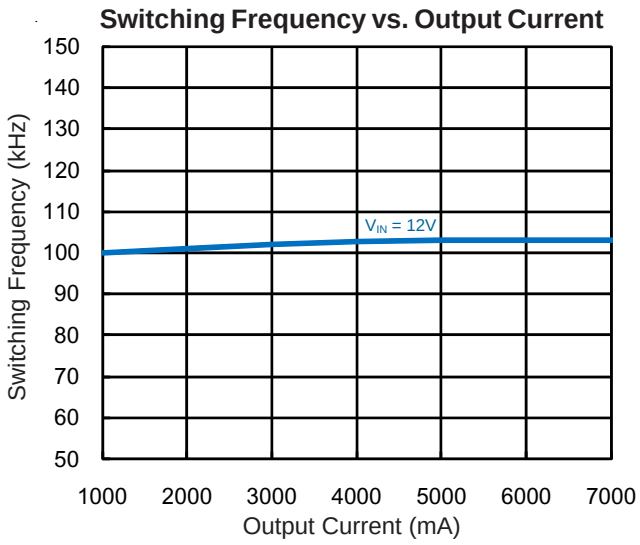
Short Circuit Protection Waveforms

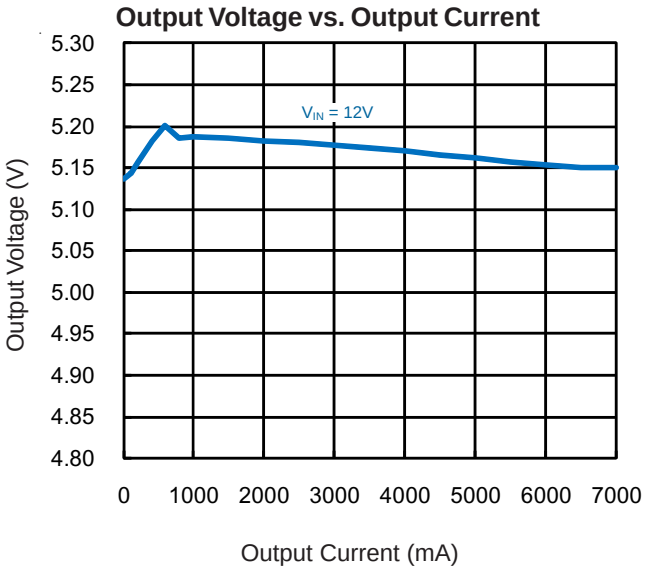


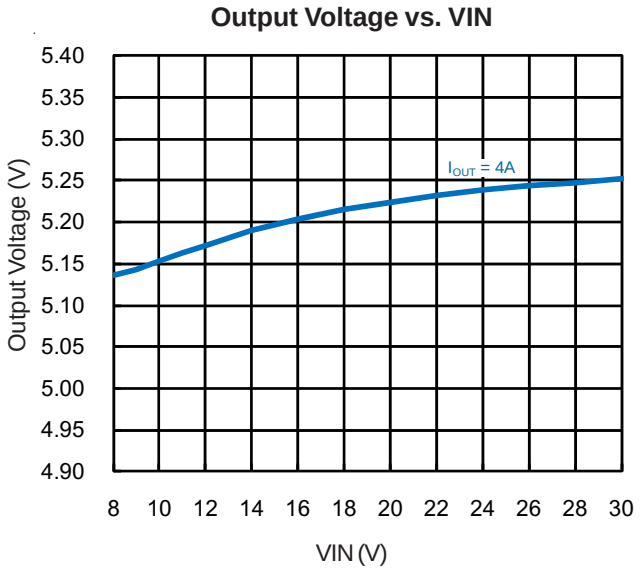
Time：100ms/Div
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 4.8A

Typical Operation Characteristics









Application Information

Output Inductor Selection

Output inductor selection is usually based the considerations of inductance, rated current value, size requirements and DC resistance (DCR). The inductance is chosen based on the desired ripple current. Large value inductors result in lower ripple currents and small value inductors result in higher ripple currents. Higher VIN or VOUT also increases the ripple current as shown in the equation below. A reasonable starting point for setting ripple current is ΔI_L=1500mA(30% of 5000mA).

$$\Delta I_L = \frac{1}{f_{OSC} \times L_{OUT}} \times V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Maximum current ratings of the inductor are generally specified in two methods: permissible DC current and saturation current. Permissible DC current is the allowable DC current that causes 40°C temperature raise. The saturation current is the allowable current that causes 10% inductance loss. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current. If possible, choose an inductor with rated current higher than 7.5A so that it will not saturate even under current limit condition.

The size requirements refer to the area and height requirement for a particular design. For better efficiency, choose a low DC resistance inductor. DCR is usually inversely proportional to size.

Different core materials and shapes will change the size, current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends on the price vs. size requirements and any radiated field/EMI requirements.

Input Capacitor Selection

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 88uF. The best choice is the ceramic type and low ESR electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current.

In the case of electrolytic types, they can be further away if a small parallel 10uF ceramic capacitor is placed right close to the IC. A 100uF electrolytic capacitor and 10uF ceramic capacitor are recommended and placed close to the VIN and PGND pins, with the shortest traces possible.

Output Capacitor Selection

The ESR of the output capacitor determines the output ripple voltage and the initial voltage drop following a high slew rate load transient edge. The output ripple voltage can be calculated as:

$$\Delta V_{OUT} = \Delta I_C \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}}\right)$$

Where f_{OSC} = operating frequency, C_{OUT} = output capacitance and $\Delta I_C = \Delta I_L$ = ripple current in the inductor. The ceramic capacitor with low ESR value provides the low output ripple and low size profile.

In the case of electrolytic capacitors, the ripple is dominated by RESR multiplied by the ripple current. Connect a 220uF electrolytic capacitor at output terminal for good performance and low output ripple and place output capacitors as close as possible to the device. When there is a ripple injection circuit, it can support ceramic and OSCON output capacitors for low ESR application, in the case of ceramic or OSCON output capacitors, RESR is very small and does not contribute to the output ripple.

PCB Layout Considerations

High speed switching and relatively large peak currents in a synchronous-rectified buck converter make the PCB layout a very important part of design. Fast current switching from one device to another in a synchronous-rectified buck converter causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise that result in overvoltage stress on devices. Careful component placement layout and printed circuit board design minimizes the voltage spikes induced in the converter.

Follow the layout guidelines for optimal performance of uP9614.

Application Information

Layout Guidelines:

1.Arrange the power components to reduce the AC loop size consisting of CIN, VIN and LX.

2.The input decoupling ceramic capacitor 10uF must be placed closest to the VIN. PGND and AGND plane should be used through vias or a short and wide path.

3.The input decoupling ceramic capacitor 4.7uF must be placed closest to the VDD. PGND plane and AGND plane should be used through vias or a short path. The VDD connecting the Resistance 10Ω to VIN to form a filter circuit.

4.The 5V LDO Output and Gate Drive Supply Voltage Input capacitor 1uF must be placed closest to the VDRV/VREG pin.

5.AGND and PGND (power ground) should be connected together at a single point. Connect exposed pad of AGND to power ground copper area with copper and vias.

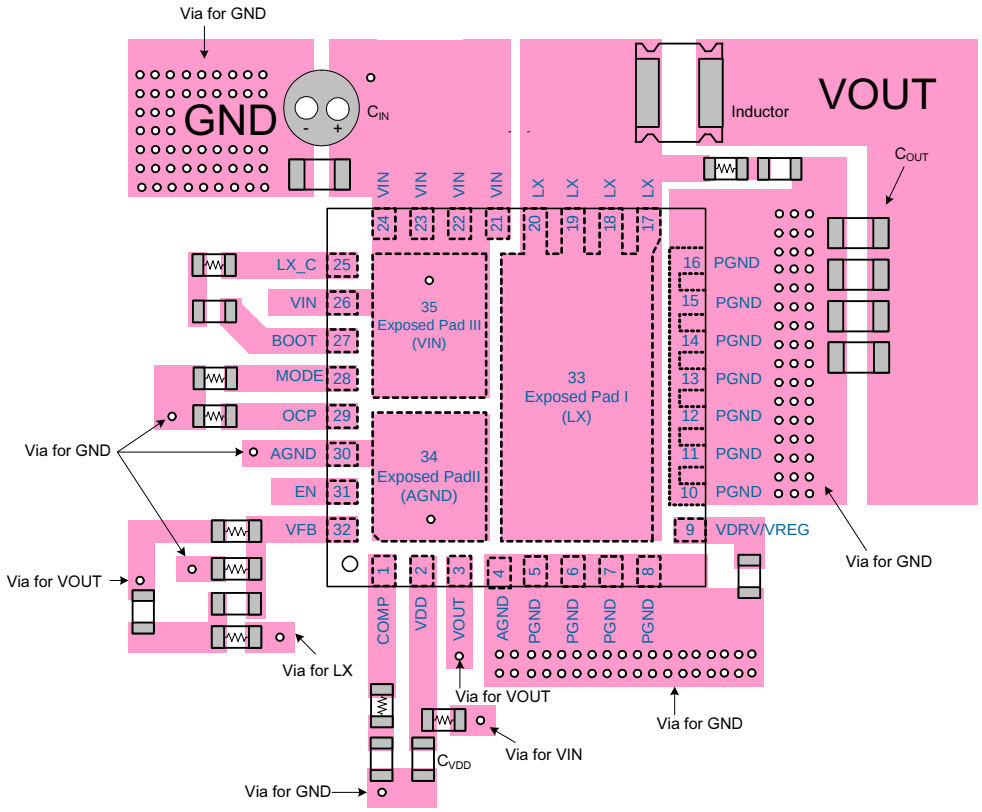
6.The 4-layered PCB layout can increase heat dissipation area by taking advantage of the middle layers of the GND plane. This may also lower the temperature of IC and its peripheral components of the demo board such as inductor.

7.Apply copper plane to Exposed Pad AGND for best heat dissipation and noise immunity. The exposed pad is the main path for heat convection and should be well-soldered to the PCB for best thermal performance.

8.Use a short trace connecting the bootstrap capacitor CBOOT to BOOT and LX_C to form a bootstrap circuit.

9.Use a short trace connecting R-C to LX and PGND Plane to form a Snubber Circuit to eliminate the high frequency voltage spike at LX node.

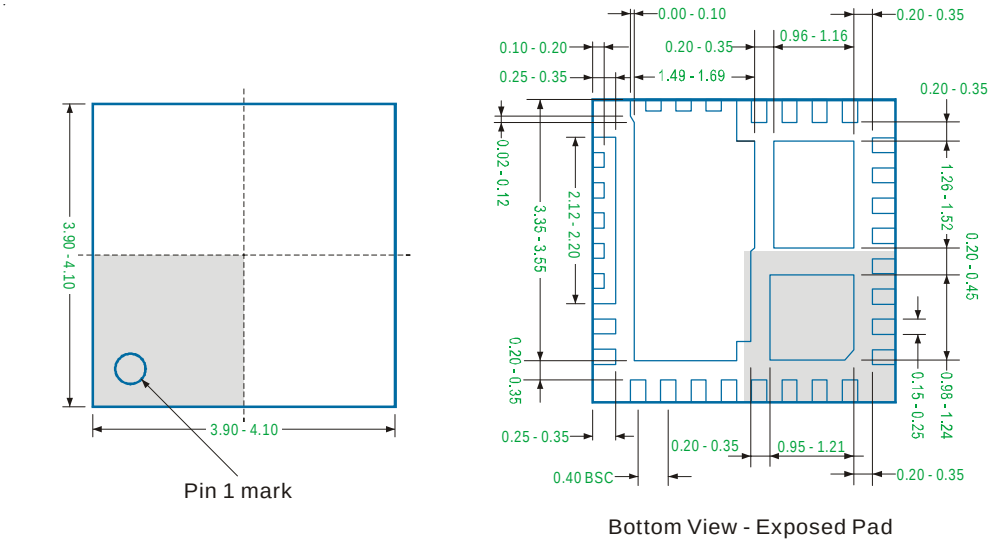
10.The LX pad is the noise node switching from VIN to GND. LX node copper area should be minimized and wide to reduce EMI and should be isolated from the rest of circuit for good EMI and low noise operation.



Layout Reference of WQFN4x4-32L

Package Information

WQFN4x4 - 32L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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