

3A Non-Synchronous Buck Regulator

General Description

The uP9622 is a high efficiency buck regulator with integrated high side NMOS switch. It operates from a 4.5V to 27V input voltage range and supplies up to 3A of load current. The output voltage is adjustable down to 0.8V by a voltage divider. Other features include internal soft-start, chip enable, over-voltage, under-voltage, over-temperature and over-current protections. The uP9622 is available in a space-saving SOP-8L package.

Ordering Information

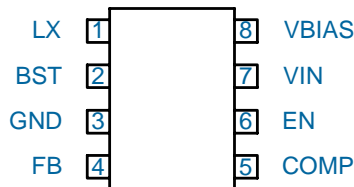
Order Number	Package Type	Top Marking
uP9622PSA8	SOP-8L	uP9622P

Note:

(1) Please check the sample/production availability with uPI representatives.

(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



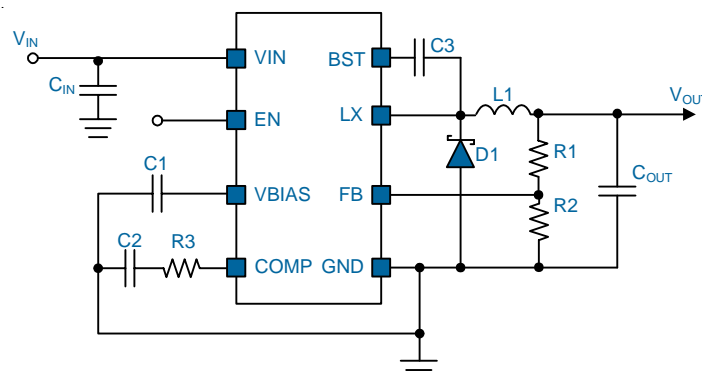
Features

- 4.5V to 27V Input Voltage Range
- 70mΩ Internal High Side NMOS, Efficiency: Up to 95%
- Internal Soft Start
- Output Voltage Adjustable down to 0.8V
- 3A Continuous Output Current
- Fixed 370kHz PWM Operation
- Cycle-by-Cycle Current Limit
- Short Circuit Protection
- Thermal Shutdown
- Small Size SOP-8L Package
- RoHS Compliant and Halogen Free

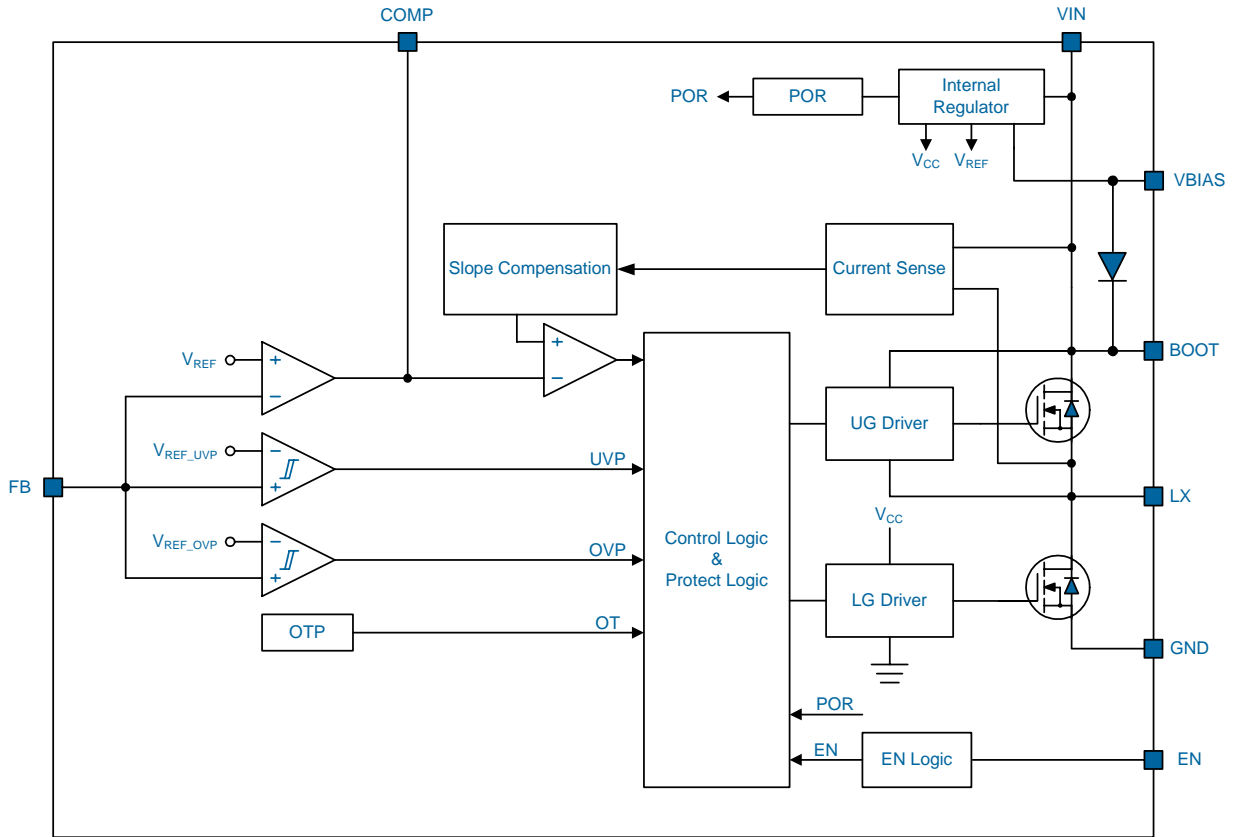
Applications

- Point of Load DC/DC Conversion
- TV Set Top Box
- DVD Driver and HDD
- LCD Monitors and TVs
- Cable Modems
- Telecom/Networking/Datacom Equipment

Typical Application Circuit



Functional Block Diagram



VIN	VOUT	L1	C _{IN}	C _{OUT}	C2	R1	R2	R3
9V	4.98V	6.8uH	150uF	1*22uF+1*220uF	1800pF	52.3kΩ	10kΩ	8.45kΩ
24V	3.3V	6.8uH	2*10uF+1*330uF	2*22uF+1*100uF	1800pF	59kΩ	18.7kΩ	8.45kΩ
24V	4.24V	6.8uH	2*10uF	2*22uF	1800pF	43kΩ	10kΩ	8.45kΩ
24V	5V	6.8uH	2*10uF	2*22uF	1800pF	52.5kΩ	10kΩ	8.45kΩ

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	LX	PWM Output Connection to Inductor. LX pin needs to be connected externally (thermal connection for output stage).
2	BST	Bootstrap Voltage Input. High side NMOS driver supply. Connected to 0.1uF capacitor between BST and LX.
3	GND	Ground.
4	FB	Feedback Input. This It is regulated to 0.8V. The FB pin is used to determine the PWM output voltage via a resistor divider between the ouput and GND.
5	COMP	External Loop Compensation. Output of internal error amplifier. Connect a series RC network to GND for control loop compensation.
6	EN	Enable Pin. The enable pin is active HIGH. Connect EN pin to VIN if not used. DO NOT leave the EN pin floating.
7	VIN	Supply Voltage Input. Range from 4.5V to 27V. When VIN rises above the UVLO threshold the device starts up. All VIN pins need to be connected externally.
8	VBIAS	Compensation Pin of Internal Linear Regulator. Place a 1uF capacitor between this pin and GND.

Functional Description

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Chip Enable/Disable and Soft-Start

The uP9622 features an EN pin for enable/disable control of the output voltage. Pulling the EN pin lower than 0.6V shuts down the uP9622 and reduces its shutdown current lower than 3uA. Pulling EN pin higher than 2.5V enables the uP9622. In the soft start process, the output voltage is typically ramped to regulation voltage in 4.6ms. The 4.6ms soft start time is set internally.

Operation

The uP9622 integrates an internal NMOS as the high side NMOS switch. Since the NMOS requires a gate voltage higher than the input voltage, a boost capacitor connected between the LX and BST pins drives the gate.

The uP9622 adopts slope-compensated, current mode PWM control. During normal operation, the uP9622 operates at PWM mode to regulate output voltage by transferring the power to the output voltage cycle by cycle at a constant frequency. The uP9622 turns on the high side switch at each rising edge of the internal oscillator allowing the inductor current to ramp up linearly. The switch remains on until either the current limit is tripped or the PWM comparator turns off the switch for regulating output voltage.

The D1 turns on with optimal dead time and picks up the inductor current after the high side switch turns off allowing the inductor current to ramp down linearly. The D1 remains on until the next rising edge of oscillator turns on the high side switch. The uP9622 regulates the output voltage by controlling the ramp up/down duty cycle of inductor current. The high frequency switching ripple is easily smoothed by the output filter.

The high side switch current is sensed, slope compensated and compared with the error amplifier output COMP to determine the adequate duty cycle. The feedback voltage VFB is sensed through a resistive voltage divider and regulated to internal 0.8V reference voltage. The error amplifier amplifies and compensates voltage variation to get appropriate COMP pin voltage. When the load current increases, it causes a slight decrease in the feedback voltage relative to the 0.8V reference, which in turn, causes the error amplifier output voltage to increase until the average inductor current matches the new load current.

Output Voltage Setting and Feedback Network

The output voltage can be set by feeding back the output to the FB pin with a resistor divider network as:

$$V_{OUT} = \frac{R1 + R2}{R1} \times V_{REF}$$

The internal VREF is 0.8V with 2.25% accuracy.

Over Current Protection (OCP)

The uP9622 employs peak current mode control and continuously monitors the inductor peak current for current limit by sensing the voltage drop across the high side NMOS switch when it turns on. When the inductor peak current is sensed to reach the current limit threshold (6A typical) for 9 consecutive switching cycles, the internal protection circuit is triggered and switching frequency reduced to 1/16 of normal frequency.

Output Over Voltage Protection (OVP)

Output over voltage protection (OVP) is triggered if the FB voltage is higher than 1.02V. The OVP is a non-latch type protection. Once OVP is triggered, the uP9622 turn off high side NMOS switch. When the OVP condition resolved, the uP9622 will turn on high side NMOS switch and resume the normal state automatically.

Under Voltage Protection (UVP)

The uP9622 provides UVP protection function. Once the output short-circuits, the UVP be triggered and then always hiccup, the hiccup cycle time is set by an internal counter. When the UVP condition is removed or disappears, the uP9622 will resume normal operation and the hiccup status will terminate.

Over Temperature Protection (OTP)

The OTP is triggered and shuts down the uP9622 if the junction temperature is higher than (150°C typical). The OTP is a non-latch type protection. The uP9622 automatically initiates another soft start cycle if the junction temperature drops below (100°C typical).

Absolute Maximum Rating

(Note 1)

Supply Voltage Range between VIN and GND	30V
LX to GND Voltage Range	-0.7V to VIN+0.3V
EN to GND Voltage Range	-0.3V to VIN+0.3V
FB to GND Voltage Range	-0.3V to 6V
COMP to GND Voltage Range	-0.3V to 6V
VBIAS to GND Voltage Range	-0.3V to 6V
BST to GND Voltage Range	VLX to 6V
Storage Temperature Range (T _s)	-65°C to +150°C
Junction Temperature (T _j)	150°C
Lead Temperature (Soldering, 10 sec)	260°C
ESD Rating (Note 2)	
HBM (Human Body Mode)	2kV
CDM (Charged Device Mode)	1kV

Thermal Information

Package Thermal Resistance (Note 3)

SOP-8L θ _{JA}	160°C/W
SOP-8L θ _{JC}	39°C/W
Power Dissipation, P _D @ T _A = 25°C	
SOP-8L	0.63W

Recommended Operation Conditions

(Note 4)

Supply Input Voltage, V _{IN}	4.5V to +27V
Operating Junction Temperature Range	-40°C to +125°C
Operating Ambient Temperature Range	-40°C to +85°C

Note 1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

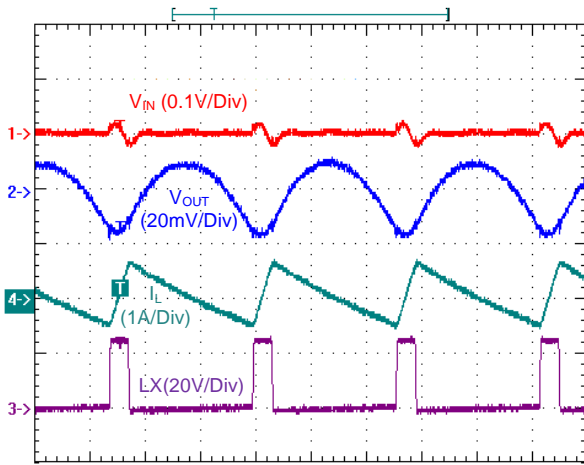
Electrical Characteristics

($V_{IN} = V_{EN} = 12V$, $V_{OUT} = 3.3V$, $T_A = 25^\circ C$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Voltage	V_{IN}		4.5	--	27	V
Input Under Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising	--	4.3	--	V
		V_{IN} falling	--	4.1	--	
Supply Current (Quiescent)	I_{IN}	$I_{OUT} = 0A$, $V_{FB} = 1.2V$, $V_{EN} > 2V$	--	2	3	mA
Shutdown Supply Current	I_{OFF}	$V_{EN} = 0V$	--	3	20	uA
Feedback Voltage	V_{FB}		0.782	0.8	0.818	V
Load Regulation			--	0.5	--	%
Line Regulation			--	0.08	--	%/V
Feedback Voltage Input Current	I_{FB}		--	--	200	nA
Enable						
EN Input Threshold	V_{EN}	Off threshold	--	--	0.6	V
		On threshold	2.5	--	--	
EN Input Hysteresis	V_{HYS}		--	200	--	mV
Enable Sink/Source Current	I_{EN}		--	--	50	nA
Modulator						
Frequency	f_O		315	370	425	kHz
Maximum Duty Cycle	D_{MAX}		85	--	--	%
Minimum Duty Cycle	D_{MIN}		--	--	6	%
Error Amplifier Voltage Gain	G_{VEA}		--	1000	--	V/V
Error Amplifier Transconductance	G_{EA}		--	256	--	uA/V
Protection						
Current Limit	I_{LM}		5	--	7	A
Over Temperature Shutdown Limit		T_J rising	--	150	--	$^\circ C$
		T_J falling	--	100	--	$^\circ C$
Short Circuit Hiccup Time	t_{SC}	$V_{FB} = 0V$	--	0.7	--	s
Soft Start Interval	t_{SS}		--	4.6	--	ms
PWM Output Stage						
High Side NMOS Switch On Resistance	$R_{DS(ON)}$		--	70	100	m Ω
High Side NMOS Switch Leakage		$V_{EN} = 0V$, $V_{LX} = 0V$	--	--	10	uA

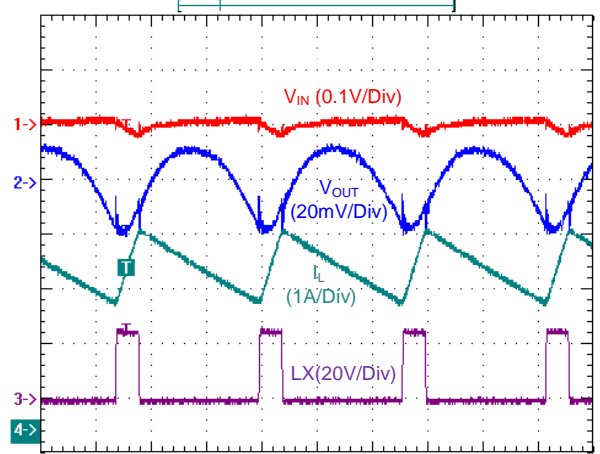
Typical Operation Characteristics

Light Load Operation



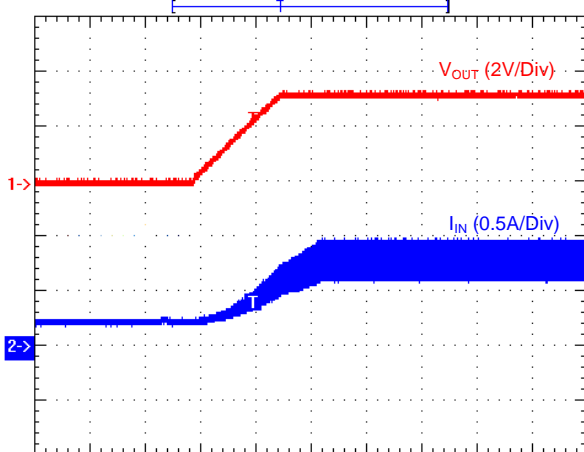
Time : 1us/Div
 $T_A = 25^\circ\text{C}, V_{IN} = V_{EN} = 24\text{V}, V_{OUT} = 3,3\text{V}$

Full Load Operation



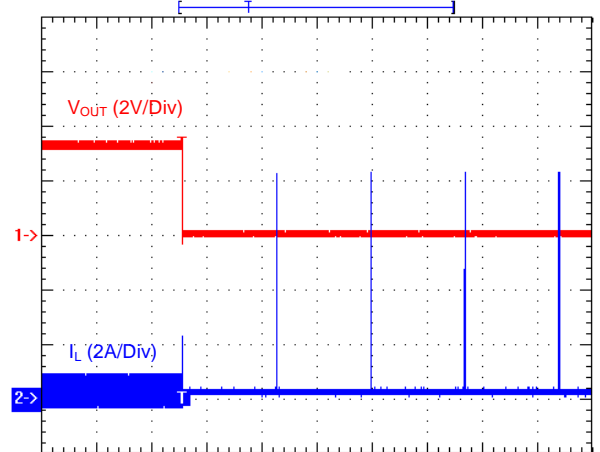
Time : 1us/Div
 $T_A = 25^\circ\text{C}, V_{IN} = V_{EN} = 24\text{V}, V_{OUT} = 3,3\text{V}$

Start-up to Full Load



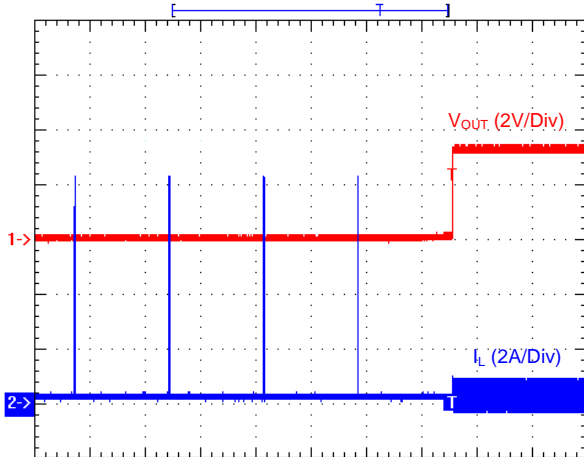
Time : 2ms/Div
 $T_A = 25^\circ\text{C}, V_{IN} = V_{EN} = 24\text{V}, V_{OUT} = 3,3\text{V}$

Short Circuit Protection



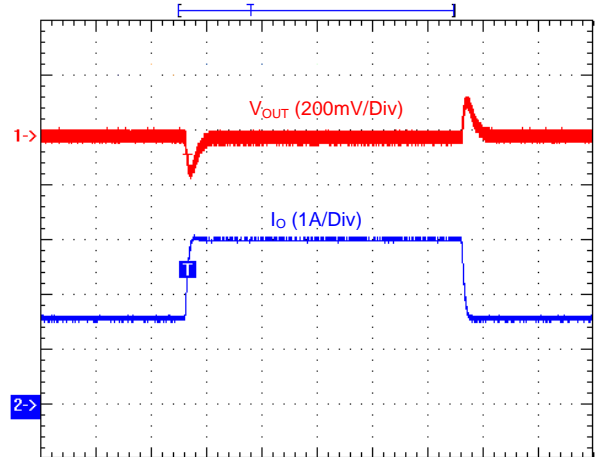
Time : 400ms/Div
 $T_A = 25^\circ\text{C}, V_{IN} = V_{EN} = 24\text{V}, V_{OUT} = 3,3\text{V}$

Short Circuit Recovery



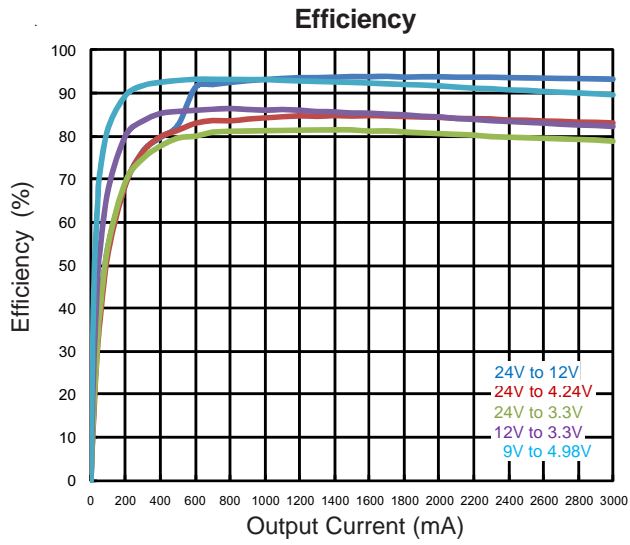
Time : 400ms/Div
 $T_A = 25^\circ\text{C}, V_{IN} = V_{EN} = 24\text{V}, V_{OUT} = 3,3\text{V}$

50% to 100% Load Transient

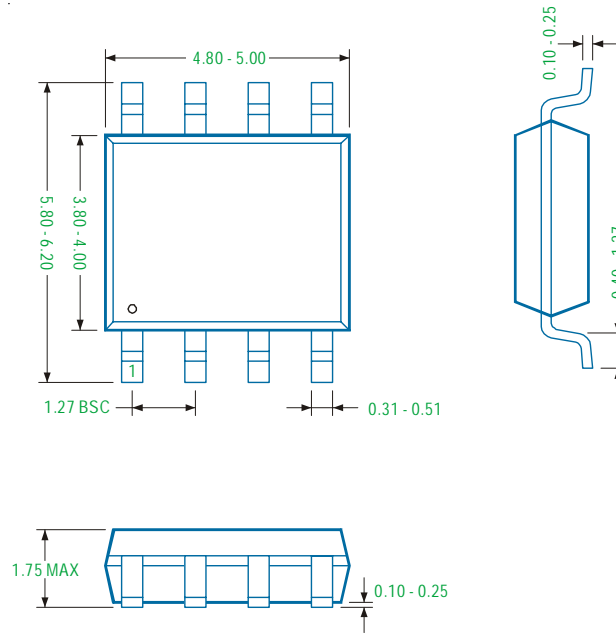


Time : 200us/Div
 $T_A = 25^\circ\text{C}, V_{IN} = V_{EN} = 24\text{V}, V_{OUT} = 3,3\text{V}$

Typical Operation Characteristics



SOP-8L Package



Note

1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

TYP: Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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