6A Dual-Channel, Wide Input Range CC/CV Synchronous Rectified Buck Converter

General Description

The uP9626P is a high-efficiency synchronous-rectified buck converter with internal power switch. With internal low RDS(ON) switches, the high-efficiency buck converter is capable of delivering up to 6.0A output current for charger interface and a wide input voltage range from 4.75V to 36V.That operates in either CV (Constant Output Voltage) mode or CC (Constant Output Current) mode, function provides a current limitation function. The output voltage ranges from 3V to 21V for portable charger devices application.

Other features for the buck converter include internal soft-start, adjust operating frequency from 100kHz to 500kHz, adjust output CC(Constant Current) current limit, adjust input current limit setting, adjust output total current limit for dual channel application ,chip enable, built in fixed and adjustable line-compensation, short circuit protection, over voltage, and over temperature protections. It is available in a space WQFN4x4-24L package.

Ordering Information

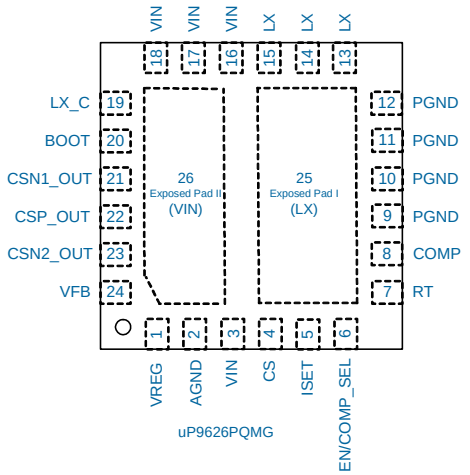
Order Number	Package Type	Top Marking
uP9626PQMG	WQFN4X4-24L	uP9626P

Note:

(1) Please check the sample/production availability with uPI representatives.

(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



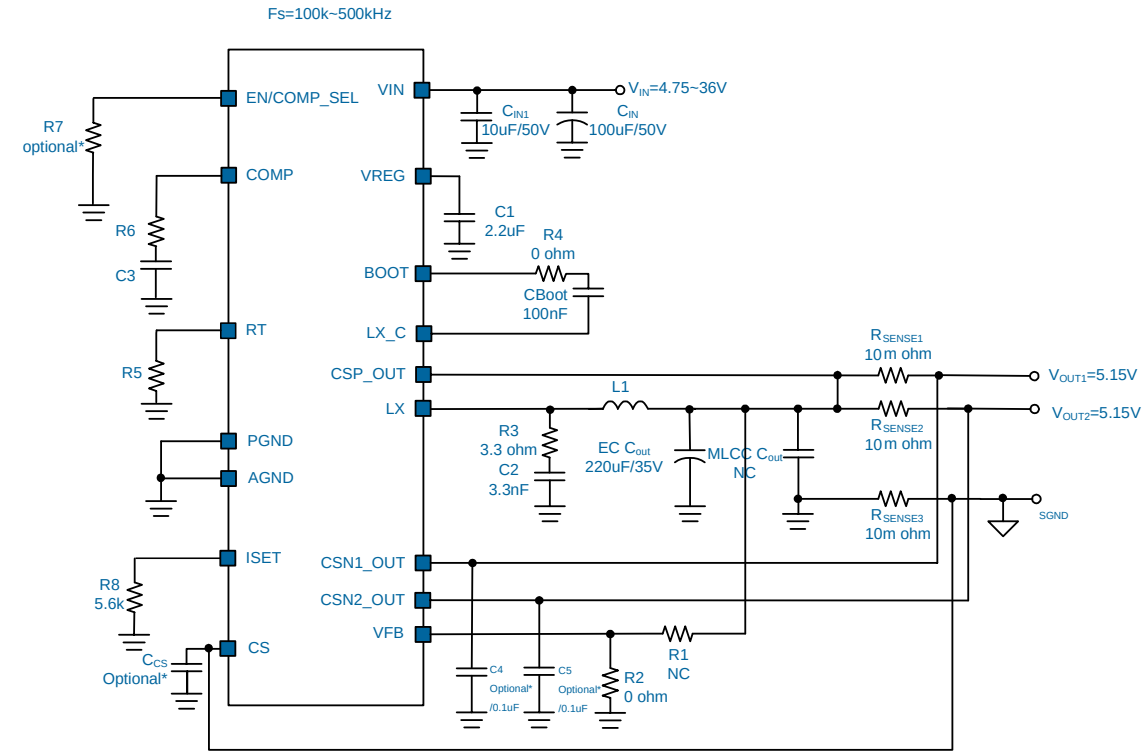
Features

- 4.75 to 36V Wide Input Voltage Range
- Up to 6.0A Output Current
- CV/CC Mode Control (Constant Voltage and Constant Current)
- Adjust Output Total Current Limit for Dual Channel Application
- Adjust Input Current Limit Setting
- Output Voltage Range: 3V to 21V
- Default Output Voltage Accuracy: ± 1.5%
- Built-In Internal V_{REF} = 1.03V Accuracy: ± 1%
- Frequency Adjustable: 100kHz to 500kHz
  - 0~6A Single/Dual-Channel Application at Fs = 100kHz
  - 0~3A Single-Channel Application at Fs = 200kHz ~ 500kHz
- Up to 98% Conversion Efficiency
- Internal Soft Start Time:
  20ms at F_S=100kHz, 4ms at F_S=500kHz
- Adjustable Line-Compensation
- Adjustable External Constant Current Setting
- Constant Current Limit Accuracy with R_{SENSE}: ± 10%
- Output Under Voltage and Short Circuit Protection
- Input and Output Over Voltage Protection
- Over Temperature Protection
- WQFN4x4-24L Package
- RoHS Compliant and Halogen Free

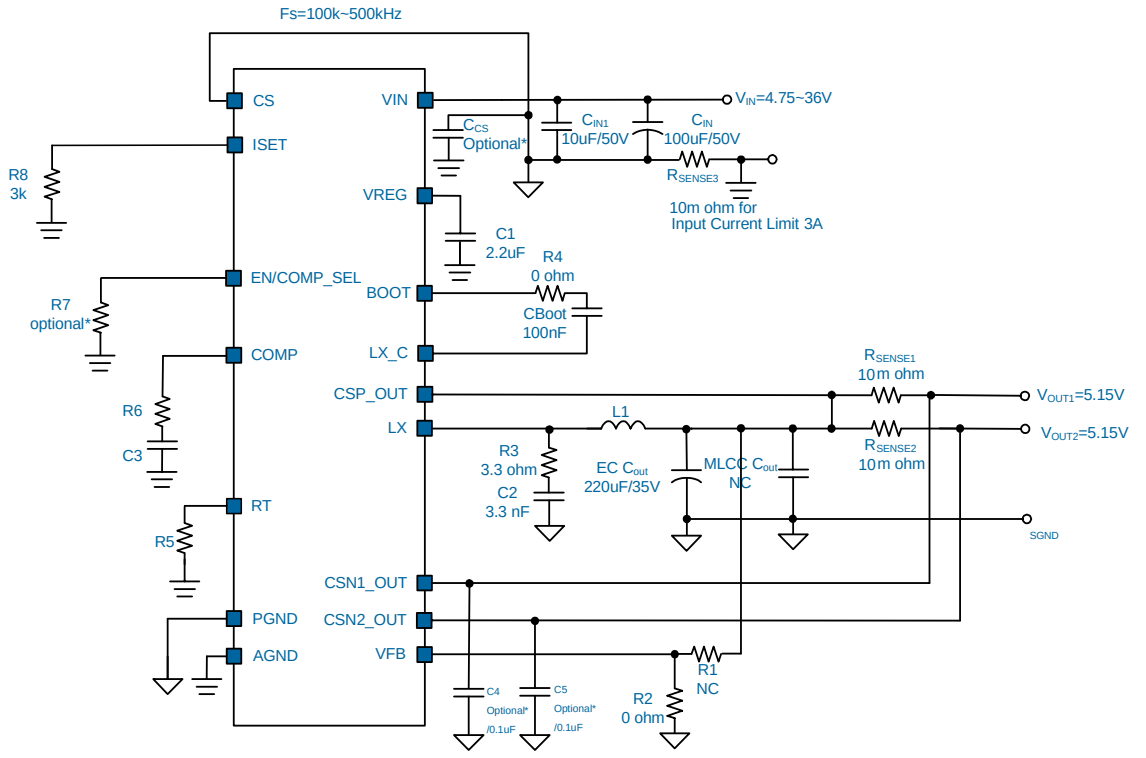
Applications

- PDA Like Device Car Charger
- Portable Charging Devices
- Wall Adaptors

Typical Application Circuit



uP9626P Application Circuit for Output Total Current Limit

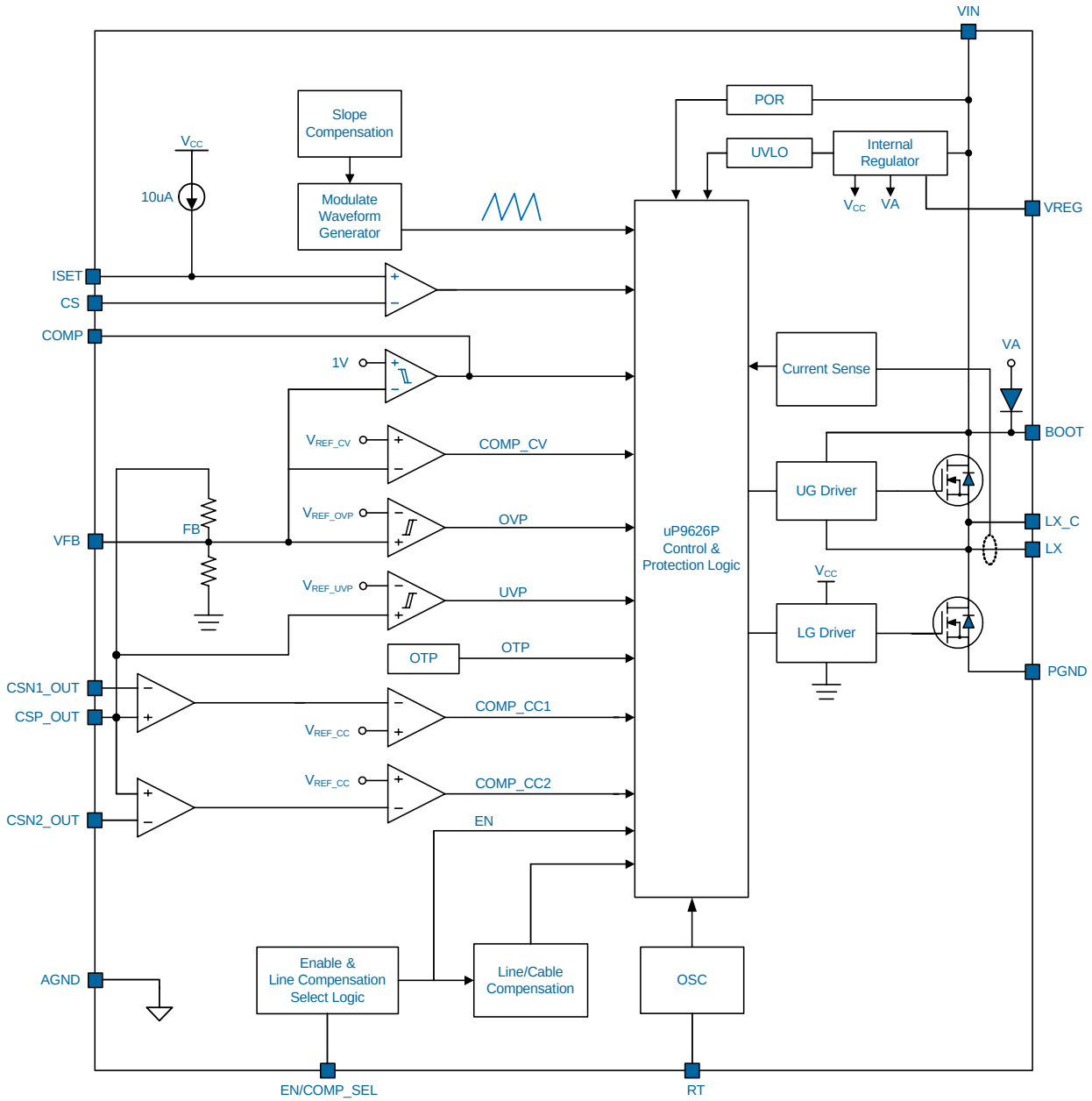


uP9626P Application Circuit for Input Current Limit

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VREG	**5.1V LDO Output and Gate Drive Supply Voltage Input.**
2	AGND	**Signal Ground.**
3,16~18	VIN	**Power Supply Input.** Input voltage that supplies current to the output voltage and powers the internal control circuit. Bypass the input voltage with a minimum 10uFx2 X5R or X7R ceramic capacitor.
4	CS	**The Current Sense Input Pin.** A external sense resistor for detect output total current limit at dual channel application and input current limit application.
5	ISET	**Output total current limit and input current limit setting pin.** Connect a resistor from this pin to GND to set output total current limit and input current limit.
6	EN/COMP_SEL	**Car Charger Enable (Active High) and Adjustable Cable Compensation.** Connect a resistor from 43kΩ ~360kΩ between EN/COMP_SEL and GND pins to select USB cable compensation for prevent output voltage drop in the output cable. Pull the EN/COMP_SEL pin<14kΩ to GND disables the car charger, the EN/COMP_SEL pin internal pull high to enable the car charger.
7	RT	**Switching Frequency Programming.** Connect a resistor from this pin to GND to set the switching frequency.
8	COMP	**Compensation.** This pin is output of the error amplifier. The current comparator threshold increases with this control voltage. Connect an RC network to ground for control loop compensation.
9-12	PGND	**Power Ground.**
13-15	LX	**Internal Switches Output.** Connect this pin to the output inductor.
19	LX_C	**Internal Switches Output.** Connect the bootstrap capacitor CBOOT to BOOT pin.
20	BOOT	**Bootstrap Supply for the Floating Upper Gate Driver.** Connect the bootstrap capacitor C_{BOOT} between BOOT pin and the LX pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Typical value for CBOOT is 0.1uF or greater. Ensure that C_{BOOT} is placed near the IC.
21	CSN1_OUT	**The Current Sense Input (-) HV Pin.**
22	CSP_OUT	**The Current Sense Input (+) HV Pin.**
23	CSN2_OUT	**The Current Sense Input (-) HV Pin.**
24	VFB	**Feedback Input.** This pin is the inverting input to the error amplifier. A resistor divider from output to GND is used to set regulator voltage.When VFB is shorted to GND, the default VOUT is 5.15V.
25	LX_Exposed Pad I	**Switch Node.** This pin is used as the sink for the upper MOSFET gate driver. This pin is also monitored by the shoot through protection circuitry to determine when the upper MOSFET has turned off. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET.
26	VIN_Exposed Pad II	**Power Supply Input.** Input voltage that supplies current to the output voltage.

Functional Block Diagram



uP9626P

Functional Description

CV/CC Mode Control

The uP9626P provides CV/CC function. That operates in either CV (Constant Output Voltage) mode or CC (Constant Output Current) mode, function provides a current limitation function and adjust CC (Constant Output Current) limit setting(Default=3A).In the CV mode, the output voltage is controlled within ±1%. In the CC mode, the output current variation is less than ±10% of the nominal value which can be set up to 5A by the current sensing resistor.

When Output current increase until it reaches the CC limit set by the RSENSE resistor. At this point, the device will transition from regulating output voltage to regulating output current, and the output voltage will drop with increasing load.

The CC (Constant Output Current) limit is set at 3A by default with an external resistance RSENSE1/2 =10mΩ, When the (CSN_OUT) - (CSP_OUT) voltage gets higher than 30mV and reaches the current limit, the driver is turned off. The CC (Constant Output Current) limit is set according to the following equation:

CC (Constant Output Current) Limit=30mV /$R_{SENSE1/2}$

Output Total Current Limit and Input Current Limit Setting

Adjust output total current limit for dual channel application, The output total current limit is set at 5.6A by default with an external resistance R_{SENSE3} = 10mΩ, When the (CS) - (PGND) voltage gets higher than 56mV(default) and reaches the current limit, the driver is turned off. Use an external resistance RISET can adjust difference Voltage between CS and PGND at Current Limit Mode Operation. The output total current limit is set according to the following equation:

When R_{ISET} = 5.6kΩ,

Output total current limit = 56mV /R_{SENSE3}

Input current limit for AC/DC application, The input current limit is setting at 3A by default with an external resistance RSENSE3 =10mΩ, When the (CS) - (Input GND) voltage gets higher than 30mV(default) and reaches the current limit, the driver is turned off. Use an external resistance R_{ISET} can adjust difference Voltage between CS and Input GND at Current Limit Mode Operation. The input current limit is set according to the following equation:

When R_{ISET} = 3kΩ,

Input current limit =30mV /R_{SENSE3}

USB Cable Resistance Compensation Select

This pin floating (Signal H) or connect a $R_{EN/COMP\_SEL}$ resistor < 360kΩ between EN/COMP_SEL and GND pins (Signal L) to select USB cable compensation for preventing output voltage drop in the output cable, as shown in Figure 1 and Table 1.

Enable Control and Output Cable Resistance Compensation

The uP9626P pull the EN/COMP_SEL pin<14kΩ to GND disables the car charger, the EN/COMP_SEL pin internal pull high to enable the car charger. Connect a resistor between EN/COMP_SEL and GND pins to adjust USB cable compensation for preventing output voltage drop in the output cable.

In charger applications, the large load will cause voltage drop in the output cable. The uP9626P has a built-in cable compensation function. When the load increases, the cable compensator will increase a adjustable regulation of the error amplifier that can make the output voltage constant. Use the curve and table to adjust the internal reference voltage values for fixed USB and adjustable cable compensation by the external resistance R_{SENSE1} and R_{SENSE3}=10mΩ (default) , as shown in Figure 1 and Table 1. The R_{COMP} is the internal equivalent resistor.

The fixed and adjustable cable compensation is calculated as follows:

R_{SENSE1} and R_{SENSE3} = 10mΩ for USB Cable Resistance Compensation Application Table				
$R_{EN/COMP\_SEL}$ (kΩ)	43±10%	360±10% or Floating (default)	180±10%	91±10%
R_{COMP} (mΩ)	0 (disable)	40 (default)	60	80
I_{LOAD} (mA)	USB Cable Compensation Voltage (mV)			
0	0	0	0	0
500	0	0	0	0
1000	0	40	60	80
1500	0	60	90	120
2000	0	80	120	160
2500	0	100	150	200
3000	0	120	180	240

Table 1. USB Cable Resistance Compensation Application Table

Functional Description

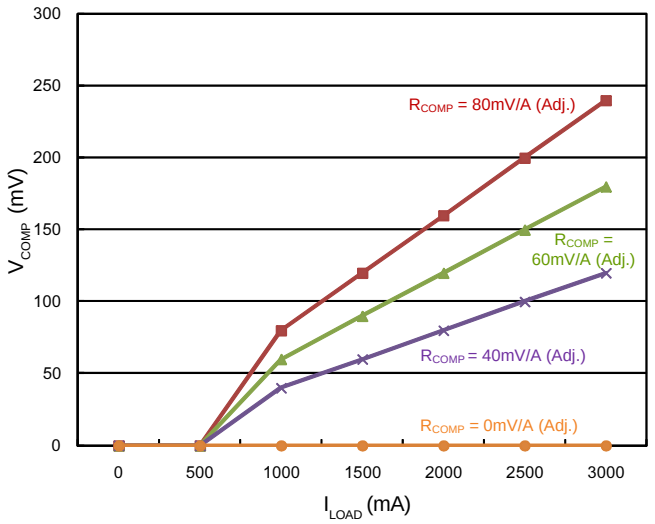


Figure 1. USB Compensation at Various Resistor Divider Values

Switching Frequency Programming

Connection a resistor from this pin to GND to set the switching frequency from 100kHz to 500kHz. When R_{RT} is left open, the switching frequency is 100kHz. Figure 2 shows the switching frequency vs. R_{RT}.

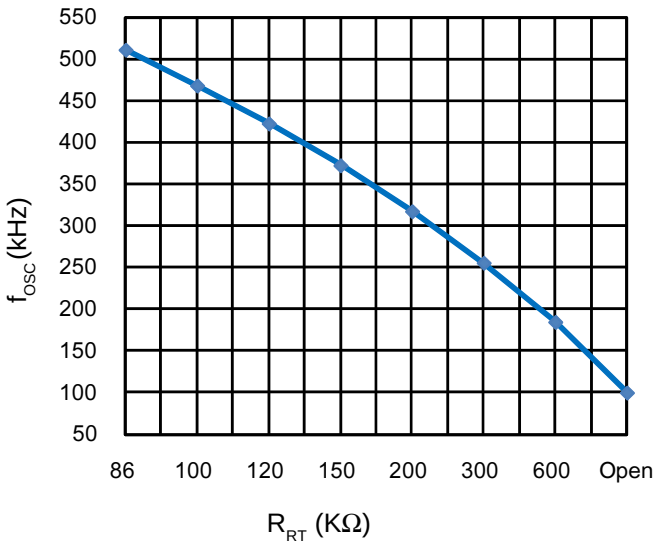


Figure 2. R_{RT} vs. f_{OSC}

Current Limit Protection

The uP9626P continuously monitors the inductor current, when the inductor current is higher than current limit

threshold 10A(typ.), the current limit function activates and forces the upper switch turning off to limit inductor current cycle by cycle.

Output Short Circuit Protection

The uP9626P provides output short circuit protection function. Once the output loader short-circuits or the output voltage becomes lower than 2.7V, the SCP will be triggered then always hiccup. The hiccup cycle time is set by an internal counter. When the SCP condition disappears, the converter will resume normal operation and the hiccup status will terminate.

Output Over Voltage Protection

The uP9626P monitors FB voltage to detect over voltage. When the FB voltage becomes higher than 110% of the target voltage, the OVP will be triggered, the power MOS will turn off and allow low side MOS to turn on to charge bootstrap capacitor. When the OVP condition is disappeared, the converter will resume normal operation and recover to normal state.

Input Over Voltage Protection

The uP9626P monitors VIN voltage to detect input over voltage protection.When the VIN voltage becomes higher than the target voltage, the VIN OVP will be triggered, the power MOS will turn off and allow low side MOS turn on to charge bootstrap capacitor until output voltage under the collapse threshold 2.7V. When the VIN OVP condition is disappeared, the converter will recover to normal state and restart the soft start sequence.

Over Temperature Protection

The OTP is triggered and shuts down the uP9626P if the junction temperature is higher than 130°C. The OTP is a non-latch type protection. The uP9626P automatically nitiates another soft start cycle if the junction temperature drops below 110°C.

Output Voltage Setting and Feedback Network

The output voltage can be set from V_{REF} to V_{IN} by a voltage divider. The output voltage can be set as follows,

$$V_{OUT} = \left(\frac{R1+R2}{R2}\right) \times V_{REF} .$$

R2 must be higher than 10kΩ.

The internal V_{REF} is 1.03V with 1.0% accuracy in real apploications, when control loop compensation connects to an RC entwork to ground at COMP pin for better transient response.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, V_{IN} ---------- -0.3V to +40V
LX/LX_C Voltage to GND ---------- -0.3V to (V_{IN}+ 0.3V)
BOOT to LX Voltage ---------- -0.3V to +6V
CSN1/CSN2_OUT/CSP_OUT Pin Voltage ---------- -0.3V to +24V
CS Pin Voltage ---------- -0.3V to +6V
EN/COMP_SEL Voltage ---------- -0.3V to +6V
Other Pin Voltage ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
CDM (Charged Device Mode) ---------- 500V

Thermal Information

Package Thermal Resistance (Note 3)
WQFN4x4-24L $\theta_{JA, controller}$ ---------- 54°C/W
WQFN4x4-24L $\theta_{JA, HS}$ ---------- 42°C/W
WQFN4x4-24L $\theta_{JA, LS}$ ---------- 38°C/W
WQFN4x4-24L $\theta_{JC, controller}$ ---------- 21°C/W
WQFN4x4-24L $\theta_{JC, HS}$ ---------- 10°C/W
WQFN4x4-24L $\theta_{JC, LS}$ ---------- 6°C/W
Power Dissipation, P_D @ T_A = 25°C
WQFN4x4-24L $P_{D, controller}$ ---------- 1.85W
WQFN4x4-24L $P_{D, HS}$ ---------- 2.38W
WQFN4x4-24L $P_{D, LS}$ ---------- 2.63W

Recommended Operation Conditions

(Note 4)

Supply Input Voltage, V_{IN} ---------- +4.75V to +36V
Output Voltage, V_{OUT} ---------- +3V to +21V
Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{IN} = 12V, T_A=25°C, unless otherwise specified)

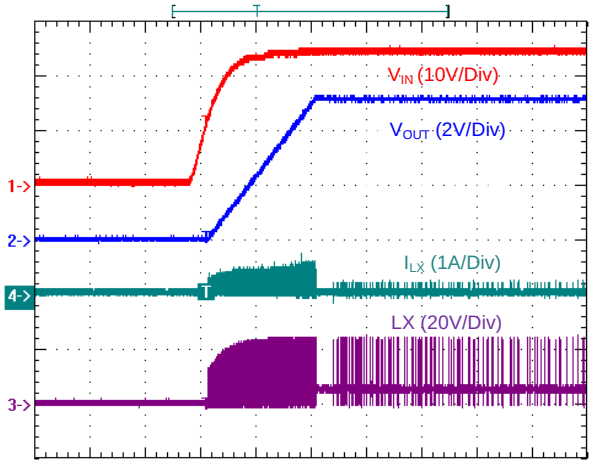
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input Voltage						
Input Voltage Range	V_{IN}		4.75	--	36	V
VIN POR Threshold		V_{IN} rising	--	4.6	--	V
		V_{IN} falling	--	4.3	--	
Input OVP Threshold	V_{IN_OVP}	V_{IN_OVP} rising	37.5	--	--	V
		V_{IN_OVP} falling	37	--	--	
Supply Input Current						
Input Quiescent Current	I_Q	No switching	--	--	1	mA
Input Shutdown Current	I_S	EN disable for uP9626P	--	60	--	uA
Oscillator						
Oscillation Frequency Range	Δf_{OSC}	Refer to Figure 2 R_{RT} vs. f_{OSC} curve	100	--	500	kHz
Oscillation Frequency	f_{OSC}	at RT = open	--	100	--	kHz
Maximum Duty Cycle	D_{MAX}	f_s = 100kHz, at Rt = open	96	98	--	%
Minimum On Time	t_{ON-MIN}		--	200	--	ns
Minimum Off Time	$t_{OFF-MIN}$		--	200	400	ns
Power Switches						
Hi-Side Switch On Resistance	$R_{DS(ON)}$	VCC = 5.1V	--	18	--	mΩ
Low-Side Switch On Resistance	$R_{DS(ON)}$	VCC = 5.1V	--	12	--	mΩ
Internal Reference Voltage						
Feedback Voltage	V_{FB}		1.0197	1.03	1.0403	V
Default Output Voltage	V_{OUT}	VFB short to GND, at I_{OUT} = 0A	5.073	5.15	5.227	V
Error Amplifier Transconductance	GEA		--	580	--	uA/V
VREG LDO Voltage						
LDO Output Voltage	V_{REG}		4.93	5.1	5.27	V
LDO Output Current	I_{REG}		40	--	--	mA
Soft Start						
Soft Start Time	T_{SS}	From VOUT = 0% to 100% at f_S = 100kHz	16	20	24	ms
		From VOUT = 0% to 100% at f_S = 500kHz	2	4	8	

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Enable/Cable Resistance Compensation						
EN/COMP_SEL Logic Low	$R_{EN/COMP}$	$R_{EN/COMP}$ falling	--	--	14	kΩ
EN/COMP_SEL_Current	$I_{EN/COMP}$		--	5	--	uA
Disable Line Compensation	V_{OUT}	V_{OUT}=5.15V,I_{OUT}=(2A-1A), $R_{EN/COMP\_SEL}$=43kΩ, R_{SENSE1} and R_{SENSE3}=10mΩ, measured at VOUT	--	0	--	mV/A
Adjustable Line Compensation 1	V_{OUT}	V_{OUT}=5.15V,I_{OUT}=(2A-1A), $R_{EN/COMP\_SEL}$=91kΩ, R_{SENSE1} and R_{SENSE3}=10mΩ, measured at VOUT	--	80	--	mV/A
Adjustable Line Compensation 2	V_{OUT}	V_{OUT}=5.15V,I_{OUT}=(2A-1A), $R_{EN/COMP\_SEL}$=180kΩ, R_{SENSE1} and R_{SENSE3}=10mΩ, measured at VOUT	--	60	--	mV/A
Adjustable Line Compensation 3 (default)	V_{OUT}	V_{OUT}=5.15V,I_{OUT}=(2A-1A), $R_{EN/COMP\_SEL}$=360kΩ or NC, R_{SENSE1} and R_{SENSE3}=10mΩ, measured at VOUT	--	40	--	mV/A
Current Sense Amplifier						
Voltage Difference between CSP and CSN1/CSN2 at CC Mode Operation	ΔV_{SEN}	$R_{SENSE1/2}$=10mΩ	27	30	33	mV
Voltage Difference between CS and PGND at Current Limit Mode Operation	CS	R_{SENSE3}=10mΩ, R_{ISET}=5.6kΩ	49.28	56	62.72	mV
Output Total Current Limit and Input Current Limit Setting	I_{SET}		9	10	11	uA
Protection						
CC1 (Constant Output Current) Limit	I_{OUT1}	R_{SENSE1}=10mΩ at CSN1_OUT=5.15V	2.7	3	3.3	A
CC2 (Constant Output Current) Limit	I_{OUT2}	R_{SENSE2}=10mΩ at CSN2_OUT=5.15V	2.7	3	3.3	A
CC (Constant Output Current) Limit	I_{OUT}	R_{SENSE3}=10mΩ for IOUT1+IOUT2	4.928	5.6	6.272	A
High Side Current Limit Protection	I_{LIM}		8	10	--	A
Output Voltage Needs to Collapse Threshold	CSN	Into CC(Constant Output Current) Limit, measreued at CSN1_OUT or CSN2_OUT, with respect to VOUT UVP threshold voltage	--	2.7	--	V
Reference Voltage of the Over Voltage Comparator	V_{OVP}	measrued at FB, with respect to reference voltage	105	110	115	%
Hiccup Short Circuit Protection	TH1	at f_S=100kHz	--	650	--	ms
	TH2	at f_S=500kHz	--	130	--	
Thermal Shutdown Temperature	T_{SD}	Shutdown Temperature	--	130	--	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	Hysteresis	--	20	--	°C

Typical Operation Characteristics

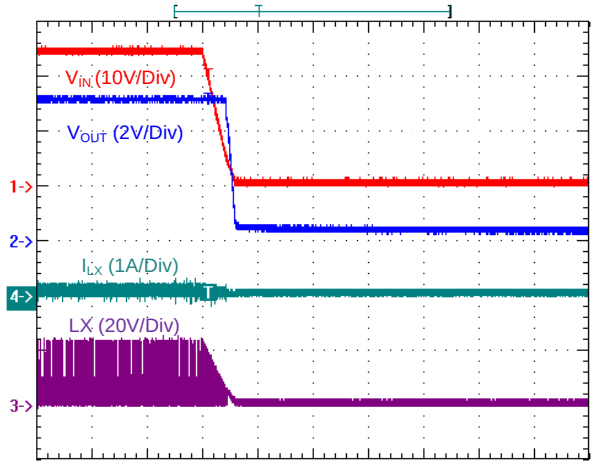
Power On Waveform



Time:10ms/Div

V_{IN} = 24V, V_{OUT} = 5.15V, I_{OUT} = 0A, Fs = 100kHz

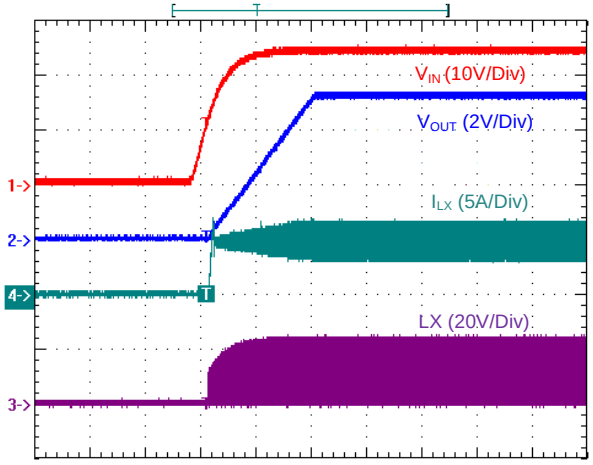
Power Off Waveform



Time:400ms/Div

V_{IN} = 24V, V_{OUT} = 5.15V, I_{OUT} = 0A, Fs = 100kHz

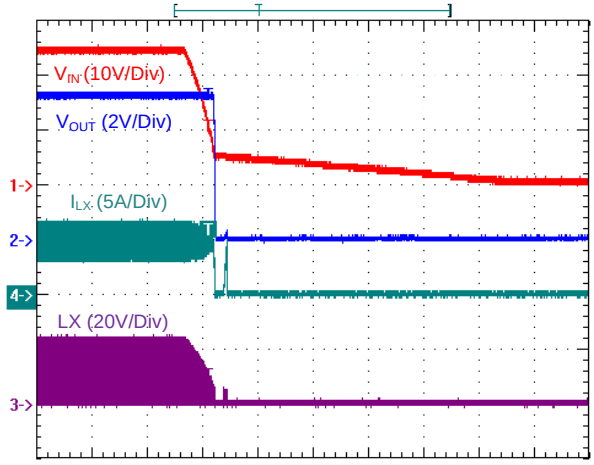
Power On Waveform



Time:10ms/Div

V_{IN} = 24V, V_{OUT} = 5.15V, I_{OUT} = 4.8A, Fs = 100kHz

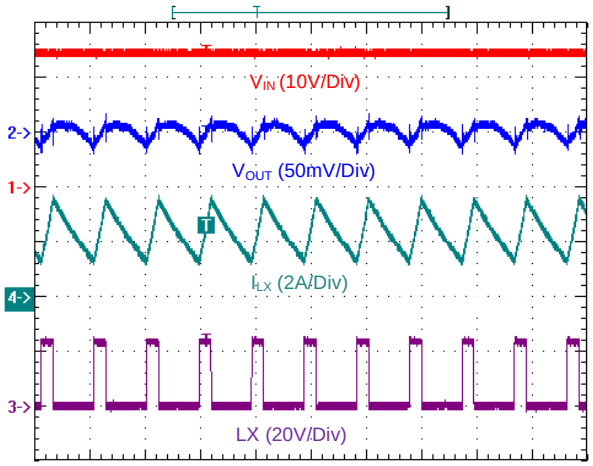
Power Off Waveform



Time:10ms/Div

V_{IN} = 24V, V_{OUT} = 5.15V, I_{OUT} = 4.8A, Fs = 100kHz

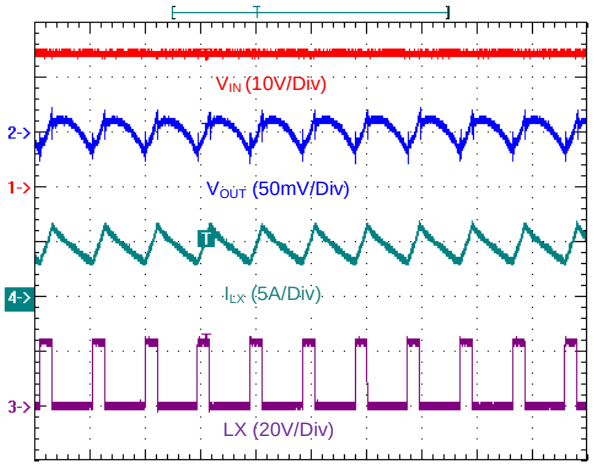
Steady State Waveform



Time:10us/Div

V_{IN} = 24V, V_{OUT} = 5.15V, I_{OUT} = 2.4A, Fs = 100kHz

Steady State Waveform

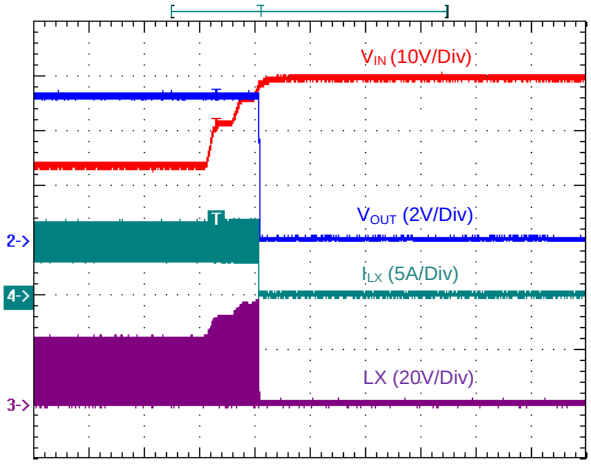


Time:10us/Div

V_{IN} = 24V, V_{OUT} = 5.15V, I_{OUT} = 4.8A, Fs = 100kHz

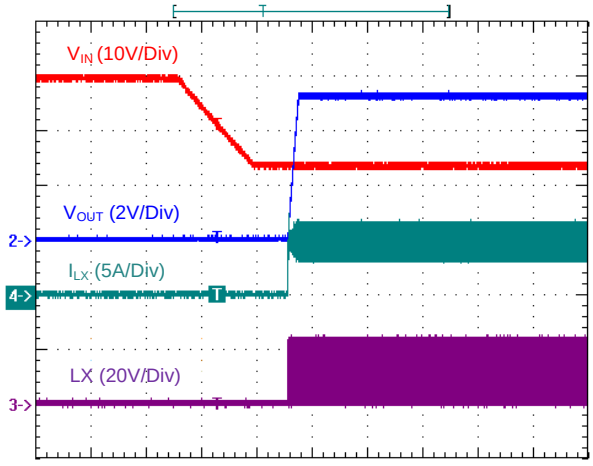
Typical Operation Characteristics

VIN Over Voltage Protection



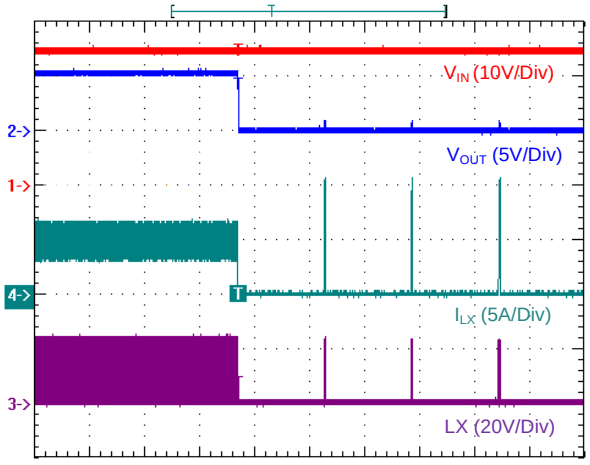
Time:20ms/Div
V_{IN} = 24V to 40V, V_{OUT} = 5.15V, I_{OUT} = 4.8A,
Fs = 100kHz

VIN Over Voltage Protection Recover



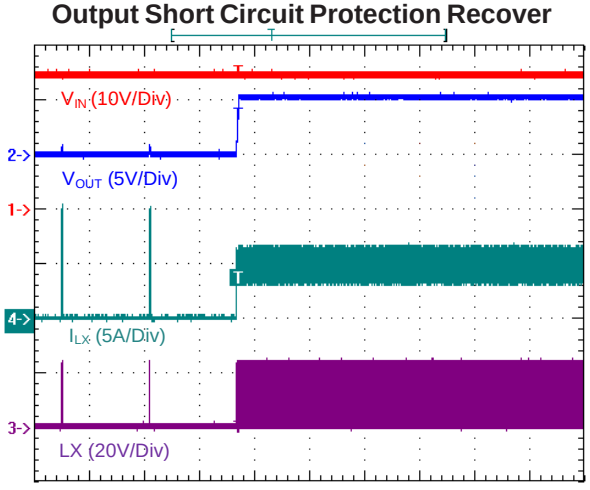
Time:100ms/Div
V_{IN} = 40V to 24V, V_{OUT} = 5.15V, I_{OUT} = 4.8A,
Fs = 100kHz

Output Short Circuit Protection



Time:400ms/Div
V_{IN} = 24V, V_{OUT} = 5.15V, I_{OUT} = 4.8A, Fs = 100kHz

Output Short Circuit Protection Recover



Time:400ms/Div
V_{IN} = 24V, V_{OUT} = 5.15V, I_{OUT} = 4.8A, Fs = 100kHz

Application Information

Output Inductor Selection

Output inductor selection is usually based the considerations of inductance, rated current value, size requirements and DC resistance (DCR). The inductance is chosen based on the desired ripple current. Large value inductors result in lower ripple currents and small value inductors result in higher ripple currents. Higher VIN or VOUT also increases the ripple current as shown in the equation below. A reasonable starting point for setting ripple current is IL = 900mA (30% of 3000mA).

$$\Delta I_L = \frac{1}{f_{OSC} \times L_{OUT}} \times V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Maximum current ratings of the inductor are generally specified in two methods: permissible DC current and saturation current. Permissible DC current is the allowable DC current that causes 40ºC temperature raise. The saturation current is the allowable current that causes 10% inductance loss. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current. If possible, choose an inductor with rated current higher than 7A so that it will not saturate even under current limit condition.

The size requirements refer to the area and height requirement for a particular design. For better efficiency, choose a low DC resistance inductor. DCR is usually inversely proportional to size.

Different core materials and shapes will change the size, current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don¡¦t radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends on the price vs. size requirements and any radiated field/EMI requirements.

Input Capacitor Selection

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 100uF. The best choice is the ceramic type and low ESR electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current.

In the case of electrolytic types, they can be further away if a small parallel 10uF ceramic capacitor is placed right close to the IC. A 100uF OSCON capacitor and 10uF ceramic capacitor are recommended and placed close to the VIN and GND pins, with the shortest traces possible.

Output Capacitor Selection

The ESR of the output capacitor determines the output ripple voltage and the initial voltage drop following a high slew rate load transient edge. The output ripple voltage can be calculated as:

$$\Delta V_{OUT} = \Delta I_C \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}}\right)$$

Where f_{OSC} = operating frequency, C_{OUT} = output capacitance and $\Delta I_C = \Delta I_L$ = ripple current in the inductor. The ceramic capacitor with low ESR value provides the low output ripple and low size profile.
The ceramic capacitor with low ESR value provides the low output ripple and low size profile.
In the case of electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current.
Connect a 220uF OSCON capacitor at output CSP terminal for good performance and low output ripple and place output capacitors as close as possible to the device.
IIn the case of ceramic output capacitors, RESR is very small and does not contribute to the output ripple at Fs=100kHz. Only if increase Fs=300kHz to 500kHz can use ceramic output capacitors to decrease output ripple.
Connect a 0.1uF optional ceramic capacitor close to IC CSN1 and CSN2 pins for best
noise immunity and good CC performance.
Connect a 4.7uF~10uF optional ceramic capacitor close to USB connector VOUT1 and VOUT2 for good CC performance.

PCB Layout Consideration

The PCB layout is an important step to maintain the high performance of the uP9626P. High switching frequencies and relatively large peak currents make the PCB layout is a very important part of all high frequency switching power supplies design. Both the high current and the fast switching nodes demand full attention to the PCB layout to save the robustness of the uP9626P through the PCB layout. Improper layout might show the symptoms of poor load or line regulation, radiate excessive noise at ground or input, output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. Follow the PCB layout guidelines for optimal performances of uP9626P.

Application Information

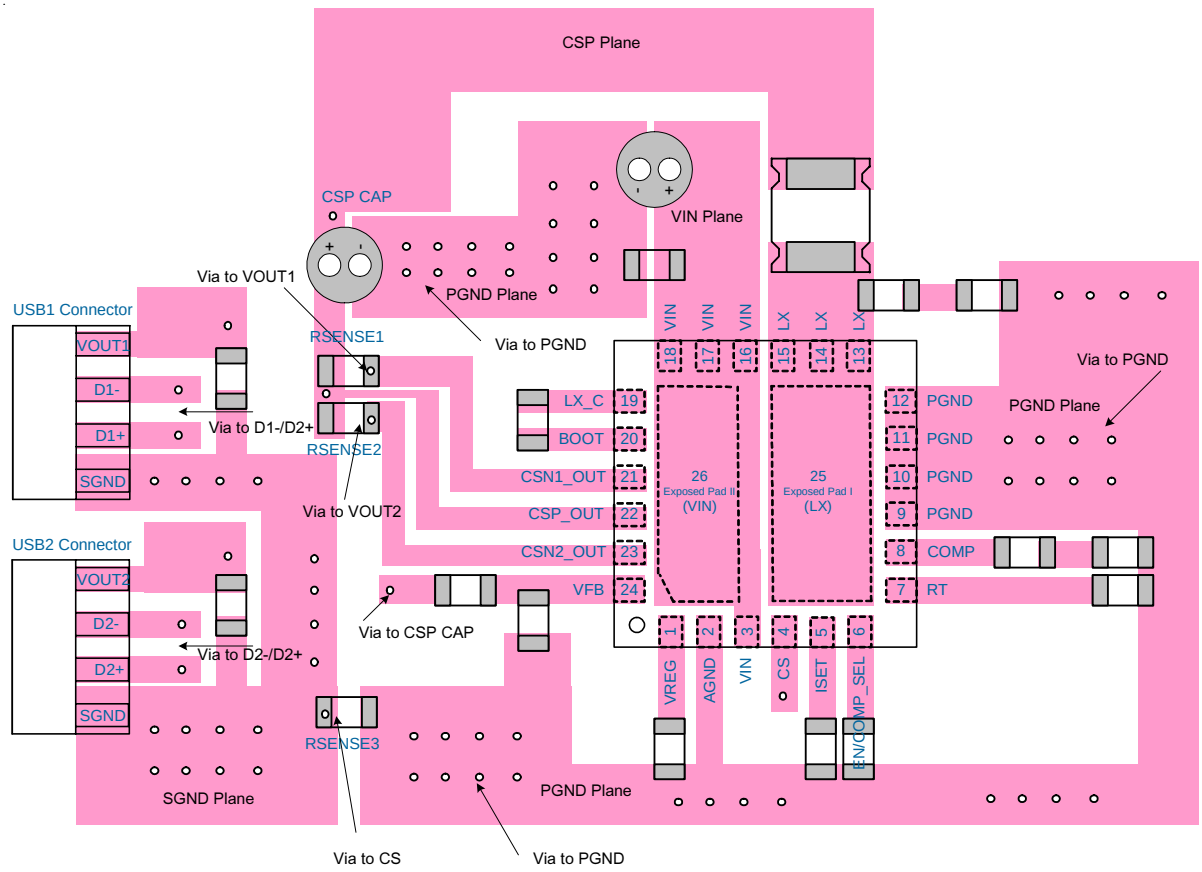
Application Limitation for uP9626P:

For output voltage setting from 3.6V to 21V, uP9626P is capable of sourcing load current up to 3.0A at CSN1 and CSN2 during power on. When output voltage setting is under 3.6V, the sourcing capability at CSN1 and CSN2 is not guaranteed, but there is no such limitation after power on.

Layout Guidelines For uP9626P:

1. The input decoupling ceramic capacitor 10uF must be placed close to the VIN (Pin16,17,18) and PGND plane through vias or a short and wide path.
2. The 5.1V VREG LDO output capacitor (2.2uF, MLCC) for gate drive supply voltage must be placed close to the VREG(Pin1) and connected to AGND (Pin2) directly, to avoid noise and instability.
3. When adjust output total current limit for dual channel application, AGND and PGND (power ground) should be connected together at a single point, the power ground copper area with copper plane and vias for best heat dissipation and noise immunity.
4. Use a short trace connecting the bootstrap capacitor C_{BOOT} close to BOOT (Pin 20) and LX_C (Pin19) to form a bootstrap circuit.
5. The FB feedback resistor should be close to VFB(Pin 24) and be away from switching node.
6. The current sense traces should be connected to the current sense resistor's (RSENSE1/2/3) pads in Kelvin sense way as the figure on next page, routed in parallel (differential routing), and be away from switching node as LX and inductor.
7. The current sense resistor's (RSENSE1/2/3) should be close to CSN1/CSP/CSN2/CS(Pin 21,22,23,4) to avoid noise and constant current instability.
8. The optional ceramic capacitor 0.1uF must be placed close to the CSN1/CSN2/CS (Pin 21,23,4) and PGND plane through vias or a short path to to avoid noise and constant current instability.
9. The optional ceramic capacitor 4.7uF must be placed close to USB connector VOUT1 and VOUT2 for good CC performance.
10. The RC snubber is connected between LX and PGND or VIN and LX to absorb switching noise. The snubber should be close to LX and PGND or VIN and LX pin to eliminate the high frequency voltage spike and minimize the loop area to optimize EMI.
11. The LX pad (Pin25) and LX (Pin 13,14,15) are the noise nodes switching from VIN to GND. LX node copper area should be minimized and wide to reduce EMI and should be isolated from the rest of circuit for good EMI and low noise operation. The inductor must be placed close to the LX (Pin13,14,15) for good efficiency and decrease PCB trace loss.
12. The D+ and D- of the USB Connector are the USB detect data line input nodes, the D+ and D- Pin of the via or trace area should be isolated using 0.96mm space to prevent direct contact with VOUT area components which may cause voltage of D+ and D- pins to exceed maximum rating voltage.
13. The 4-layered PCB layout can increase heat dissipation area by taking advantage of the middle layers of the PGND plane. This may also lower the temperature of IC and its peripheral components of the demo board such as inductor.

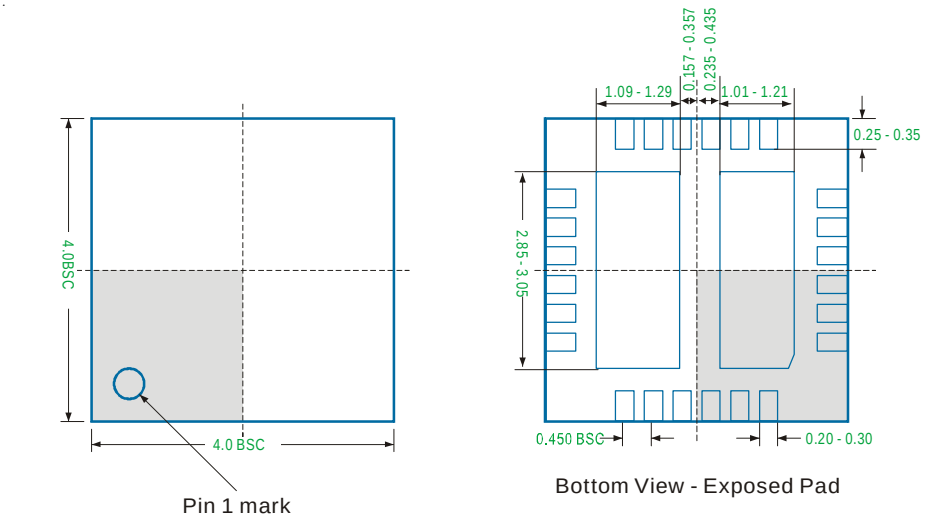
Application Information



uP9626PQMG

Package Information

WQFN4x4 - 24L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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