uP9628P

High Performance Single-Phase Synchronous Buck Converter

General Description

The uP9628P is a high performance synchronous buck converter specifically designed to work with 2.7V~22V input voltage and deliver high quality output voltage for microprocessor and chipset supplies.

The uP9628P provides flexible selection of output LC filter and excellent transient response to load and line regulation. The uP9628P has complete functions including under voltage protection, over voltage protection, current limit protection, soft-start, power good indication and over temperature protection. This part is available in WQFN4X4-23L package.

Features

- **Support NVIDIA Open VReg Type 1 Technology**
- **Wide Input Voltage Range from 2.7V to 22V**
- **Output Current Up to 12A**
- **Adjustable Output Voltage from 0.6V to 2.5V**
- **Selectable Operation Frequency from 300kHz to 600kHz**
- **Constant On Time Control**
- **Fast Load Transient Response**
- **Adjustable Soft-Start Function**
- **Support Output Discharge (Soft-Off) Function**
- **Selectable Forced CCM or DCM**
- **Power Good Indication**
- **Current Limit Protection**
- **Over/Under Voltage Protection**
- **Over Temperature Protection**
- **RoHS Compliant and Halogen Free**

Applications

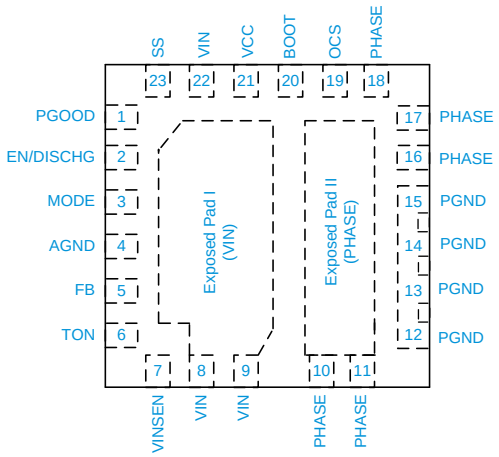
- **CPU Core I/O Supplies**
- **Graphic Cards**
- **Microprocessor and Chipset Supplies**
- **Desktop PCs, Notebook Computers**

Ordering Information

Order Number	Package Type	Top Marking
uP9628PQMX	WQFN4x4-23L	uP9628P

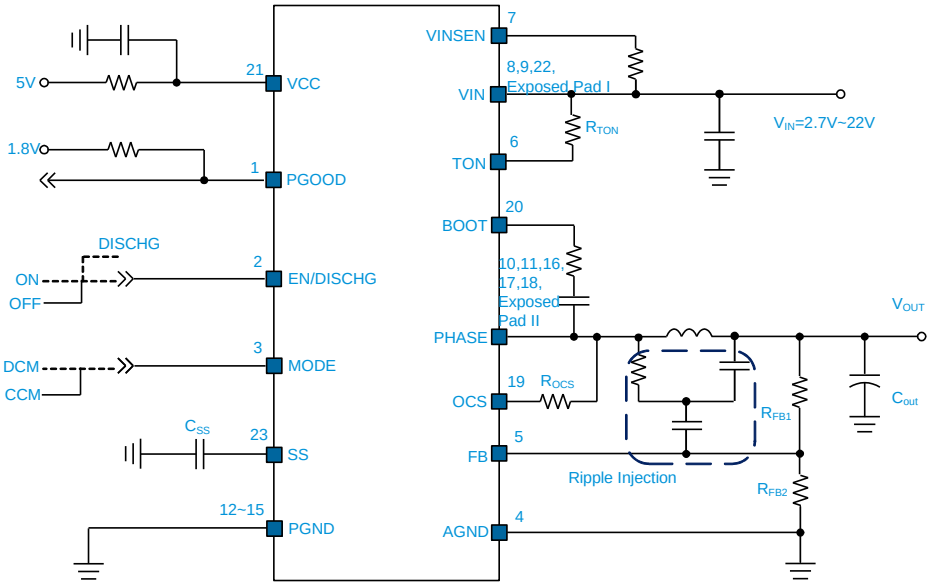
Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



uP9628P

Typical Application Circuit



Functional Pin Description

Pin No.	Name	Pin Function
1	PGOOD	**Power Good Indication.** This pin is an open drain structure and it is active high. Pull up this pin through a proper resistor to a voltage source.
2	EN/DISCHG	**Chip Enable and Discharge Control Pin.** This pin is used for enable control and output discharge control.
3	MODE	**Operation Mode Selection.** An input pin receiving operation mode control signal. Mode input voltage determines the controller operating mode. There is 1MΩ pull-down resistor internal to this pin.
4	AGND	**Analog GND.** This pin is the ground of logic control circuits, it must be connected to the PCB ground plane.
5	FB	**Feedback Pin.** This pin is the inverting input of the error amplifier.
6	TON	**On-time Setting Pin.** Connect a resistor from this pin to VIN to set the PWM on time.
7	VINSEN	**Power Stage Input Voltage Sense.** Connect this pin to the power stage input with a 0Ω resistance. The input voltage to this pin is used to determine the PWM on time.
8,9,22	VIN	**Supply Input.** Supply input to the converter power stage. These pins are connected to the drain of embedded high-side MOSFET.
10,11,16,17,18	PHASE	**Switch Node.** These pins are the joint of source of embedded high-side MOSFET and drain of low-side MOSFET. Connect these pins to the output inductor.
12~15	PGND	**Power Ground.** These pins are connected to the source of embedded low-side MOSFET and should be connected to the ground plane through multiple vias.
19	OCS	**Over Current Setting.** Connect a resistor from this pin to PHASE to set the inductor valley current limit threshold.
20	BOOT	**Bootstrap Supply for the Floating High-Side MOSFET Gate Driver.** The bootstrap capacitor provides the charge to turn on the embedded high-side MOSFET. Connect a 0.1uF MLCC from this pin to PHASE to form a bootstrap circuit.
21	VCC	**5V Power Supply Input.** This pin provides power for internal circuit. Bypass this pin with an at least 1uF ceramic capacitor to ground.
23	SS	**Soft-Start Pin.** Connect an MLCC from this pin to GND to determine output voltage ramp up time.
Exposed Pad I (VIN)		**Supply Input.** Supply input to the converter power stage. This exposed pad is connected to the drain of embedded high-side MOSFET. Place the input MLCC as close to the IC as possible.
Exposed Pad II (PHASE)		**Switch Node.** This exposed pad is the joint of source of embedded high-side MOSFET and drain of low-side MOSFET. Connect this pad to the output inductor.

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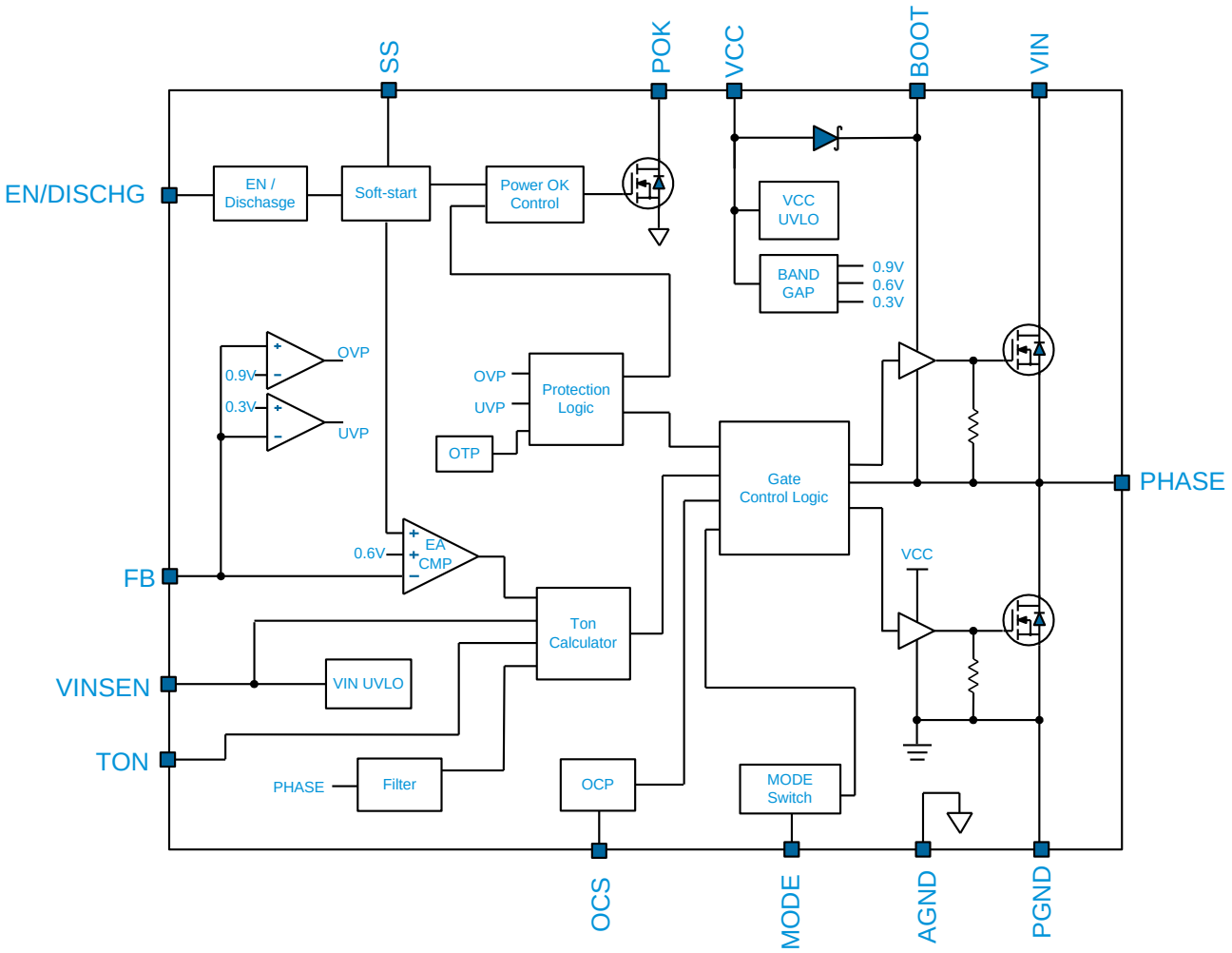
Functional Block Diagram



Functional Description

Power Input and Power On Reset

The uP9628P has four power inputs VCC, VIN, VINSEN and EN/DISCHG. VCC is the 5V supply input for control logic circuit of the converter. RC filter to VCC is required for locally bypassing this supply input and VCC has power on reset (POR) function. VIN is the power stage input voltage pin. VINSEN is the power stage input sense pin, connect a 0Ω resistance from this pin to the VIN for PWM on-time calculator and this pin has power on reset function. EN/DISCHG is the chip enable pin. Logic high to this pin enables the converter, logic low to this disables the converter and this pin also has power on reset function. The above three inputs (VCC, VINSEN and EN/DISCHG) are monitored to determine whether the converter is ready for operation.

Figure 1 shows the power ready detection circuit. The VCC voltage is monitored for power on reset with typically 4V threshold at its rising edge. The VINSEN voltage is monitored for power on reset with typically 2.1V threshold at its rising edge. When VCC and VINSEN are all ready, the converter waits for EN/DISCHG to start up. When EN/DISCHG pin is driven above 1V, the converter begins its start up sequence.

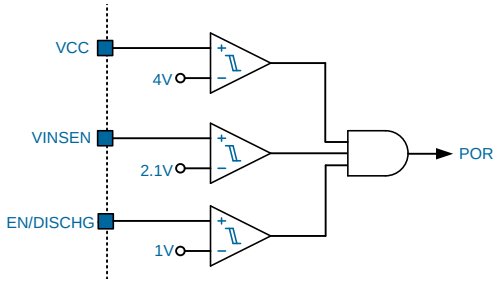


Figure 1. Circuit of Power Ready Detection

Enable and Output Voltage Discharge

The EN/DISCHG is a multi-function pin. It is used for chip enable and discharge control. The uP9628P provides output discharge control function. When Output Discharge=ON and after the EN/DISCHG pin is pulled low, the converter discharges the output capacitor. The output voltage monotonically ramps down and it is similar to the reverse process of the Soft-Start. Table 1 lists the setting voltage level of chip enable and discharge control.

Table 1.EN/DISCHG Setting Voltage

EN/DISCHG	Function
$V_{EN/DISCHG}$ < 0.4V	Chip Disable
1V < $V_{EN/DISCHG}$ < 1.4V	Chip Enable and Output Discharge = ON
$V_{EN/DISCHG}$ > 1.6V	Chip Enable and Output Discharge = OFF

Soft Start Time

The uP9628P features a programmable soft start function to limit the input surge current. Connect a soft start capacitor C_{SS} from SS pin to ground to determine output voltage ramp up time. The output voltage ramp up time (T_{ramp}) during soft start period is determined by the internal current source (I_{SS}) and C_{SS}, and it can be calculated as below.

$$T_{ramp} = \frac{0.6 \times C_{SS}}{I_{SS}} = 0.6 \times 10^{8} \times C_{SS} (ms)$$

Functional Description

PWM On-Time Setting

The PWM on-time is set by an external resistor R_{TON} connected between TON pin and VINSEN pin. The converter senses VINSEN voltage to obtain input voltage information for PWM on-time calculation. The PWM on time and frequency can be calculated as the equation below:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_{SW}}$$

$$F_{SW}(kHz) = \frac{94000}{R_{TON}(k\Omega)}$$

Output Current Limit

The uP9628P monitors the inductor valley current by low-side MOSFET $R_{DS(ON)}$ when it turns on. The over current limit is triggered once the sensed current level is higher than V_{OCS} setting. When triggered, the over current limit will keep high-side MOSFET off even the voltage loop commands it to turn on.

The output voltage will decrease if the load continuously demands more current than current limit level. Further increase in load current higher than the current limit level will eventually let output voltage decrease to trip UVP to shut down the converter.

The current limit threshold is set by connecting a resistor from OCS to PHASE. The OCS pin will source a 20uA current and create a voltage drop across R_{OCS} as the V_{OCS}.

$V_{OCS} = 20uA \times R_{OCS}$ Note: R_{OCS} minimum ≥ 3.3kΩ

When the voltage drop across the low-side MOSFET equals the voltage across the setting resistor, the current limit will be activated. The current limit level is calculated as:

$$I_{LIM} = \frac{V_{OCS} - 30(mV)}{R_{DS(ON)}} + \frac{I_{RIPPLE}}{2}$$

where I_{RIPPLE} is the peak-to peak inductor current at steady state.

Output Voltage Setting

The uP9628P is capable of precisely regulating an output voltage as low as 0.6V. In fact, the device comes with fixed 0.6V internal reference that guarantees the output regulated voltage to be within ±1% tolerance. Output voltage higher than 0.6V can be easily achieved by adding a resistor between FB pin and ground. The steady state DC output voltage will be:

$$V_{OUT} = V_{REF} \times \frac{R_{FB1} + R_{FB2}}{R_{FB2}}$$

Functional Description

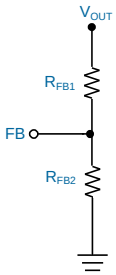


Figure 2. Feedback Circuit

Operation Mode Selection

The uP9628P provides power saving features for platform designers to program platform specific power saving configuration. The uP9628P switches between CCM and DCM operation modes according to the input voltage level of the MODE pin. Table 2 shows recommended MODE pin setting voltage level of two operation modes.

When the DCM mode is activated, the uP9628P automatically reduces switching frequency at light load to maintain high efficiency. As the load current increases, the rectifying MOSFET is turned on and the converter runs in continuous conduction mode. The uP9628P operation mode can be changed after PGOOD is pulled high.

Table 2. Recommended MODE Pin Setting

Operation Mode	Recommended Voltage Setting at MODE
DCM	1.2V
CCM	0V

Over Voltage Protection (OVP)

The over voltage protection is triggered if FB voltage higher than 150% of the target voltage sustained for 20us. When OVP is activated, the uP9628P turns on low-side MOSFET and turns off high-side MOSFET. The over voltage protection is a latch-off function and can only be reset by VCC, VINSEN or EN/DISCHG.

Under Voltage Protection (UVP)

The under voltage protection is triggered if FB voltage lower than 50% of the target voltage sustained for 10us. When UVP is activated, the uP9628P turns off high-side and low-side MOSFET. The under voltage protection is a latch-off function and can only be reset by VCC, VINSEN or EN/DISCHG.

Over Temperature Protection (OTP)

The uP9628P monitors the temperature of itself. If the temperature exceeds typical 160℃, the uP9628P is forced into shutdown mode. The over temperature protection is a latch-off function and can only be reset by VCC, VINSEN or EN/DISCHG.

Absolute Maximum Rating

(Note 1)

VIN/VINSEN to GND ---------- -0.3V to +30V
TON to GND ---------- -0.3V to +30V
BOOT to GND
- DC ---------- -0.3V to +36V
- < 200ns ---------- -5V to +42V

PHASE to GND
- DC ---------- -0.7V to +30V
- < 200ns ---------- -8V to +36V

OCS to GND
- DC ---------- -0.3V to +6V
- < 200ns ---------- -8V to +8V

BOOT to PHASE ---------- -0.3V to +6V
Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65℃ to +150℃
Junction Temperature ---------- 150℃
Lead Temperature (Soldering, 10 sec) ---------- 260℃
ESD Rating (Note 2)
- HBM (Human Body Mode) ---------- 2kV
- CDM (Charged Device Mode) ---------- 1kV

Thermal Information

Package Thermal Resistance (Note 3)
- WQFN4x4-23L θ_{JA} ---------- 37℃/W
- WQFN4x4-23L θ_{JC} ---------- 2℃/W

Power Dissipation, P_D @ T_A = 25℃
- WQFN4x4-23L ---------- 1.47W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40℃ to +125℃
Operating Ambient Temperature Range ---------- -40℃ to +85℃
Supply Input Voltage, VCC ---------- 4.5V to 5.5V
Input Voltage, V_{IN} ---------- 2.7V to 22V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25℃ on a low effective thermal conductivity test board of *JEDEC 51-3* thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(VCC = 5V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
VCC POR Rising Threshold	V_{VCCTH}	V_{CC} rising	--	4	--	V
VCC POR Hysteresis	V_{VCCHYS}	V_{CC} rising - V_{CC} falling	--	250	--	mV
VCC Shutdown Current	$I_{SHDN(VCC)}$	EN/DISCHG = 0V	--	--	1	uA
	$I_{SHDN(TON)}$		--	--	0.1	
	$I_{SHDN(EN)}$		--	--	1	
VCC Quiescent Current	I_Q	EN/DISCHG = 5V, no switching, DCM operation	--	650	--	uA
VIN Power On Reset						
VINSEN POR Threshold	$V_{VINPORH}$	VINSEN rising	--	2.1	--	V
VINSEN POR Hysteresis	$V_{VINPORHYS}$	VINSEN rising - VINSEN falling	--	0.3	--	V
Reference Voltage						
Reference Voltage	V_{FB}	Measure FB voltage	0.594	0.6	0.606	V
Input Bias Current	I_{FB}	V_{FB} = 0.6V	--	--	0.1	uA
Enable/Discharge						
Logic Low	V_{ENL}	Disable	--	--	0.4	V
Logic High	V_{ENH_DSG}	Enable, Output Discharge = ON	1	--	1.4	V
	V_{ENH_DISDSG}	Enable, Output Discharge = OFF	1.6	--	--	
Operation Mode						
CCM Operation	V_{MODE_CCM}	Measure MODE pin voltage	--	--	0.4	V
DCM Operation	V_{MODE_DCM}	Measure MODE pin voltage	1	--	1.4	V
PWM On-Time						
On Time	T_{ON}	VINSEN = 12V, Vout = 1.4V, CCM, I_{OUT} = 0A, R_{TONSET} = 261kΩ	--	324	--	ns
Minimum On Time	T_{ON_MIN}	VINSEN = 24V, Vout = 0.6V, R_{TONSET} =150kΩ	--	60	--	ns
Minimum Off Time	T_{OFF_MIN}	FB = 0.59V	--	250	--	ns
Zero Current Detection						
Zero Current Detection Offset Voltage	V_{ZCD_OFS}	Measure PHASE voltage	-2	--	2	mV

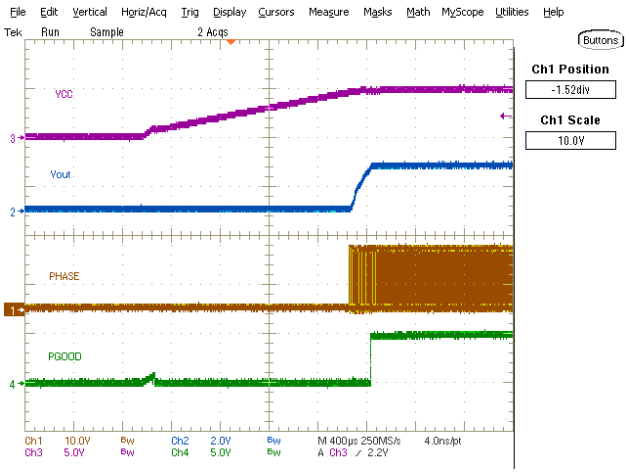
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Soft Start						
Soft Start Current	I_{SS}	V_{SS} = 0V	--	10	--	uA
PGOOD Delay Time	$T_{D\_EN\_PG}$	EN/DISCHG high to PGOOD high, C_{SS} = 2.2nF	--	400	--	us
Power MOSFET						
High Side MOSFET $R_{DS(ON)}$	R_{DSH}	V_{BOOT} - V_{PHASE} = 5V	--	15	--	mΩ
High Side MOSFET Leakage Current	I_{LEAK_RDSH}		--	--	10	uA
Low Side MOSFET $R_{DS(ON)}$	R_{DSL}	V_{VCC} - PGND = 5V	--	6	--	mΩ
Low Side MOSFET Leakage Current	I_{LEAK_RDSL}		--	--	10	uA
Bootstrap Diode						
Forward Voltage	V_F	Forward bias current = 3.5mA	--	0.4	--	V
PGOOD						
Output Low Voltage	V_{PGD_GL}	I_{PG} = 1mA	--	--	0.1	V
Output Leakage Current	I_{PGD_LEAK}	Pull up to 5V	--	--	1	uA
Protection						
OCP Setting Current	I_{OCS}	V_{OCS} =0V	18	20	22	uA
Current Sense Amplifier Offset Voltage	V_{OCS_OFS}	Measure OCS voltage	-2	--	2	mV
OCP Setting Current Temperature Coefficient	T_{IOCS}	Guaranteed by design	--	5300	--	ppm/℃
OVP Threshold	V_{OVP}	Measure FB, with respect to reference voltage	--	150	--	%
OVP Delay Time	T_{OVP}		--	20	--	us
UVP Threshold	V_{UVP}	Measure FB, with respect to reference voltage	--	50	--	%
UVP Delay Time	T_{UVP}		--	10	--	us
OTP Threshold	T_{OTP}	Guaranteed by design	--	160	--	℃

uP9628P

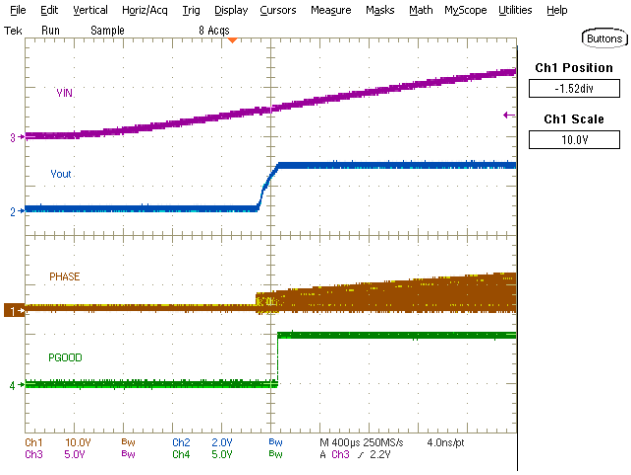
Typical Operation Characteristics

Power On from VCC



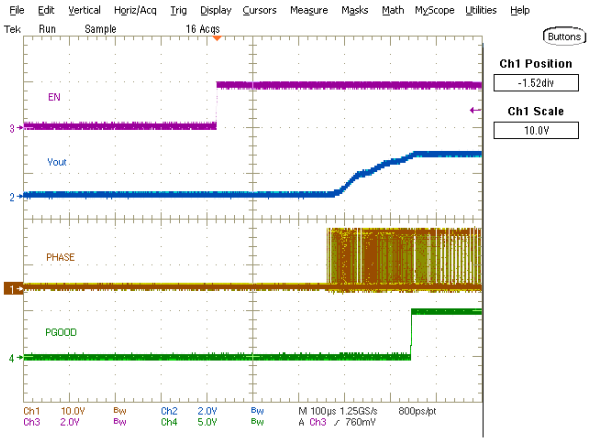
V_{IN}=12V, I_{OUT}=0A, V_{OUT}=1.8V

Power On from VIN



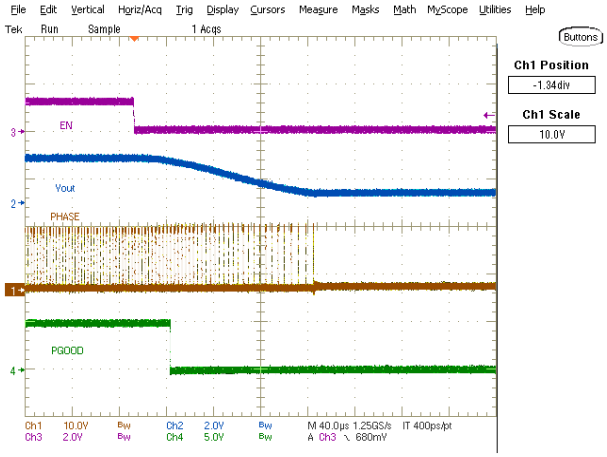
V_{IN}=12V, I_{OUT}=0A, V_{OUT}=1.8V

Power On from EN



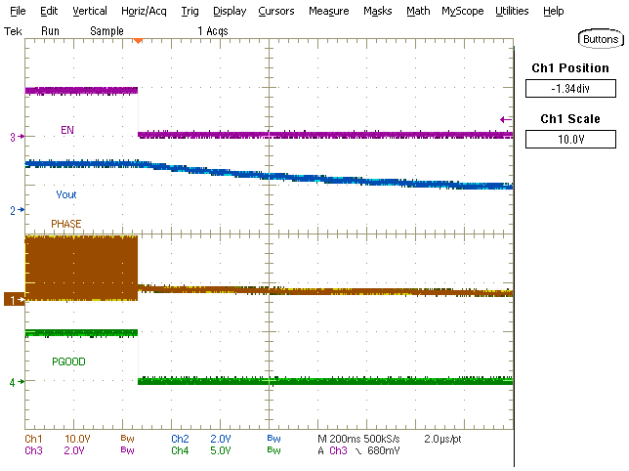
V_{IN}=12V, I_{OUT}=10A, V_{OUT}=1.8V

Power Off from EN, Output Discharge = ON



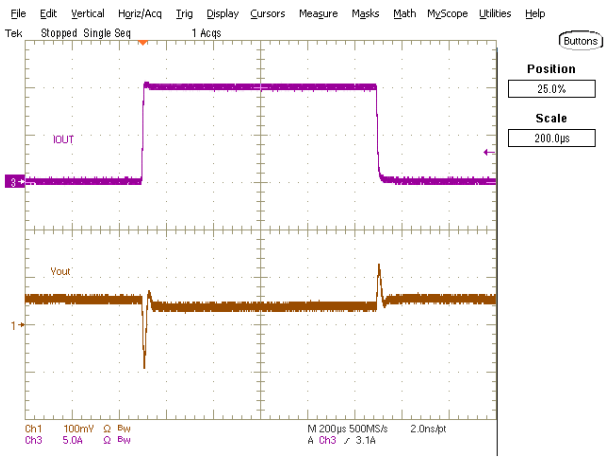
V_{IN}=12V, I_{OUT}=0A, V_{OUT}=1.8V, EN=1.2V

Power Off from EN, Output Discharge = OFF



V_{IN}=12V, I_{OUT}=0A, V_{OUT}=1.8V, EN=1.8V

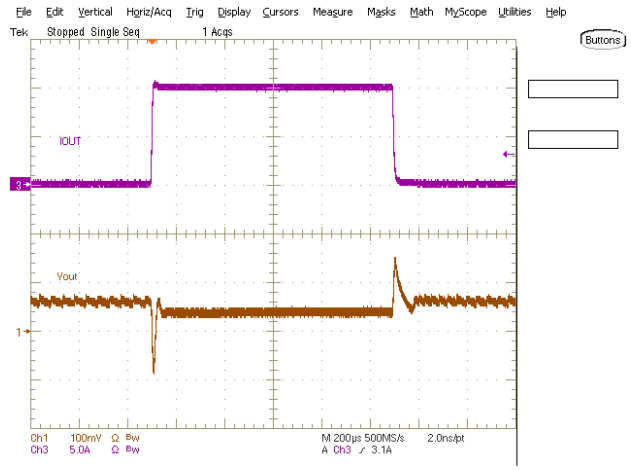
CCM Load Transient



V_{IN}=12V, L=2.2uH, I_{OUT}=0~10A, MODE=0V

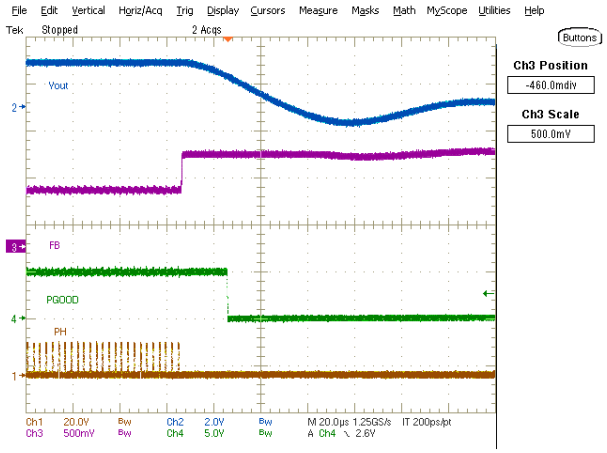
Typical Operation Characteristics

DCM Load Transient



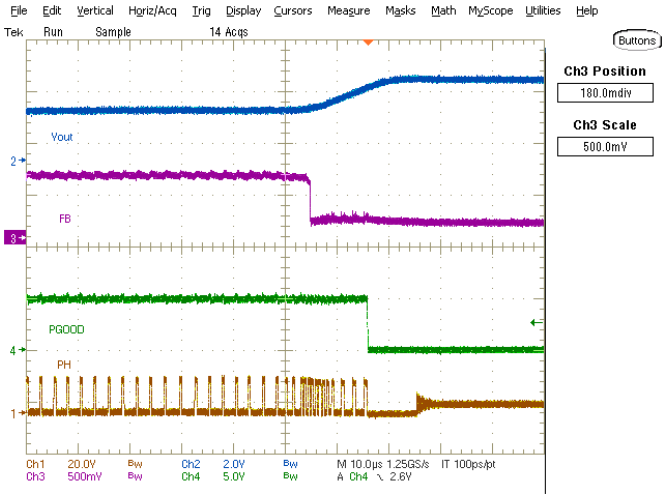
V_{IN}=12V, L=2.2uH, I_{OUT}=0~10A, MODE=1.2V

OVP



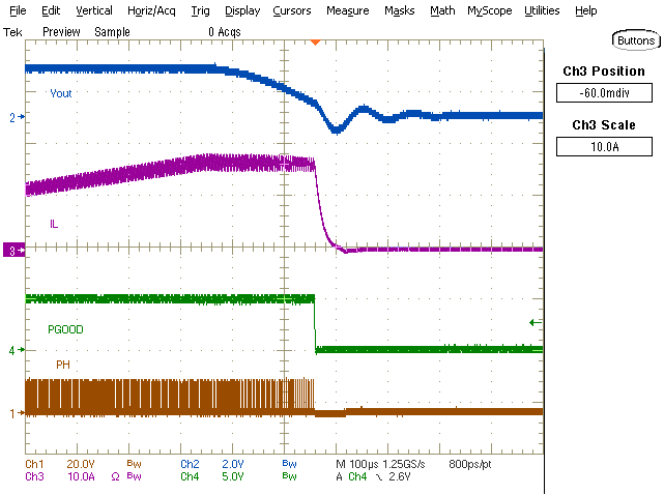
V_{IN}=12V, I_{OUT}=0A, V_{OUT} =1.8V

UVP



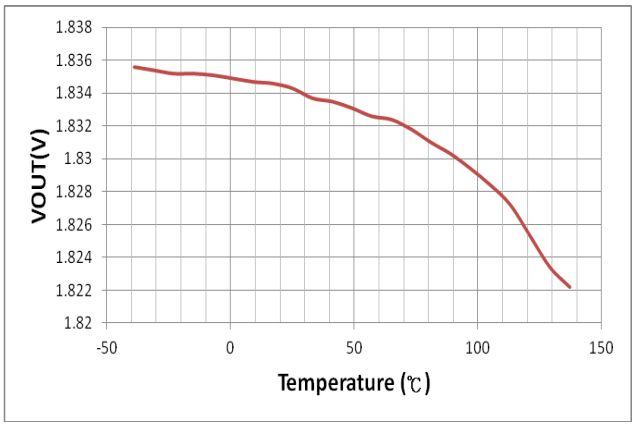
V_{IN}=12V, I_{OUT}=0A, V_{OUT}=1.8V

Output Current Limit

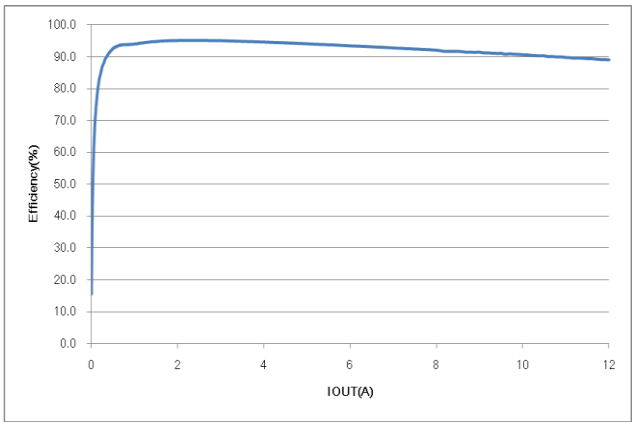


V_{IN}=12V, V_{OUT}=1.8V

Vout vs Temperature



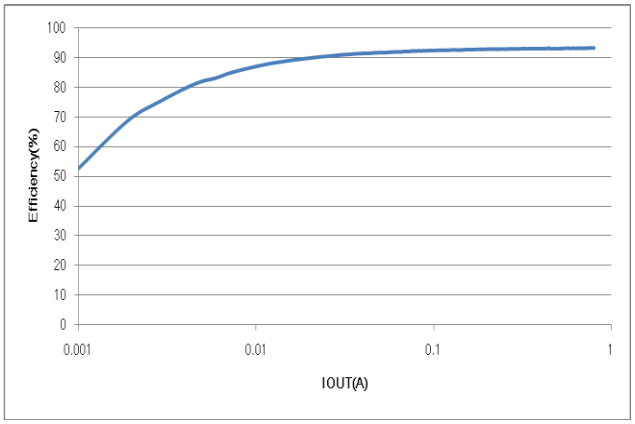
Efficiency CCM



V_{IN}=12V, V_{OUT}=1.8V, L=2.2uH, MODE=0V

Typical Operation Characteristics

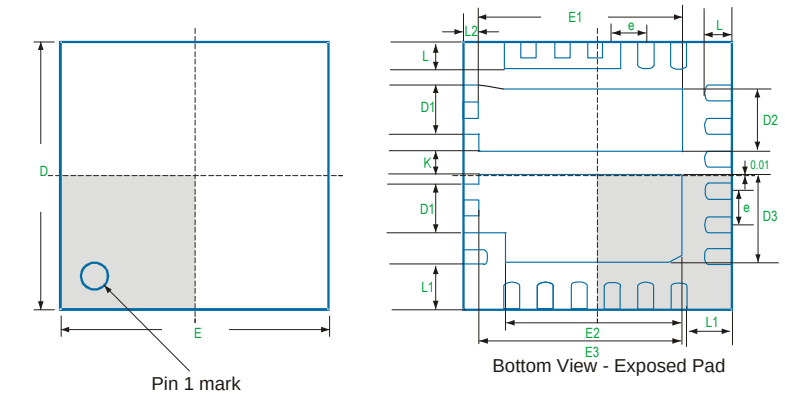
Efficiency DCM



V_{IN}=12V, V_{OUT}=1.8V, L=2.2uH, MODE=1.2V

Package Information

WQFN4x4-23L



Symbol	MIN	NOM	MAX	Symbol	MIN	NOM	MAX	Symbol	MIN	NOM	MAX
A	0.70	0.75	0.80	D1	0.65	0.75	0.85	L	0.35	0.40	0.45
A1	0.00	0.02	0.05	D2	0.85	0.95	1.05	L1	0.57	0.62	0.67
A3	0.20 REF			D3	1.24	1.34	1.44	L2	0.20	0.25	0.30
b	0.20	0.25	0.30	E1	2.95	3.05	3.15	K	0.30	0.35	0.40
D	3.90	4.00	4.10	E2	2.60	2.65	2.70				
E	3.90	4.00	4.10	E3	2.95	3.05	3.15				
e	0.50 BSC										

Note

1. Package Outline Unit Description:
   MIN: Minimum dimension specified.
   NOM: Nominal. Provided as a general value.
   MAX: Maximum dimension specified.
   BSC: Basic. Represents theoretical exact dimension or dimension target.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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