

uP9642B

Smart Power Stage (SPS) with Integrated Current and Temperature Monitors

General Description

The uP9642B is a Smart Power Stage (SPS) solution with fully optimized, integrated driver and MOSFETs for high-current, high frequency, synchronous buck DC-DC converters. The SPS enables higher performance at lower output voltages required by cutting edge CPU, GPU and DDR memory designs.

The uP9642B also enables advanced high accuracy module temperature reporting and on-chip synchronous MOSFET current monitoring. The protection includes cycle-by-cycle over current protection, phase fault detection, preliminary over voltage protection, VCC/VDRV UVLO protection, and thermal shutdown.

The uP9642B is optimized for CPU core power delivery. This device combined with a multi-phase buck PWM controller forms a complete core voltage regulator for advanced micro-processors.

Ordering Information

Order Number	Package Type	Top Marking
uP9642BQR1	VQFN6X5-39L	uP9642B

Note:

- Please check the sample/production availability with uPI representatives.
- uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

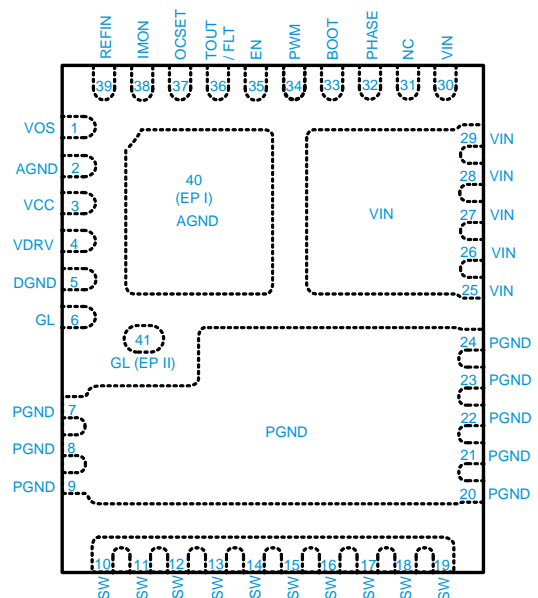
Applications

- High Frequency, Low Profile DC-DC Converter
- Voltage Regulator for CPUs, GPUs and DDR Memory Arrays

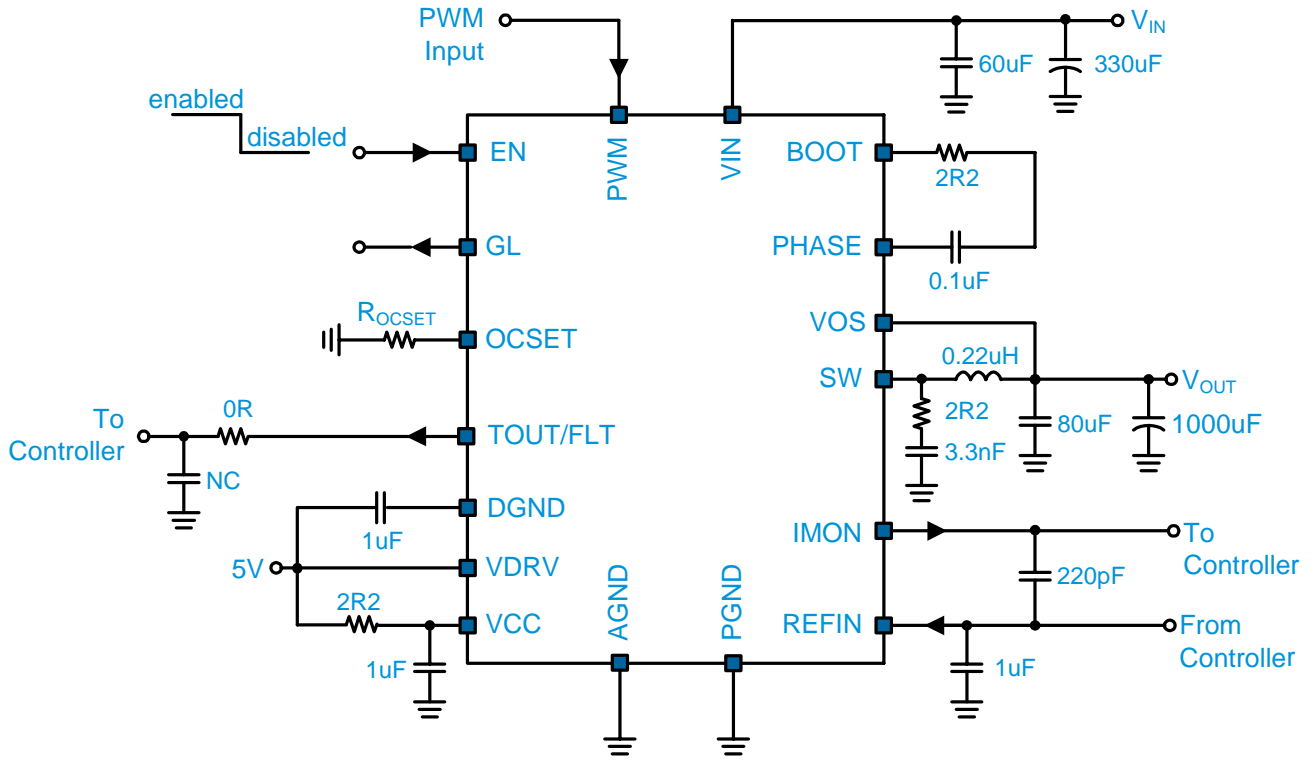
Features

- Input Voltage (V_{IN}) Range: 4.5V to 16V
- VCC and VDRV Supply Range: 4.5V to 5.5V
- Output Voltage Range: 0.4V to 2.0V
- Up to 60A of Current Handling Capability
- Switching Frequency Range: 200kHz to 700kHz
- 5mV / A On-Chip MOSFET Current Sensing
- 8mV / °C Temperature Analog Output
- On-Chip MOSFET Temperature Compensation
- VCC / VDRV Under Voltage Lockout (UVLO)
- Thermal Shutdown and Fault Flag
- MOSFET Phase Fault Detection and Flag
- Cycle-by-Cycle Over Current Protection
- Preliminary Over Voltage (OV) Protection and Flag
- Support 3.3V and 5V Tri-State PWM Input
- Deep-Sleep Mode for Power Saving
- VOS Output Voltage Sensing Input
- Lead Free and RoHS Compliant Package

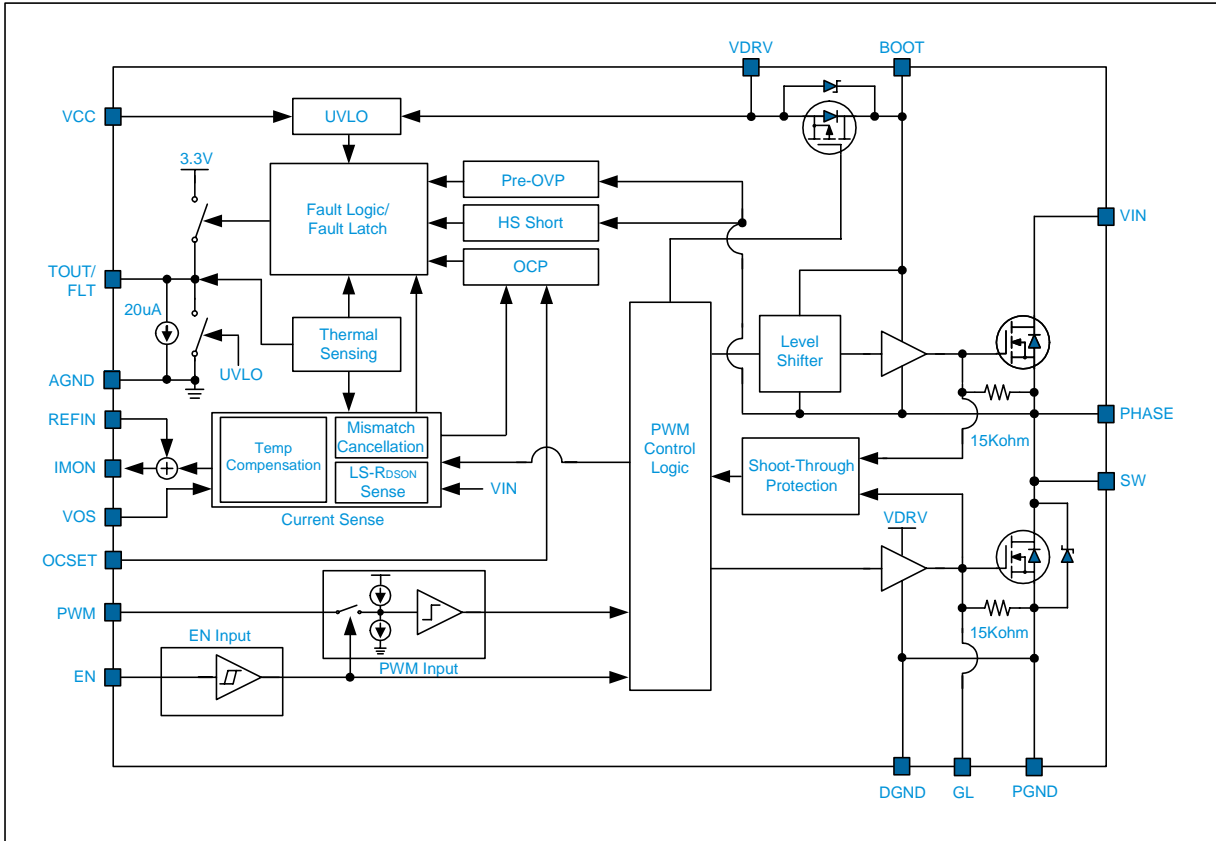
Pin Configuration



Typical Application Circuit



Functional Block Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VOS	VOUT Sense. Output voltage sensing pin for current sensing application.
2	AGND	Signal Ground. All signals are referenced to this pin.
3	VCC	Supply Voltage for the IC. 5V supply voltage for internal control logic circuit. Connect a 1uF capacitor between VCC and AGND and place it as close to the pin as possible.
4	VDRV	Drive Voltage Output. 5V supply voltage for internal gate drivers. Connect a 1uF capacitor between VDRV and DGND and place it as close to the pin as possible.
5	DGND	Driver Ground.
7-9,20-24	PGND	Power Ground. It is also the power ground of the synchronous MOSFET.
6	GL	Lower Gate Driver Output. Synchronous MOSFET gate monitor pin enables the user to easily observe the waveform.
10-19	SW	Switch Node. Switching node of internal control/synchronous MOSFETs, and connects to the external inductor.
25-30	VIN	Supply Voltage for the Power Stage. 4.5V to 16V input voltage connection.
31	NC	Not Connected. This pin needs to be left floating in application.
32	PHASE	Switch Node. For bootstrap capacitor connection only. It is connected to SW internally.
33	BOOT	Bootstrap Supply. Connect a minimum 0.1uF capacitor in series with a 2.2Ω resistor from BOOT to PHASE pin. The bootstrap capacitor provides the charge to turn on the control MOSFET.
34	PWM	PWM Input. Compatible with 3.3V/5V logic level PWM Input. PWM input: "High level" turns control MOSFET on; "Tri-state" turns both MOSFETs off; "Low level" turns the synchronous MOSFET on.
35	EN	Enable Control. Pulling EN high enables the driver and requires maximum 15us power up time; pulling EN low disables the driver and enters ultralow quiescent current mode. There is no internal pull-up or pull-down mechanism to this pin.
36	TOUT/FLT	Temperature Sense Reporting/ Fault Flag. The voltage at this pin is defined by the equation: $8\text{mV} * (\text{Temperature in Celsius of driver IC}) + 0.6\text{V}.$ This pin will be pulled up to 3.3V internally under the following conditions: over temperature, over current, preliminary over voltage condition or phase fault condition.
37	OCSET	Over Current Setting. Setting over current threshold by placing a resistor from OCSET pin to AGND. If OCSET is floating or directly tied to VCC, the over current threshold is fixed at 80A. It is recommended to keep R_{OCSET} above 37.5kΩ to keep OCP level under 80A.
38	IMON	Current Sense Reporting. Sensed current output signal referenced to the REFIN pin. $V(\text{IMON} - \text{REFIN})$ voltage represents current information at 5mV/A.
39	REFIN	Reference Input. External reference voltage input for the IMON function. This pin has a low bias current and can be tied to a fixed voltage (1.2V recommended) between 1.1V and 1.8V from a PWM controller.

uP9642B

Functional Pin Description

Pin No.		Pin Name	Pin Function
40	EP I	AGND	Signal Ground.
41	EP II	GL	Lower Gate Driver Output. Synchronous MOSFET driver pin that can be connected to a test point in order to observe the waveform.

Functional Description

The uP9642B contains features as follows, the temperature sensing functionality, accurate current monitoring, ultra-compact, low-quiescent current, high-efficiency and high speed MOSFET driver fully optimized to drive a pair of integrated control and synchronous MOSFETs up to 700kHz for simplifying system design and improving functionality accuracy.

The uP9642B incorporates a synchronous MOSFET based current sense technique to provide an accurate output signal (IMON) which reports the real-time module current and to overcome the conventional inaccuracy of inductor DCR system method and resistor sense method leading to system inefficiency. $V_{(IMON-REFIN)}$ voltage represents current information at 5mV/A. The IMON signal can be used to replace inductor DCR sensing or resistor sense methods in multi-phase applications. The superior current sense accuracy achieved with on-chip current sensing technique improves the end-system performance.

The uP9642B also provides a very accurate module thermal monitor (TOUT) in normal operation. TOUT is a voltage source signal that is calibrated to provide a 0.6V output at 25°C with 8mV/°C linear slope for monitoring power stage temperature. If used in multi-phase topologies, multiple temperature outputs can be tied together to share common thermal bus. Operating with this configuration will force the thermal bus signal to report the highest voltage (highest temperature) output TOUT signal to the controller. Also, this pin is used as a module fault flag pin. If preliminary over voltage condition, a shorted control MOSFET, a prolonged over current event, or an over temperature condition inside the power stage is detected, the TOUT will be pulled up to 3.3V internally.

The uP9642B PWM input is compatible with standard either 3.3V or 5V PWM input with tri-state.

The uP9642B also supports deep-sleep power saving mode. When in deep-sleep mode that VCC is ready but EN is low, the driver will disable most of the function circuitry (with very low quiescent current) to greatly reduce power consumptions.

The uP9642B includes protection features as follows, VCC/VDRV Under Voltage-Lockout (UVLO), thermal shutdown (OTP, when SPS driver IC over temperature condition), phase fault detection, preliminary over voltage protection (Pre-OVP, when the control MOSFET is shorted), and programmable cycle-by-cycle over current protection (OCP, when in overload condition).

Tri-State PWM Input

The uP9642B PWM accepts standard 3-level input signals. When PWM logic input is high, it turns on the control

MOSFET and turns off the synchronous MOSFET once the POR of VCC is granted and EN is kept high. When logic is low, it turns off the control MOSFET and turns on the synchronous MOSFET. If the PWM input is floated, the internal circuit will pull the PWM pin into the tri-state region and turn off the control MOSFET and synchronous MOSFET. The PWM pin voltage is kept around 1.5V by internal bias circuit when floating.

Deep-Sleep Mode

If VCC is ready but EN is pulled low, the power stage will enter deep-sleep mode. The gate driver circuitry will be disabled immediately and PWM pin will be in high input impedance state and most of the logic circuitry will be shut down to lower the biasing current to less than typical 200uA. The IMON output will be shorted to ground in deep-sleep mode. When EN pin is pulled high, the power stage will be activated and able to respond to the PWM signal after maximum 15us delay time.

Over Temperature Protection and Flag (OTP)

The TOUT/FLT pin of uP9642B is a thermal monitor output in normal operation. Once the temperature of driver IC goes above the rising threshold (130°C)(the temperature of control MOSFET may reach up to 150°C), the TOUT/FLT output will raise fault flag to 3.3V immediately and the driver will be turned off for self-protection. The TOUT/FLT will remain high until temperature of driver IC falls below the falling threshold (115°C) (the temperature of control MOSFET may reach 130°C). The driver will resume switching when the temperature of driver IC falls below 115°C.

Phase Fault Detection and Flag

The phase fault circuit monitors the SW node with respect to ground when VCC POR is granted and PWM input transits from high to low and the synchronous MOSFET is still conducting. If there is a control MOSFET failure which causes the switch node voltage to exceed the control MOSFET Short Threshold ($V_{PHASFLT_TH}=400mV$), a phase fault will be activated. The TOUT/FLT will be pulled high to 3.3V immediately and will remain high until the phase fault condition is released. When TOUT/FLT is flagged high, SPS continues to respond to PWM pulses.

VCC/VDRV Under Voltage Lockout (UVLO)

The uP9642B features both internal UVLO circuitry to monitor the VCC and VDRV pins separately. When a VCC or VDRV UVLO condition is detected, the driver will be in tri-state by shutting down both MOSFETs. In addition, IMON and TOUT/FLT pins will be pulled down to ground to indicate there is a UVLO fault. When both VCC UVLO and VDRV UVLO faults are cleared, the TOUT/FLT and IMON pins will be released and the driver will resume switching.

Functional Description

Cycle-by-Cycle Over Current Protection (OCP) and Flag

With cycle-by-cycle self-protection, the current of synchronous MOSFET will be monitored every cycle. The over current threshold is programmable by connecting an external resistor R_{OCSET} between OCSET and AGND pins, refer to (EQ1). When OCSET pin is floating or shorted to VCC, the OCSET threshold is fixed to 80A. It is recommended to keep R_{OCSET} above 37.5k Ω to keep OCP level under 80A.

Once the current exceeds the over current threshold (I_{CC_OCP}), the internal logic of SPS will automatically reduce the PWM duty cycle so that the inductor current is allowed to relieve.

$$I_{CC_OCP} (A) = \frac{3000(k\Omega \times A)}{R_{OCSET} (k\Omega)} \quad (EQ1)$$

The TOUT/FLT pin will be pulled high to 3.3V after 9 cycles rise-fall events where a severe over current event has been registered. The TOUT/FLT fault flag will clear once no severe over current event is registered within one consecutive PWM cycle. When TOUT/FLT is flagged high, SPS continue to respond to PWM pulses.

Preliminary Over Voltage Protection Flag (Pre-OVP)

The Pre-OVP feature is to protect the load during the VCC power up period, especially from control MOSFET short failure. It works against pre-biased start-up when pre-charged output voltage is higher than the Pre-OVP threshold. When the VIN rail is powered up but the controller is not powered up, the controller cannot react to any over voltage condition at the load side and all PWMs are tri-stated. Pre-OVP feature is active and allows the power stage to turn on the synchronous MOSFET when VCC is in transition from pre-POR to POR and SW node voltage exceeds Pre-OVP threshold. This function is to protect the CPU from damage.

When VCC UVLO clears and there is no existing pre-biased over voltage condition, the pre-OVP feature will be disabled after receiving the first PWM pulse from the controller. The controller must manage its output voltage from that moment on.

When VCC UVLO clears and the preliminary over voltage condition remains, the synchronous MOSFET will be latched ON regardless of the PWM input and the TOUT/FLT pin will be latched high to 3.3V so that the controller can detect the fault event after it is powered up. The fault can be cleared by an under voltage condition on VCC.

Temperature Sense Output and Fault Flag (TOUT/FLT)

The uP9642B incorporates an internal temperature sensing circuitry from driver IC to provide a linear voltage slope of 8mV/ $^{\circ}$ C with a 0.6V offset at 0 $^{\circ}$ C on the TOUT/FLT pin, refer to (EQ2). In multi-phase systems the uP9642B temperature outputs can be connected together on the bus and enable to provide the highest temperature to controller IC.

$$V_{TOUT/FLT} (V) = 0.6V + \frac{0.008V}{^{\circ}C} \times T(^{\circ}C) \quad (EQ2)$$

The TOUT/FLT also provides four fault flag conditions as follows, over temperature, phase fault, over current, and preliminary over voltage conditions. TOUT/FLT will be pulled up to 3.3V internally if any fault event of the above-mentioned is detected. The TOUT/FLT can also be used as an indicator of low VCC voltage as it will be weakly pulled down to ground under the VCC UVLO condition. In a multi-phase system where the TOUT/FLT pins are tied together, once any faults occur in the phases, TOUT/FLT is able to be pulled to 3.3V internally.

Internal Current Sensing and Reporting (IMON, REFIN)

The uP9642B provides an internal real-time synchronous MOSFET current sense circuit. To use VOS pin and REFIN pin and synchronous MOSFET to make a current signal simulating the inductor current which reports to the controller. The current sense amplifier circuit in the uP9642B is completely temperature compensated for $R_{DS(ON)}$ of synchronous MOSFET. The current signal will be reported to the controller in the form of a differential voltage between IMON pin and REFIN pin with a conversion gain 5mV/A to the actual inductor current I_L , refer to (EQ3). The REFIN voltage is an externally supplied DC voltage from controller IC or other power rail in system.

$$V_{IMON} (V) - V_{REFIN} (V) = \frac{0.005V}{A} \times I_L (A) \quad (EQ3)$$

The internal current sense circuit of the uP9642B may replace the standard inductor DCR and greatly improve system efficiency.

uP9642B

Absolute Maximum Rating

(Note 1)

VCC/VDRV/EN/PWM/VOS	-----	-0.3V to +6V
TOUT/FLT/IMON/OCSET/REFIN	-----	-0.3V to (VCC+0.3V)
VIN	-----	-0.3V to 25V
BOOT to PHASE		
DC	-----	-0.3V to +6V
< 2ns	-----	-0.3V to +6.6V
VIN to SW/PHASE		
DC	-----	-0.3V to +25V
< 2ns	-----	-6V
< 100ns	-----	+27V
SW to GND		
DC	-----	-0.3V to +25V
< 2ns	-----	-6V
< 100ns	-----	+27V
PHASE to GND		
DC	-----	-0.3V to +25V
< 2ns	-----	-11V to +30V
< 100ns	-----	-6V to +30V
BOOT to GND		
DC	-----	0V to (VDRV +25V)
< 2ns	-----	-6V to +31V
GL to GND		
DC	-----	-0.3V to 6V
< 2ns	-----	-2V to +6V
Storage Temperature Range	-----	-55°C to +150°C
Junction Temperature	-----	150°C
Lead Temperature (Soldering, 10 sec)	-----	260°C
ESD Rating (Note 2)		
HBM (Human Body Mode)	-----	2kV
CDM (Charged Device Mode)	-----	1kV

uP9642B

Thermal Information

Package Thermal Resistance

VQFN6x5-39L θ_{JA} ----- 25°C/W

VQFN6x5-39L θ_{J-PCB} ----- 2°C/W

VQFN6x5-39L θ_{J-TOP} ----- 11°C/W

Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$

VQFN6x5-39L ----- 4W

Recommended Operation Conditions

(Note 3)

Operating Junction Temperature Range ----- -40°C to +125°C

Operating Ambient Temperature Range ----- -40°C to +85°C

VIN ----- 4.5V^(Note 4) to 16V

VCC/MDRV ----- 4.5V to 5.5V

Note 1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. The on-time of synchronous MOSFET must be greater than 800ns to ensure effective and correct current sensing for IMON signal.

Electrical Characteristics

($V_{CC} = V_{DRV} = 5V$, $T_A = 25^\circ C$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
VCC Supply Current	I_{VCC_ENH}	EN=1, PWM=600kHz, Duty=15%	--	6	7.8	mA
	I_{VCC_ENF}	EN=1, PWM floating	--	6	--	
	I_{VCC_ENL}	EN=0	--	200	260	uA
VCC POR Threshold	V_{CCRTH}	V_{VCC} rising	3.8	4	4.2	V
VCC POR Hysteresis	V_{CCHYS}		--	0.2	--	V
VDRV Supply Current	I_{VDRV_ENH}	EN=1, PWM=600kHz, Duty=15%	--	30	--	mA
	I_{VDRV_ENF}	EN=1, PWM floating	--	0.02	1	
	I_{VDRV_ENL}	EN=0	--	0.5	1	uA
VDRV POR Threshold	V_{DRVRTH}	V_{VDRV} rising	3.8	4	4.2	V
VDRV POR Hysteresis	V_{DRVHYS}		--	0.2	--	V
Enable Input						
Input High	EN_H		2	--	--	V
Input Low	EN_L		--	--	0.8	V
Propagation Delay	T_{PDHDEn}	PWM=0. Measured from EN rising edge to $GL > 1V$.	--	--	15	us
	T_{PDLDEn}	PWM=0. Measured from EN falling edge to $GL < 4V$.	--	30	55	ns
PWM Input						
PWM High Voltage	V_{IH_PWM}	PWM low to high or tri-state to high	2.4	--	--	V
PWM Low Voltage	V_{IL_PWM}	PWM high to low or tri-state to low	--	--	0.6	V
Tri-State Open Voltage	V_{HiZ_PWM}	PWM input floating	1.4	1.5	1.6	V
PWM Input Current	I_{PWM}	PWM=0V	--	-210	-260	uA
		PWM=3.3V	--	210	260	
		PWM=5V	--	210	260	
PWM Propagation Delay and Dead Time Range (Refer to Timing Diagram on P.10)						
PWM High Propagation Delay	$T_{PDLGATE}$	PWM going high to GL going low V_{IH_PWM} to 90% GL	--	20	--	ns
PWM Low Propagation Delay	$T_{PDLUGATE}$	PWM going low to SW going low V_{IL_PWM} to 90% SW	--	20	--	ns
Tri-State to Turn-On Propagation Delay	$T_{PDTSGHH}$	PWM (from tri-state) going high to SW going high, V_{IH_PWM} to 10% SW	--	15	--	ns
Tri-State to Turn-Off Propagation Delay	$T_{PDTSGLH}$	PWM (from tri-state) going low to GL going high, V_{IL_PWM} to 10% GL	--	15	--	ns
Tri-State Shut-Off Time	$T_{PDTSOFF}$	PWM (from low) going tri-state to GL going low, V_{IL_PWM} to 10% GL	--	25	--	ns

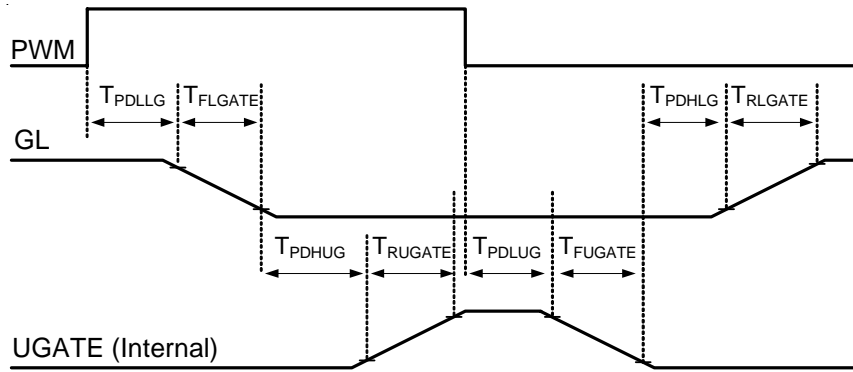
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWM Propagation Delay and Dead Time (cont.)						
GL Off to SW On Dead Time	$T_{PDHUGATE}$		--	15	--	ns
SW Off to GL On Dead Time	$T_{PDHLGATE}$		--	20	--	ns
Minimum SW Pulse Width	T_{MINSW}		--	50	--	ns
Internal Bootstrap Switch						
Forward Voltage	V_{FWD}	VDRV to BOOT, $I_{BOOT} = 10\text{mA}$, PWM = floating	--	500	--	mV
On Resistance	R_{SW}	VDRV to BOOT, $I_{BOOT} = 10\text{mA}$, PWM = 0V	--	15	--	Ω
Temperature Sense Output and Fault Flag - TOUT / FLT						
Temperature Sense Slope	T_{SNS_GAIN}	$0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ (Note 1)	7.8	8	8.2	mV/ $^{\circ}\text{C}$
Temperature Sense Offset Voltage	V_{SNS_OFFSET}	$T_J = 90^{\circ}\text{C}$, $0.6\text{V} + 8\text{mV}/^{\circ}\text{C} * T_J$	1.302	1.32	1.338	V
TOUT Source Current	I_{TOUT_SRC}		--	850	--	μA
TOUT Sink Current	I_{TOUT_SNK}		--	20	--	μA
Fault Mode Active High Voltage	$V_{FLTHIGH}$	Under over temperature, over current, phase fault or pre-OV fault	2.6	3.3	3.6	V
TOUT / FLT Active Low Voltage	V_{FLTLOW}	No fault, $V_{CC} < UVLO$	--	--	0.28	V
Fault Mode Source Current	I_{FLTSRC}	3.3V source to GND	--	3.75	--	mA
TOUT / FLT Active Pull Down Resistance	R_{PULLDN_TOUT}	No fault, $V_{CC} < UVLO$, $V_{CC} = 3.5\text{V}$	--	10	--	Ω
Current Sense Output - IMON ($T_A = T_J = 0^{\circ}\text{C}$ to 85°C)						
Accuracy	A_{CC_CS}	$T_J = 90^{\circ}\text{C}$, 20A load, $REFIN = 1.2\text{V}$, $V_{CC} = VDRV = 5.0\text{V}$	-5	--	+5	%
	A_{CC_ALL}	$I_{OUT} = 30\text{A}$ (Note 1)	-5	--	+5	%
$I_{OUT} = 40\text{A}$ (Note 1)		-7	--	+7		
Gain	G_{CS}	$T_J = 90^{\circ}\text{C}$, 20A load, $REFIN = 1.2\text{V}$, $V_{CC} = VDRV = 5.0\text{V}$ (Note 1)	4.75	5	5.25	mV/A
IMON Active Pull Down Resistance	R_{PULLDN_IMON}	$V_{CC} < UVLO$	--	170	--	Ω
IMON Sink Current	I_{CSAS}	$V_{CC} > UVLO$	--	0.3	--	mA
Current Monitor Reference Input Voltage	V_{REFIN}	Externally supplied reference voltage	1.1	1.2	1.8	V
Phase-Fault Detection						
HS Control MOSFET Short Threshold	$V_{PHASFLT_TH}$	$V(SW) - V(PGND)$ (Note 1)	--	400	--	mV
Propagation Delay for TOUT Low to Active	T_{PD_TOUT}		--	--	300	ns

Electrical Characteristics

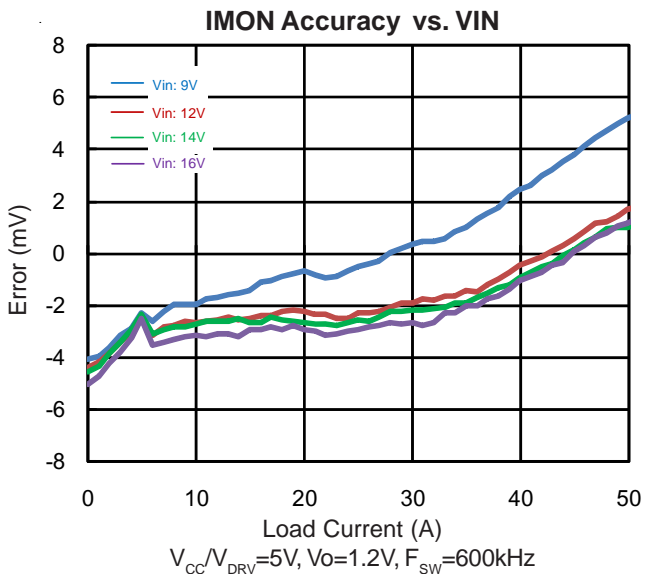
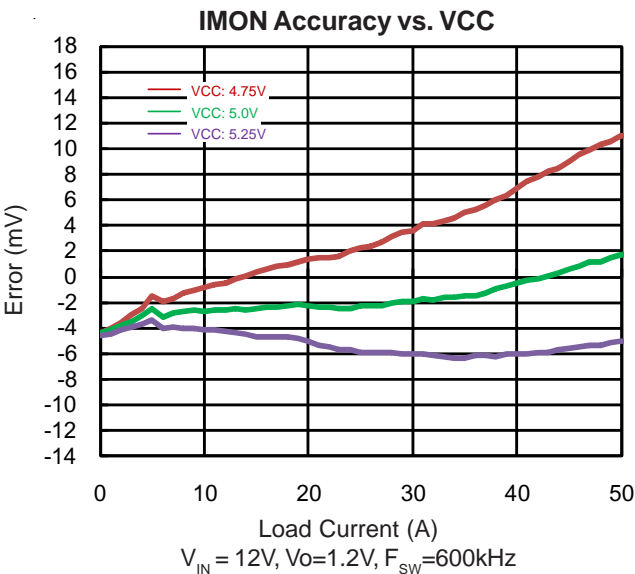
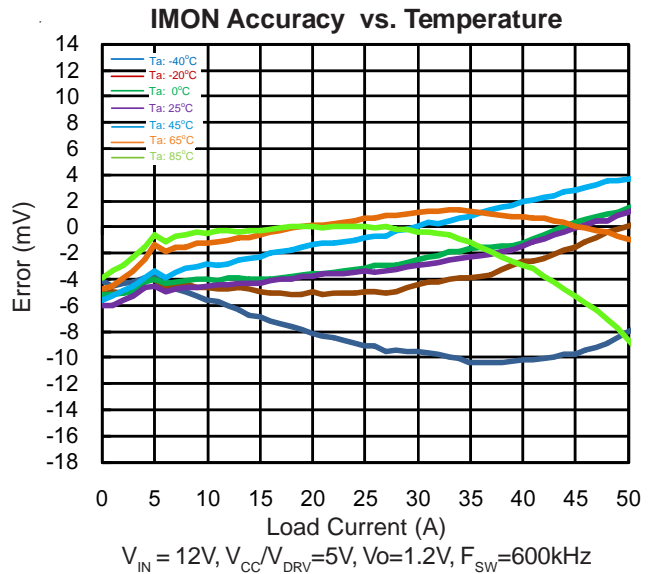
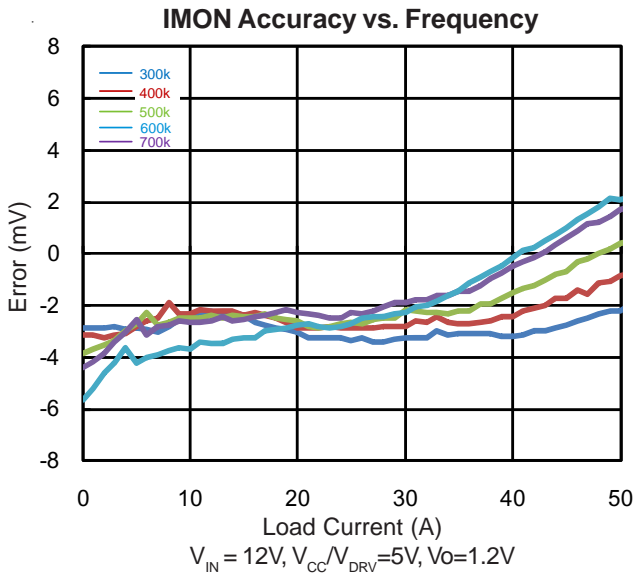
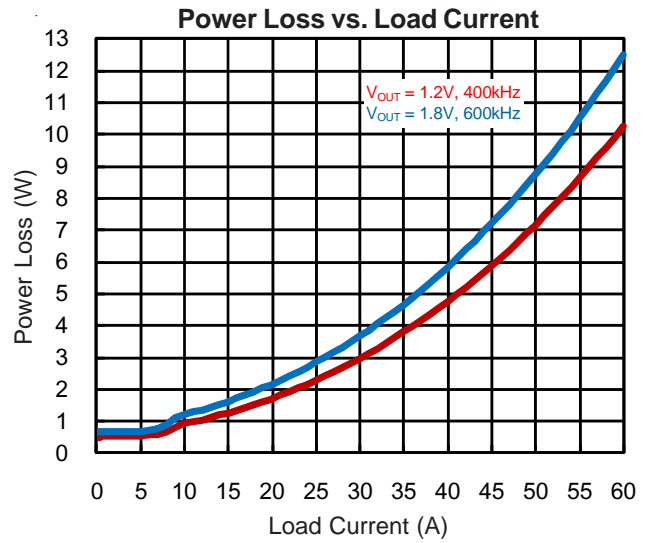
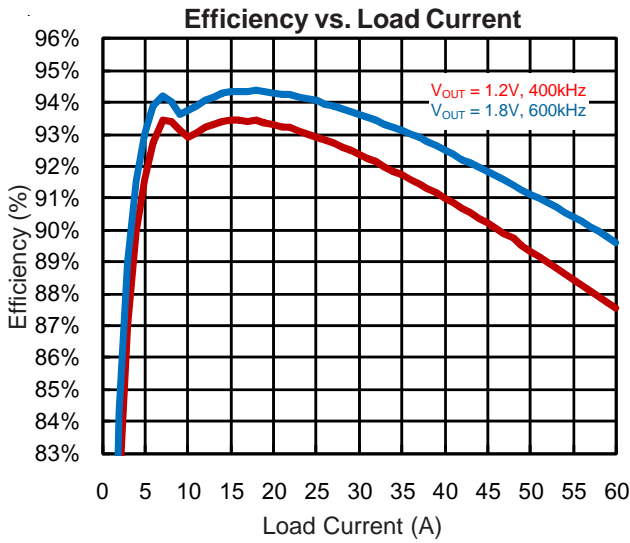
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Over Temperature Protection						
Over Temp Rising Threshold	T_{OTPR}	TOUT/FLT pulled up high, guaranteed by design (Driver IC temperature) (Note 1)	120	130	--	°C
Over Temp Falling Threshold	T_{OTPF}	TOUT/FLT released, guaranteed by design (Driver IC temperature) (Note 1)	--	115	--	°C
Preliminary Over Voltage Protection						
SW Threshold	V_{PREOVP}		--	2.7	--	V
Programmable Cycle-by-Cycle Over Current						
Programmable Over Current Threshold Range	I_{CC_OCP}	Program through R_{OCSET} (Note 1)	20	--	80	A
Over Current Threshold Programmable Gain	$I_{CC_OCP_GAIN}$	$R_{OCSET} * I_{CC_OCP}$	--	3000	--	$k\Omega * A$
Constant Over Current Threshold	V_{OCP_CST}	$T_J = 90^\circ C$, OCSET open or connects to VCC (equivalent to 80A, measure IMON to REFIN)	370	400	430	mV
Over Current Comparator Offset	$V_{OCCMP60A}$	$T_J = 90^\circ C$, OCSET open or connects to 50k Ω (equivalent to 60A, measure IMON to REFIN)	280	300	320	mV
OCP Detect Blanking Delay	$T_{BLANK_OCP_FAULT}$	PWM high-low cycles to TOUT / FLT high	--	9	--	cycle

Note 1. Guaranteed by design but not tested in production.

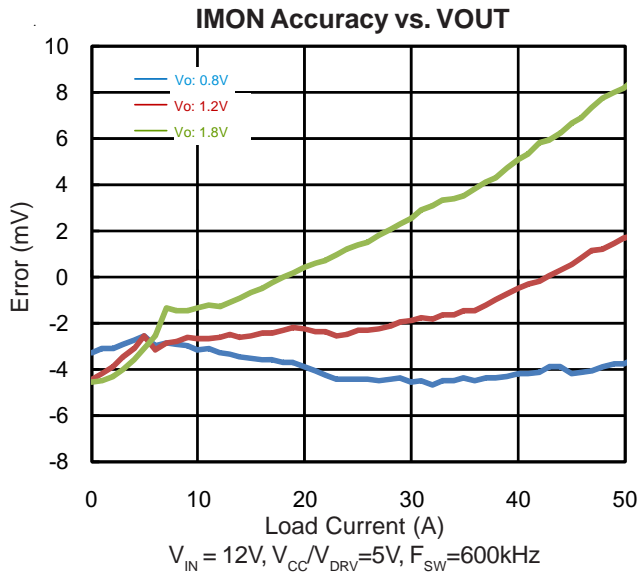


Timing Diagram

Typical Operation Characteristics

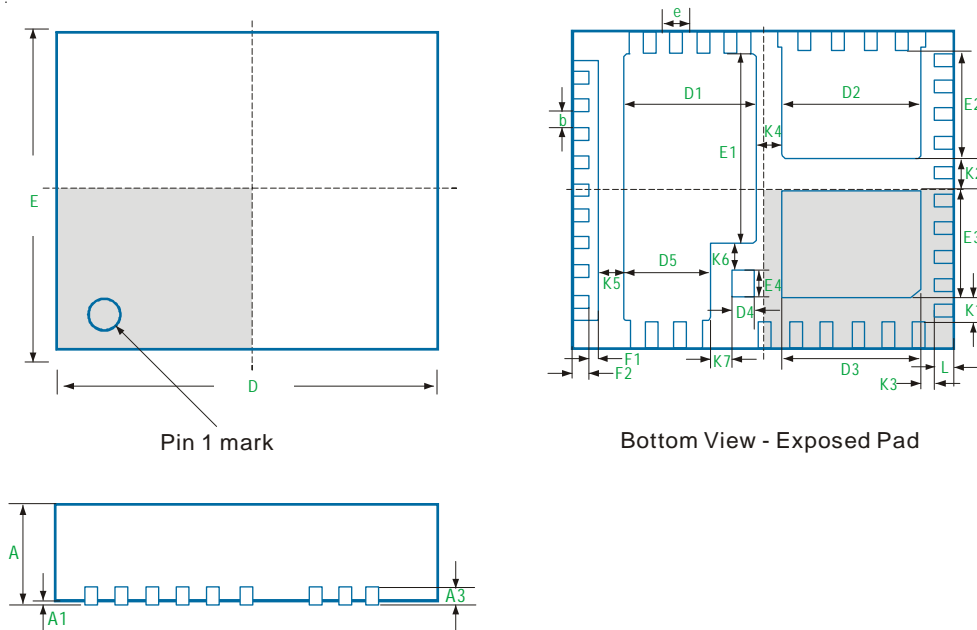


Typical Operation Characteristics



Package Information

VQFN6X5 - 39L Package



SYMBOLS	Dimension (mm)			SYMBOLS	Dimension (mm)			SYMBOLS	Dimension (mm)		
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX
A	0.800	0.900	1.000	D5	1.300	1.400	1.500	F2	0.275 BSC		
A1	0.000	0.020	0.050	E	5.000 BSC			K1	0.350 BSC		
A3	0.200 REF			E1	3.022	3.122	3.230	K2	0.400 BSC		
b	0.200	0.250	0.300	E2	1.718	1.818	1.925	K3	0.350 BSC		
D	6.000 BSC			E3	1.650	1.750	1.850	K4	0.400 BSC		
D1	2.000	2.100	2.200	E4	0.450 BSC			K5	0.400 BSC		
D2	1.850	1.950	2.050	e	0.450 BSC			K6	0.400 BSC		
D3	1.850	1.950	2.050	L	0.300	0.400	0.500	K7	0.400 BSC		
D4	0.300 BSC			F1	0.125 BSC						

Note

1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

NOM: Nominal. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

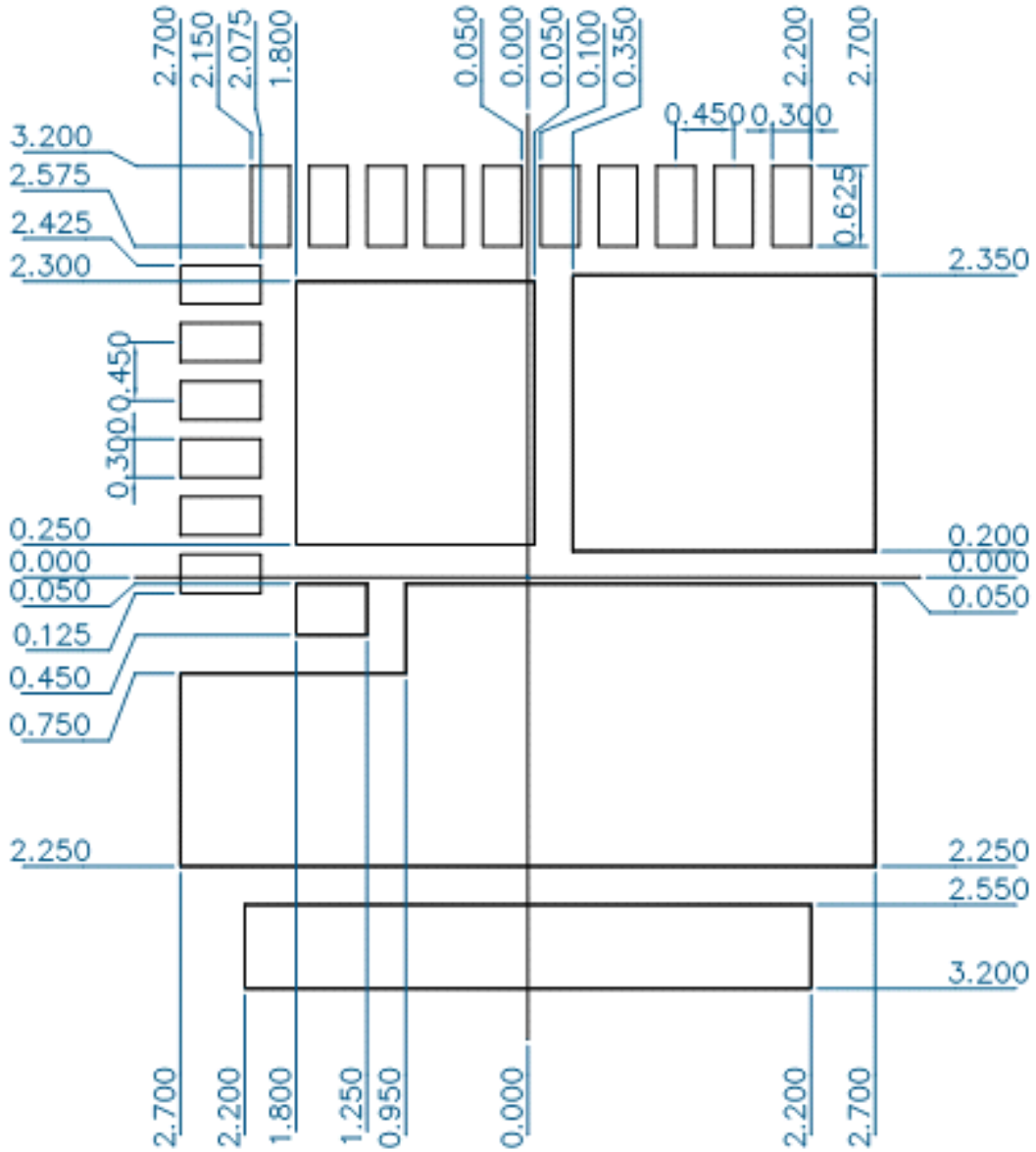
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

5. There are tie bars exposed on package side wall and the exposed position are inconsistent depending on different vendors.

uP9642B

Package Information

Recommended PCB Land Pattern



Note

- 1. Dimensions in Millimeters.
- 2. Drawing not to scale.

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