uP9646B

Driver Integrated High Current 30V Power Stage Module

General Description

The uP9646B is a driver integrated 30V power stage module for multi-phase synchronous buck DC-DC converter in desktop and notebook applications. The device is operated with 5V input for integrated MOSFET driver, and its MOSFETs are fully optimized to deliver up to 50A output current with high conversion efficiency for CPU, GPU and DDR memory power supplies. This part features Intel® PS4 mode support, thermal warning, over current protection, and zero current detection functions. The thermal warning output is used by system to secure safety operation. The over current protection function of the device further enhances protection for the converter. The zero current detection function provides more application flexibility. The uP9646B also provides comprehensive protection functions, including under voltage lockout for VCC/VDRV, and over temperature protection. The uP9646B is available with a compact WQFN 5x5-31L package.

Features

- **Capable of Delivering Continuous Current up to 50A, Peak Current Up to 120A(10us) and 80A (10ms)**
- **Switching Frequency up to 2MHz**
- **Support Intel® PS4 Low Power Mode**
- **Input Voltage V_{IN} Range: 2.5V to 25V**
- **VCC and VDRV Supply Input Range: 4.5V to 5.5V**
- **Compatible with 3.3V / 5V PWM Logic with Tri-State Input**
- **Support PWM Resistor Strap Setting Application**
- **Integrated 5V MOSFET Driver and 30V MOSFETs**
- **VCC / VDRV Under Voltage Lockout (UVLO)**
- **Over Current Protection**
- **Thermal Warning Function**
- **Over Temperature Protection**
- **Zero Current Detection (ZCDEN#) Control for Diode Emulation / CCM Operation**
- **Low Profile WQFN5x5-31L Package**
- **RoHS Compliant and Halogen Free**

Applications

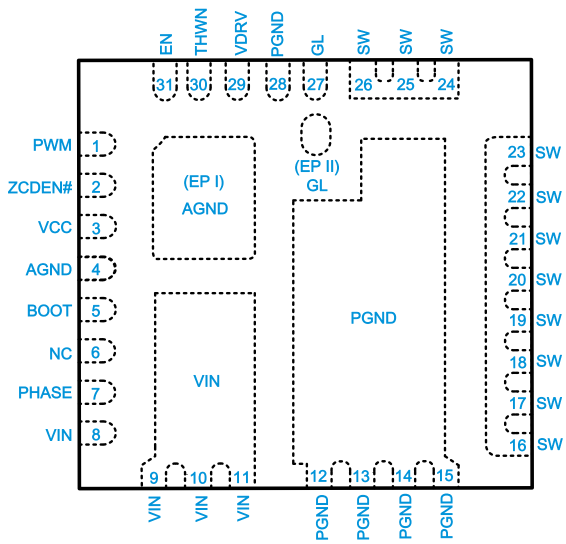
- **Desktop Computers**
- **Notebook Computers**
- **Graphic Cards**
- **High Frequency, Low Profile Buck DC-DC Converters**
- **Voltage Regulator for CPUs and DDR Memory Arrays**

Ordering Information

Order Number	Package Type	Top Marking
uP9646BQDBA	WQFN5X5-31L	uP9646B

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

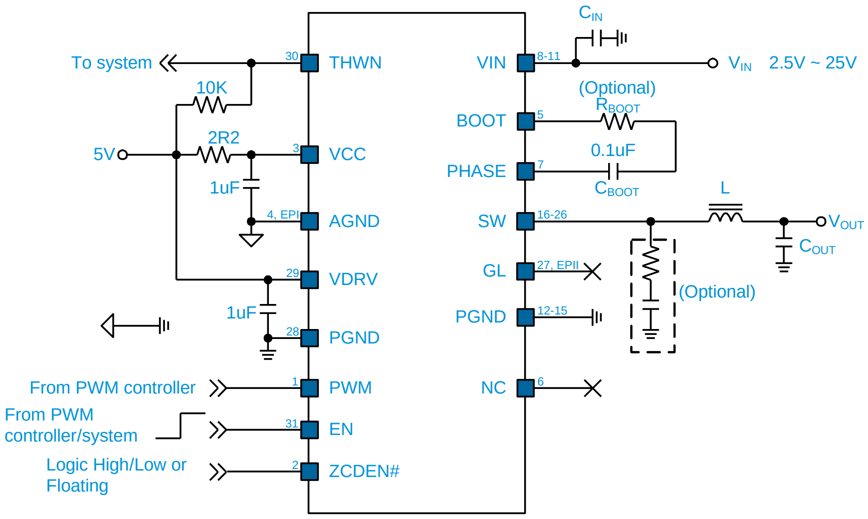


(Top View)

Copyright© uPI Semiconductor Corp. All Rights reserved.

uP9646B

Typical Application Circuit



Copyright© uPI Semiconductor Corp. All Rights reserved.

Functional Pin Description

Pin No.	Name	Pin Function
1	PWM	**PWM Input.** This pin receives logic level input and controls the on/off state of the embedded MOSFETs. The PWM pin is in high impedance state if EN input is low. When EN input is high, the PWM pin voltage will be pulled to tri-state by device internal circuit. The resistor connected from PWM pin to AGND for PWM controller function setting (if needed) must be greater than 15kΩ. Logic high input to PWM pin turns high-side MOSFET on. Tri-state input (floating) to PWM pin turns both high-side and low-side MOSFETs off. Logic low input to PWM pin turns the low-side MOSFET on.
2	ZCDEN#	**Zero Current Detection Enable Control**. Active Low. This pin controls the enable/disable of zero current detection function, hence the operation mode of the device. Note that it is active low, which means when ZCDEN# is logic low, low-side MOSFET is turned off for diode emulation operation. When ZCDEN# is logic high, continuous conduction mode (CCM) is forced. Note that there is an internal pull−up resistor 450kΩ from ZCDEN# to VCC to let the device operate in CCM by default when ZCDEN# is floating.
3	VCC	**Supply Input for Logic Control Circuit.** Connect this pin to a 5V voltage source with an RC filter to AGND. It is recommended to use 1uF minimum MLCC between VCC and AGND (pin 4) and place it as close to the pin as possible.
4	AGND	**Analog Signal Ground.** AGND is the reference ground of VCC and parameter setting pins, such as EN, PWM, ZCDEN# and THWN. Connect AGND to the ground of the PCB near the device. Pin 4 is internally connected to pad EPI.
5	BOOT	**Bootstrap Supply.** This pin is the supply input for the embedded high-side MOSFET gate driver. Connect a bootstrap capacitor C_{BOOT} between BOOT pin and PHASE pin. Use 0.1uF minimum MLCC as C_{BOOT}, and place it close to the device. The bootstrap capacitor provides the charge to turn on the high-side MOSFET.
6	NC	**Not Internally Connected.** This pin needs to be left floating in application.
7	PHASE	**Return Path for BOOT Capacitor.** For bootstrap capacitor connection only. Connect a bootstrap capacitor C_{BOOT} between this pin and BOOT pin. This pin is connected to SW internally.
8-11	VIN	**Supply Voltage for Power Stage**. These pins are the input to power stage. Apply 2.5V to 25V as the input voltage V_{IN}.
12-15	PGND	**Power Ground for Power Stage High Current Path.** These pins are the ground of the power stage, namely the power ground of the low-side MOSFET. Connect these pins to the large PCB area and connect to ground with multiple via to maximize heat dissipation.
16-26	SW	**Switch Node.** Switching node of internal high-side and low-side MOSFETs. Connect to the external inductor. The SW voltage is also monitored for over current protection and zero current detect function.

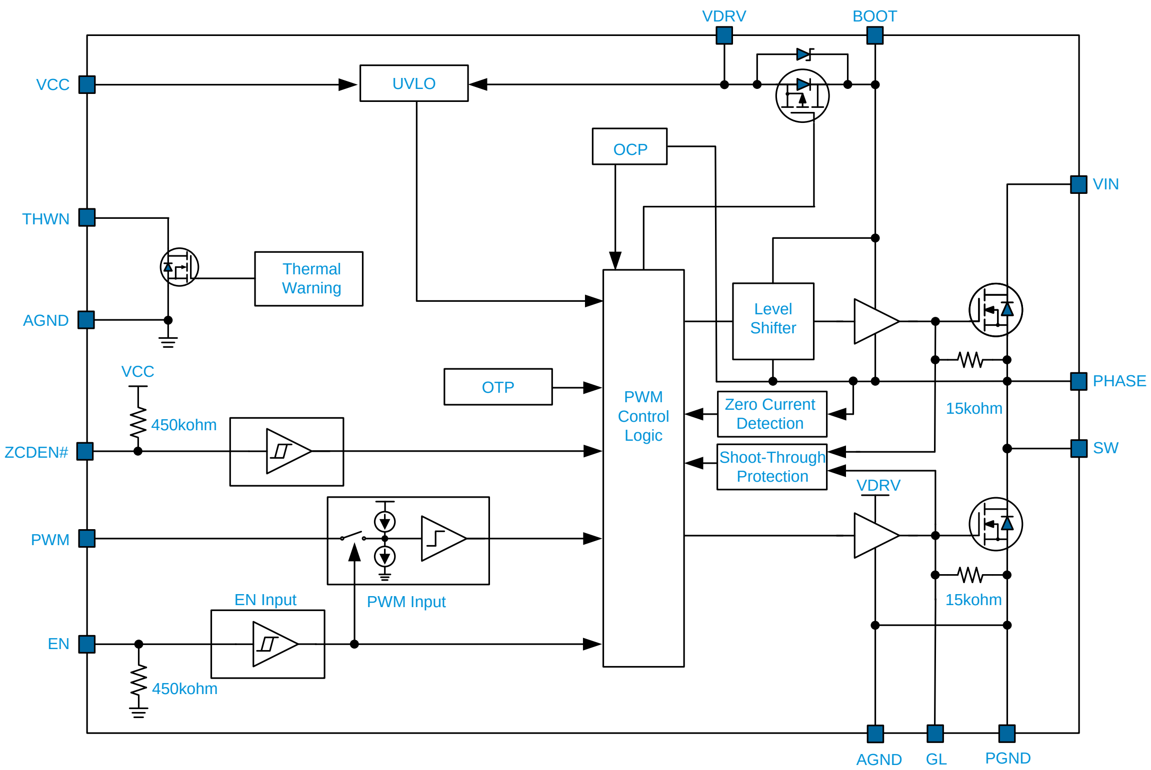
Copyright© uPI Semiconductor Corp. All Rights reserved.
www.upi-semi.com

Functional Pin Description

Pin No.	Name	Pin Function
27	GL	**Lower Gate Driver Output.** This pin is the gate of low-side MOSFET, and it is used for signal monitoring only. Leave this pin floating. Pin 27 is internally connected to pad EPII.
28	PGND	**Ground for MOSFET Driver VDRV.** This pin is the return path for the MOSFET driver supply input VDRV. Connect a capacitor directly between VDRV and this pin. This pin is internally connected to other PGND pins.
29	VDRV	**Supply Input for MOSFET Driver.** Connect this pin to a 5V voltage source. It is recommended to use 1uF minimum MLCC between VDRV and PGND (pin 28) and place it as close to the pin as possible.
30	THWN	**Thermal Warning Indicator.** This pin is an open−drain output. When the temperature of the driver die reaches the thermal warning threshold, this pin is pulled low as the warning flag signal to the system for the over heating condition. Note that even if THWN is pulled low, the PWM switching operation remains.
31	EN	**Enable Control.** Logic input to this pin controls the enable/disable state of the device. Logic high input to EN pin enables the device, and the device requires a maximum 15us power up delay time. Logic low input to EN pin disables the device, and the device enters ultralow quiescent current mode. Note that there is a weak pull low resistor 450kΩ internal to the EN pin to avoid inadvertent enable of the device.
EPI	AGND	**Analog Signal Ground.** AGND is the reference ground of VCC and parameter setting pins, such as EN, PWM, ZCDEN# and THWN. Pad EPI is internally connected to pin 4. Connect AGND to the ground of the PCB underneath the device with multiple via.
EPII	GL	**Lower Gate Driver Output.** This pin is the gate of low-side MOSFET, and it is used for signal monitoring only. Leave this pin floating. Pad EPII is internally connected to Pin 27.

Copyright© uPI Semiconductor Corp. All Rights reserved.
www.upi-semi.com

Functional Block Diagram



Copyright© uPI Semiconductor Corp. All Rights reserved.

Functional Description

The uP9646B is a driver integrated power stage, which is optimized to achieve high conversion efficiency to meet the high current demanding application of multi-phase synchronous buck converter for CPU/GPU/DDR memory power supplies. This device integrates MOSFET driver and 30V MOSFETs within a compact WQFN5x5 package, capable of delivering 50A continuous current, capable of operating at up to 2MHz switching frequency. The space-saving package, high current capability, high switching frequency and high conversion efficiency makes this device ideal for modern CPU/GPU core voltage regulator in desktop and notebook applications. This part features Intel® PS4 mode support, thermal warning, over current protection, and zero current detection functions. It also provides comprehensive protection functions, including under voltage lockout for VCC/VDRV, and over temperature protection. Each feature and other functions are described in the following sections.

VCC/VDRV Power on Reset and Under Voltage Lockout

The uP9646B has three power inputs, VCC, VDRV and VIN. VCC is the supply power for logic control circuit of the device, and VDRV is the supply power for MOSFET driver. VIN is the supply power for the MOSFETs. Both VCC and VDRV inputs are monitored for power on reset (POR) function. Once VCC and VDRV rises across the POR rising threshold, the device waits for EN input to operate. After EN is high, the device operates per PWM input state. When VCC or VDRV falls below the POR threshold, an under voltage lockout condition is detected, and then both the high-side and low-side MOSFETs are off regardless of the PWM and EN input state. Unlike VCC and VDRV, the VIN input is not monitored for power on reset function.

Enable Control and PWM Resistor Strap Setting Support

The EN pin controls enable/disable state of the device. Logic low input to EN pin disables the device. Both high-side and low-side MOSFETs are turned off (the gate of high-side MOSFET and GL are kept low), and the PWM pin is in high input impedance state. Logic high input to EN pin enables the device. As shown in Figure 1, the internal MOSFET gate drivers are enabled after a delay time T_{PDHDEN}. During this delay time period, the PWM pin stays at high input impedance state, the internal control circuit does not respond to the PWM input, and both the MOSFETs are kept off. When T_{PDHDEN} is expired, the device weakly drives the PWM to tri-state voltage level. After that, the device begins to respond to the PWM input. This mechanism is specifically designed to support the PWM resistor strap setting function from some of the uPI's PWM controllers, which use its PWM pin as a multi-functional pin.

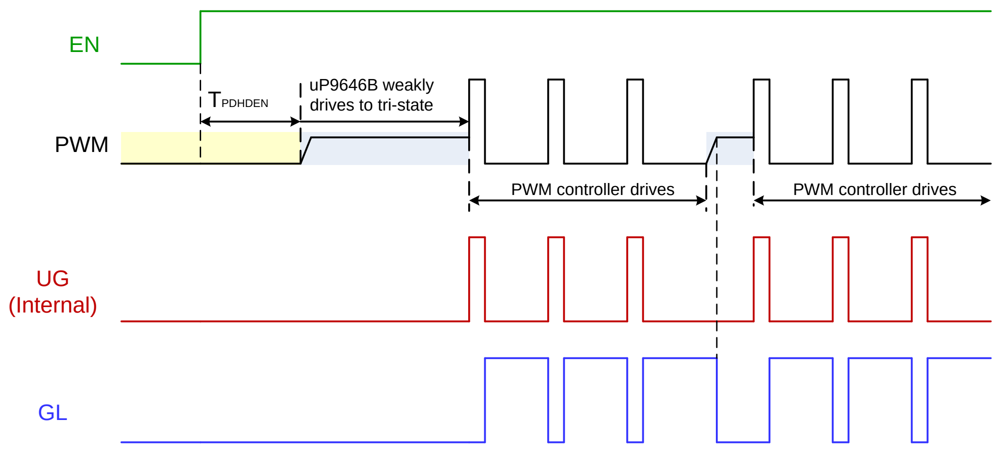


Figure 1. Enable Control

Copyright© uPI Semiconductor Corp. All Rights reserved.
www.upi-semi.com

Functional Description

PS4 Low Power Mode (Deep-Sleep Mode)

The uP9646B supports Intel® PS4 mode. When the PWM controller receives the PS4 command, the voltage regulator enters PS4 state, all PWMs are in tri-state and normally the EN of power stage module is logic low. As for uP9646B, when its VCC and VDRV are ready but EN is pulled low, the device enters deep-sleep mode for power saving. The switching stops immediately, both the high-side and low-side MOSFET are turned off (the gate of high-side MOSFET and GL are kept low), and the PWM pin is in high input impedance state. Most of the logic circuit of the device is shutdown to lower the VCC supply current to less than 15uA to minimize the power consumption as the multi-phase voltage regulator is in PS4 state. When the PWM controller exits the PS4 state, the EN input of power stage module goes back to logic high. The power stage module is enabled again and starts to respond to the PWM signal from controller after a maximum 40us delay time.

3.3V/ 5V Three-Level PWM Input

The uP9646B is compatible with standard 3.3V and 5V PWM logic with tri-state input to accommodate most of the PWM controllers. Once the POR of VCC/VDRV is granted and EN is high, the device start to operate according to the PWM input state. When logic input to PWM pin is high, it turns on the high-side MOSFET and turns off the low-side MOSFET. When logic input to PWM pin is low, it turns off the high-side MOSFET and turns on the low-side MOSFET. If the input to PWM pin is floating, the internal circuit weakly drives the PWM pin voltage into the tri-state region to turn off both the two MOSFETs. The PWM pin voltage is kept around 1.5V by internal bias circuit when floating. Since the device supports PWM resistor strap setting application, the resistor connected from PWM pin to AGND for PWM controller function setting (if needed) must be greater than 15kΩ to ensure normal operation.

Zero Current Detection Control (ZCDEN#)

The uP9646B features zero current detection function to support device-controlled diode emulation mode, which is determined by ZCDEN# pin. When the input to ZCDEN# pin is logic low, the zero current detection function is enabled. The device monitors SW voltage for zero current detection. As shown in Figure 2, the PWM input signal turns to tri-state after its high state expired, and then GL goes high to turn on the low-side MOSFET to let inductor current to decrease. When the zero current condition is detected while PWM input voltage is in tri-state level, GL goes low to turn off the low-side MOSFET for diode emulation operation. This diode emulation operation is controlled by the power stage module, not by the PWM controller. To use this device-controlled diode emulation mode, the companion PWM controller needs to actively drive the PWM voltage to tri-state level to support this specific PWM switching behavior as the zero current detection is determined by the power stage module.

When the input to ZCDEN# pin is logic high, the device executes continuous conduction mode (CCM), which is most of the applications in multi-phase buck converter. ZCDEN# can be left floating if zero current detection function is not used. There is an internal pull−up resistor 450kΩ from ZCDEN# to VCC to let the device operate in CCM by default when ZCDEN# is floating. Table 1 lists the complete logic input states of EN, ZCDEN#, PWM and the corresponding driver output conditions.

Copyright© uPI Semiconductor Corp. All Rights reserved.

Functional Description

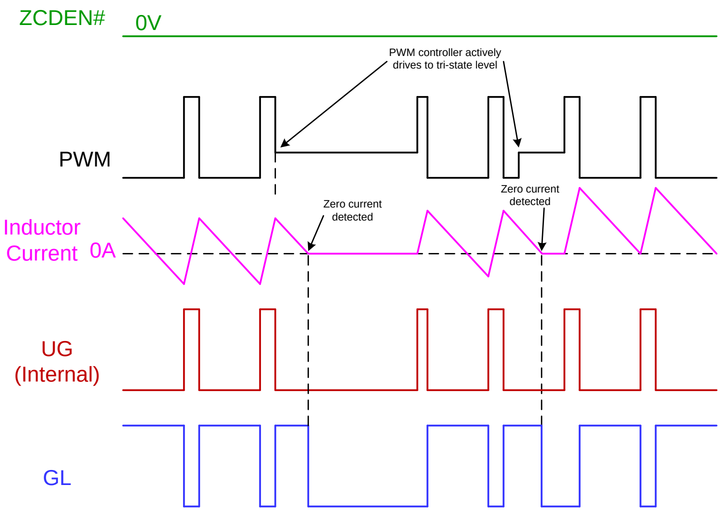


Figure 2. PWM Control with Zero Current Detection Enabled

Table 2. Device Logic Truth Table

EN	ZCDEN#	PWM	UG (internal signal)	GL
H	H	H	H	L
		Tri-state	L	L
		L	L	H
H	L	H	H	L
		H->Tri-state	L	H, if I_L >0 L, if I_L <0
		L->Tri-state	L	H, if I_L >0 L, if I_L <0
		L	L	H
L	X	X	L	L
Note: H=high, L=low, Tri-state=floating, I_L=inductor current				

Bootstrap Circuit

An integrated bootstrap switch and an external bootstrap capacitor form a charge pump circuit, which supplies voltage to the BOOT pin for driving the high-side MOSFET of the device. The bootstrap switch is integrated such that only an external capacitor is necessary to complete the bootstrap circuit. Connect a minimum 0.1uF MLCC as bootstrap capacitor C_{BOOT} in series with an optional resistor 1~3.3Ω from BOOT pin to PHASE pin. The PHASE pin is for bootstrap capacitor connection only, and it is connected to SW internally. To ensure that uP9646B operates normally under DCM (discontinuous conduction mode), it is recommended that the maximum output voltage should not exceed 1.6V.

Copyright© uPI Semiconductor Corp. All Rights reserved.

Functional Description

Shoot Through Protection

The shoot through protection circuit prevents the high-side MOSFET and low-side MOSFET from being turned on simultaneously and conducting destructive large current. This operation is done by turning on one MOSFET only after the other MOSFET is off already with adequate delay time. At the high-side MOSFET off edge, UG (internal) and PHASE voltages are monitored for anti-shoot-through protection. The low-side MOSFET driver (GL) will not begin to output high until both (V_{UG} – V_{PHASE}) and V_{PHASE} are lower than a threshold V_{TH}, making sure the high-side MOSFET is turned off completely. At the low-side off edge, GL voltage is monitored for anti-shoot-through protection. The high-side MOSFET driver will not begin to output high until V_{GL} is lower than a threshold voltage V_{TH}, ensuring the low-side MOSFET is turned off completely.

Over Current Protection

The uP9646B features over current protection function, which protects the device from over current condition. The SW voltage is monitored for the over current protection (OCP). When the inductor valley current exceeds the over current protection level, the device will protect the integrated power MOSFETs by forcing an early termination of the high-side MOSFET conduction time. That is, the PWM cycle is skipped as the PWM high state of that cycle is masked. While the PWM high state is masked, the high-side MOSFET is off, and the inductor current keeps decreasing as the low-side MOSFET is on. For next PWM cycle, the device allows its high-side MOSFET to turn on only when the inductor valley current falls below the OCP threshold. In this fashion, the inductor valley current is well limited so as to provide over current protection to the device.

Thermal Warning Function

The uP9646B features thermal warning function, which is a flag signal to indicate that the device is in over heating condition. The THWN pin is an open drain output, and it requires a pull-up resistor to VCC. When the temperature of the driver die exceeds the thermal warning threshold T_{THWN} 120^{o}C, THWN is pulled low for thermal warning. At this point, the device continues to function. The device responds to the PWM input normally. In general, the system responds to the THWN and takes action to decrease the load current of the multi-phase voltage regulator. As the load current decreases, the temperature of the device also decreases. The thermal warning function has a hysteresis. Once thermal warning is triggered, the THWN pin goes back to high when the temperature of the driver die drops T_{THWN_HYS} below T_{THWN}. If the driver die temperature exceeds T_{OTP} 145 ^{o}C, the device enters thermal shutdown and both MOSFETs are turned off. Once the temperature drops to T_{OTP_HYS} below T_{OTP}, the part resumes normal operation.

Over Temperature Protection

The uP9646B has over temperature protection (OTP). When the temperature of driver IC goes above the rising threshold 145^{o}C (the temperature of the high-side MOSFET may reach up to 165 ^{o}C), the driver turns off both the two MOSFETs regardless of the PWM input. The over temperature protection has a hysteresis. Once OTP is tripped, the device resumes PWM switching when the temperature of driver IC falls below 120^{o}C (the temperature of high-side MOSFET approximately falls below 140^{o}C).

Copyright© uPI Semiconductor Corp. All Rights reserved.

Absolute Maximum Rating

(Note 1)

VCC/VDRV/EN/PWM -- -0.3V to +6V
VIN -- -0.3V to +30V
BOOT to PHASE
DC -- -0.3V to +6V
< 100ns -- -0.3V to +6.6V
< 10ns -- -0.3V to +7.5V
VIN to SW
DC -- -0.3V to +30V
< 100ns -- -8V to +33V
SW to GND
DC -- -0.3V to +30V
< 100ns -- -8V to +33V
PHASE to GND
DC -- -0.3V to +30V
< 100ns -- -6V to +33V
BOOT to GND
DC -- 0V to (VDRV+30V)
< 100ns -- -5V to +36V
GL to GND
DC -- -0.3V to +6V
< 100ns -- -2V to +6.6V
Storage Temperature Range -- -55°C to +150°C
Junction Temperature -- 150°C
Lead Temperature (Soldering,10 sec) -- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) -- 2kV
CDM (Charged Device Mode) -- 1kV

Thermal Information

Package Thermal Resistance (Note 3)
VQFN5x5-31L θ_{JA} -- 22°C/W
VQFN5x5-31L $\theta_{J\text{-}PCB}$ -- 2.2°C/W
VQFN5x5-31L $\theta_{J\text{-}TOP}$ -- 7.6°C/W

Recommended Operation Conditions

(Note 3)

Operating Junction Temperature Range -- -40°C to +125°C
Operating Ambient Temperature Range -- -40°C to +85°C
VIN -- 2.5V to 25V
VCC/VDRV -- 4.5V to 5.5V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Copyright© uPI Semiconductor Corp. All Rights reserved.

Electrical Characteristics

VCC=VDRV = 5V (T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCC Supply Power						
VCC Supply Current	I_{VCC_ENH}	EN=5V, PWM=400kHz,duty=15%	--	1	2	mA
	I_{VCC_ENF}	EN=5V, PWM=floating	--	--	2	
PS4 Mode Supply Current	I_{VCC_ENL}	EN=0V, ZCDEN#=VCC	--	--	5	uA
		EN=0V, ZCDEN#=GND	--	15	--	
VCC POR Threshold	V_{CCRTH}	VCC rising	3.8	4	4.2	V
VCC POR Hysteresis	V_{CCHYS}		--	0.25	--	V
VDRV Supply Current	I_{VDRV_ENH}	EN=5V,PWM = 400kHz,duty=15%	--	20.5	--	mA
	I_{VDRV_ENF}	EN=5V, PWM=floating	--	14	--	uA
	I_{VDRV_ENL}	EN=0V	--	--	1	uA
VDRV POR Threshold	V_{DRVRTH}	V_{DRV} rising	3.8	4	4.2	V
VDRV POR Hysteresis	V_{DRVHYS}		--	0.25	--	V
EN Input						
Input Resistance		Pull-low resistance to GND	--	450	--	kΩ
Input High	V_{ENH}		2	--	--	V
Input Low	V_{ENL}		--	--	0.8	V
Enable Delay Time (for PS4 SPEC.)						
Enable Delay Time	T_{PDHDEN}	PWM=0. Measured from EN rising edge to GL>1V.	--	--	40	us
Disable Delay Time	T_{PDLDEN}	PWM=0. Measured from EN falling edge to GL<4V.	--	1.3	--	us
ZCDEN#						
Input Voltage High	$V_{ZCDEN\#\_H}$		2	--	--	V
Input Voltage Low	$V_{ZCDEN\#\_L}$		--	--	0.8	V
Input Resistance		Pull-up resistance to VCC	--	450	--	kΩ
Zero Cross Detect Threshold	V_{ZCD}		--	0	--	mV
ZCD Blanking + De-bounce Time	T_{BLNK}		--	230	--	ns
Thermal Warning						
Thermal Warning	T_{THWN}	Guarantee by design	--	120	--	°C
Thermal Warning hysteresis	T_{THWN_HYS}	Guarantee by design	--	25	--	°C
THWN Pull-Down Resistance	R_{THWN}		--	13	--	Ω

Copyright© uPI Semiconductor Corp. All Rights reserved.

www.upi-semi.com

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWM Input						
PWM High Voltage	V_{IH_PWM}	PWM low to high or tri-state to high	2.6	--	--	V
PWM Low Voltage	V_{IL_PWM}	PWM high to low or tri-state to low	--	--	0.7	V
PWM Input Tri-State Window	V_{Tri}		1.2	--	2.2	V
Tri-State Open Voltage	V_{Tri_PWM}	PWM input floating	1.4	--	1.6	V
PWM Input Current	I_{PWM}	PWM=0V	--	-220	--	uA
		PWM=3.3V	--	220	--	
		PWM=5V	--	220	--	
PWM Input Bias Voltage			--	1.5	--	V
PWM Propagation Delay and Dead Time Range(Refer to Timing Diagram on P.13)						
PWM High Propagation Delay	$T_{PDLLGATE}$	PWM going high to GL going low VIH_PWM to 90% GL	--	20	--	ns
PWM Low Propagation Delay	$T_{PDLUGATE}$	PWM going low to SW going low VIL_PWM to 90% SW	--	20	--	ns
Tri-State to Turn-On Propagation Delay	$T_{PDTSGHH}$	PWM(from tri-state) going high to SW going high, VIH_PWM to 10% SW	--	15	--	ns
Tri-State to Turn-Off Propagation Delay	$T_{PDTSGLH}$	PWM(from tri-state) going low to GL going high, VIL_PWM to 10% GL	--	15	--	ns
Tri-State Shut-Off Delay	$T_{PDTSOFF}$	PWM (from low) going tri-state to GL going low, VIL_PWM to 90% GL	--	25	--	ns
PWM Propagation Delay and Dead Time						
GL Off to SW On Dead Time	$T_{PDHUGATE}$	GL=10% to SW=10%	--	20	--	ns
SW Off to GL On Dead Time	$T_{PDHLGATE}$	SW=10% to GL=10%	--	20	--	ns
Minimum SW Pulse Width	T_{MINSW}		--	25	--	ns
Internal Bootstrap Switch						
Forward Voltage	V_{FWD}	VDRV to BOOT, I_{BOOT} = 10mA, PWM = floating	--	500	--	mV
On Resistance	R_{SW}	VDRV to BOOT, I_{BOOT} = 10mA, PWM = 0V	--	15	--	Ω
Protection						
Over Current Protection	I_{OCP}		--	80	--	A
Over Temperature Protection	T_{OTP}	Guarantee by design	--	145	--	°C
Over Temperature Protection Hysteresis		Guarantee by design	--	25	--	°C

Copyright© uPI Semiconductor Corp. All Rights reserved.
www.upi-semi.com

Electrical Characteristics

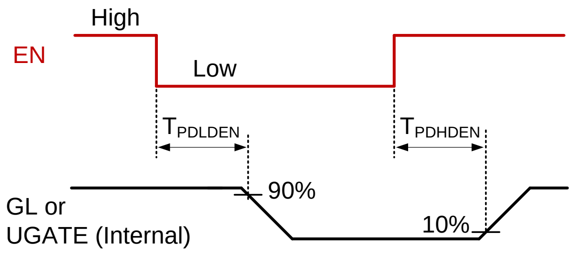


Figure 3. EN Control Input Timing Diagram

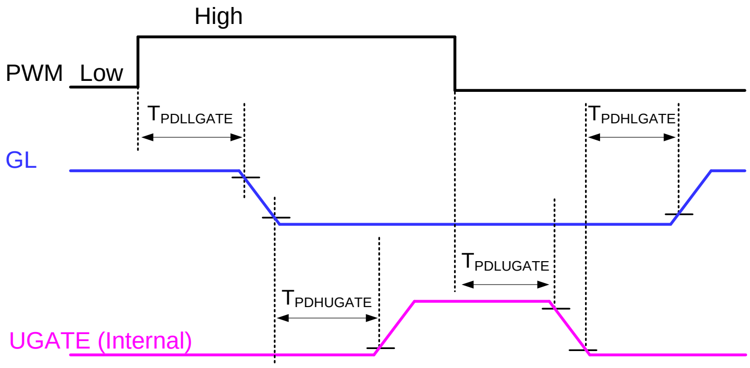


Figure 4. PWM Logic Input Timing Diagram

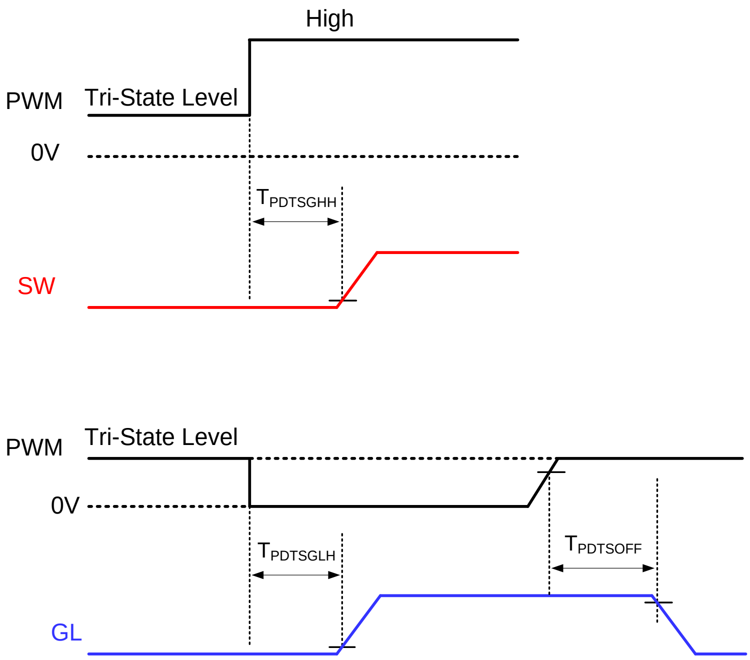
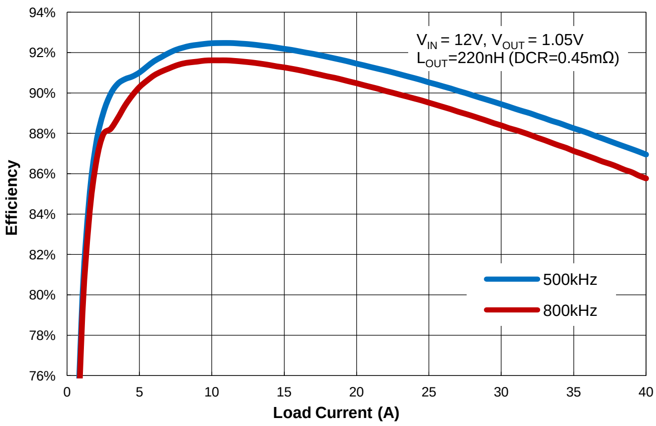


Figure 5. PWM Tri-state Input Timing Diagram

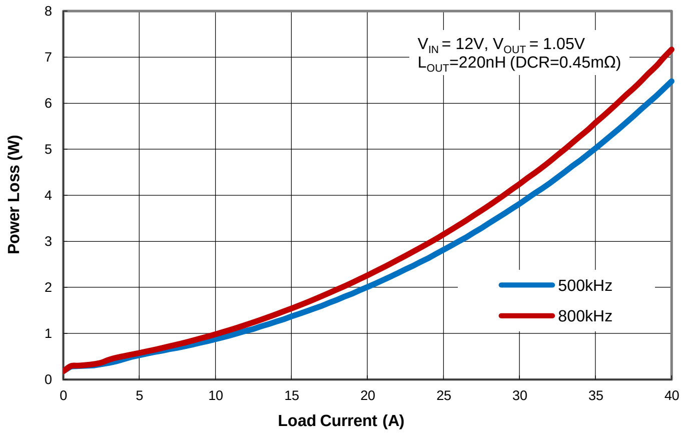
Copyright© uPI Semiconductor Corp. All Rights reserved.

Typical Operation Characteristics

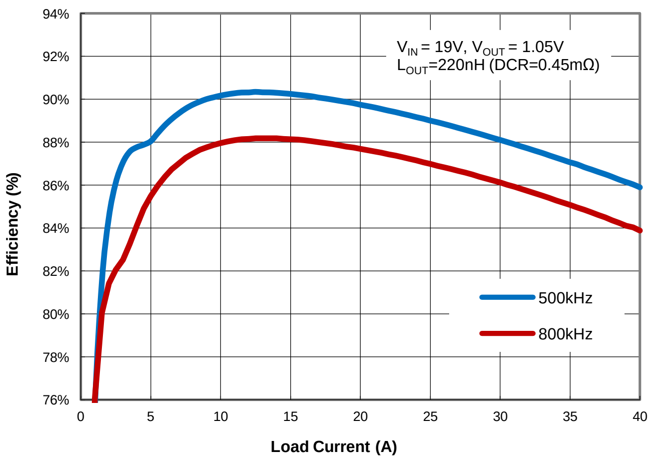
Efficiency vs. Load Current (12V Input, 1.05V Output)



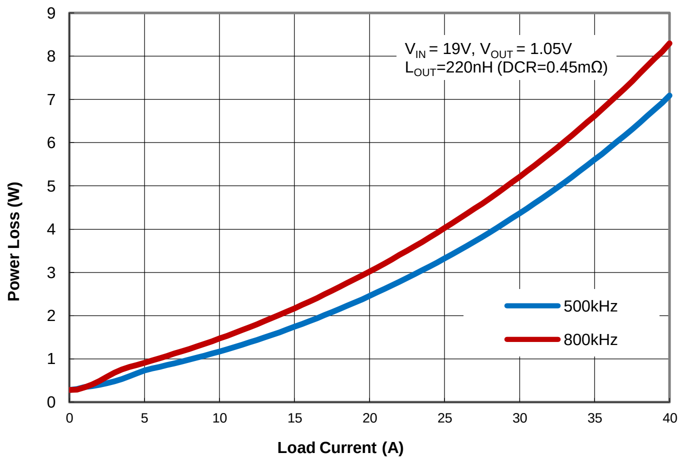
Power Loss vs. Load Current (12V Input, 1.05V Output)



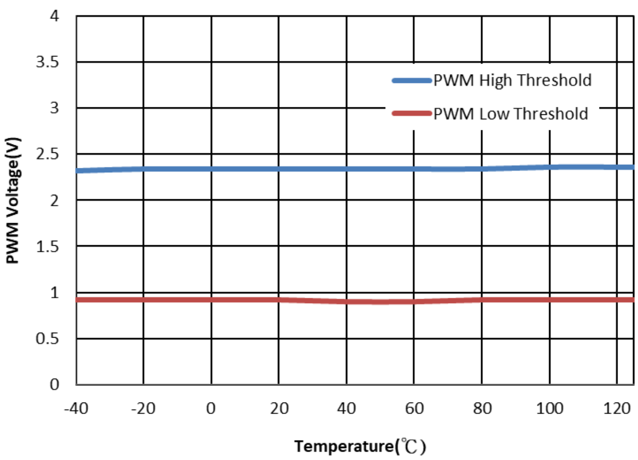
Efficiency vs. Load Current (19V Input, 1.05V Output)



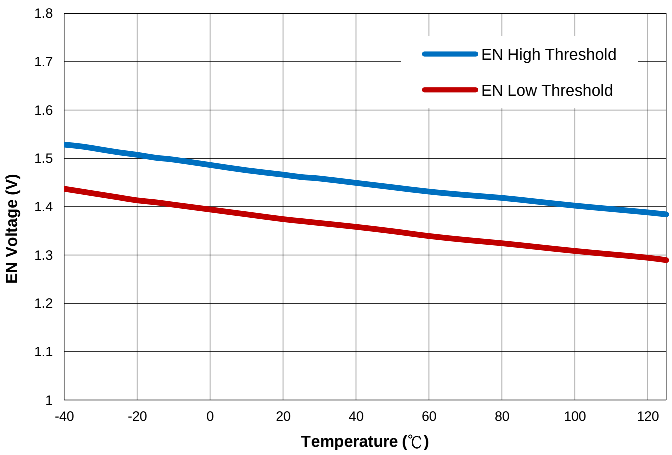
Power Loss vs. Load Current (19V Input, 1.05V Output)



PWM Threshold vs. Temperature



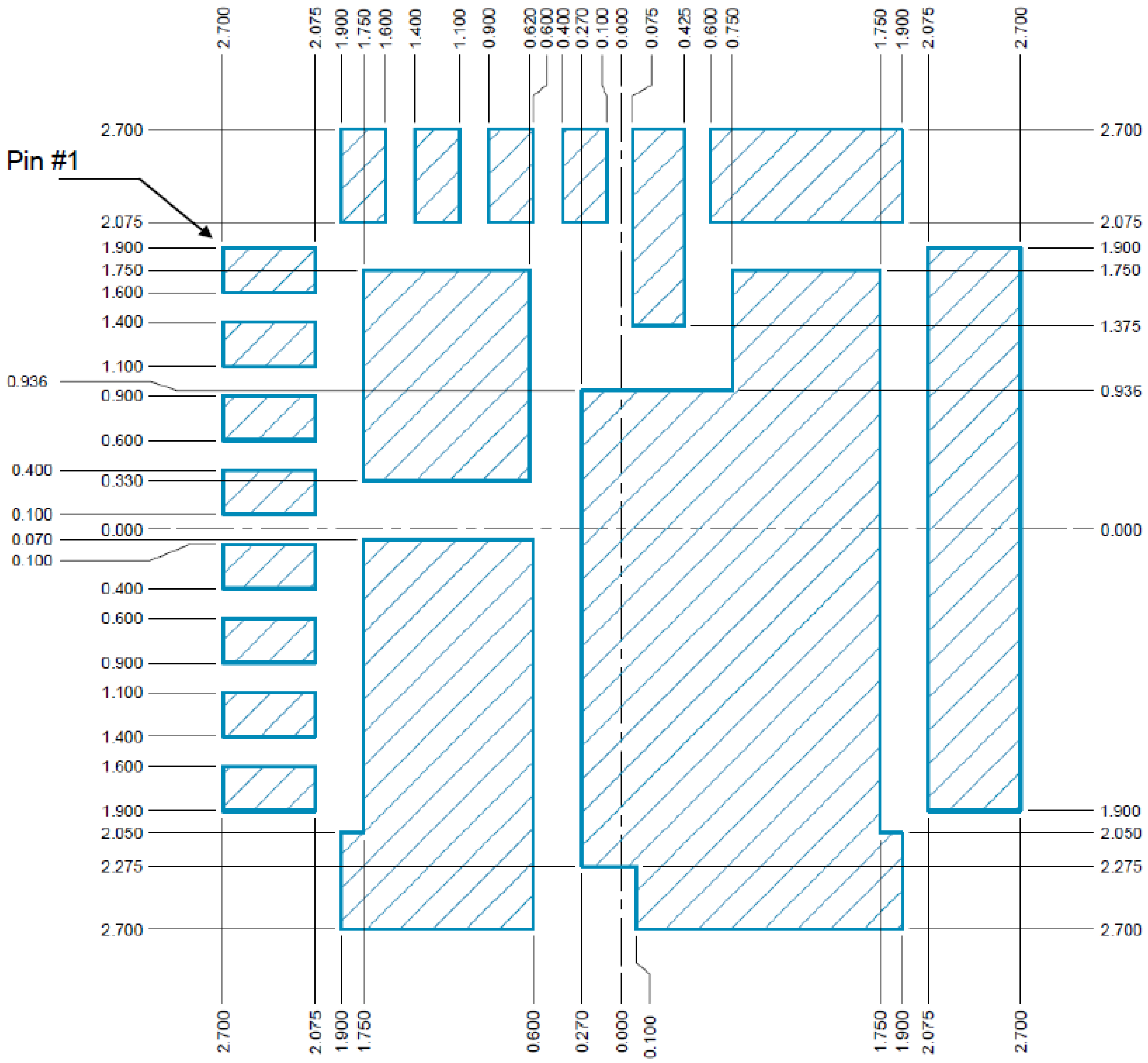
EN Threshold vs. Temperature



Copyright© uPI Semiconductor Corp. All Rights reserved.

Recommended Land Pattern

WQFN5x5-31L (Lead Pitch = 0.5mm)



Top View (unit: mm)

Note:

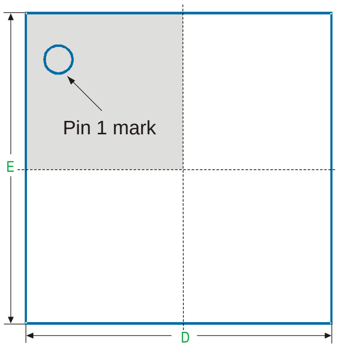
This PCB land pattern should serve as recommendation only. Other parameters may also affect soldering so this PCB land pattern does not guarantee absolute success.

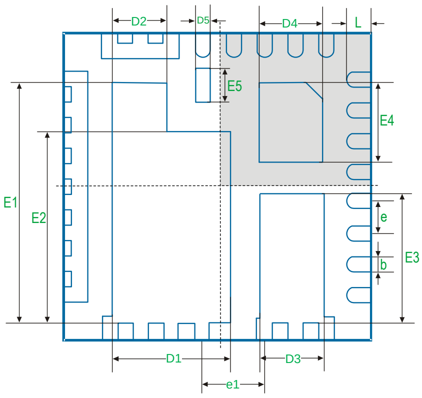
Copyright© uPI Semiconductor Corp. All Rights reserved.

www.upi-semi.com

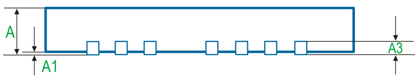
Package Information

WQFN5x5-31L





Bottom View - Exposed Pad



Symbol	Dimension (mm)			Symbol	Dimension (mm)		
	MIN	NOM	MAX		MIN	NOM	MAX
A	0.700	0.750	0.800	**E**	4.900	5.000	5.100
A1	0.000	--	0.050	**E1**	3.875	3.925	3.975
A3	0.200 REF			**E2**	3.061	3.111	3.161
b	0.200	0.250	0.300	**E3**	2.055	2.105	2.155
D	4.900	5.000	5.100	**E4**	1.270	1.320	1.370
D1	1.870	1.920	1.970	**E5**	0.500	0.550	0.600
D2	0.850	0.900	0.950	**e**	0.500 BSC		
D3	0.980	1.030	1.080	**e1**	1.000 BSC		
D4	0.980	1.030	1.080	**L**	0.300	0.400	0.500
D5	0.250	0.300	0.350				

Note

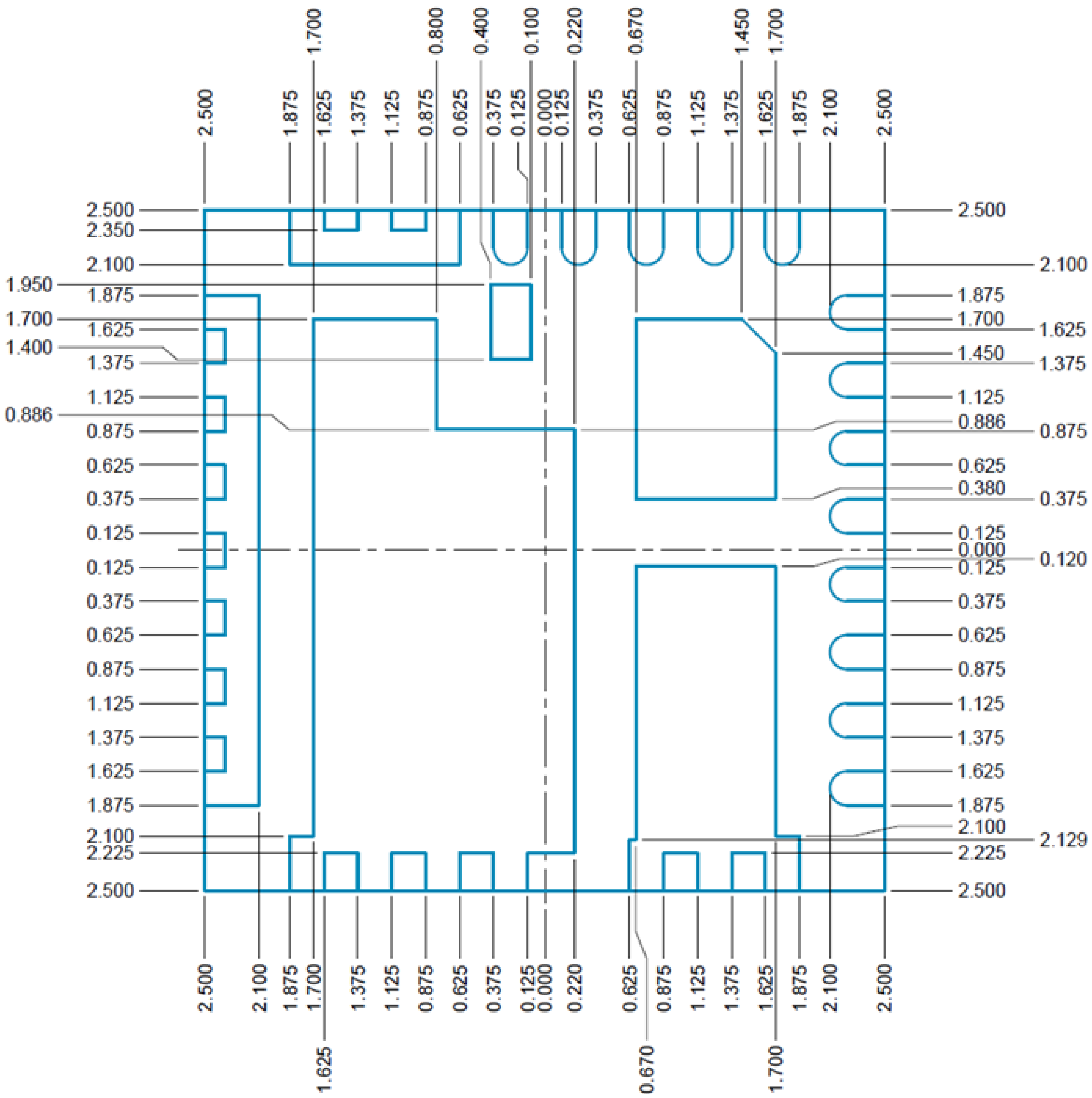
1. Package Outline Unit Description:
   MIN: Minimum dimension specified.
   NOM: Nominal. Provided as a general value.
   MAX: Maximum dimension specified.
   BSC: Basic. Represents theoretical exact dimension or dimension target.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Copyright© uPI Semiconductor Corp. All Rights reserved.

uP9646B

Package Information

Reference Dimension



Bottom View (unit: mm)

Copyright© uPI Semiconductor Corp. All Rights reserved.

Legal Notice

The contents of this document are provided in connection with uPI Semiconductor Corp. (“uPI”) products. uPI makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice.

No license, whether express, implied, arising by estoppels or otherwise, to any intellectual property rights, is granted by this publication. Except as provided in uPI’s terms and conditions of sale for such products, uPI assumes no liability whatsoever, and uPI disclaims any express or implied warranty relating to sale and/or use of uPI products, including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. uPI products are not designed, intended, authorized or warranted for use as components in systems intended for medical, life-saving, or life sustaining applications. uPI reserves the right to discontinue or make changes to its products at any time without notice.

Copyright 2023 ©, uPI Semiconductor Corp. All rights reserved.
uPI, uPI design logo, and combinations thereof, are registered trademarks of
uPI Semiconductor Corp.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

uPI Semiconductor Corp.
9F.,No.5, Taiyuan 1st St. Zhubei City, Hsinchu, Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888
sales@upi-semi.com

Copyright© uPI Semiconductor Corp. All Rights reserved.