uP9650

Smart Power Stage (SPS) with Integrated Current and Temperature Monitors

General Description

The uP9650 is a Smart Power Stage (SPS) solution with fully optimized, integrated driver and MOSFETs for high-current, high frequency, synchronous buck DC-DC converters. The SPS enables higher performance at lower output voltages required by cutting edge CPU, GPU and DDR memory voltage regulator design.

The uP9650 also enables advanced high accuracy module temperature reporting and on-chip synchronous MOSFET current monitoring. The protection includes cycle-by-cycle over current protection, phase fault detection, preliminary over voltage protection, VCC/VDRV UVLO protection, and thermal shutdown.

The uP9650 is optimized for CPU and GPU core power delivery. This device combined with a multi-phase buck PWM controller forms a complete core voltage regulator for advanced CPU and GPU.

Features

- **Input Voltage (VIN) Range: 4.5V to 22V**
- **VCC and VDRV Supply Range: 4.5V to 5.5V**
- **Up to 60A of Current Handling Capability**
- **Optimized Switching Frequency Up to 1MHz**
- **5mV/A On-Chip MOSFET Current Sensing**
- **8mV/°C Temperature Analog Output**
- **On-Chip MOSFET Temperature Compensation**
- **VCC/VDRV Under Voltage Lockout (UVLO)**
- **Thermal Shutdown and Fault Flag**
- **MOSFET Phase Fault Detection and Flag**
- **Cycle-by-Cycle Over Current Protection**
- **Preliminary Over Voltage (OV) Protection and Flag**
- **Compatible with 3.3V and 5V Tri-state PWM Input**
- **Deep-Sleep Mode for Power Saving**
- **VOS Output Voltage Sensing Input**
- **RoHS Compliant and Halogen Free**

Applications

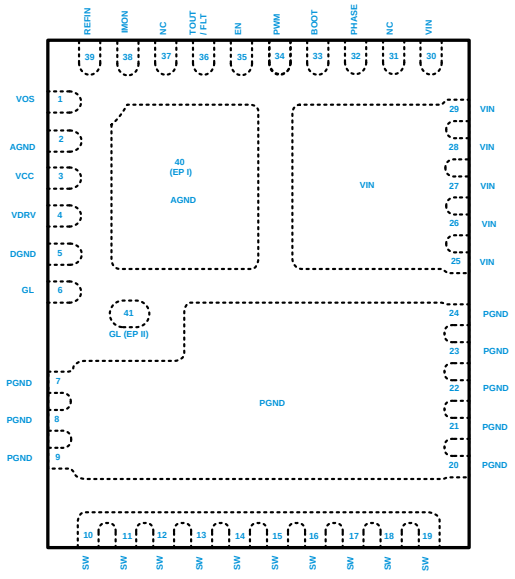
- **High Frequency, Low Profile DC-DC Converter**
- **Voltage Regulator for CPUs, GPUs, and DDR Memory Arrays**
- **Desktop Computers**
- **Notebook Computers**
- **Graphic Cards**

Ordering Information

Order Number	Package Type	Top Marking
uP9650AQR1	VQFN6x5-39L	uP9650A

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



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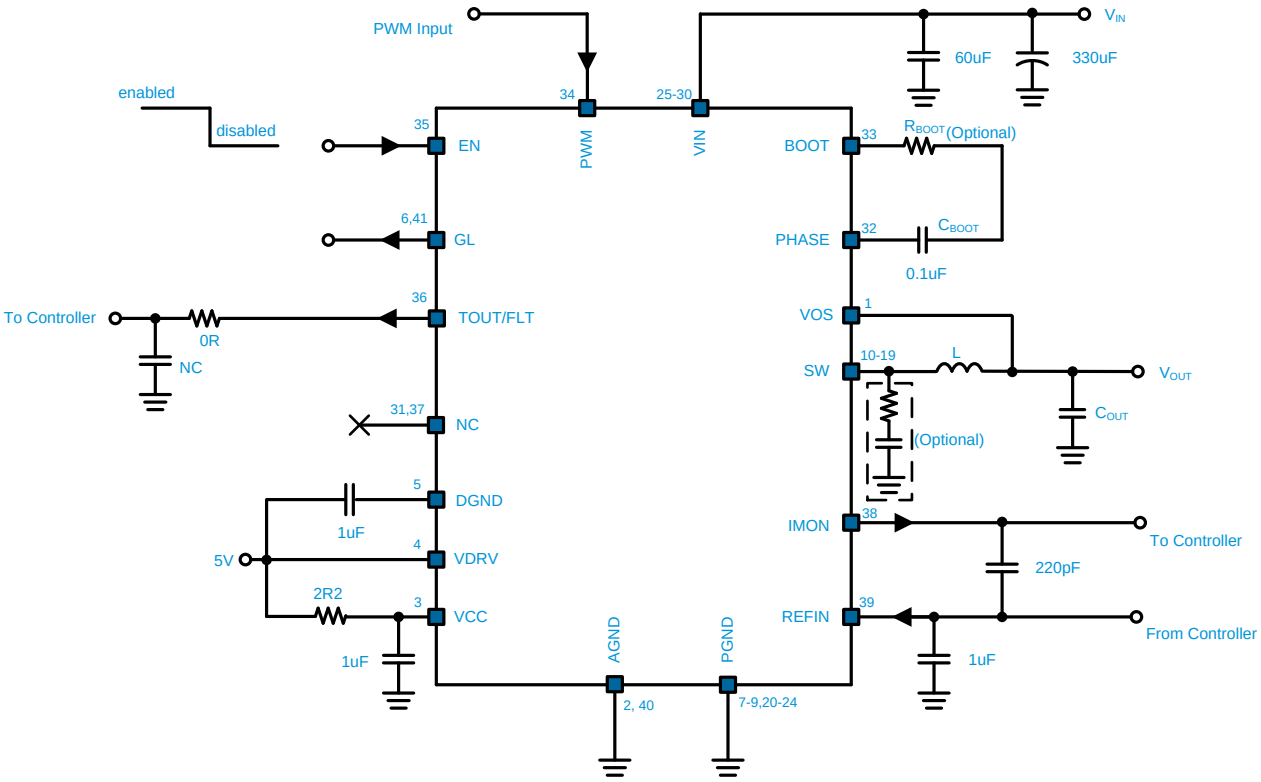
Typical Application Circuit



Functional Pin Description

Pin No.	Name	Pin Function
1	VOS	**VOUT Sense.** Output voltage sensing pin for current sensing application.
2	AGND	**Signal Ground.** All signals are referenced to this pin.
3	VCC	**Supply Voltage for the IC.** 5V supply voltage for internal control logic circuit. Connect a 1uF capacitor between VCC and AGND and place it as close to the pin as possible.
4	VDRV	**Driver Voltage Input.** 5V supply voltage for internal gate drivers. Connect a 1uF capacitor between VDRV and DGND and place it as close to the pin as possible.
5	DGND	**Driver Ground.**
7-9,20-24	PGND	**Power Ground.** It is also the power ground of the synchronous MOSFET.
6	GL	**Lower Gate Driver Output.** Synchronous MOSFET gate monitor pin enables the user to easily observe the waveform.
10-19	SW	**Switch Node.** Switching node of internal control/synchronous MOSFETs, and connects to the external inductor.
25-30	VIN	**Supply Voltage for the Power Stage.** 4.5V to 22V input voltage connection.
31,37	NC	**Do not connect to any circuit.** This pin must be left floating.
32	PHASE	**Switch Node.** For bootstrap capacitor connection only. It is connected to SW internally.
33	BOOT	**Bootstrap Supply.** Connect a minimum 0.1uF capacitor C_{BOOT} in series with an optional resistor of 1Ω~3.3Ω from BOOT to PHASE pin. The bootstrap capacitor provides the charge to turn on the control MOSFET.
34	PWM	**PWM Input.** Compatible with 3.3V/5V logic level PWM Input. PWM input: “High level” turns control MOSFET on; “Tri-state” turns both MOSFETs off; “Low level” turns the synchronous MOSFET on.
35	EN	**Enable Control.** Pulling EN high enables the driver and requires maximum 15us power up time; pulling EN low disables the driver and enters ultralow quiescent current mode. There is no internal pull-up or pull-down mechanism to this pin.
36	TOUT/FLT	**Temperature Sense Reporting/Fault Flag.** The voltage at this pin is defined by the equation: 8mV * (Temperature in Celsius of driver IC) + 0.6V. This pin will be pulled up to 3.3V internally under the following conditions: over temperature, over current, preliminary over voltage condition or phase fault condition.
38	IMON	**Current Sense Reporting.** Sensed current output signal referenced to the REFIN pin. V(IMON - REFIN) voltage represents current information at 5mV/A.

Functional Pin Description

Pin No.		Name	Pin Function
39		REFIN	**Reference Input.** External reference voltage input for the IMON function. This pin has a low bias current and can be tied to a fixed voltage (1.2V recommended) between 1.1V and 1.8V from a PWM controller.
40	EP I	AGND	**Signal Ground.**
41	EP II	GL	**Lower Gate Driver Output.** Synchronous MOSFET driver pin that can be connected to a test point in order to observe the waveform.

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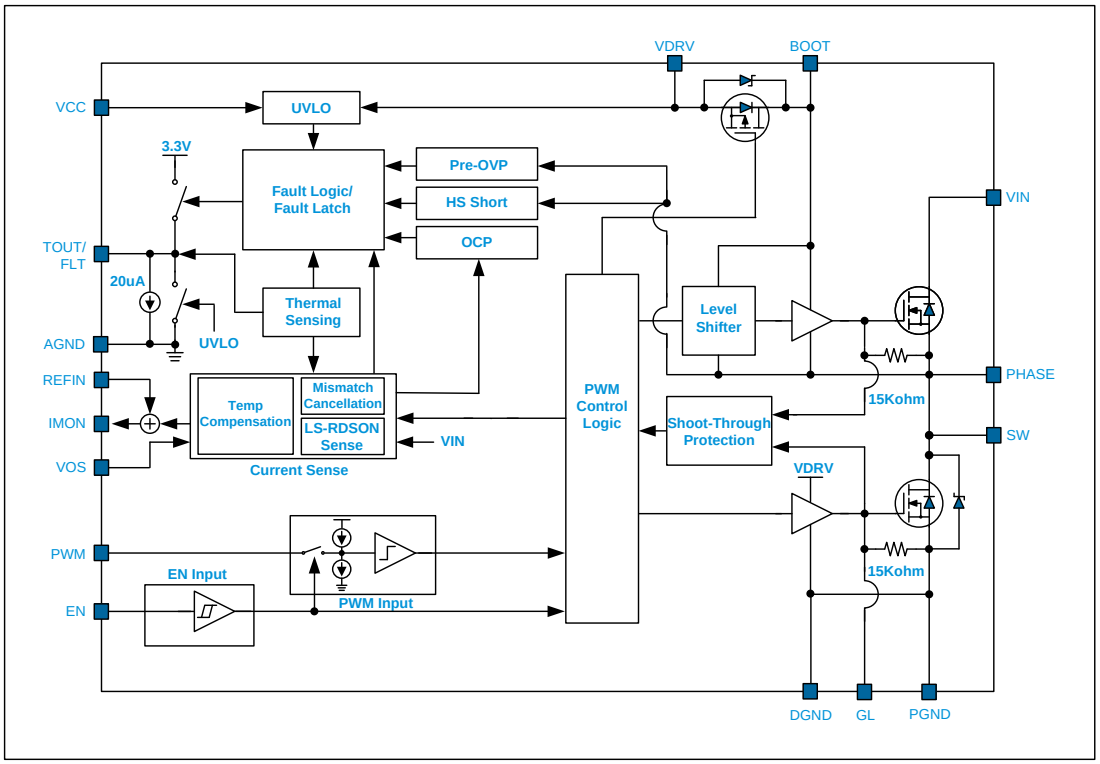
Functional Block Diagram



Functional Description

The uP9650 contains features as follows, the temperature sensing functionality, accurate current monitoring, ultra-compact, low-quiescent current, high-efficiency and high speed MOSFET driver fully optimized to drive a pair of integrated control and synchronous MOSFETs up to 1MHz for simplifying system design and improving functionality accuracy.

The uP9650 incorporates a synchronous MOSFET based current sense technique to provide an accurate output signal (IMON) which reports the real-time module current and to overcome the conventional inaccuracy of inductor DCR system method and resistor sense method leading to system inefficiency. $V_{(IMON - REFIN)}$ voltage represents current information at 5mV/A. The IMON signal can be used to replace inductor DCR sensing or resistor sense methods in multi-phase applications. The superior current sense accuracy achieved with on-chip current sensing technique improves the end-system performance.

The uP9650 also provides a very accurate module thermal monitor (TOUT) in normal operation. TOUT is a voltage source signal that is to provide a 0.8V output at 25^{o}C with 8mV/^{o}C linear slope for monitoring power stage temperature. If used in multi-phase topologies, multiple temperature outputs can be tied together to share a common thermal bus. Operating with this configuration will force the thermal bus signal to report the highest voltage (highest temperature) output TOUT signal to the controller. Also, this pin is used as a module fault flag pin. If a preliminary over voltage condition, a shorted control MOSFET, a prolonged over current event, or an over temperature condition inside the power stage is detected, the TOUT will be pulled up to 3.3V internally.

The uP9650 includes protection features as follows, VCC/VDRV Under Voltage-Lockout (UVLO), thermal shutdown (OTP, when SPS driver IC over temperature condition), phase fault detection, preliminary over voltage protection (Pre-OVP, when the control MOSFET is shorted), and cycle-by-cycle over current protection (OCP, when in overload condition).

Tri-State PWM Input

The uP9650 is compatible with standard 3.3V and 5V PWM logic with tri-state input to accommodate most of the PWM controllers.

The uP9650 PWM accepts standard 3-level input signals. When PWM logic input is high, it turns on the control MOSFET and turns off the synchronous MOSFET once the POR of VCC is granted and EN is kept high. When PWM logic input is low, it turns off the control MOSFET and turns on the synchronous MOSFET. If the PWM input is floating, the internal circuit will pull the PWM pin into the tri-state region and turn off the control MOSFET and synchronous MOSFET. The PWM pin voltage is kept around 1.5V by internal bias circuit when floating.

Deep-Sleep Mode

If VCC is ready but EN is pulled low, the power stage will enter deep-sleep mode. The gate driver circuitry will be disabled immediately and PWM pin will be in high input impedance state and most of the logic circuitry will be shut down to lower the biasing current to typical 200uA. The IMON output will be shorted to ground in deep-sleep mode. When EN pin is pulled high, the power stage will be activated and able to respond to the PWM signal after maximum 15us delay time.

Functional Description

Over Temperature Protection and Flag (OTP)

The TOUT/FLT pin of uP9650 is a thermal monitor output in normal operation. Once the temperature of driver IC goes above the rising threshold (130°C)(the temperature of control MOSFET may reach up to 150°C), the TOUT/FLT output will raise fault flag to 3.3V immediately and the driver will be turned off for self-protection. The TOUT/FLT will remain high until temperature of driver IC falls below the falling threshold (115°C) (the temperature of control MOSFET may reach 130°C). The driver will resume switching when the temperature of driver IC falls below 115°C.

Phase Fault Detection and Flag

The phase fault circuit monitors the SW node with respect to ground when VCC POR is granted and PWM input transits from high to low and the synchronous MOSFET is still conducting. That is, the phase fault detection mechanism is activated during every on-state period of synchronous MOSFET. If there is a control MOSFET failure which causes the switch node voltage to exceed the control MOSFET Short Threshold ($V_{PHASFLT\_TH}$=400mV) in a switching cycle, a phase fault event is detected. Then the TOUT/FLT will be pulled high to 3.3V immediately at the GL falling edge of that switching cycle, and it will remain high until the phase fault condition is released. Once the phase fault condition is released, the TOUT/FLT will be released back to normal at the GL falling edge of next switching cycle. When TOUT/FLT is flagged high, SPS continues to respond to PWM pulses.

VCC/VDRV Under Voltage Lockout (UVLO)

The uP9650 features both internal UVLO circuitry to monitor the VCC and VDRV pins separately. When a VCC or VDRV UVLO condition is detected, the driver will be in tri-state by shutting down both MOSFETs. In addition, IMON and TOUT/FLT pins will be pulled down to ground to indicate there is a UVLO fault. When both VCC UVLO and VDRV UVLO faults are cleared, the TOUT/FLT and IMON pins will be released and the driver will resume switching.

Cycle-by-Cycle Over Current Protection (OCP) and Flag

This device monitors the output current and provides cycle-by-cycle peak over current protection. The over current threshold is fixed to 80A. Once the inductor peak current exceeds the over current threshold (I_{CC_OCP}), the internal logic of SPS will automatically reduce the SW high state width by turning off the control MOSFET even if PWM input is still high, so that the inductor current is allowed to relieve.

The TOUT/FLT pin will be pulled high to 3.3V after 9 consecutive PWM high-low cycles of over current events where a severe over current event has been registered. The TOUT/FLT fault flag will clear once no severe over current event is registered within one consecutive PWM cycle. When TOUT/FLT is flagged high, SPS continues to respond to PWM pulses.

Preliminary Over Voltage Protection Flag (Pre-OVP)

The Pre-OVP feature is to protect the load during the VCC power up period, especially from control MOSFET short failure. It works against pre-biased start-up when pre-charged output voltage is higher than the Pre-OVP threshold. When the VIN rail is powered up but the controller is not powered up, the controller cannot react to any over voltage condition at the load side and all PWMs are tri-stated. Pre-OVP feature is active and allows the power stage to turn on the synchronous MOSFET when VCC is in transition from pre-POR to POR and SW node voltage exceeds Pre-OVP threshold. This function is to protect the CPU from damage.

When VCC UVLO clears and there is no existing pre-biased over voltage condition, the pre-OVP feature will be disabled. The controller must manage its output voltage from that moment on.

When VCC UVLO clears and the preliminary over voltage condition remains, the synchronous MOSFET will be latched ON regardless of the PWM input and the TOUT/FLT pin will be latched high to 3.3V so that the controller can detect the fault event after it is powered up. The fault can be cleared by an under voltage condition on VCC.

Functional Description

Temperature Sense Output and Fault Flag (TOUT/FLT)

The uP9650 incorporates an internal temperature sensing circuitry from driver IC to provide a linear voltage slope of 8mV/°C with a 0.6V offset at 0°C on the TOUT/FLT pin, refer to (EQ1). In multi-phase systems the uP9650 temperature outputs can be tied together and connect to the PWM controller temperature sense input to provide the highest temperature to PWM controller.

$$V_{TOUT/FLT}(V) = 0.6V + \frac{0.008V}{°C} \times T(°C) \qquad (EQ1)$$

The TOUT/FLT also provides four fault flag conditions as follows, over temperature, phase fault, over current, and preliminary over voltage conditions. TOUT/FLT will be pulled up to 3.3V internally if any of the above-mentioned fault event conditions is detected. The TOUT/FLT can also be used as an indicator of low VCC voltage as it will be weakly pulled down to ground under the VCC UVLO condition. In a multi-phase system where the TOUT/FLT pins are tied together, once any faults occur in the phases, TOUT/FLT is able to be pulled to 3.3V internally.

Internal Current Sensing and Reporting (IMON, REFIN)

The uP9650 provides an internal real-time synchronous MOSFET current sense circuit. This device utilizes the inputs from VOS pin and REFIN pin and synchronous MOSFET to create a current signal simulating the inductor current which reports to the controller. The current sense amplifier circuit in the uP9650 is completely temperature compensated for $R_{DS(ON)}$ of synchronous MOSFET. The current signal will be reported to the controller in the form of a differential voltage between IMON pin and REFIN pin with a conversion gain 5mV/A to the actual inductor current IL, refer to (EQ2). The REFIN voltage is an externally supplied DC voltage from controller IC or other power rail in system.

$$V_{IMON}(V) - V_{REFIN}(V) = \frac{0.005V}{A} \times I_L(A) \qquad (EQ2)$$

The internal current sense circuit of the uP9650 may replace the standard inductor DCR and greatly improve system efficiency.

Absolute Maximum Rating

(Note 1)

VCC/VDRV/EN/PWM/VOS ---------- -0.3V to +6V
TOUT/FLT/IMON/REFIN ---------- -0.3V to (VCC+0.3V)
VIN ---------- -0.3V to +30V
BOOT to PHASE
DC ---------- -0.3V to +6V
< 5ns ---------- -0.3V to +8V
VIN to SW/PHASE
DC ---------- -0.3V to +30V
< 5ns ---------- -6V to +33V
SW to PGND
DC ---------- -0.3V to +30V
< 5ns ---------- -6V to +33V
PHASE to PGND
DC ---------- -0.3V to +30V
< 5ns ---------- -11V to +33V
BOOT to AGND
DC ---------- 0V to +34V
< 5ns ---------- -6V to +34V
GL to AGND
DC ---------- -0.3V to +6V
< 5ns ---------- -2V to +6V
EAS-HS MOSFET (Note 2) ---------- 42.9mJ
EAS-LS MOSFET (Note 3) ---------- 232.3mJ
Storage Temperature Range ---------- -55°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering,10 sec) ---------- 260°C
ESD Rating (Note 4)
HBM (Human Body Mode) ---------- 2kV
CDM (Charged Device Mode) ---------- 1kV

Thermal Information

Package Thermal Resistance
VQFN6x5-39L θ_{JA} ---------- 25°C/W
VQFN6x5-39L $\theta_{J\text{-}PCB}$ ---------- 2°C/W
VQFN6x5-39L $\theta_{J\text{-}TOP}$ ---------- 11°C/W

Recommended Operation Conditions

(Note 5)

Operating Junction Temperature Range ---------- -40 °C to +125 °C
Operating Ambient Temperature Range ---------- -40°C to +85 °C
VIN ---------- +4.5V (Note 6) to +22V
VCC/VDRV ---------- +4.5V to 5.5V

Recommended Operation Conditions

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. EAS is a Single Pulse Avalanche Energy. The test condition is V_{DD} = 75V, I_{AV} = 92.6A,V_{GS} =10V, L=0.01mH, Rg=25Ω. The AMR related EAS test was done on MOSFET only.

Note 3. EAS is a Single Pulse Avalanche Energy. The test condition is V_{DD} = 75V, I_{AV} = 96.4A,V_{GS} =10V, L=0.05mH, Rg=25Ω.The AMR related EAS test was done on MOSFET only.

Note 4. Devices are ESD sensitive. Handling precaution recommended.

Note 5. The device is not guaranteed to function outside its operating conditions.

Note 6. The on-time of synchronous MOSFET must be greater than 800ns to ensure effective and correct current sensing for IMON signal.

Electrical Characteristics

(V_{CC} = V_{DRV} = 5V, T_J = 25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
VCC Supply Current	I_{VCC_ENH}	EN=5V,PWM = 600kHz, duty=15%	--	6	7.8	mA
	I_{VCC_ENF}	EN=5V,PWM floating	--	6	--	
	I_{VCC_ENL}	EN=0V		200	260	uA
VCC POR Threshold	V_{CCRTH}	V_{VCC} rising	3.8	4	4.2	V
VCC POR Hysteresis	V_{CCHYS}		--	0.25	--	V
VDRV Supply Current	I_{VDRV_ENH}	EN=5V,PWM = 600kHz, duty=15%	--	38	--	mA
	I_{VDRV_ENF}	EN=5V,PWM floating	--	0.02	1	
	I_{VDRV_ENL}	EN=0V	--	0.5	1	uA
VDRV POR Threshold	V_{DRVRTH}	V_{VDRV} rising	3.8	4	4.2	V
VDRV POR Hysteresis	V_{DRVHYS}		--	0.25	--	V
Enable Input						
Input High	EN_H		2	--	--	V
Input Low	EN_L		--	--	0.8	V
Propagation Delay	T_{PDHDEN}	PWM=0V. Measured from EN rising edge to 10% of GL.	--	--	15	us
	T_{PDLDEN}	PWM=0V. Measured from EN falling edge to 90% of GL.	--	30	55	ns
PWM Input						
PWM High Voltage	V_{IH_PWM}	PWM low to high or tri-state to high	2.4	--	--	V
PWM Low Voltage	V_{IL_PWM}	PWM high to low or tri-state to low	--	--	0.6	V
Tri-State Open Voltage	V_{HiZ_PWM}	PWM input floating	1.4	1.5	1.6	V
Input Mid-State	V_{PWM_MID}		1	--	2	V
PWM Input Current	I_{PWM}	PWM=0V	--	-210	-260	uA
		PWM=3.3V	--	210	260	
		PWM=5V	--	210	260	
PWM Propagation Delay and Dead Time Range						
PWM High Propagation Delay	$T_{PDLLGATE}$	PWM going high to GL going low VIH_PWM to 90% GL	--	15	--	ns
PWM Low Propagation Delay	$T_{PDLUGATE}$	PWM going low to SW going low VIL_PWM to 90% SW	--	20	--	ns
Tri-State to Turn-On Propagation Delay	$T_{PDTSGHH}$	PWM (from tri-state) going high to SW going high, VIH_PWM to 10% SW	--	20	--	ns
Tri-State to Turn-Off Propagation Delay	$T_{PDTSGLH}$	PWM (from tri-state) going low to GL going high, VIL_PWM to 10% GL	--	15	--	ns

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWM Propagation Delay and Dead Time Range						
PWM Low to Tri-State Shut-Off Time	$T_{PDTSOFF1}$	PWM (from low) going tri-state to GL going low, VIL_PWM to 10% GL	--	40	--	ns
PWM High to Tri-State Shut-Off Time	$T_{PDTSOFF2}$	PWM (from High) going tri-state to SW going low, VIL_PWM to 90% SW	--	35	--	ns
GL Off to SW On Dead Time	$T_{PDHUGATE}$	GL=10% to SW=10%	--	20	--	ns
SW Off to GL On Dead Time	$T_{PDHLGATE}$	SW=10% to GL=10%	--	10	--	ns
Minimum SW Pulse Width	T_{MINSW}	10% of SW rising edge to 10% of SW falling edge, load = 10A (Note 1)	--	50	--	ns
Internal Bootstrap Switch						
Forward Voltage	V_{FWD}	VDRV to BOOT, IBOOT = 10mA, PWM = floating	--	500	--	mV
On Resistance	R_{SW}	VDRV to BOOT, IBOOT = 10mA, PWM = 0V	--	15	--	Ω
Temperature Sense Output and Fault Flag - TOUT / FLT						
Temperature Sense Slope	T_{SNS_GAIN}	$0^oC < T_J < 125^oC$ (Note 1)	7.8	8	8.2	mV/°C
Temperature Sense Offset	V_{SNS_OFFSET}	$T_J = 90^oC$, 0.6V+8mV/°C*T_J	1.302	1.32	1.338	V
TOUT Source Current	I_{TOUT_SRC}		--	850	--	uA
TOUT Sink Current	I_{TOUT_SNK}		--	20	--	uA
Fault Mode Active High Voltage	$V_{FLTHIGH}$	Under over temperature, over current, phase fault or pre-OV fault	3.0	3.2	3.6	V
TOUT / FLT Active Low Voltage	V_{FLTLOW}	No fault, VCC < UVLO	--	--	0.28	V
Fault Mode Source Current	I_{FLTSRC}	$T_J = 90^oC$, 3.3V source to GND	--	6.6	--	mA
TOUT / FLT Active Pull Down Resistance	R_{PULLDN_TOUT}	No fault, VCC < UVLO, VCC = 3.5V	--	10	--	Ω
Current Sense Output - IMON						
Gain	G_{CS}	$T_J = 25^oC$ and 90^oC, 0A~20A load, REFIN=1.2V,VCC=VDRV=5.0V (Note 1)	4.75	5	5.25	mV/A
Offset Current	A_{CC_OFFSET}	$T_J = 25^oC$ and 90^oC, 0A load (Note 2)	-1	--	+1	A
Accuracy	A_{CC_CS}	$T_J=25^oC$, 20A load, REFIN=1.2V,VCC=VDRV=5.0V (Note 2)	-5	--	+5	%
		$T_J=90^oC$, 20A load, REFIN=1.2V,VCC=VDRV=5.0V (Note 2)	-5	--	+5	%

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Current Sense Output - IMON (Cont.)						
Overall Accuracy	A_{CC_ALL}	T_J = 0°C~125°C, < 20A load, REFIN=1.2V,VCC=VDRV=5.0V (Note 1)	-1	--	+1	A
		T_J = 0°C~125°C, 20A~40A load, REFIN=1.2V,VCC=VDRV=5.0V (Note 1)	-5	--	+5	%
		T_J = 0°C~125°C, 40A~50A load, REFIN=1.2V,VCC=VDRV=5.0V (Note 1)	-6	--	+6	%
IMON Active Pull Down	$R_{PULLLDN\_IMON}$	VCC < UVLO	--	170	--	Ω
IMON Sink Current	I_{CSAS}	VCC > UVLO	--	0.3	--	mA
Current Monitor Reference Input Voltage	V_{REFIN}	Externally supplied reference voltage	1.1	1.2	1.8	V
Phase-Fault Detection						
HS Control MOSFET Short Threshold	$V_{PHASFLT\_TH}$	V(SW) - V(PGND)(Note 1)	--	400	--	mV
Over Temperature Protection						
Over Temp Rising Threshold	T_{OTPR}	TOUT/FLT pulled up high, (Driver IC temperature) (Note 1)	--	130	--	°C
Over Temp Protection Hysteresis	OTP_hys	TOUT/FLT released, (Driver IC temperature) (Note 1)	--	15	--	°C
Preliminary Over Voltage Protection						
SW Threshold	V_{PREOVP}		--	2.7	--	V
Cycle-by-Cycle Over Current Protection						
Over Current Threshold	I_{CC_OCP}		--	80	--	A
Constant Over Current Threshold	V_{OCP_CST}	T_J = 90°C (equivalent to 80A, measure IMON to REFIN)	370	400	430	mV
OCP Detect Blanking Delay	$T_{BLANK\_OCP-FAULT}$	PWM high-low cycles to TOUT / FLT high	--	9	--	cycle

Note 1: Guaranteed by design but not tested in production

Note 2: Guaranteed by independent ATE testing

Electrical Characteristics

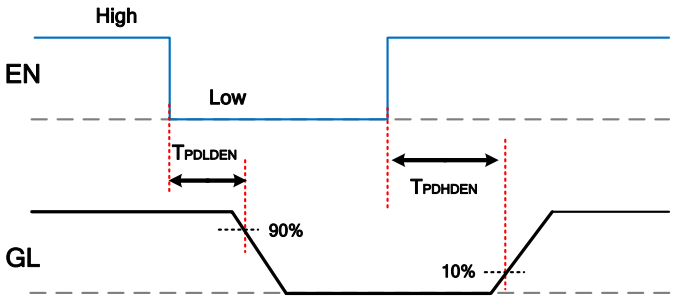


Figure 1. EN Control Input Timing Diagram

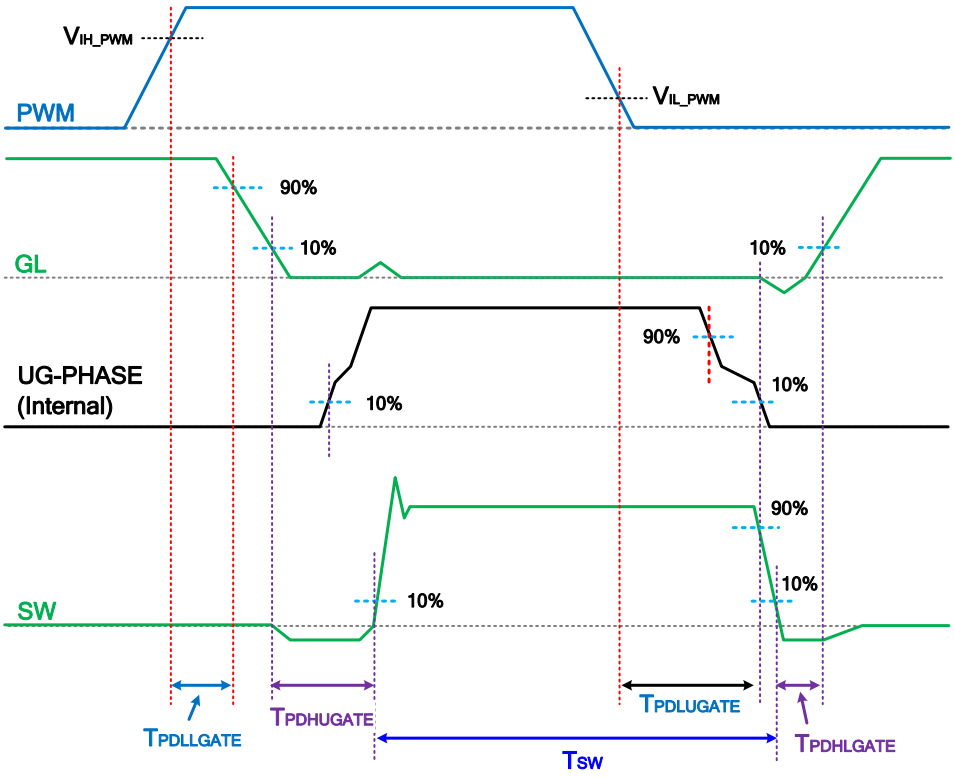


Figure 2. PWM Logic Input Timing Diagram

Electrical Characteristics

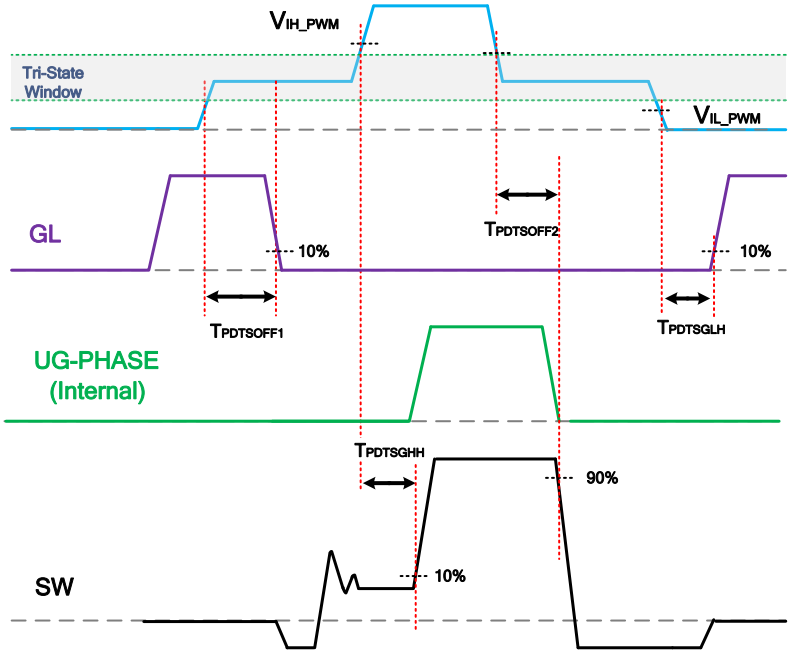
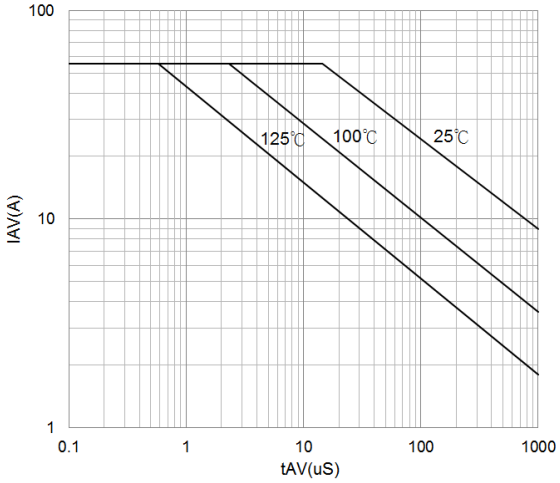


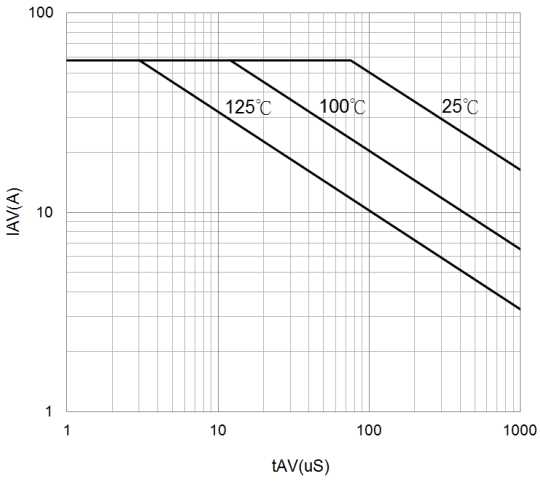
Figure 3. PWM Tri-State Input Timing Diagram

Typical Operation Characteristics

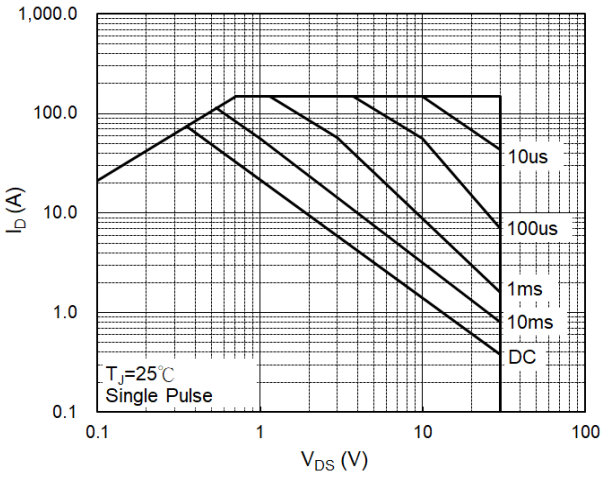
High Side FET Avalanche Characteristics



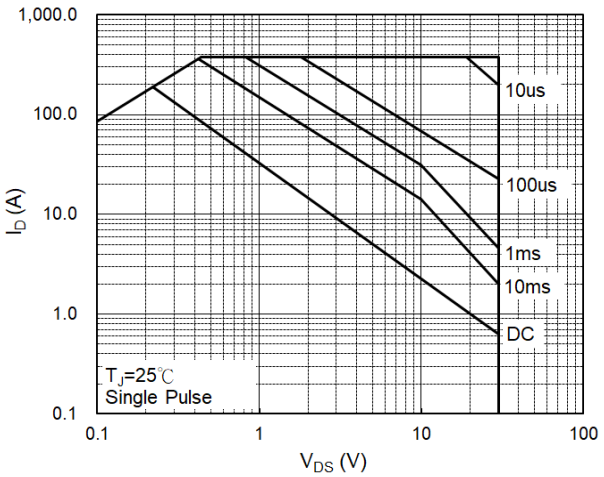
Low Side FET Avalanche Characteristics



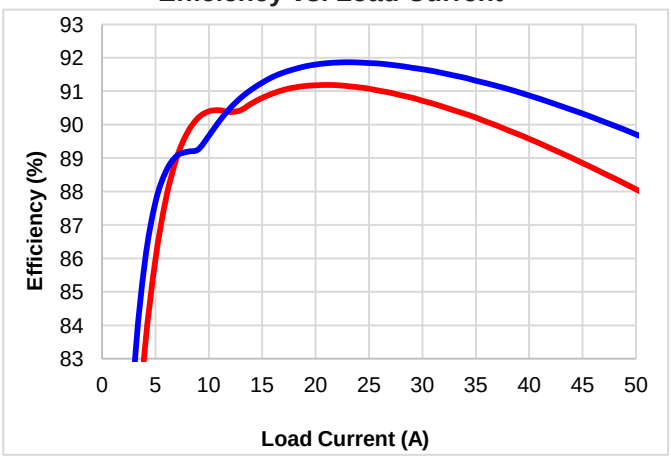
High Side FET Safe Operating Area



Low Side FET Safe Operating Area

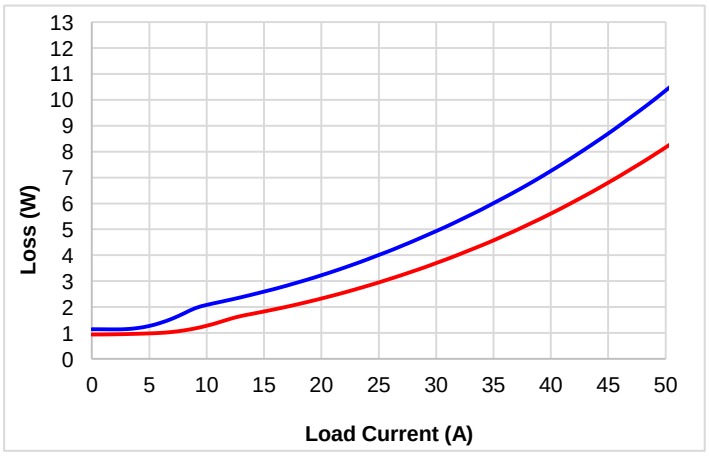


Efficiency vs. Load Current



V_{OUT}=1.2V,300kHz,V_{OUT}=1.8V,600kHz

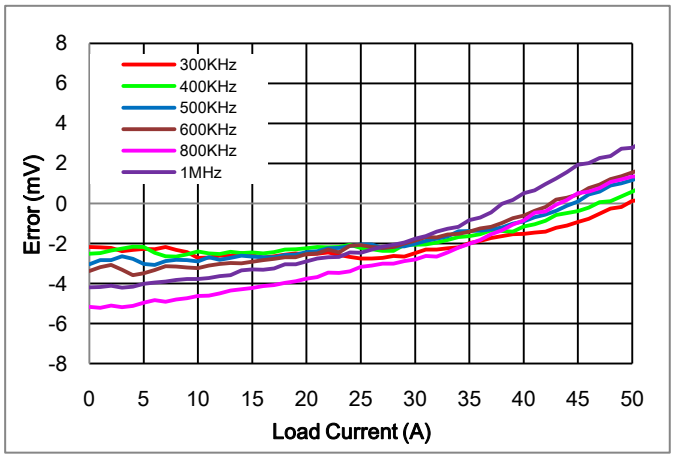
Power Loss vs. Load Current



V_{OUT}=1.2V,300kHz,V_{OUT}=1.8V,600kHz

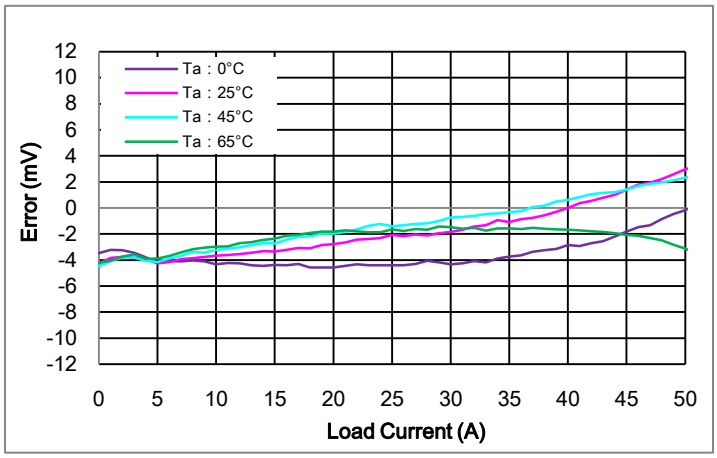
Typical Operation Characteristics

IMON Accuracy vs. Frequency



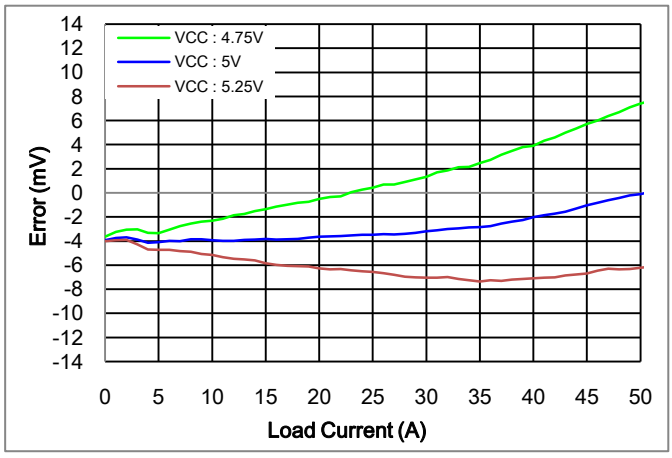
V_{IN}=19V,V_{OUT}=1.2V,V_{CC}/V_{DRV}=5V

IMON Accuracy vs. Temperature



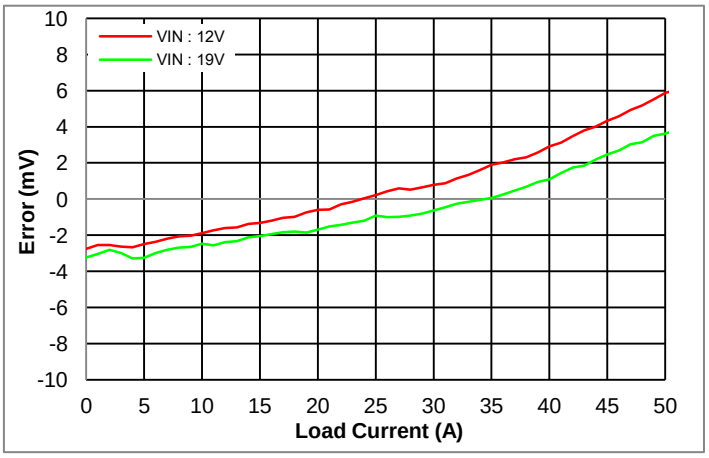
V_{IN}=19V,V_{OUT}=1.2V,V_{CC}/V_{DRV}=5V,F_{sw}=600kHz

IMON Accuracy vs. VCC



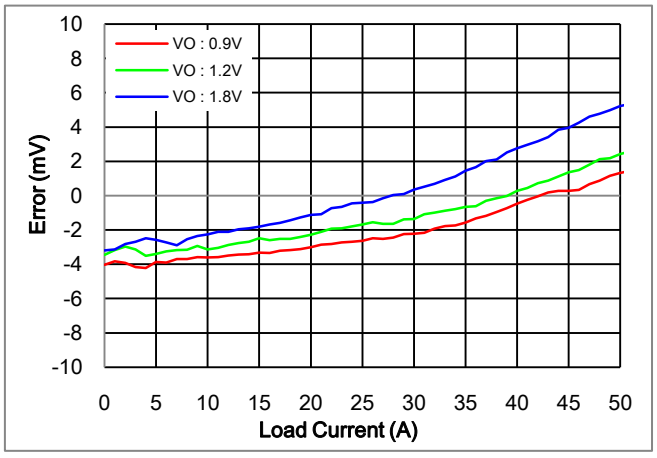
V_{IN}=19V,V_{OUT}=1.2V,V_{CC}/V_{DRV}=5V,F_{sw}=600kHz

IMON Accuracy vs. VIN



V_{OUT}=1.2V,V_{CC}/V_{DRV}=5V,F_{sw}=600kHz

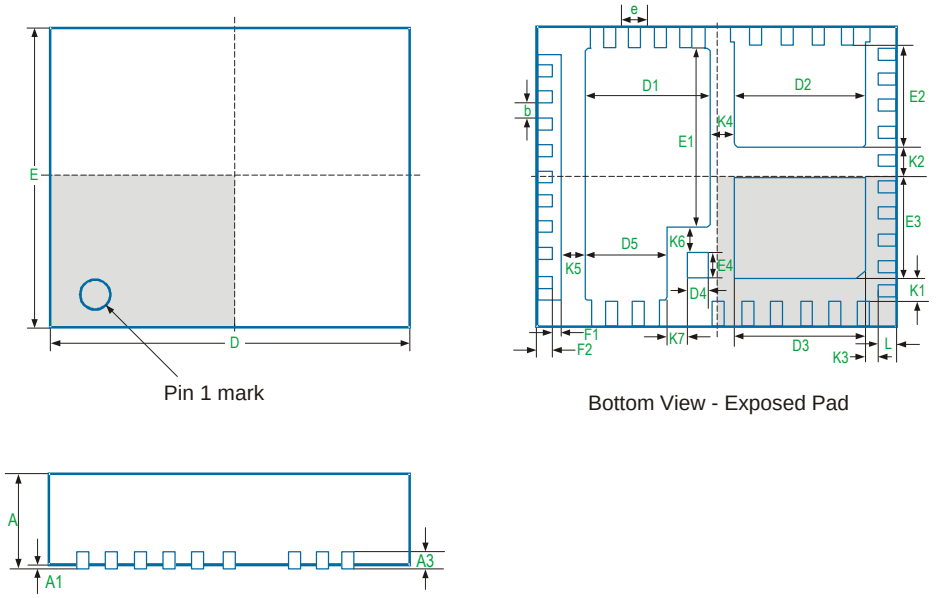
IMON Accuracy vs. VOUT



V_{IN}=19V , V_{CC}/V_{DRV}=5V , F_{sw}=600kHz

Package Information

VQFN6x5-39L



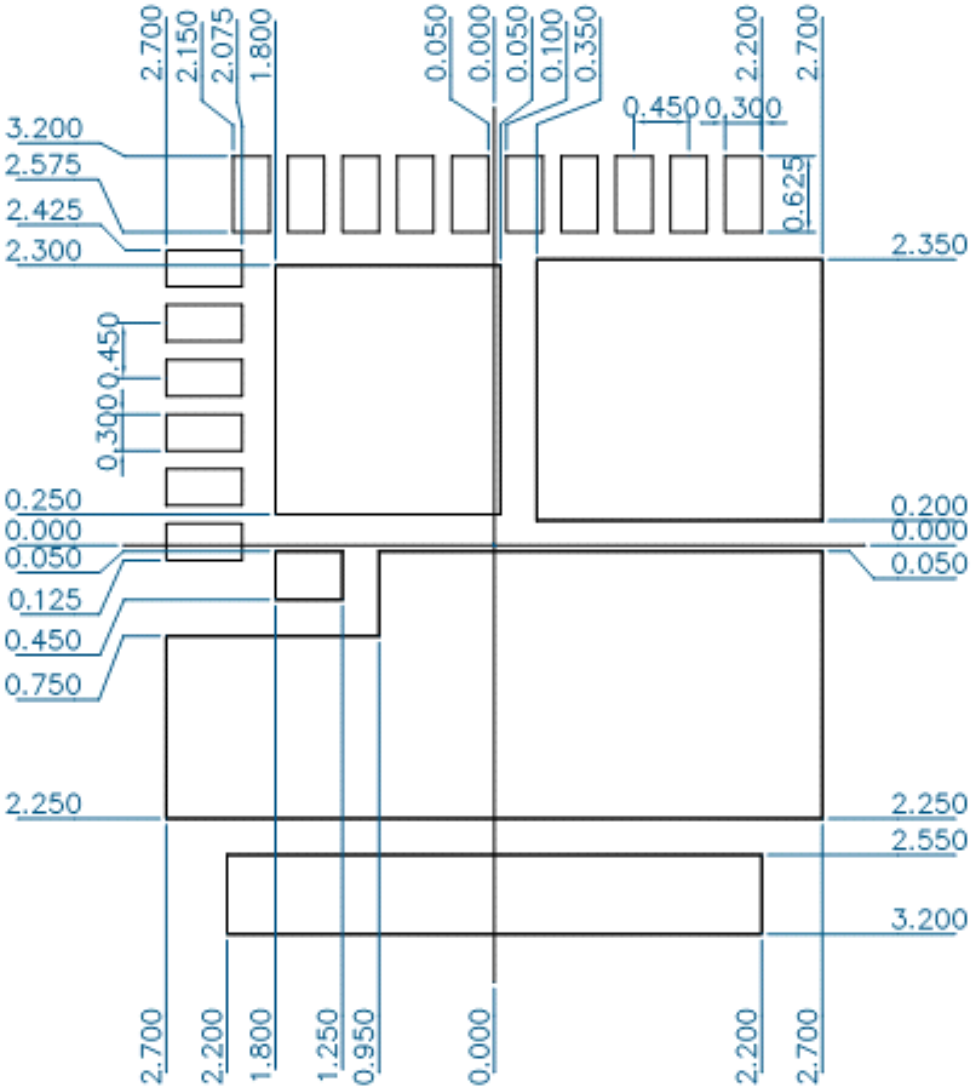
Symbol	Dimension (mm)			Symbol	Dimension (mm)			Symbol			
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX
A	0.800	0.900	1.000	D5	1.300	1.400	1.500	F2	0.275 BSC		
A1	0.000	0.020	0.050	E	5.000 BSC			K1	0.350 BSC		
A3	0.200 REF			E1	3.022	3.122	3.230	K2	0.400 BSC		
b	0.200	0.250	0.300	E2	1.718	1.818	1.925	K3	0.350 BSC		
D	6.000 BSC			E3	1.650	1.750	1.850	K4	0.400 BSC		
D1	2.000	2.100	2.200	E4	0.450 BSC			K5	0.400 BSC		
D2	1.850	1.950	2.050	e	0.450 BSC			K6	0.400 BSC		
D3	1.850	1.950	2.050	L	0.300	0.400	0.500	K7	0.400 BSC		
D4	0.300 BSC			F1	0.125 BSC						

Note:

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   NOM: Nominal. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.
5. There are tie bars exposed on package side wall and the exposed position are inconsistent depending on different vendors.

Package Information

Recommended PCB Land Pattern



Note

1. Dimensions in Millimeters
2. Drawing not to scale

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