RENESAS

MOS INTEGRATED CIRCUIT

μPD161608

176-RGB x 220-DOT 1-CHIP DRIVER IC FOR 262,144-COLOR TFT-LCD DISPLAY

DESCRIPTION

The μPD161608 is TFT-LCD display driver IC. Also, it is possible by 176-RGB x 220-dot to display 262,144 colors.

FEATURES

- 176-RGB x 220-dot TFT-LCD display driver IC for 262,144 colors (528ch-source driver/220ch-gate driver)
- 18-bit RGB interface and serial peripheral interface (SPI)
- Various color-display control functions
  - 262,144 colors can be displayed at the same time (including: γ- adjust)
- Low-power operation supports
  - Maximum 6-times DC/DC converter circuit for generating driving voltage
  - Voltage followers to decrease direct current flow in the LCD drive breeder-resistors
  - Equalizing function for the switching performance of DC/DC converter circuits and operational amplifiers
- Internal power supply circuit
- Operating voltage
  · Apply voltage
  - V_{DD}-V_{SS} = 1.6 to 2.7 V (non-regulating) (logic voltage range - non-regulated)
    V_{DDIO}-V_{SS} = 1.6 to 3.3 V (regulating) (logic voltage range - regulated)
  - VCI-V_{SS} = 2.5 to 3.3 V (internal reference power-supply voltage)
  · Generate voltage
  - For the source driver: VCIX2-V_{SS} = 5.0 to 5.5 V (power supply for driving circuits)
  - For the gate driver: VGH-VGL = 17.5 to 30.25 V, VGH-V_{SS} = +10 to +16.5 V
- On chip EEPROM

ORDERING INFORMATION

Part Number	Package
μPD161608P	Chip

Remark Purchasing the above chip entail the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representatives.

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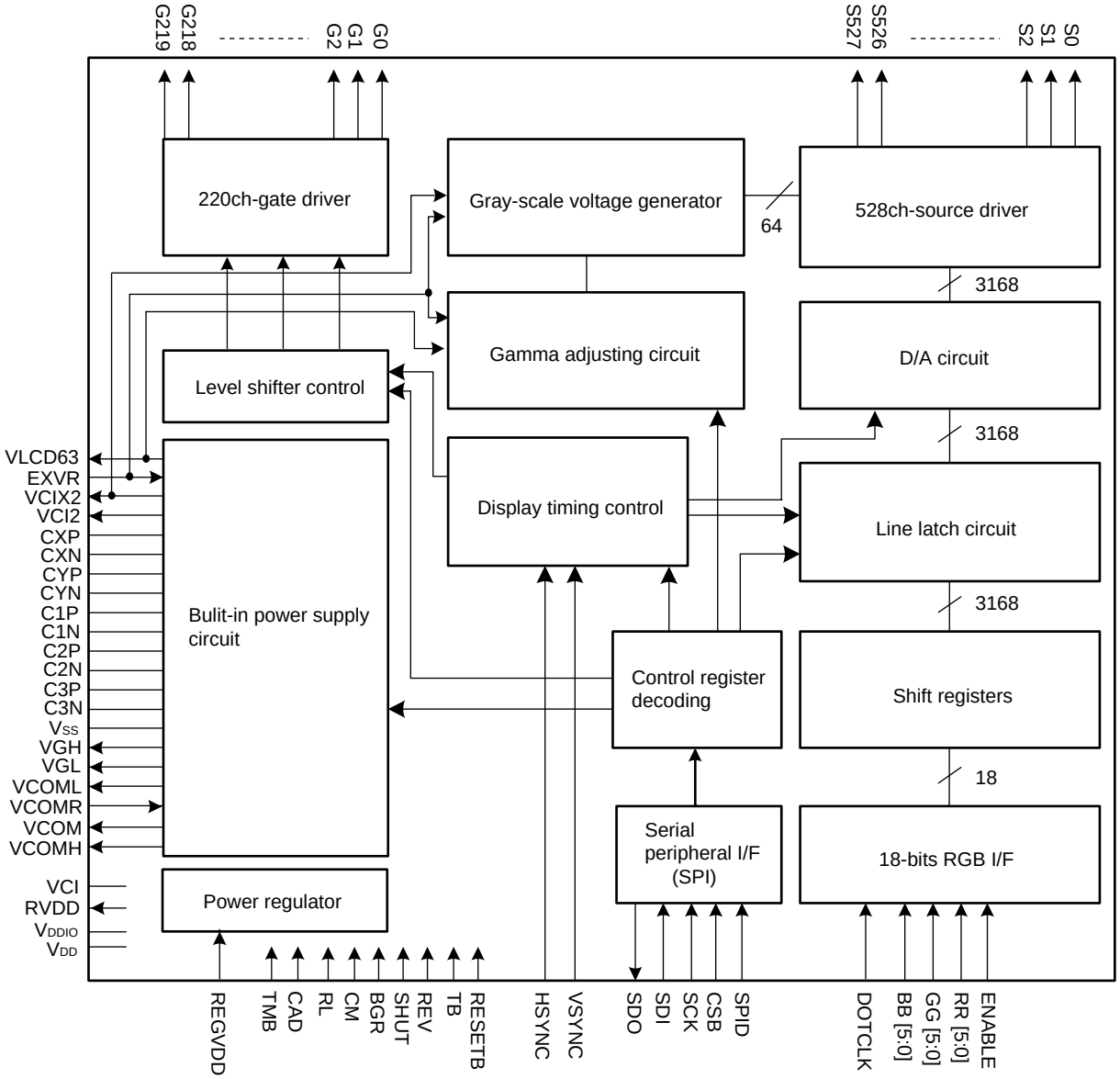
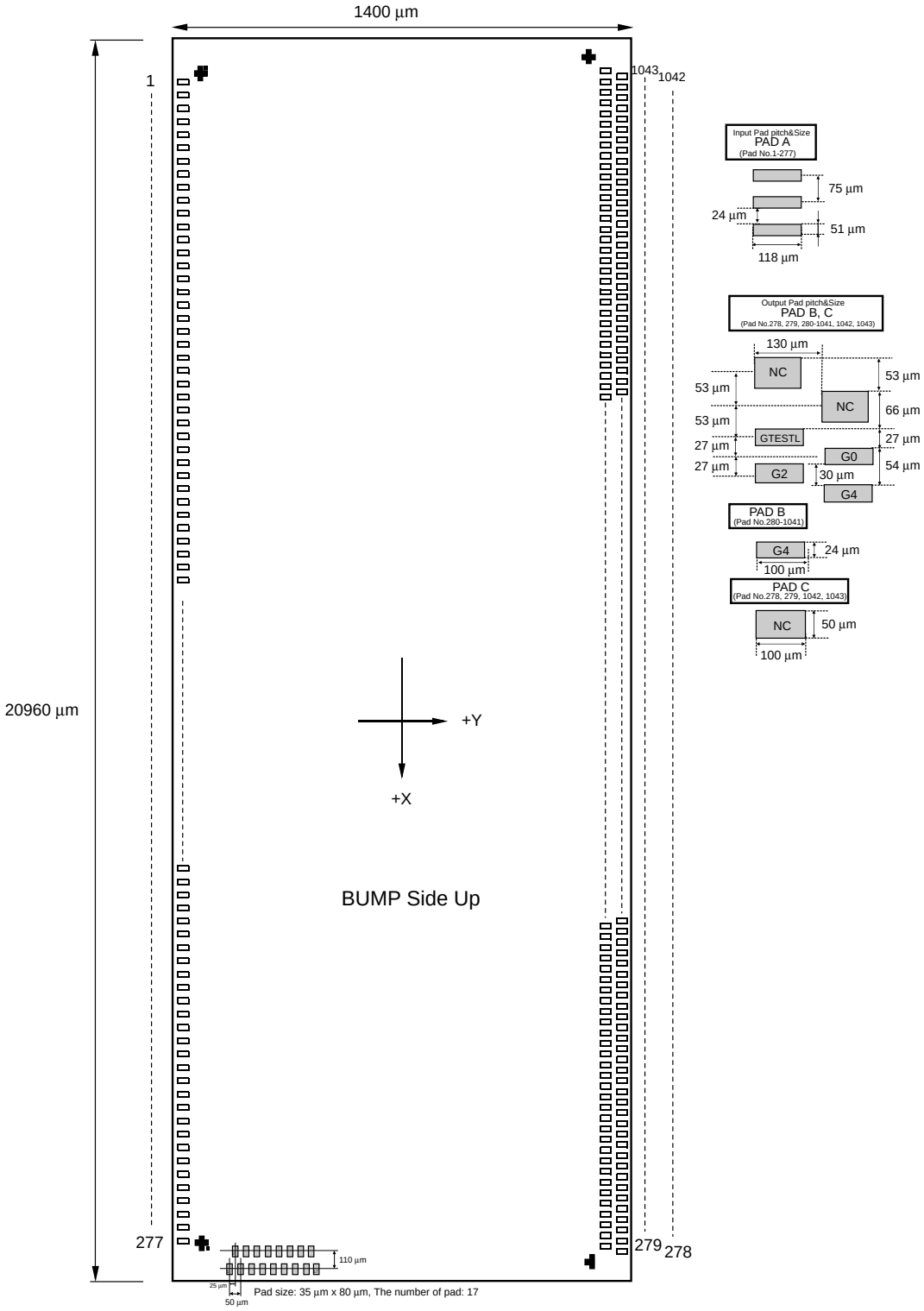
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

<R> 1. BLOCK DIAGRAM



2. PAD CONFIGURATION



Remark NC: No Connection

Table 2–1. Pad Dimensions

Items	Pad Name	Size		Unit
		X	Y	
Chip size (With scribe lane: 100 μm)	–	20960	1400	μm
Chip thickness	–	400		
Pad pitch	1 to 277	75		
	278, 279, 1042, 1043	53		
	280 to 1041	27		
Bump pad size	1 to 277	51	118	
	278, 279, 1042, 1043	50	100	
	280 to 1041	24	100	
Bump height	–	15		

Figure 2–1. Alignment Mark Configurations (unit: μm)

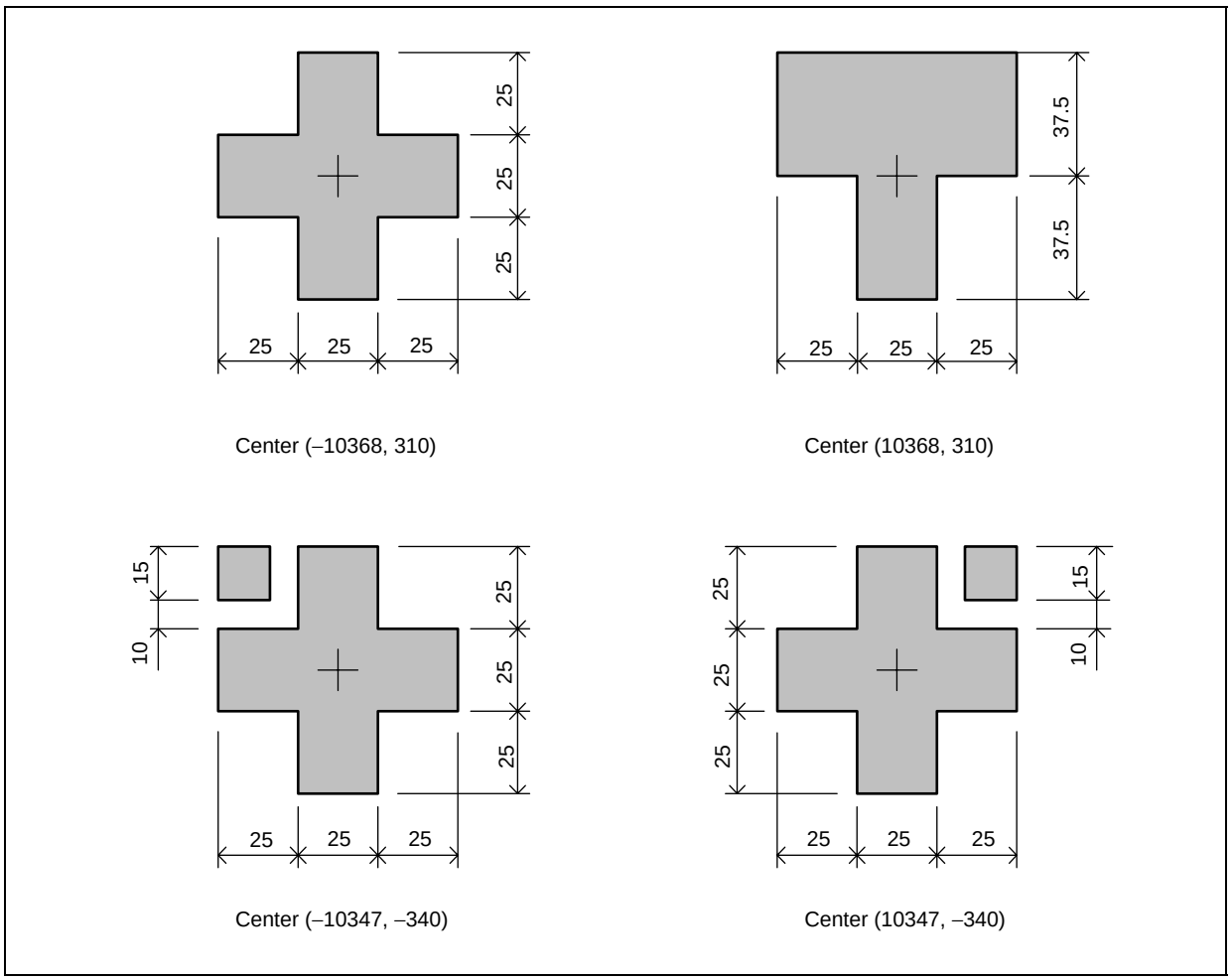


Table 2–2. Pad Coordinate (1/5)

Pad No.	Name	X	Y
1	NC	-10350	-520
2	NC	-10275	-520
3	VCOM	-10200	-520
4	VCOM	-10125	-520
5	VCOM	-10050	-520
6	DUMMY	-9975	-520
7	DUMMY	-9900	-520
8	CDUM0	-9825	-520
9	CDUM0	-9750	-520
10	CDUM0	-9675	-520
11	CDUM1	-9600	-520
12	CDUM1	-9525	-520
13	CDUM1	-9450	-520
14	NC	-9375	-520
15	NC	-9300	-520
16	NC	-9225	-520
17	NC	-9150	-520
18	NC	-9075	-520
19	NC	-9000	-520
20	NC	-8925	-520
21	VSS	-8850	-520
22	NC	-8775	-520
23	NC	-8700	-520
24	NC	-8625	-520
25	NC	-8550	-520
26	NC	-8475	-520
27	NC	-8400	-520
28	C3N	-8325	-520
29	C3N	-8250	-520
30	C3N	-8175	-520
31	C3P	-8100	-520
32	C3P	-8025	-520
33	C3P	-7950	-520
34	C2N	-7875	-520
35	C2N	-7800	-520
36	C2N	-7725	-520
37	C2P	-7650	-520
38	C2P	-7575	-520
39	C2P	-7500	-520
40	TESTC	-7425	-520
41	TESTB	-7350	-520
42	C1N	-7275	-520
43	C1N	-7200	-520
44	C1N	-7125	-520
45	C1P	-7050	-520
46	C1P	-6975	-520
47	C1P	-6900	-520
48	VSS	-6825	-520
49	VSS	-6750	-520
50	CYN	-6675	-520
51	CYN	-6600	-520
52	CYN	-6525	-520
53	CYP	-6450	-520
54	CYP	-6375	-520
55	CYP	-6300	-520
56	VCI	-6225	-520
57	VDD	-6150	-520
58	CXN	-6075	-520
59	CXN	-6000	-520
60	CXN	-5925	-520
61	CXP	-5850	-520
62	CXP	-5775	-520
63	CXP	-5700	-520
64	VCOML	-5625	-520
65	VCOML	-5550	-520
66	VCOML	-5475	-520
67	VCOMH	-5400	-520
68	VCOMH	-5325	-520
69	VCOMH	-5250	-520
70	VGL	-5175	-520
71	VGL	-5100	-520
72	VGL	-5025	-520
73	VGH	-4950	-520
74	VGH	-4875	-520
75	VGH	-4800	-520
76	VCOML	-4725	-520
77	VCOML	-4650	-520
78	VCOML	-4575	-520
79	VCI2	-4500	-520
80	VCI2	-4425	-520
81	VCI2	-4350	-520
82	NC	-4275	-520
83	VCIX2	-4200	-520
84	VCIX2	-4125	-520
85	VCIX2	-4050	-520
86	VCIX2	-3975	-520
87	VCIX2	-3900	-520
88	VCIX2	-3825	-520
89	VCIX2	-3750	-520
90	VLCD63	-3675	-520
91	VLCD63	-3600	-520
92	VLCD63	-3525	-520
93	VLCD63	-3450	-520
94	VLCD63	-3375	-520
95	VLCD63	-3300	-520
96	VLCD63	-3225	-520
97	VLCD63	-3150	-520
98	TESTA	-3075	-520
99	VCOMH	-3000	-520
100	VCOMH	-2925	-520
101	VCOMH	-2850	-520
102	NC	-2775	-520
103	RVDD	-2700	-520
104	RVDD	-2625	-520
105	RVDD	-2550	-520
106	RVDD	-2475	-520
107	RVDD	-2400	-520
108	RVDD	-2325	-520
109	EXVR	-2250	-520
110	VCOMR	-2175	-520
111	VCOMR	-2100	-520
112	NC	-2025	-520
113	VSS	-1950	-520
114	VSS	-1875	-520
115	VSS	-1800	-520
116	VSS	-1725	-520
117	VSS	-1650	-520
118	VSS	-1575	-520
119	VSS	-1500	-520
120	VSS	-1425	-520
121	NC	-1350	-520
122	VSS	-1275	-520
123	VSS	-1200	-520
124	VSS	-1125	-520
125	VSS	-1050	-520
126	TMB	-975	-520
127	VSS	-900	-520
128	VSS	-825	-520
129	VSS	-750	-520
130	VSS	-675	-520
131	NC	-600	-520
132	VSS	-525	-520
133	VSS	-450	-520
134	VSS	-375	-520
135	VSS	-300	-520
136	VSS	-225	-520
137	NC	-150	-520
138	VCI	-75	-520
139	VCI	0	-520
140	VCI	75	-520
141	VCI	150	-520
142	VCI	225	-520
143	VCI	300	-520
144	VCI	375	-520
145	VCI	450	-520
146	VCI	525	-520
147	VCI	600	-520
148	VDD	675	-520
149	VDD	750	-520
150	VDD	825	-520
151	VDD	900	-520
152	NC	975	-520
153	VDDIO	1050	-520
154	VDDIO	1125	-520
155	SDO	1200	-520
156	SDO	1275	-520
157	SDI	1350	-520
158	SDI	1425	-520
159	SCK	1500	-520
160	SCK	1575	-520
161	CSB	1650	-520
162	CSB	1725	-520
163	CSB	1800	-520
164	RESB	1875	-520
165	RESB	1950	-520
166	RESB	2025	-520
167	VSS	2100	-520
168	TESTIN1	2175	-520
169	TESTIN2	2250	-520
170	VDDIO	2325	-520
171	SPID	2400	-520
172	SPID	2475	-520
173	VSS	2550	-520
174	REGVDD	2625	-520
175	REGVDD	2700	-520
176	VDDIO	2775	-520
177	CAD	2850	-520
178	CAD	2925	-520
179	VSS	3000	-520
180	REV	3075	-520
181	REV	3150	-520
182	VDDIO	3225	-520
183	BGR	3300	-520
184	BGR	3375	-520
185	VSS	3450	-520
186	TB	3525	-520
187	TB	3600	-520
188	VDDIO	3675	-520
189	RL	3750	-520
190	RL	3825	-520
191	VSS	3900	-520
192	SHUT	3975	-520
193	SHUT	4050	-520
194	SHUT	4125	-520
195	DOTCLK	4200	-520
196	DOTCLK	4275	-520
197	DOTCLK	4350	-520
198	HSYNC	4425	-520
199	HSYNC	4500	-520
200	HSYNC	4575	-520
201	VSYNC	4650	-520
202	VSYNC	4725	-520
203	VSYNC	4800	-520
204	ENABLE	4875	-520
205	ENABLE	4950	-520
206	ENABLE	5025	-520
207	VDDIO	5100	-520
208	RR5	5175	-520
209	RR5	5250	-520
210	RR5	5325	-520
211	RR4	5400	-520
212	RR4	5475	-520
213	RR4	5550	-520
214	RR3	5625	-520
215	RR3	5700	-520
216	RR3	5775	-520
217	RR2	5850	-520
218	RR2	5925	-520
219	RR2	6000	-520
220	RR1	6075	-520
221	RR1	6150	-520
222	RR1	6225	-520
223	RR0	6300	-520
224	RR0	6375	-520
225	RR0	6450	-520
226	GG5	6525	-520
227	GG5	6600	-520
228	GG5	6675	-520
229	GG4	6750	-520
230	GG4	6825	-520
231	GG4	6900	-520
232	GG3	6975	-520
233	GG3	7050	-520
234	GG3	7125	-520
235	GG2	7200	-520
236	GG2	7275	-520
237	GG2	7350	-520
238	GG1	7425	-520
239	GG1	7500	-520
240	GG1	7575	-520

Table 2–2. Pad Coordinate (2/5)

Pad No.	Name	X	Y
241	GG0	7650	-520
242	GG0	7725	-520
243	GG0	7800	-520
244	BB0	7875	-520
245	BB0	7950	-520
246	BB0	8025	-520
247	BB1	8100	-520
248	BB1	8175	-520
249	BB1	8250	-520
250	BB2	8325	-520
251	BB2	8400	-520
252	BB2	8475	-520
253	BB3	8550	-520
254	BB3	8625	-520
255	BB3	8700	-520
256	BB4	8775	-520
257	BB4	8850	-520
258	BB4	8925	-520
259	BB5	9000	-520
260	BB5	9075	-520
261	BB5	9150	-520
262	CM	9225	-520
263	CM	9300	-520
264	CM	9375	-520
265	TESTIN3	9450	-520
266	TESTIN4	9525	-520
267	TESTIN5	9600	-520
268	TESTOUT	9675	-520
269	TESTOUT	9750	-520
270	TESTOUT	9825	-520
271	DUMMY	9900	-520
272	DUMMY	9975	-520
273	VCOM	10050	-520
274	VCOM	10125	-520
275	VCOM	10200	-520
276	NC	10275	-520
277	NC	10350	-520
278	NC	10379.5	574
279	NC	10326.5	444
280	G1	10273.5	574
281	G3	10246.5	444
282	G5	10219.5	574
283	G7	10192.5	444
284	G9	10165.5	574
285	G11	10138.5	444
286	G13	10111.5	574
287	G15	10084.5	444
288	G17	10057.5	574
289	G19	10030.5	444
290	G21	10003.5	574
291	G23	9976.5	444
292	G25	9949.5	574
293	G27	9922.5	444
294	G29	9895.5	574
295	G31	9868.5	444
296	G33	9841.5	574
297	G35	9814.5	444
298	G37	9787.5	574
299	G39	9760.5	444
300	G41	9733.5	574

Pad No.	Name	X	Y
301	G43	9706.5	444
302	G45	9679.5	574
303	G47	9652.5	444
304	G49	9625.5	574
305	G51	9598.5	444
306	G53	9571.5	574
307	G55	9544.5	444
308	G57	9517.5	574
309	G59	9490.5	444
310	G61	9463.5	574
311	G63	9436.5	444
312	G65	9409.5	574
313	G67	9382.5	444
314	G69	9355.5	574
315	G71	9328.5	444
316	G73	9301.5	574
317	G75	9274.5	444
318	G77	9247.5	574
319	G79	9220.5	444
320	G81	9193.5	574
321	G83	9166.5	444
322	G85	9139.5	574
323	G87	9112.5	444
324	G89	9085.5	574
325	G91	9058.5	444
326	G93	9031.5	574
327	G95	9004.5	444
328	G97	8977.5	574
329	G99	8950.5	444
330	G101	8923.5	574
331	G103	8896.5	444
332	G105	8869.5	574
333	G107	8842.5	444
334	G109	8815.5	574
335	G111	8788.5	444
336	NC	8761.5	574
337	NC	8734.5	444
338	G113	8707.5	574
339	G115	8680.5	444
340	G117	8653.5	574
341	G119	8626.5	444
342	G121	8599.5	574
343	G123	8572.5	444
344	G125	8545.5	574
345	G127	8518.5	444
346	G129	8491.5	574
347	G131	8464.5	444
348	G133	8437.5	574
349	G135	8410.5	444
350	G137	8383.5	574
351	G139	8356.5	444
352	G141	8329.5	574
353	G143	8302.5	444
354	G145	8275.5	574
355	G147	8248.5	444
356	G149	8221.5	574
357	G151	8194.5	444
358	G153	8167.5	574
359	G155	8140.5	444
360	G157	8113.5	574

Pad No.	Name	X	Y
361	G159	8086.5	444
362	G161	8059.5	574
363	G163	8032.5	444
364	G165	8005.5	574
365	G167	7978.5	444
366	G169	7951.5	574
367	G171	7924.5	444
368	G173	7897.5	574
369	G175	7870.5	444
370	G177	7843.5	574
371	G179	7816.5	444
372	G181	7789.5	574
373	G183	7762.5	444
374	G185	7735.5	574
375	G187	7708.5	444
376	G189	7681.5	574
377	G191	7654.5	444
378	G193	7627.5	574
379	G195	7600.5	444
380	G197	7573.5	574
381	G199	7546.5	444
382	G201	7519.5	574
383	G203	7492.5	444
384	G205	7465.5	574
385	G207	7438.5	444
386	G209	7411.5	574
387	G211	7384.5	444
388	G213	7357.5	574
389	G215	7330.5	444
390	G217	7303.5	574
391	G219	7276.5	444
392	GTESTR	7249.5	574
393	NC	7222.5	444
394	NC	7195.5	574
395	S527	7168.5	444
396	S526	7141.5	574
397	S525	7114.5	444
398	S524	7087.5	574
399	S523	7060.5	444
400	S522	7033.5	574
401	S521	7006.5	444
402	S520	6979.5	574
403	S519	6952.5	444
404	S518	6925.5	574
405	S517	6898.5	444
406	S516	6871.5	574
407	S515	6844.5	444
408	S514	6817.5	574
409	S513	6790.5	444
410	S512	6763.5	574
411	S511	6736.5	444
412	S510	6709.5	574
413	S509	6682.5	444
414	S508	6655.5	574
415	S507	6628.5	444
416	S506	6601.5	574
417	S505	6574.5	444
418	S504	6547.5	574
419	S503	6520.5	444
420	S502	6493.5	574

Pad No.	Name	X	Y
421	S501	6466.5	444
422	S500	6439.5	574
423	S499	6412.5	444
424	S498	6385.5	574
425	S497	6358.5	444
426	S496	6331.5	574
427	S495	6304.5	444
428	S494	6277.5	574
429	S493	6250.5	444
430	S492	6223.5	574
431	S491	6196.5	444
432	S490	6169.5	574
433	S489	6142.5	444
434	S488	6115.5	574
435	S487	6088.5	444
436	S486	6061.5	574
437	S485	6034.5	444
438	S484	6007.5	574
439	S483	5980.5	444
440	S482	5953.5	574
441	S481	5926.5	444
442	S480	5899.5	574
443	S479	5872.5	444
444	S478	5845.5	574
445	S477	5818.5	444
446	S476	5791.5	574
447	S475	5764.5	444
448	S474	5737.5	574
449	S473	5710.5	444
450	S472	5683.5	574
451	S471	5656.5	444
452	S470	5629.5	574
453	S469	5602.5	444
454	S468	5575.5	574
455	S467	5548.5	444
456	S466	5521.5	574
457	S465	5494.5	444
458	S464	5467.5	574
459	S463	5440.5	444
460	S462	5413.5	574
461	S461	5386.5	444
462	S460	5359.5	574
463	S459	5332.5	444
464	S458	5305.5	574
465	S457	5278.5	444
466	S456	5251.5	574
467	S455	5224.5	444
468	S454	5197.5	574
469	S453	5170.5	444
470	S452	5143.5	574
471	S451	5116.5	444
472	S450	5089.5	574
473	S449	5062.5	444
474	S448	5035.5	574
475	S447	5008.5	444
476	S446	4981.5	574
477	S445	4954.5	444
478	S444	4927.5	574
479	S443	4900.5	444
480	S442	4873.5	574

Table 2–2. Pad Coordinate (3/5)

Pad No.	Name	X	Y
481	S441	4846.5	444
482	S440	4819.5	574
483	S439	4792.5	444
484	S438	4765.5	574
485	S437	4738.5	444
486	S436	4711.5	574
487	S435	4684.5	444
488	S434	4657.5	574
489	S433	4630.5	444
490	S432	4603.5	574
491	S431	4576.5	444
492	S430	4549.5	574
493	S429	4522.5	444
494	S428	4495.5	574
495	S427	4468.5	444
496	S426	4441.5	574
497	S425	4414.5	444
498	S424	4387.5	574
499	S423	4360.5	444
500	S422	4333.5	574
501	S421	4306.5	444
502	S420	4279.5	574
503	S419	4252.5	444
504	S418	4225.5	574
505	S417	4198.5	444
506	S416	4171.5	574
507	S415	4144.5	444
508	S414	4117.5	574
509	S413	4090.5	444
510	S412	4063.5	574
511	S411	4036.5	444
512	S410	4009.5	574
513	S409	3982.5	444
514	S408	3955.5	574
515	S407	3928.5	444
516	S406	3901.5	574
517	S405	3874.5	444
518	S404	3847.5	574
519	S403	3820.5	444
520	S402	3793.5	574
521	S401	3766.5	444
522	S400	3739.5	574
523	S399	3712.5	444
524	S398	3685.5	574
525	S397	3658.5	444
526	S396	3631.5	574
527	S395	3604.5	444
528	S394	3577.5	574
529	S393	3550.5	444
530	S392	3523.5	574
531	S391	3496.5	444
532	S390	3469.5	574
533	S389	3442.5	444
534	S388	3415.5	574
535	S387	3388.5	444
536	S386	3361.5	574
537	S385	3334.5	444
538	S384	3307.5	574
539	S383	3280.5	444
540	S382	3253.5	574
541	S381	3226.5	444
542	S380	3199.5	574
543	S379	3172.5	444
544	S378	3145.5	574
545	S377	3118.5	444
546	S376	3091.5	574
547	S375	3064.5	444
548	S374	3037.5	574
549	S373	3010.5	444
550	S372	2983.5	574
551	S371	2956.5	444
552	S370	2929.5	574
553	S369	2902.5	444
554	S368	2875.5	574
555	S367	2848.5	444
556	S366	2821.5	574
557	S365	2794.5	444
558	S364	2767.5	574
559	S363	2740.5	444
560	S362	2713.5	574
561	S361	2686.5	444
562	S360	2659.5	574
563	S359	2632.5	444
564	S358	2605.5	574
565	S357	2578.5	444
566	S356	2551.5	574
567	S355	2524.5	444
568	S354	2497.5	574
569	S353	2470.5	444
570	S352	2443.5	574
571	S351	2416.5	444
572	S350	2389.5	574
573	S349	2362.5	444
574	S348	2335.5	574
575	S347	2308.5	444
576	S346	2281.5	574
577	S345	2254.5	444
578	S344	2227.5	574
579	S343	2200.5	444
580	S342	2173.5	574
581	S341	2146.5	444
582	S340	2119.5	574
583	S339	2092.5	444
584	S338	2065.5	574
585	S337	2038.5	444
586	S336	2011.5	574
587	S335	1984.5	444
588	S334	1957.5	574
589	S333	1930.5	444
590	S332	1903.5	574
591	S331	1876.5	444
592	S330	1849.5	574
593	S329	1822.5	444
594	S328	1795.5	574
595	S327	1768.5	444
596	S326	1741.5	574
597	S325	1714.5	444
598	S324	1687.5	574
599	S323	1660.5	444
600	S322	1633.5	574
601	S321	1606.5	444
602	S320	1579.5	574
603	S319	1552.5	444
604	S318	1525.5	574
605	S317	1498.5	444
606	S316	1471.5	574
607	S315	1444.5	444
608	S314	1417.5	574
609	S313	1390.5	444
610	S312	1363.5	574
611	S311	1336.5	444
612	S310	1309.5	574
613	S309	1282.5	444
614	S308	1255.5	574
615	S307	1228.5	444
616	S306	1201.5	574
617	S305	1174.5	444
618	S304	1147.5	574
619	S303	1120.5	444
620	S302	1093.5	574
621	S301	1066.5	444
622	S300	1039.5	574
623	S299	1012.5	444
624	S298	985.5	574
625	S297	958.5	444
626	S296	931.5	574
627	S295	904.5	444
628	S294	877.5	574
629	S293	850.5	444
630	S292	823.5	574
631	S291	796.5	444
632	S290	769.5	574
633	S289	742.5	444
634	S288	715.5	574
635	S287	688.5	444
636	S286	661.5	574
637	S285	634.5	444
638	S284	607.5	574
639	S283	580.5	444
640	S282	553.5	574
641	S281	526.5	444
642	S280	499.5	574
643	S279	472.5	444
644	S278	445.5	574
645	S277	418.5	444
646	S276	391.5	574
647	S275	364.5	444
648	S274	337.5	574
649	S273	310.5	444
650	S272	283.5	574
651	S271	256.5	444
652	S270	229.5	574
653	S269	202.5	444
654	S268	175.5	574
655	S267	148.5	444
656	S266	121.5	574
657	S265	94.5	444
658	S264	67.5	574
659	NC	40.5	444
660	NC	13.5	574
661	NC	-13.5	444
662	NC	-40.5	574
663	S263	-67.5	444
664	S262	-94.5	574
665	S261	-121.5	444
666	S260	-148.5	574
667	S259	-175.5	444
668	S258	-202.5	574
669	S257	-229.5	444
670	S256	-256.5	574
671	S255	-283.5	444
672	S254	-310.5	574
673	S253	-337.5	444
674	S252	-364.5	574
675	S251	-391.5	444
676	S250	-418.5	574
677	S249	-445.5	444
678	S248	-472.5	574
679	S247	-499.5	444
680	S246	-526.5	574
681	S245	-553.5	444
682	S244	-580.5	574
683	S243	-607.5	444
684	S242	-634.5	574
685	S241	-661.5	444
686	S240	-688.5	574
687	S239	-715.5	444
688	S238	-742.5	574
689	S237	-769.5	444
690	S236	-796.5	574
691	S235	-823.5	444
692	S234	-850.5	574
693	S233	-877.5	444
694	S232	-904.5	574
695	S231	-931.5	444
696	S230	-958.5	574
697	S229	-985.5	444
698	S228	-1012.5	574
699	S227	-1039.5	444
700	S226	-1066.5	574
701	S225	-1093.5	444
702	S224	-1120.5	574
703	S223	-1147.5	444
704	S222	-1174.5	574
705	S221	-1201.5	444
706	S220	-1228.5	574
707	S219	-1255.5	444
708	S218	-1282.5	574
709	S217	-1309.5	444
710	S216	-1336.5	574
711	S215	-1363.5	444
712	S214	-1390.5	574
713	S213	-1417.5	444
714	S212	-1444.5	574
715	S211	-1471.5	444
716	S210	-1498.5	574
717	S209	-1525.5	444
718	S208	-1552.5	574
719	S207	-1579.5	444
720	S206	-1606.5	574

Table 2–2. Pad Coordinate (4/5)

Pad No.	Name	X	Y
721	S205	-1633.5	444
722	S204	-1660.5	574
723	S203	-1687.5	444
724	S202	-1714.5	574
725	S201	-1741.5	444
726	S200	-1768.5	574
727	S199	-1795.5	444
728	S198	-1822.5	574
729	S197	-1849.5	444
730	S196	-1876.5	574
731	S195	-1903.5	444
732	S194	-1930.5	574
733	S193	-1957.5	444
734	S192	-1984.5	574
735	S191	-2011.5	444
736	S190	-2038.5	574
737	S189	-2065.5	444
738	S188	-2092.5	574
739	S187	-2119.5	444
740	S186	-2146.5	574
741	S185	-2173.5	444
742	S184	-2200.5	574
743	S183	-2227.5	444
744	S182	-2254.5	574
745	S181	-2281.5	444
746	S180	-2308.5	574
747	S179	-2335.5	444
748	S178	-2362.5	574
749	S177	-2389.5	444
750	S176	-2416.5	574
751	S175	-2443.5	444
752	S174	-2470.5	574
753	S173	-2497.5	444
754	S172	-2524.5	574
755	S171	-2551.5	444
756	S170	-2578.5	574
757	S169	-2605.5	444
758	S168	-2632.5	574
759	S167	-2659.5	444
760	S166	-2686.5	574
761	S165	-2713.5	444
762	S164	-2740.5	574
763	S163	-2767.5	444
764	S162	-2794.5	574
765	S161	-2821.5	444
766	S160	-2848.5	574
767	S159	-2875.5	444
768	S158	-2902.5	574
769	S157	-2929.5	444
770	S156	-2956.5	574
771	S155	-2983.5	444
772	S154	-3010.5	574
773	S153	-3037.5	444
774	S152	-3064.5	574
775	S151	-3091.5	444
776	S150	-3118.5	574
777	S149	-3145.5	444
778	S148	-3172.5	574
779	S147	-3199.5	444
780	S146	-3226.5	574
781	S145	-3253.5	444
782	S144	-3280.5	574
783	S143	-3307.5	444
784	S142	-3334.5	574
785	S141	-3361.5	444
786	S140	-3388.5	574
787	S139	-3415.5	444
788	S138	-3442.5	574
789	S137	-3469.5	444
790	S136	-3496.5	574
791	S135	-3523.5	444
792	S134	-3550.5	574
793	S133	-3577.5	444
794	S132	-3604.5	574
795	S131	-3631.5	444
796	S130	-3658.5	574
797	S129	-3685.5	444
798	S128	-3712.5	574
799	S127	-3739.5	444
800	S126	-3766.5	574
801	S125	-3793.5	444
802	S124	-3820.5	574
803	S123	-3847.5	444
804	S122	-3874.5	574
805	S121	-3901.5	444
806	S120	-3928.5	574
807	S119	-3955.5	444
808	S118	-3982.5	574
809	S117	-4009.5	444
810	S116	-4036.5	574
811	S115	-4063.5	444
812	S114	-4090.5	574
813	S113	-4117.5	444
814	S112	-4144.5	574
815	S111	-4171.5	444
816	S110	-4198.5	574
817	S109	-4225.5	444
818	S108	-4252.5	574
819	S107	-4279.5	444
820	S106	-4306.5	574
821	S105	-4333.5	444
822	S104	-4360.5	574
823	S103	-4387.5	444
824	S102	-4414.5	574
825	S101	-4441.5	444
826	S100	-4468.5	574
827	S99	-4495.5	444
828	S98	-4522.5	574
829	S97	-4549.5	444
830	S96	-4576.5	574
831	S95	-4603.5	444
832	S94	-4630.5	574
833	S93	-4657.5	444
834	S92	-4684.5	574
835	S91	-4711.5	444
836	S90	-4738.5	574
837	S89	-4765.5	444
838	S88	-4792.5	574
839	S87	-4819.5	444
840	S86	-4846.5	574
841	S85	-4873.5	444
842	S84	-4900.5	574
843	S83	-4927.5	444
844	S82	-4954.5	574
845	S81	-4981.5	444
846	S80	-5008.5	574
847	S79	-5035.5	444
848	S78	-5062.5	574
849	S77	-5089.5	444
850	S76	-5116.5	574
851	S75	-5143.5	444
852	S74	-5170.5	574
853	S73	-5197.5	444
854	S72	-5224.5	574
855	S71	-5251.5	444
856	S70	-5278.5	574
857	S69	-5305.5	444
858	S68	-5332.5	574
859	S67	-5359.5	444
860	S66	-5386.5	574
861	S65	-5413.5	444
862	S64	-5440.5	574
863	S63	-5467.5	444
864	S62	-5494.5	574
865	S61	-5521.5	444
866	S60	-5548.5	574
867	S59	-5575.5	444
868	S58	-5602.5	574
869	S57	-5629.5	444
870	S56	-5656.5	574
871	S55	-5683.5	444
872	S54	-5710.5	574
873	S53	-5737.5	444
874	S52	-5764.5	574
875	S51	-5791.5	444
876	S50	-5818.5	574
877	S49	-5845.5	444
878	S48	-5872.5	574
879	S47	-5899.5	444
880	S46	-5926.5	574
881	S45	-5953.5	444
882	S44	-5980.5	574
883	S43	-6007.5	444
884	S42	-6034.5	574
885	S41	-6061.5	444
886	S40	-6088.5	574
887	S39	-6115.5	444
888	S38	-6142.5	574
889	S37	-6169.5	444
890	S36	-6196.5	574
891	S35	-6223.5	444
892	S34	-6250.5	574
893	S33	-6277.5	444
894	S32	-6304.5	574
895	S31	-6331.5	444
896	S30	-6358.5	574
897	S29	-6385.5	444
898	S28	-6412.5	574
899	S27	-6439.5	444
900	S26	-6466.5	574
901	S25	-6493.5	444
902	S24	-6520.5	574
903	S23	-6547.5	444
904	S22	-6574.5	574
905	S21	-6601.5	444
906	S20	-6628.5	574
907	S19	-6655.5	444
908	S18	-6682.5	574
909	S17	-6709.5	444
910	S16	-6736.5	574
911	S15	-6763.5	444
912	S14	-6790.5	574
913	S13	-6817.5	444
914	S12	-6844.5	574
915	S11	-6871.5	444
916	S10	-6898.5	574
917	S9	-6925.5	444
918	S8	-6952.5	574
919	S7	-6979.5	444
920	S6	-7006.5	574
921	S5	-7033.5	444
922	S4	-7060.5	574
923	S3	-7087.5	444
924	S2	-7114.5	574
925	S1	-7141.5	444
926	S0	-7168.5	574
927	NC	-7195.5	444
928	NC	-7222.5	574
929	G218	-7249.5	444
930	G216	-7276.5	574
931	G214	-7303.5	444
932	G212	-7330.5	574
933	G210	-7357.5	444
934	G208	-7384.5	574
935	G206	-7411.5	444
936	G204	-7438.5	574
937	G202	-7465.5	444
938	G200	-7492.5	574
939	G198	-7519.5	444
940	G196	-7546.5	574
941	G194	-7573.5	444
942	G192	-7600.5	574
943	G190	-7627.5	444
944	G188	-7654.5	574
945	G186	-7681.5	444
946	G184	-7708.5	574
947	G182	-7735.5	444
948	G180	-7762.5	574
949	G178	-7789.5	444
950	G176	-7816.5	574
951	G174	-7843.5	444
952	G172	-7870.5	574
953	G170	-7897.5	444
954	G168	-7924.5	574
955	G166	-7951.5	444
956	G164	-7978.5	574
957	G162	-8005.5	444
958	G160	-8032.5	574
959	G158	-8059.5	444
960	G156	-8086.5	574

Table 2–2. Pad Coordinate (5/5)

Pad No.	Name	X	Y
961	G154	-8113.5	444
962	G152	-8140.5	574
963	G150	-8167.5	444
964	G148	-8194.5	574
965	G146	-8221.5	444
966	G144	-8248.5	574
967	G142	-8275.5	444
968	G140	-8302.5	574
969	G138	-8329.5	444
970	G136	-8356.5	574
971	G134	-8383.5	444
972	G132	-8410.5	574
973	G130	-8437.5	444
974	G128	-8464.5	574
975	G126	-8491.5	444
976	G124	-8518.5	574
977	G122	-8545.5	444
978	G120	-8572.5	574
979	G118	-8599.5	444
980	G116	-8626.5	574
981	G114	-8653.5	444
982	G112	-8680.5	574
983	G110	-8707.5	444
984	G108	-8734.5	574
985	G106	-8761.5	444
986	NC	-8788.5	574
987	NC	-8815.5	444
988	G104	-8842.5	574
989	G102	-8869.5	444
990	G100	-8896.5	574
991	G98	-8923.5	444
992	G96	-8950.5	574
993	G94	-8977.5	444
994	G92	-9004.5	574
995	G90	-9031.5	444
996	G88	-9058.5	574
997	G86	-9085.5	444
998	G84	-9112.5	574
999	G82	-9139.5	444
1000	G80	-9166.5	574
1001	G78	-9193.5	444
1002	G76	-9220.5	574
1003	G74	-9247.5	444
1004	G72	-9274.5	574
1005	G70	-9301.5	444
1006	G68	-9328.5	574
1007	G66	-9355.5	444
1008	G64	-9382.5	574
1009	G62	-9409.5	444
1010	G60	-9436.5	574
1011	G58	-9463.5	444
1012	G56	-9490.5	574
1013	G54	-9517.5	444
1014	G52	-9544.5	574
1015	G50	-9571.5	444
1016	G48	-9598.5	574
1017	G46	-9625.5	444
1018	G44	-9652.5	574
1019	G42	-9679.5	444
1020	G40	-9706.5	574
1021	G38	-9733.5	444
1022	G36	-9760.5	574
1023	G34	-9787.5	444
1024	G32	-9814.5	574
1025	G30	-9841.5	444
1026	G28	-9868.5	574
1027	G26	-9895.5	444
1028	G24	-9922.5	574
1029	G22	-9949.5	444
1030	G20	-9976.5	574
1031	G18	-10003.5	444
1032	G16	-10030.5	574
1033	G14	-10057.5	444
1034	G12	-10084.5	574
1035	G10	-10111.5	444
1036	G8	-10138.5	574
1037	G6	-10165.5	444
1038	G4	-10192.5	574
1039	G2	-10219.5	444
1040	G0	-10246.5	574
1041	GTESTL	-10273.5	444
1042	NC	-10326.5	574
1043	NC	-10379.5	444

Table 2–3. Test Pad Coordinate (no bump)

Pad No.	Name	X	Y
1	VSS3	-236	-10370
2	VDC	-211	-10260
3	VSS	-186	-10370
4	VDD	-161	-10260
5	VCC2	-136	-10370
6	VCC1	-111	-10260
7	VDD1	-86	-10370
8	ROMRV	-61	-10260
9	DOTCLK	-36	-10370
10	VSTBY	-11	-10260
11	RESETB	14	-10370
12	CSB	39	-10260
13	SCK	64	-10370
14	SDI	89	-10260
15	SDO	114	-10370
16	ATEST3	139	-10260
17	SPID	164	-10370

Remark These pins belong to no bumps. Therefore, there are not above mentioned pins inside block diagram.

3. PIN DESCRIPTIONS

3.1 Power Supply Pins

Symbol	Pad No.	I/O	Description
V_{DD}	57, 148 to 151	–	System power supply for internal logic.
V_{DDIO}	153, 154, 170, 176, 182, 188, 207	–	Voltage input pin for I/O logic. - Connect to system V_{DD}
V_{SS}	21, 48, 49, 113 to 120, 122 to 125, 127 to 130, 132 to 136, 167, 173, 179, 185, 191	–	System ground (0 V)
VCI	56, 138 to 147	–	Step-up input voltage pin. - Connect to voltage source between 2.5 to 3.3 V
VCIX2	83 to 89	Output	A power output pin for analog circuit that is generated from DC/DC converter circuit 1. Connect a capacitor to this pin for stabilization. And VCIX2 output voltage is limited to 5.5 V by internal limiter circuit.
VCI2	79 to 81	Output	A negative power output pin for analog circuit. Connect a capacitor to this pin for stabilization. VCI2 output voltage is (–VCI).
VLCD63	90 to 97	Output	A reference voltage level for gray-scale voltage generator. Connect a capacitor to this pin for stabilization.
VCOM	3 to 5, 273 to 275	Output	Output pin for TFT-LCD common.
VCOMH	67 to 69, 99 to 101	Output	A regulator output for VCOM output “High” level. Connect a capacitor to this pin for stabilization.
VCOML	64 to 66, 76 to 78	Output	A regulator output for VCOM output “Low” level. Connect a capacitor to this pin for stabilization.
EXVR	109	Input	External reference of internal Gamma resistor. - Connect to V_{SS}
VCOMR	110, 111	Input	This pin provides voltage reference for internal voltage regulator when register VDV [4:0] of **13.8 Power Supply Control 4 (R0DH)** set to “01111”. - Connect to an external voltage source for reference
VGH	73 to 75	Output	A positive power output pin for gate driver. - Connect a capacitor for stabilization
VGL	70 to 72	Output	A negative power output pin for gate driver. - Connect a capacitor for stabilization
CXP, CXN	58 to 63	–	Connect capacitor between CXP and CXN.
CYP, CYN	50 to 55	–	Connect capacitor between CYP and CYN.
C1P, C1N	42 to 47	–	Connect capacitor between C1P and C1N.
C2P, C2N	34 to 39	–	Connect capacitor between C2P and C2N.
C3P, C3N	28 to 33	–	Connect capacitor between C3P and C3N.

3.2 Interface Pins

(1/2)

Symbol	Pad No.	I/O	Description
RL	189, 190	Input	This pin's setting is valid. Source output direction is controlled as follows. - Connect to V_{DDIO}: S0 → S527 source driving mode. - Connect to V_{SS}: S527 → S0 source driving mode.
TB	186, 187	Input	Input pin to select the Gate driver scan direction. - Connect to V_{DDIO} for Gate scan from G0 to G219 - Connect to V_{SS} for Gate scan from G219 to G0
BGR	183, 184	Input	Input pin to select the color mapping. - Connect to V_{DDIO} for Blue-Green-Red mapping - Connect to V_{SS} for Red-Green-Blue mapping
REV	180, 181	Input	Input pin to select the display reversion. - Connect to V_{DDIO} for mapping data "0" to maximum pixel voltage for normally white panel - Connect to V_{SS} for mapping data "0" to minimum pixel voltage for normally black panel
SHUT	192 to 194	Input	This pin's setting is valid. Power circuit Shut down is controlled as follows. High level: Shut down (power off, Standby sequence) Low level: Display on sequence (power circuit start operation sequentially)
CM	262 to 264	Input	Input pin to select 262 K-color or 8-color display mode. After entered 8-color display mode, only MSB of the data Red, Green and Blue will be considered. High level: 8-color display mode Low level: 262 K-color display mode When set to 8-color mode, S0-S527 output VCIX2 voltage and V_{SS} levels for LCD driving.
CSB	161 to 163	Input	Chip Select input pin. High level: μPD161608 is not selected and cannot be accessed. Low level: μPD161608 is selected and can be accessed. When not used this pin, leave it open.
<R> SCK	159, 160	Input	Serial clock input pin for a clock-synchronous serial interface. When not used this pin, leave it open. This pin is also pulled up inside IC.
<R> SDI	157, 158	Input	Serial data input pin for a clock-synchronous serial interface. The input data is latched by the rising edge of SCK signal. When not used this pin, leave it open. This pin is also pulled up inside IC.
SDO	155, 156	Output	Serial data Output pin for a clock-synchronous serial interface. The data is output at the falling edge of SCK signal. When not used this pin, leave it open.
<R> SPID	171, 172	Input	ID selection pin for the SPI serial interface. When sending serial data, the "ID" bit must much with the logic stage of this pin. High level: ID = 1 Low level: ID = 0
DOTCLK	195 to 197	Input	Dot clock signal for RGB interface. A non-stop external clock must be provided to that pin even at front or back porch non-display period. Display data are fetched at rising edge of DOTCLK
ENABLE	204 to 206	Input	Data enabling signal for using RGB interface. High level: Valid (possible to access), it qualifies the valid are of display data input. Low level: Invalid (not possible to access)
CAD	177, 178	Input	Although it is intact, since potential fixation is required, give as low fixation.
TMB	126	Input	Gamma initial value setting pin. High level: Mode 1 Low level: Mode2 This pin is pulled up internally IC. So if this pin leave open, Mode1 is selected.

(2/2)

Symbol	Pad No.	I/O	Description
RR [5:0], GG [5:0], BB [5:0]	208 to 225, 226 to 243, 244 to 261	Input	Graphic Data Input Pins: - RR [5:0] : Red data - 6-bit - GG [5:0] : Green data - 6-bit - BB [5:0] : Blue data - 6-bit
HSYNC	198 to 206	Input	Horizontal Synchronous signal. Active level is low.
VSYNC	201 to 203	Input	Vertical Synchronous signal. Active level is low.
RESETB	164 to 166	Input	Reset input pin. Initializes the IC when low.

3.3 Display Pins

Symbol	Pad No.	I/O	Description
S0 to S527	395 to 658, 663 to 926	Output	Source driver output pins S0, S3, S6, ... S (3n−2): Red display (R) (BGR = Low) S1, S4, S7, ... S (3n−1): Green display (G) (BGR = Low) S2, S5, S8, ... S (3n) : Blue display (B) (BGR = Low)
G0 to G219	929 to 985, 988 to 1040	Output	Gate driver output pins. These pins output VGH, VGL level.

3.4 Internal Power Regulator Pins for Logic Circuit

Symbol	Pad No.	I/O	Description
REGVDD	174, 175	Input	Internal power regulator control input pin. When REGVDD is fixed to L level, the internal regulated power (RVDD) is used as internal logic supply voltage. Be sure to set V_{DDIO} to V_{DD}. When REGVDD is fixed to H level, the external logic power (V_{DD}) is used as internal logic supply voltage. Be sure to set $V_{DDIO} \geq V_{DD}$.
RVDD	103 to 108	Output	Internal power regulated-V_{DDIO} output. When REGVDD is H level, RVDD is connected to V_{DD} pin. And connect with 1.0 μF capacitor between V_{SS}. When REGVDD is L level, RVDD is outputted regulator voltage. And connect with 1.0 μF capacitor between V_{SS}.

3.5 Control Pins

Symbol	Pad No.	I/O	Description
TESTA	98	Output	Use as EEPROM read voltage output. Connect to stabilizer capacitor.
TESTB	41	Output	This pin is auxiliary output of VCIX2. Connect to stabilizer capacitor as necessary.
TESTC	40	−	Unused. Leave this pin open.
CDUM0	8 to 10	Input	This pin is used for test. Leave this pin open.
CDUM1	11 to 13	Input	This pin is used for test. Leave this pin open.
TESTIN1 to TESTIN5	168, 169, 265 to 267	Input	These pins are used for test. Normally, leave it open.
TESTOUT	268 to 270	Output	These pins are used for test. Normally, leave it open.
GTESTR	392	Output	Gate driver test output pin. Leave this pin open.
GTESTL	1041	Output	Gate driver test output pin. Leave this pin open.

4. FUNCTIONAL DESCRIPTION

4.1 External Interface (RGB Interface)

The μPD161608 supports RGB interface as an external interface for motion picture display.

RGB display data of one line (S0 to S527) are latched to the data latch register through parallel data bus (PD) in orderly. If one line data is latched, data latch register data is transferred to the source driver amp and then the display is outputted.

The display data (PD17-PD0) are written according to the control of the data enable signal (ENABLE) in synchronization with the VSYNC, HSYNC, and DOTCLK signals. This performs flicker-free updating of the screen.

Refer to **6. EXTERNAL DISPLAY INTERFACE**.

4.2 System Interface

The μPD161608 builds in a Serial Peripheral Interface port (SPI).

This system interface transfers the data to the internal control register for power control, display control, gamma adjustment.

Table 4–1. Register Selection (Serial Peripheral Interface)

R/W Bit	RS Bit	Operations
0	0	Writes indexes into IR
0	1	Writes instruction into control registers
1	0	Status read
1	1	Instruction data read

4.3 Gray-scale Voltage Generator

The gray-scale voltage generator generates LCD driver voltages which correspond to the gray-scale levels as specified in the gray-scale γ-adjusting resistor. 262,144 possible colors can be displayed at the same time. For details, refer to **16. GAMMA ADJUSTMENT REGISTER**.

4.4 Display Timing Control

The display timing generator generates the interface signals such source output, common output and gate driver from RGB interface signal input.

4.5 Built-in Power Supply Circuit

The built-in power supply circuit generates (powers of) VCIX2, VLCD63, VGH, VGL and VCOM voltages that are corresponded to display the TFT-LCD panel.

4.6 LCD Display Circuit

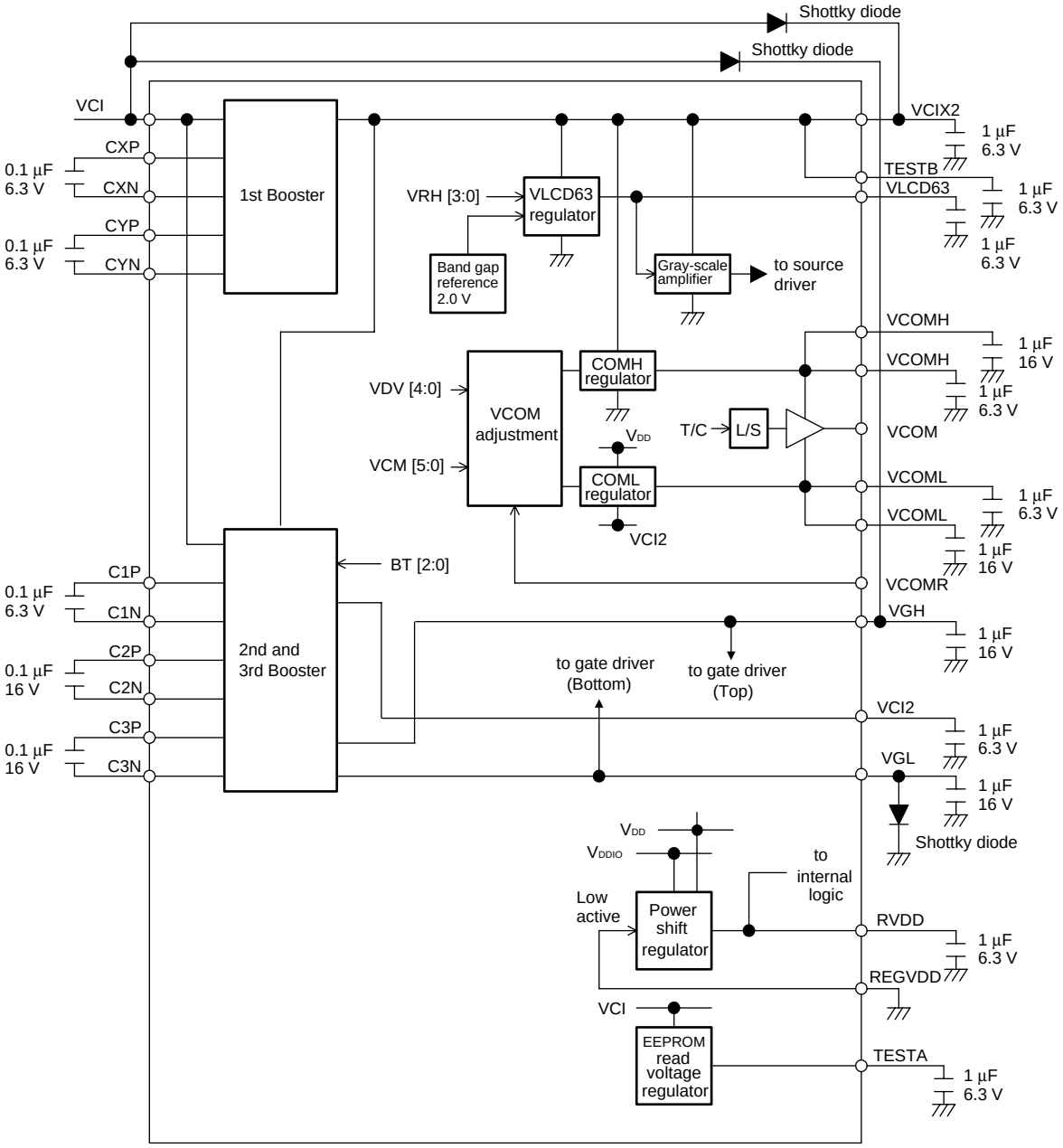
The LCD display circuit consists of 528 source drivers (S0 to S527).

Display pattern data are latched when 528-bit data have arrived. The latched data then enable the source drivers to generate drive waveform outputs. The RL pin can change the shift direction of 528-bit data by selecting an appropriate direction for the device-mounted configuration.

5. POWER SUPPLY CIRCUIT

<R> Figure 5–1 shows a configuration of the voltage generation circuit for the μPD161608. The DC/DC converter circuits consist of DC/DC converter circuits 1, 2 and 3. DC/DC converter circuit 1 doubles the voltage supplied to VCI, and that voltage is doubled or tripled in DC/DC converter circuit 2. And DC/DC converter circuit 3 flips the VCI level and generates the VCI2 level. These DC/DC converter circuits generate power supplies VCIX2, VGH, VGL.

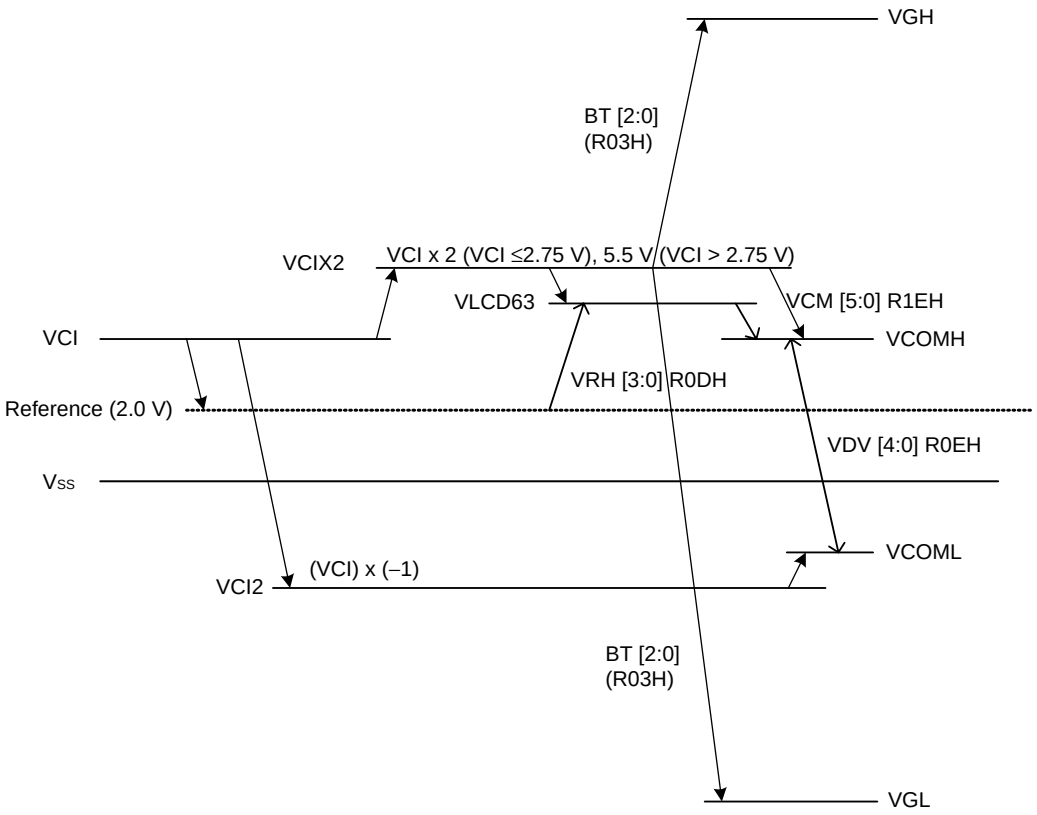
<R> **Figure 5–1. Configuration of the Internal Power Supply Circuit**



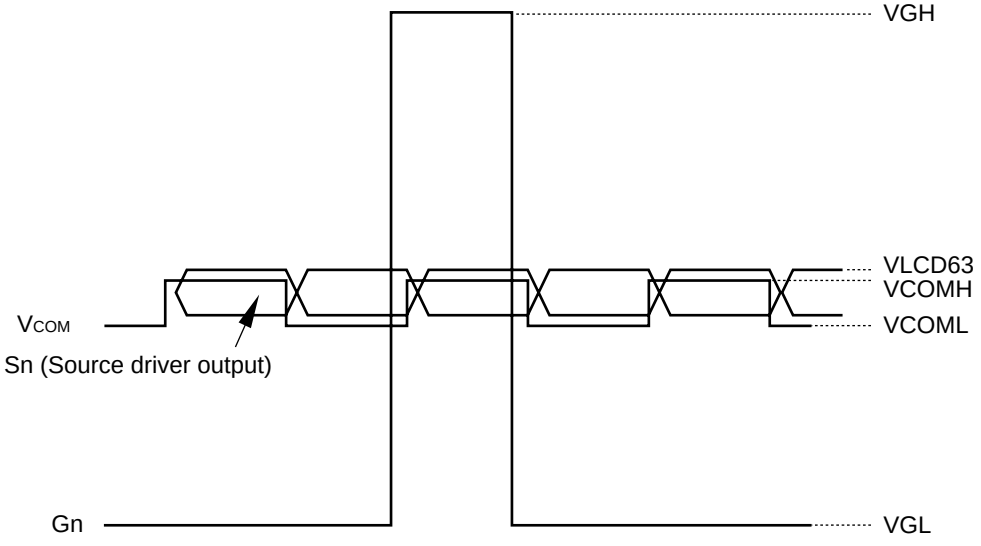
5.1 Pattern Diagrams for Voltage Setting

The following figure shows a pattern diagram of the voltage setting and an example of waveforms.

Figure 5–2. Pattern Diagram



Caution Adjust the conditions of VCIX2-VVLD63 > 0.5 V and VCOML-VCI2 > 0.5 V with loads because they differ depending on the display load to be driven.



5.2 Recommendation Wiring Resistance Value to Each Pin

The wiring resistance value to recommend is shown below. Since wiring resistance influences the current capability of a power supply, it asks for panel design so that it may become below recommendation value.

Pin Name	Wiring Resistance Value (Ω)
V_{SS}	< 10
V_{DD}	< 20
V_{DDIO}	< 20
VCI	< 10
TESTA	< 30
TESTB	< 30
RVDD	< 10
VLCD63	< 10
VCIX2	< 10
VGH	< 30
VGL	< 10
VCI2	< 10
VCOMH	< 10
VCOML	< 10
VCOM	< 10
CXP	< 10
CXN	< 10
CYP	< 10
CYN	< 10
C1P	< 10
C1N	< 10
C2P	< 30
C2N	< 30
C3P	< 30
C3N	< 30

5.3 Recommendation Capacitance Value to Each Pin

The recommendation value of a capacitor is shown below.

Please determine a capacity value, after a module fully evaluates.

Pin Name	Capacitance (μF)
V_{DD}	0.1 to 1
V_{DDIO}	0.1 to 1
VCI	0.1 to 1
TESTA	1 to 2.2
TESTB	1 to 2.2
RVDD	1 to 4.7
VLCD63	1 to 4.7
VCIX2	1 to 4.7
VGH	0.47 to 1
VGL	0.47 to 1
VCI2	1 to 4.7
VCOMH	1 to 4.7
VCOML	1 to 4.7
CXP	0.1 to 2.2
CXN	
CYP	0.1 to 2.2
CYN	
C1P	0.1 to 2.2
C1N	
C2P	0.1 to 1
C2N	
C3P	0.1 to 1
C3N	

5.4 Recommendation of a Schottky Diode

It recommends inserting a schottky diode between VCI-VCIX2, VCI-VGH, and VGL-V_{SS}.

Please fully evaluate by the module.

Recommendation specification

Forward voltage (V_F): 0.6 V at I_F = 200 mA

Reverse current (I_R): 1 μA at V_R = 10 V

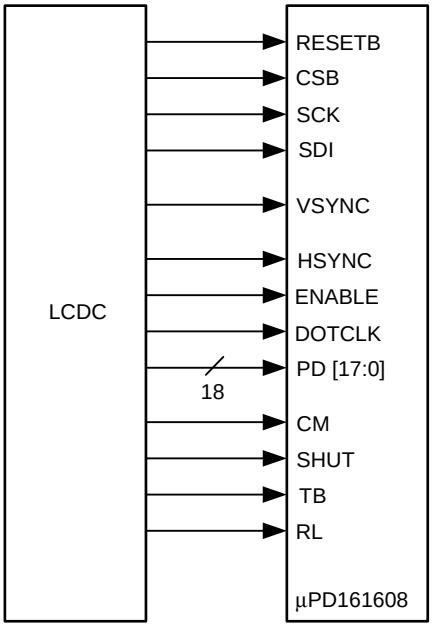
DC reverse voltage (V_R): More than 20 V

6. EXTERNAL DISPLAY INTERFACE

6.1 RGB Interface

The following interfaces are available as external display interface.

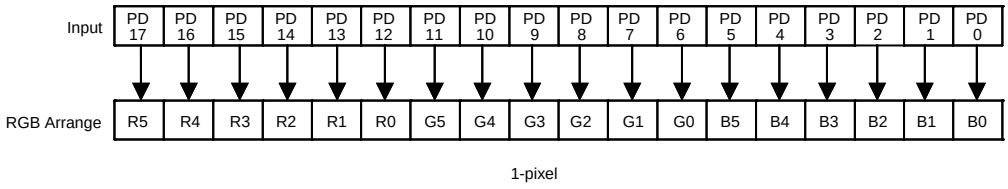
Figure 6–1. Interface Signal Mapping from Graphic Controller



6.2 18-bit RGB Interface

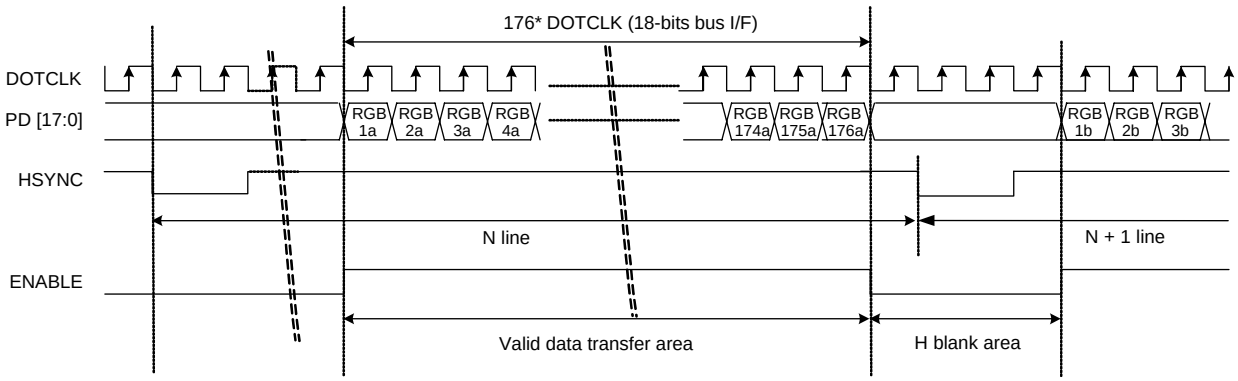
Display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Data for display is transferred via 18-bit RGB data bus (PD17-PD0).

Figure 6–2. RGB Data Arrange in the 18-bit RGB Interface Mode



Remark 262,144-color display is possible using the 18-bit RGB interface.

Figure 6–3. 18-bit RGB Interface Timing



7. SYSTEM INTERFACE

7.1 Serial Data Transfer

It indicates serial data transfer as follows.

(1) The μPD161608 initiates serial data transfer by transferring the start byte at the falling edge of CSB input. It ends serial data transfer at the rising edge of CSB input.

(2) The μPD161608 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the μPD161608. The μPD161608, when selected, receives the subsequent data string.

(3) The ID pin can determine the least significant bit of the identification code. The five upper bits must be 01110. Two different chip addresses must be assigned to a single μPD161608 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, data can be written to the index register or status can be read, and when RS = 1, an instruction can be issued. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is read when the R/W bit is 0, and is written when the R/W bit is 1.

(4) After reading the start byte, the μPD161608 reads or writes the subsequent data byte-by-byte. The data is transferred with the MSB first. All μPD161608 instructions are 16 bits. Two bytes are read with the MSB first, and then the instructions are internally executed. After the start byte has been read, the first byte is transmitted internally as the upper eight bits of the instruction and the second byte is transmitted internally as the lower eight bits of the instruction.

Table 7–1. Start Byte Format

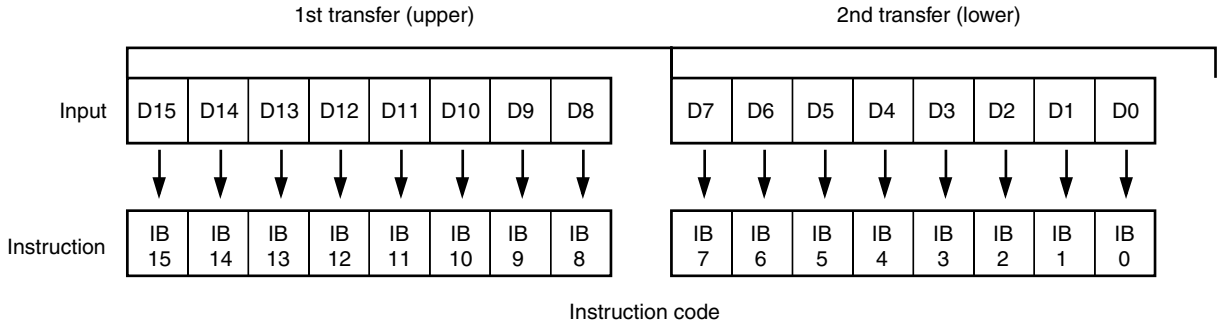
Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Caution ID pin selects ID bit.

Table 7–2. RS and R/W Bit Function

R/W Bit	RS Bit	Operations
0	0	Writes indexes into IR
0	1	Writes instruction into control registers
1	0	Status read
1	1	Instruction data read

Figure 7–1. Instruction of Serial Data Transfer



7.2 Procedure for Transfer on Clock Synchronized Serial Bus Interface

Figure 7–2. Timing Basic Data Transfer through Clock-Synchronized Serial Bus Interface

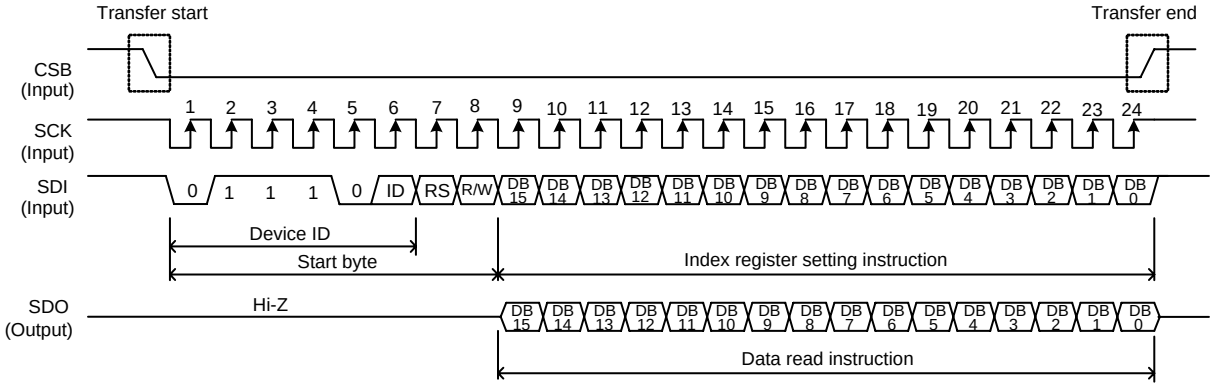
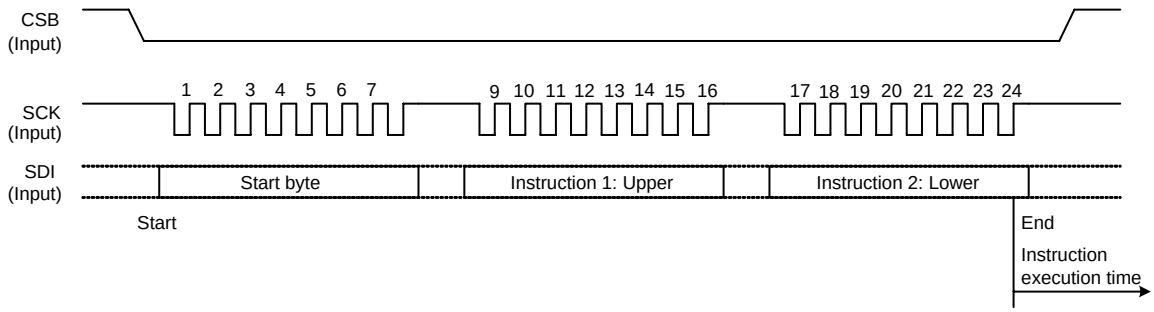


Figure 7–3. Timing of Consecutive Data-Transfer through Clock-synchronized Serial Bus Interface



Caution The first byte after the start byte is always the upper eight bits.

8. TIMING SPECIFICATION

The μPD161608 executes power up/down by internal sequential timing.

Following table shows AC timing characteristics and Figure 8–1 shows horizontal/vertical pixel clock timing (262 K-Full Screen Timing).

8.1 AC Timing Requirements

260 K-color mode and common

Characteristics	Symbol	MIN.	TYP.	MAX.	Unit
Vertical Frequency (Refresh)	f_V	57.2	60.1	63.1	Hz
Horizontal Frequency (Line)	f_H	12.8	13.5	14.1	kHz
DOTCLK frequency	f_{DOTCLK}	2.51	2.64	2.77	MHz
DOTCLK clock period	t_{DOTCLK}	398	379	361	ns
Horizontal Back Porch	t_{HBP}		10		t_{DOTCLK}
Horizontal Front Porch	t_{HFP}		10		t_{DOTCLK}
Horizontal Blanking Period	$t_{HBP} + t_{HFP}$		20		t_{DOTCLK}
Horizontal Display Area	H_{DISP}		176		t_{DOTCLK}
Horizontal Cycle	Hcycle		196		t_{DOTCLK}
VSYNC Back porch	t_{VBP}		3		Line
VSYNC Front porch	t_{VFP}		1		Line
Vertical Blanking Period	$t_{VBP} + t_{VFP}$		4		Line
Vertical Display Area	V_{DISP}		220		Line
Vertical Cycle	Vcycle		224		Line

8-color mode specified

Characteristics	Symbol	MIN.	TYP.	MAX.	Unit
Vertical Frequency (Refresh)	f_V	f_{V8}–5%	f_{V8}	f_{V8}+5%	Hz
Horizontal Frequency (Line)	f_H	f_{H8}–5%	f_{H8}	f_{H8}+5%	kHz
DOTCLK frequency	f_{DOTCLK}	$f_{DOTCLK8}$–5%	$f_{DOTCLK8}$	$f_{DOTCLK8}$+5%	MHz
DOTCLK clock period	t_{DOTCLK}	$t_{DOTCLK8}$–5%	$t_{DOTCLK8}$	$t_{DOTCLK8}$+5%	ns
Vertical Partial Back Porch	V_{PBP}	0		219	Line
Vertical Active Area	V_{PDSP}	1		220	Line

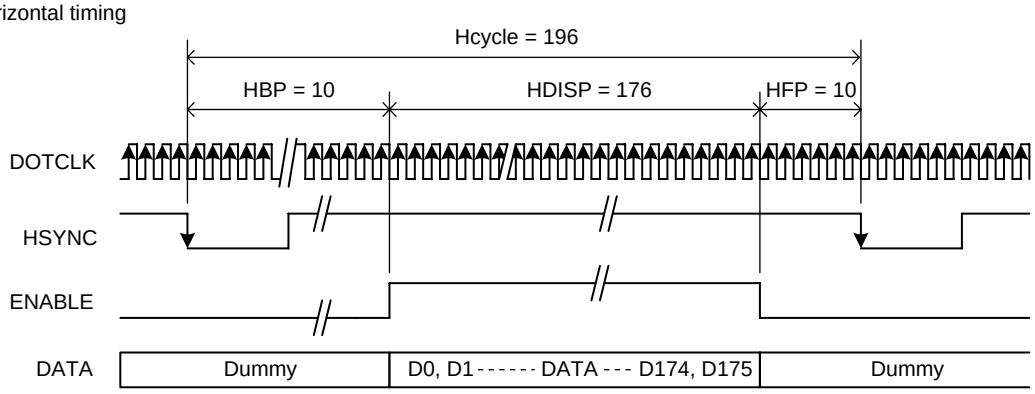
Remark f_{V8}: 30.1 to 60.1Hz, f_{H8}: 6.73 to 13.5 kHz, $f_{DOTCLK8}$: 1.32 to 2.64 MHz, $t_{DOTCLK8}$: 758 to 379 ns

RGB Common timing

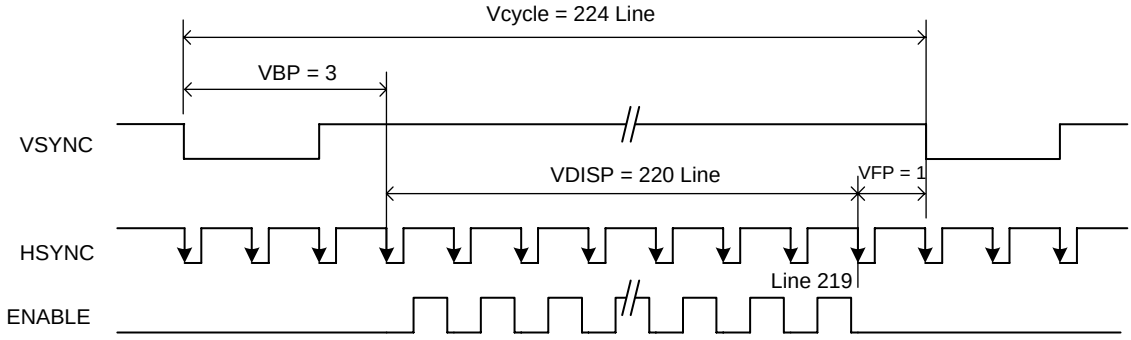
Characteristics	Symbol	MIN.	TYP.	MAX.	Unit
DOTCLK frequency	f_{DOTCLK}	2.51	2.64	2.77	MHz
DOTCLK period	t_{DOTCLK}	398	379	361	ns
Vertical Sync Setup time	t_{VSYS}	30			ns
Vertical Sync Hold time	t_{VSYH}	30			ns
Horizontal Sync Setup time	t_{HSYS}	30			ns
Horizontal Sync Hold time	t_{HSYH}	30			ns
Phase difference of Sync signal Falling Edge	t_{HV}	0		176	t_{DOTCLK}
DOTCLK Low Period	t_{CKL}	150			ns
DOTCLK High Period	t_{CKH}	150			ns
Data Setup time	t_{DS}	40			ns
Data Hold time	t_{DH}	40			ns

Figure 8–1. 262 K-Full Screen Timing

Horizontal timing



Vertical timing



Pixel clock timing

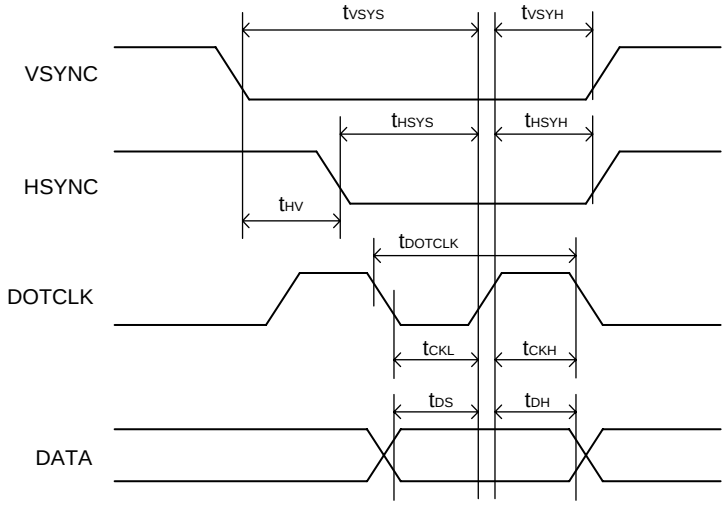
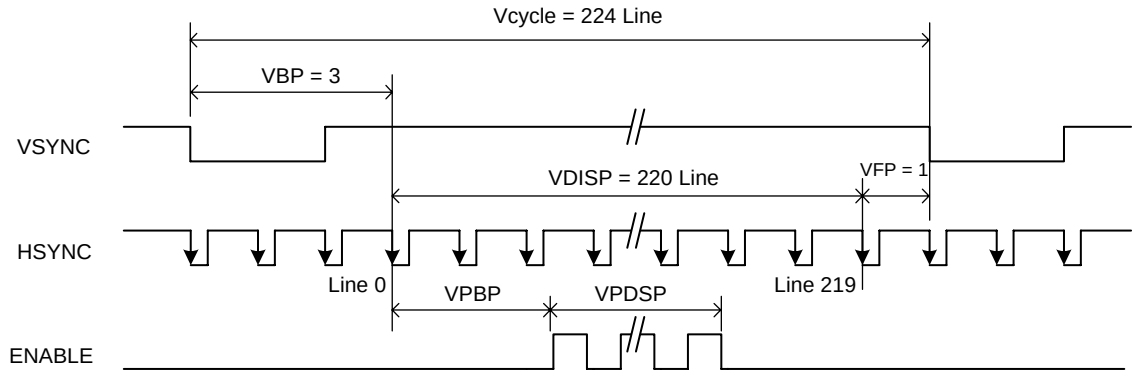
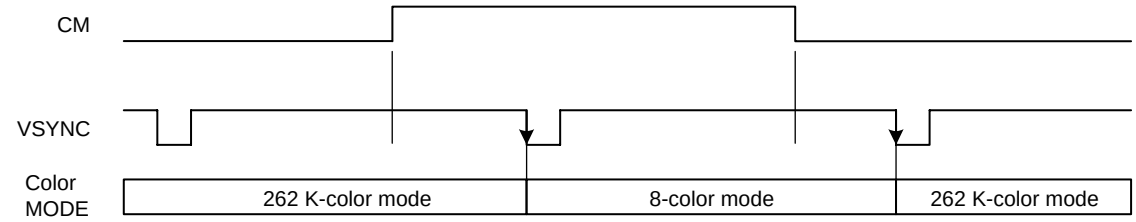


Figure 8–2. 8-color Mode Timing

8-color mode vertical timing



MODE conversion timing



9. POWER UP SEQUENCE

The μPD161608 operates power up and display ON by V_{DD}, SHUT, DOTCLK, HSYNC, and VSYNC as shown as following figure.

<R>

Figure 9–1. Power up Sequence Timing

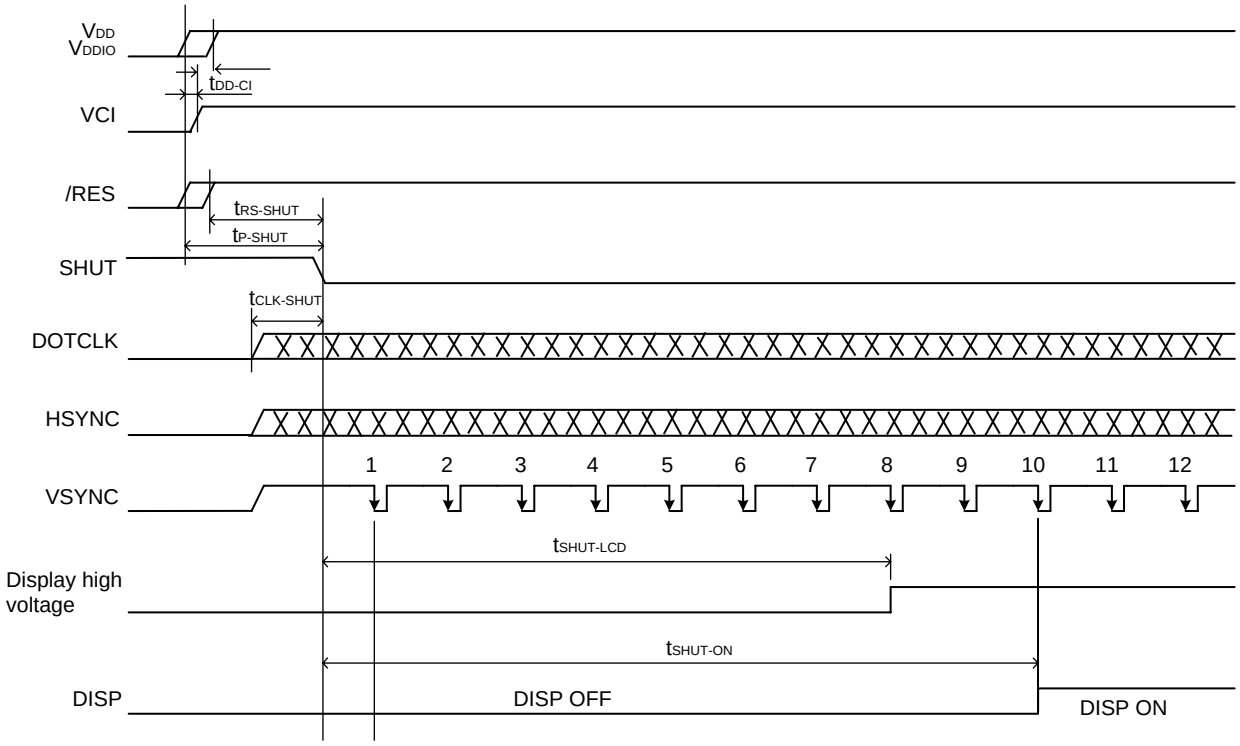


Table 9–1. Power up AC Characteristics

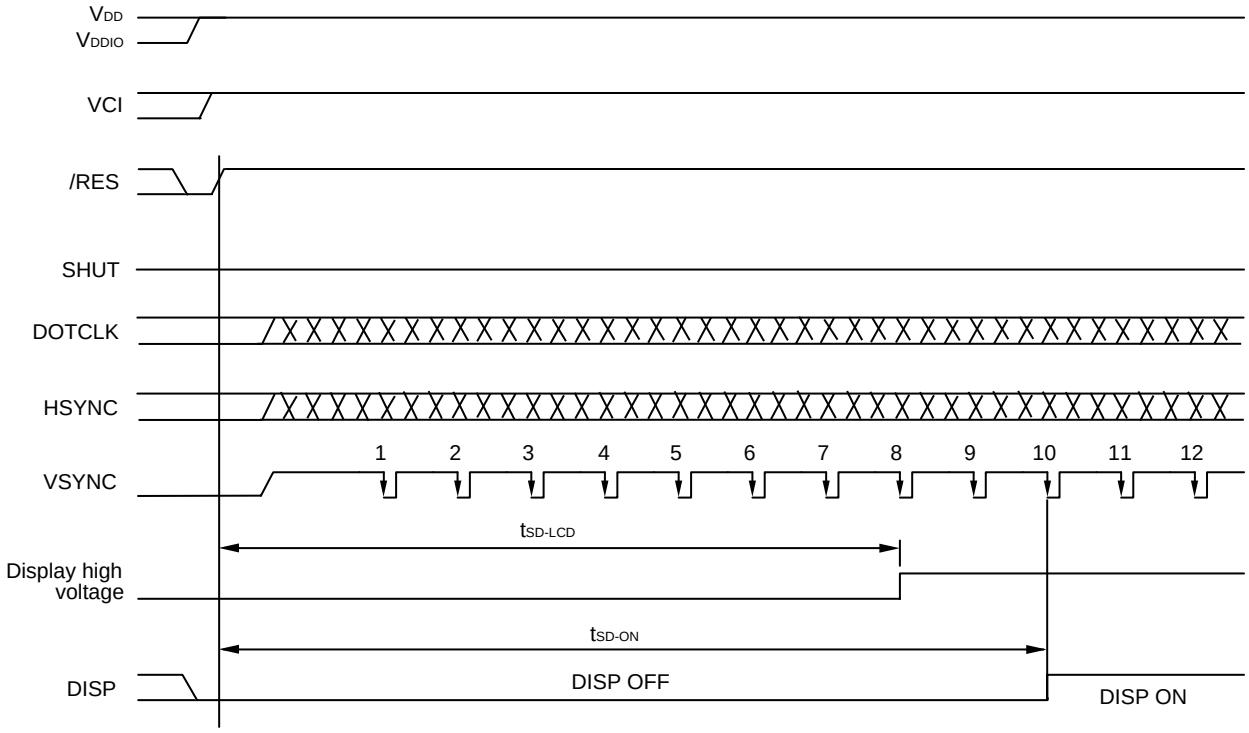
Characteristics	Symbol	MIN.	TYP.	MAX.	Unit
VDD/VCI on to falling edge of SHUT	t_{P-SHUT}	1			ms
/RES to falling edge of SHUT	$t_{RS-SHUT}$	10			μs
DOTCLK input to falling edge of SHUT	$t_{CLK-SHUT}$	1			CLK
Falling edge of SHUT to LCD power ON	$t_{SHUT-LCD}$			128	ms
Falling edge of SHUT to display start	$t_{SHUT-ON}$		166		ms
1H = 196 DOTCLK, 1frame = 224H, DOTCLK = 2.64 MHz			10		Frame

Remark t_{DD-CI} can be ≤ 0 μs, > 0 μs, therefore, V_{DD}, V_{DDIO} and VCI power up sequence should not have any impact on the driver/display functionalities/performance.

10. RECOVERY SEQUENCE WHEN A POWER SUPPLY TURNS OFF MOMENTARILY

The μPD161608 operates power up and display ON by V_{DD}, SHUT, DOTCLK, HSYNC, and VSYNC as shown as following figure when a power supply turns off momentarily.

<R>



11. POWER DOWN SEQUENCE

The μPD161608 operates power off and display OFF by VDD, SHUT, DOTCLK, HSYNC, and SYNC as shown as following figure.

<R>

Figure 11–1. Power down Sequence Timing

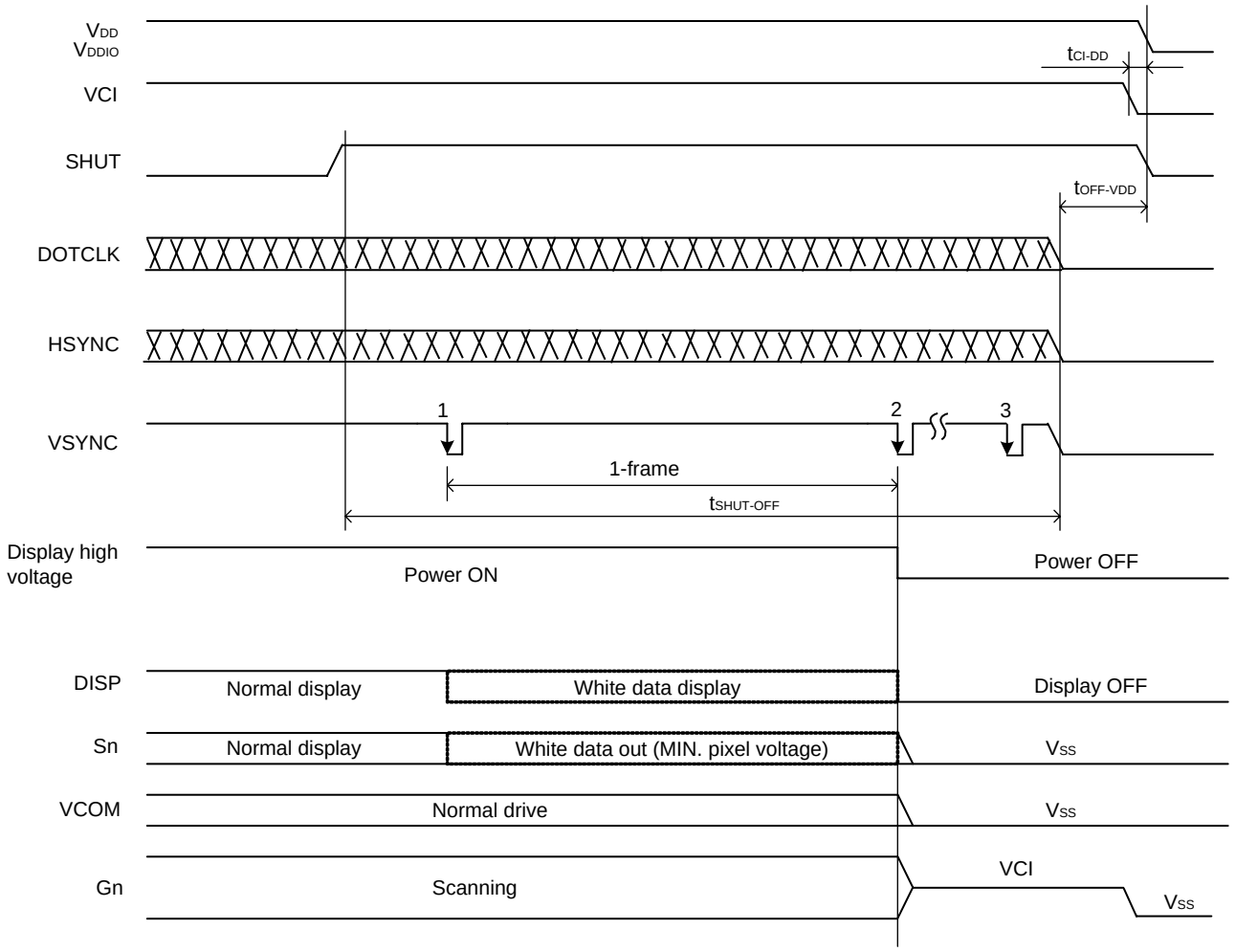


Table 11–1. Power down AC Characteristics

Characteristics	Symbol	MIN.	TYP.	MAX.	Unit
Rising edge of SHUT to display OFF,	$t_{SHUT-OFF}$	50			ms
1H = 196 DOTCLK, 1frame = 224H, DOTCLK = 2.64 MHz		3			Frame
Input-signal-off to V_{DD}/VCI OFF	$t_{OFF-VDD}$	1			μs

Remark t_{CI-DD} can be ≤ 0 μs, > 0 μs, therefore, V_{DD}, V_{DDIO} and VCI power down sequence should not have any impact on the driver/display functionalities/performance.

12. INSTRUCTIONS

12.1 Outline

The operation of the μPD161608 is determined by signals sent through Serial Peripheral Interface (SPI). These signals, which include the register selection signal (RS), the read/write signal (R/W), and the internal 16-bit data bus signals (IB15 to IB0), make up the μPD161608 instructions.

There are five categories of instructions that:

(1) Specify the index
(2) Read the status
(3) Control the display
(4) Control power management
(5) Set gray-scale level for the internal gray-scale palette table

<R> 12.2 Instruction Table

		Upper Code								Lower Code							
Register No.	Register Name	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
-	Index	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0
-	Status Read	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
01H	Driver Output Control	0	0	REV	0	BGR	SM	TB	RL	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
02H	LCD Driving Waveform Control	0	0	0	0	0	0	B/C	EOR	0	NW6	NW5	NW4	NW3	NW2	NW1	NW0
03H	Power Supply Cotrol 1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
04H	Setting Disabled																
05H	Setting Disabled																
06H	Setting Disabled																
07H	Setting Disabled																
08H	Setting Disabled																
09H	Setting Disabled																
0AH	Setting Disabled																
0BH	Frame cycle control	NO1	NO0	SDT1	SDT0	EQ1	EQ0	PT1	PT0	0	0	0	0	0	0	0	0
0CH	Setting Disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0DH	Power Supply Control 3	0	0	0	0	0	0	0	0	0	0	NOTP1	Dummy1	VRH3	VRH2	VRH1	VRH0
0EH	Power Supply Control 4	NOTP2	Dummy2	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
0FH	Gate scan start position	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
10H	Setting Disabled																
11H	Setting Disabled																
12H	Setting Disabled																
13H	Setting Disabled																
14H	Setting Disabled																
15H	Setting Disabled																
16H	Horizontal porch	1	0	1	0	1	1	1	1	0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
17H	Vertical porch	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
18H	Setting Disabled																
19H	Setting Disabled																
1AH	Setting Disabled																
1BH	Setting Disabled																
1CH	Setting Disabled																
1DH	Setting Disabled																
1EH	Power Supply control 5	0	0	0	0	0	0	0	0	NOTP3	Dummy3	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
1FH	Setting Disabled																
20H	Setting Disabled																
21H	Setting Disabled																
22H	Setting Disabled																
23H	Setting Disabled																
24H	Setting Disabled																
25H	Setting Disabled																
26H	Setting Disabled																
27H	Setting Disabled																
28H	Software reset	Software reset															
29H	Setting Disabled																
2AH	Setting Disabled																
2BH	Setting Disabled																
2CH	Setting Disabled																
2DH	Setting Disabled																
2EH	Setting Disabled																
2FH	Setting Disabled																
30H	Gamma Control (1)	0	0	0	NOTP4	Dummy4	PKP12(0)	PKP11(0)	PKP10(0)	0	0	0	0	0	PKP02(1)	PKP01(0)	PKP00(0)
31H	Gamma Control (2)	0	0	0	0	0	PKP32(0)	PKP31(0)	PKP30(0)	0	0	0	0	0	PKP22(0)	PKP21(0)	PKP20(0)
32H	Gamma Control (3)	0	0	0	0	0	PKP52(0)	PKP51(0)	PKP50(1)	0	0	0	0	0	PKP42(0)	PKP41(0)	PKP40(1)
33H	Gamma Control (4)	0	0	0	0	0	PRP12(0)	PRP11(1)	PRP10(0)	0	0	0	0	0	PRP02(0)	PRP01(1)	PRP00(0)
34H	Gamma Control (5)	0	0	0	0	0	PKN12(1)	PKN11(1)	PKN10(0)	0	0	0	0	0	PKN02(1)	PKN01(1)	PKN00(0)
35H	Gamma Control (6)	0	0	0	0	0	PKN32(1)	PKN31(1)	PKN30(1)	0	0	0	0	0	PKN22(1)	PKN21(1)	PKN20(1)
36H	Gamma Control (7)	0	0	0	0	0	PKN52(0)	PKN51(1)	PKN50(1)	0	0	0	0	0	PKN42(1)	PKN41(1)	PKN40(1)
37H	Gamma Control (8)	0	0	0	0	0	PRN12(0)	PRN11(1)	PRN10(0)	0	0	0	0	0	PRN02(0)	PRN01(1)	PRN00(0)
38H	Setting Disabled																
39H	Setting Disabled																
3AH	Gamma Control (9)	0	0	0	VRP14(1)	VRP13(1)	VRP12(1)	VRP11(1)	VRP10(1)	0	0	0	0	VRP03(0)	VRP02(0)	VRP01(0)	VRP00(0)
3BH	Gamma Control (10)	0	0	0	VRN14(1)	VRN13(1)	VRN12(1)	VRN11(1)	VRN10(1)	0	0	0	0	VRN03(0)	VRN02(0)	VRN01(0)	VRN00(0)
3CH	Setting Disabled																
3DH	Setting Disabled																
3EH	Setting Disabled																
3FH	Setting Disabled																
52H	Power Supply Control 6	DCSEL	VGHON	VCIX2ON	VCI2ON	VGLON	VL63ON	VCOMON	DCON	0	0	1	1	1	1	0	0
54H	VGH OFF setting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VGHOFF
60H	EEPROM Mode setting	0	0	0	0	0	0	0	0	0	0	0	0	0	EP_READ	EP_WRITE	EP_PWR
61H	EEPROM Operation Control	0	0	0	0	0	0	0	0	0	0	0	0	0	IE2OPC2	IE2OPC1	IE2OPC0
70H	Power Supply Control 3	There are no actual Registers. When these registers are read, value is '0'.							Parity	0	0	Dummy5	Dummy1	VRH3	VRH2	VRH1	VRH0
71H	Power Supply Control 4								Parity	Dummy6	Dummy2	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0
72H	Power Supply Control 5								Parity	Dummy7	Dummy3	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
73H	Gamma control 1								Parity	Dummy8	Dummy4	PKP12	PKP11	PKP10	PKP02	PKP01	PKP00
74H	Gamma control 2								Parity	0	PKP32	PKP31	PKP30	0	PKP22	PKP21	PKP20
75H	Gamma control 3								Parity	0	PKP52	PKP51	PKP50	0	PKP42	PKP41	PKP40
76H	Gamma control 4								Parity	0	PRP12	PRP11	PRP10	0	PRP02	PRP01	PRP00
77H	Gamma control 5								Parity	0	PKN12	PKN11	PKN10	0	PKN02	PKN01	PKN00
78H	Gamma control 6								Parity	0	PKN32	PKN31	PKN30	0	PKN22	PKN21	PKN20
79H	Gamma control 7								Parity	0	PKN52	PKN51	PKN50	0	PKN42	PKN41	PKN40
7AH	Gamma control 8								Parity	0	PRN12	PRN11	PRN10	0	PRN02	PRN01	PRN00
7BH	Gamma control 9								Parity	VRP12	VRP11	VRP10	0	VRP03	VRP02	VRP01	VRP00
7CH	Gamma control 10								Parity	VRN12	VRN11	VRN10	0	VRN03	VRN02	VRN01	VRN00
7DH	Gamma control 9,10								Parity	0	0	VRN14	VRN13	0	0	VRP14	VRP13

Remark *: Don't care

13. INSTRUCTION DESCRIPTIONS

Ensure that you are aware of the assignments of instruction bits (IB15-IB0) for each interface that are illustrated below.

13.1 Index Register (IR)

The index instruction specifies the control register indexes (R00H to R7DH). It sets the register number in the range of 0000000 to 1111111 in binary form. However, do not access to index register and instruction bit that is not allocated in index register.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Remark *: Don't care

13.2 Status Read (SR)

The status read instruction reads the internal status of the μPD161608.

L7-L0: Indicate the driving raster-row position where the liquid crystal display is being driven.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

13.3 Driver Output Control (R01H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	REV	0	BGR	SM	TB	RL	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0

REV: Displays all character and graphics display sections with reversal when REV = "1". Since the gray-scale level can be reversed, display of the same data is enabled on normally white and normally black panels. Source output level is indicated below.

REV	RGB data	Source output level	
		VCOM = H	VCOM = L
1	00000H : 3FFFFH	V63 : V0	V0 : V63
0	00000H : 3FFFFH	V0 : V63	V63 : V0

SM: Change the division of gate driver.

SM = 0: Odd/even division (interlace mode) is selected.

SM = 1: Upper/lower division is selected. Select the division mode according to the mounting method (POR = 0)

TB: Selects the output shift direction of the gate driver.

TB = 0: G219 shifts to G0.

TB = 1: G0 shifts to G219.

RL: Selects the output shift direction of the source driver.

RL = 0: Start point: S527, end point S0

RL = 1: Start point: S0, end point S527

Caution About TB, RL REV, and BGR function, it is initialized by the level of a hardware pin when hardware reset and software reset is performed. By changing the level of the hardware pin, an internal state is also changeable.

After sending the data of R01H by software, the data sent by software becomes valid. In this case, a setup of a hardware pin becomes invalid until it performs hardware reset.

In addition, when TB, RL, REV, and BGR pin are changed, the timing which becomes 2 kinds valid inside IC is as follows.

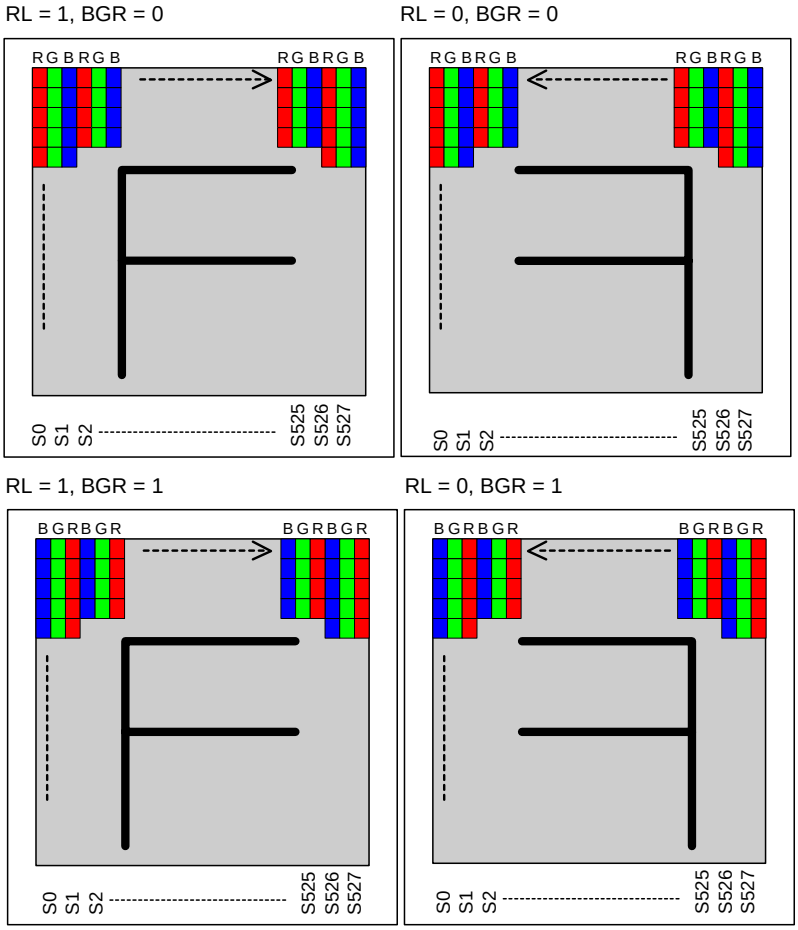
(1) About RL and TB function, these setup becomes valid inside IC in the top of a frame.

(2) About REV and BGR function, these setup becomes valid inside IC immediately.

BGR: Selects the <R><G><B> arrangement.

BGR = 0: <R><G><B> color is assigned from S0.

BGR = 1: <B><G><R> color is assigned from S0.



MUX7-MUX0: Specify number of lines for the LCD driver. Setting exceeds 220 lines will be treated as dummy line of vertical front porch.

Caution When set MUX7-MUX0 to 8'hDB, Vertical front porch is set under 36 line.

13.4 LCD Driving Waveform Control (R02H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	B/C	EOR	0	NW6	NW5	NW4	NW3	NW2	NW1	NW0

B/C: When B/C = 0, it performs scanniing in every frame for LCD drive. When B/C = 1, n-raster-row inversion waveform is generated and alternates in each raster-row specified by bits EOR and NW6-NW0 in the LCD-driving-waveform control register. For details, refer to **20. n-RASTER-ROW RESERVED AC DRIVE** (Default: B/C = 1).

EOR: When the n-raster-row inversion waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EOR for alternating drive. EOR is used when combining the set values of the number of the LCD drive raster-row and the n raster-row does not alternate the LCD. For details, refer to **20. n-RASTER-ROW RESERVED AC DRIVE** (Default: EOR = 1).

NW6-NW0: Specify the number of raster-rows n that will alternate at the n-raster-row inversion waveform setting (B/C = 1). NW6-NW0 alternate for every set value + 1 raster-row, and the first to the 128th raster-rows can be selected (Default: NW6-NW0 = 0)

13.5 Power Supply Control 1 (R03H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0

DCT3-DCT0: Set the step-up cycle of the step-up circuit for 8-color mode (CM = V_{DDIO}). When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases as well. Adjust the cycle taking into account the display quality and power consumption.

DCT3	DCT2	DCT1	DCT0	Step-up Cycle
0	0	0	0	F line x 14
0	0	0	1	F line x 11
0	0	1	0	F line x 9
0	0	1	1	F line x 7
0	1	0	0	F line x 6
0	1	0	1	F line x 5
0	1	1	0	F line x 4
0	1	1	1	F line x 3
1	0	0	0	F line x 2
1	0	0	1	F line x 1
1	0	1	0	f_{OSC}/24
1	0	1	1	f_{OSC}/40
1	1	0	0	f_{OSC}/48
1	1	0	1	f_{OSC}/56
1	1	1	0	f_{OSC}/64
1	1	1	1	f_{OSC}/80

Remark F line: Horizontal frequency (f_H TYP. 13.5 kHz)

f_{OSC}: DOTCLK frequency (f_{DOTCLK} TYP. 2.64 MHz)

Caution When DCTn setting is changed to F line x n (DCT3-DCT0 = 0000 to 1001), the change of the setting is updated following 2 cases.

1. **Power up sequence using SHUT pin**
2. **From the head of the frame immediately after changing the level of CM pin**

BT2-BT0: The output factor of step-up is switched. Adjust scale factor of the DC/DC converter circuit by the voltage used.

BT2	BT1	BT0	VCIX2	VGH Output	VGL Output
0	0	0	2 x VCI	6 x VCI	–5 x VCI
0	0	1	2 x VCI	6 x VCI	–4 x VCI
0	1	0	2 x VCI	6 x VCI	–3 x VCI
0	1	1	2 x VCI	5 x VCI	–5 x VCI
1	0	0	2 x VCI	5 x VCI	–4 x VCI
1	0	1	2 x VCI	5 x VCI	–3 x VCI
1	1	0	2 x VCI	4 x VCI	–4 x VCI
1	1	1	2 x VCI	4 x VCI	–3 x VCI

Remark When set to 8-color mode (CM = "H"), VGL output voltage is fixed to "–3 x VCI".

DC3-DC0: Set the step-up cycle of the step-up circuit for 262 K-color mode (CM = V_{SS}). When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases as well. Adjust the cycle taking into account the display quality and power consumption.

DC3	DC2	DC1	DC0	Step-up Cycle
0	0	0	0	F line x 14
0	0	0	1	F line x 11
0	0	1	0	F line x 9
0	0	1	1	F line x 7
0	1	0	0	F line x 6
0	1	0	1	F line x 5
0	1	1	0	F line x 4
0	1	1	1	F line x 3
1	0	0	0	F line x 2
1	0	0	1	F line x 1
1	0	1	0	f_{OSC}/24
1	0	1	1	f_{OSC}/40
1	1	0	0	f_{OSC}/48
1	1	0	1	f_{OSC}/56
1	1	1	0	f_{OSC}/64
1	1	1	1	f_{OSC}/80

Remark F line: Horizontal frequency (f_H TYP. 13.5 kHz)

f_{OSC}: DOTCLK frequency (f_{DOTCLK} TYP. 2.64 MHz)

Caution When DCn setting is changed to F line x n (DC3-DC0 = 0000 to 1001), the change of the setting is updated following 2 cases.

1. **Power up sequence using SHUT pin**
2. **From the head of the frame immediately after changing the level of CM pin**

AP2-AP0: Adjust the amount of current from the stable-current source in the internal operational amplifier circuit.

When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current taking into account the power consumption. During times when there is no display, such as when the system is in a sleep mode.

AP2	AP1	AP0	Amount of Current in Operational Amplifier
0	0	0	Smallest
0	0	1	Small
0	1	0	Medium small
0	1	1	Medium
1	0	0	Large small
1	0	1	Large medium
1	1	0	Large
1	1	1	Largest

13.6 Frame Cycle Control (R0BH)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	PT1	PT0	0	0	0	0	0	0	0	0

NO1, NO0: Set the gate non-overlap period.

NO1	NO0	Gate non-overlap Period
0	0	0 clock cycle
0	1	4 clock cycle
1	0	6 clock cycle
1	1	8 clock cycle

Remark Clock cycle: DOTCLK cycle

SDT1, SDT0: Specify the timing on which a source signal is output after falling edge of a gate signal.

SDT1	SDT0	Delay amount of the source output
0	0	4 clock cycle
0	1	4 clock cycle
1	0	4 clock cycle
1	1	4 clock cycle

Remark Clock cycle: DOTCLK cycle

EQ1, EQ0: Equalized period is added as specified by bits of EQ1-EQ0. The equalization signal is output for scan line.

EQ1	EQ0	Equalizing Period
0	0	Not equalized
0	1	18 clock cycle
1	0	26 clock cycle
1	1	A:B ratio = 1:7 **Note**

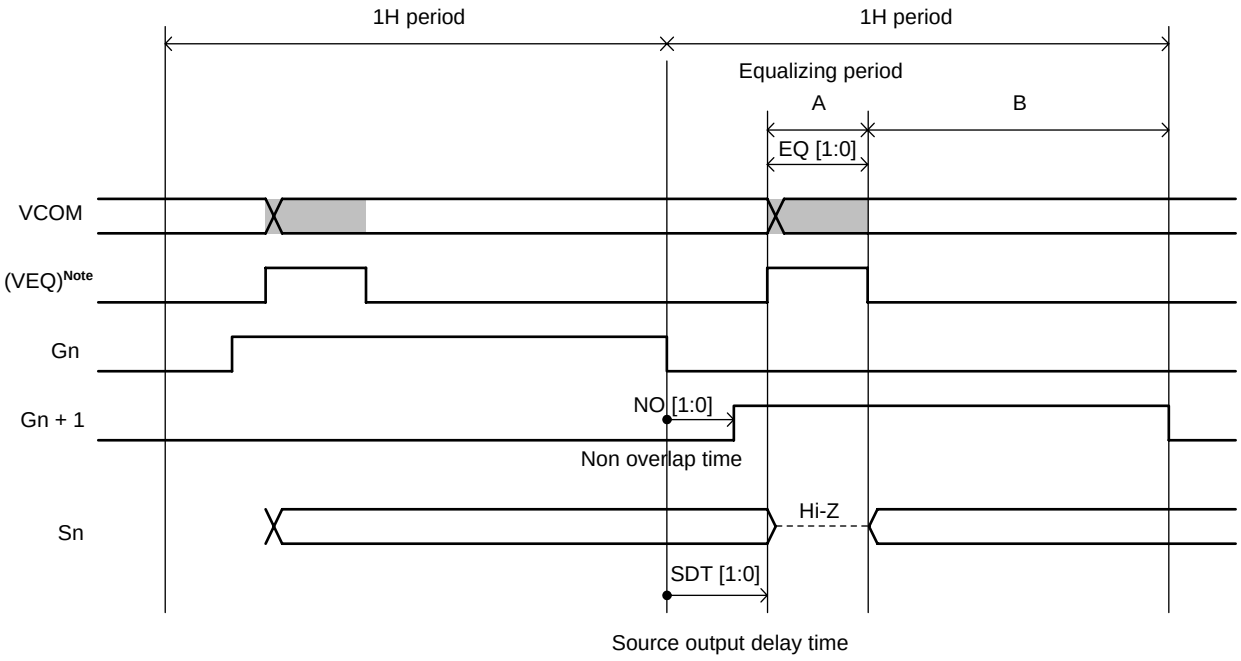
Remark Clock cycle: DOTCLK cycle

Note In power up sequence, only when being setup before starting SHUT pin, the setup of this command is valid.

PT1, PT0: Set the division ratio of clocks for internal operation. Internal operations are driven by clocks which frequency are divided according to the PT1, PT0 setting.

PT1	PT0	Internal Operation clock frequency
0	0	f_{OSC}/1
0	1	Reserved
1	0	Reserved
1	1	Reserved

Remark f_{OSC} = DOTCLK frequency



Note The signal in parenthesis are shown internal signal.

13.7 Power Supply Control 3 (R0DH)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	NOTP1	Dummy1	VRH3	VRH2	VRH1	VRH0

NOTP1: NOTP1 becomes “0” after power on reset and VLCD63 voltage becomes programmed EEPROM value. When NOTP1 set to “1”, setting of VRH3-VRH0 becomes valid and voltage of VLCD63 can be adjusted.

VRH3-VRH0: Set amplitude magnification of VLCD63. These bits amplify the VLCD63 voltage 1.330 to 2.775 times the Vref voltage set by VRH3-VRH0.

VRH3	VRH2	VRH1	VRH0	VLCD63 Output
0	0	0	0	Vref x 1.330
0	0	0	1	Vref x 1.450
0	0	1	0	Vref x 1.550
0	0	1	1	Vref x 1.650
0	1	0	0	Vref x 1.750
0	1	0	1	Vref x 1.800
0	1	1	0	Vref x 1.850
0	1	1	1	Stopped
1	0	0	0	Vref x 1.900
1	0	0	1	Vref x 2.175.
1	0	1	0	Vref x 2.325
1	0	1	1	Vref x 2.475
1	1	0	0	Vref x 2.625
1	1	0	1	Vref x 2.700
1	1	1	0	Vref x 2.775
1	1	1	1	Stopped

Caution VLCD63 output voltage that is set by VRH [3:0] setting is limited under VCIX2 voltage. Vref is the internal reference voltage equals to 2.0 V.

13.8 Power Supply Control 4 (R0EH)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NOTP2	Dummy2	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0

NOTP2: NOTP2 becomes “0” after power on reset and VCOM amplitude voltage becomes programmed EEPROM value. When NOTP1 set to “1”, setting of VDV4-VDV0 becomes valid and voltage of VCOM amplitude voltage can be adjusted.

VCOMG: When VCOMG = “1”, it is possible to set output voltage of VCOML to any level, and the instruction (VDV4-VDV0) becomes available. When VCOMG = “0”, VCOML output is fixed to Hi-Z level, VCI2 output for VCOML power supply stops, and the instruction (VDV4-VDV0) becomes unavailable. Set VCOMG according to the sequence of power supply setting flow as it relates with power supply operating sequence.

VDV4-VDV0: Set the alternating amplitudes of VCOM at the VCOM alternating drive. These bits amplify VCOM amplitude 0.6 to 1.23 times the VLCD63 voltage. When VCOMG = “0”, the settings become invalid. External voltage at VCOMR is referenced when VDV4-VDV0 = “01111”.

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude
0	0	0	0	0	VLCD63 x 0.60
0	0	0	0	1	VLCD63 x 0.63
0	0	0	1	0	VLCD63 x 0.66
:	:	:	:	:	: Step = 0.03 :
0	1	1	0	1	VLCD63 x 0.99
0	1	1	1	0	VLCD63 x 1.02
0	1	1	1	1	Reference from external variable resister
1	0	0	0	0	VLCD63 x 1.05
1	0	0	0	1	VLCD63 x 1.08
:	:	:	:	:	: Step = 0.03 :
1	0	1	0	1	VLCD63 x 1.20
1	0	1	1	0	VLCD63 x 1.23
1	0	1	1	1	Setting disable
1	1	*	*	*	Setting disable

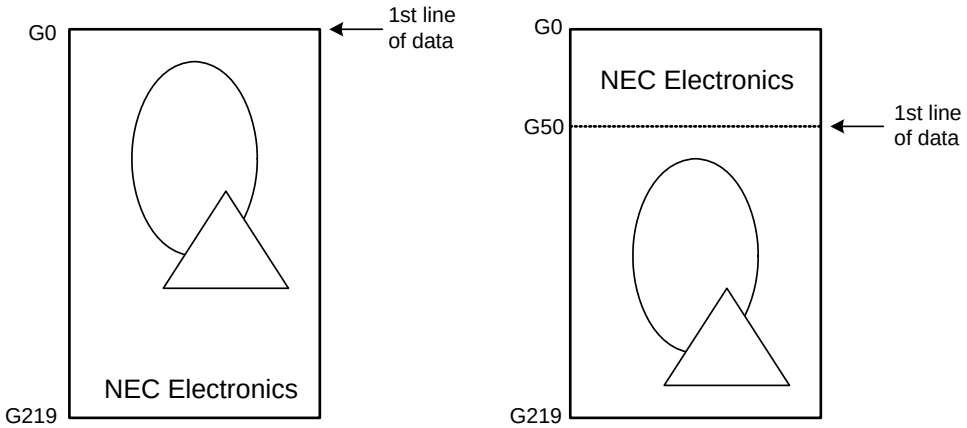
Remark *: Don’t care

Caution When set to 8-color mode (CM = H), VCOML output voltage is fixed to 0 V and above-mentioned setting is ignored.

13.9 Gate Scan Start Position (R0FH)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

SCN7-SCN0: Set the scanning starting position of the gate driver.



13.10 Horizontal Porch (R16H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	1	0	1	0	1	1	1	1	0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0

HBP5-HBP0: Set the delay period from falling edge of HSYNC signal to first valid data. The pixel data exceed 176 and before the first valid data will be treated as dummy data.

HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	Number of clock cycle of DOTCLK
0	0	0	0	0	0	8
0	0	0	0	0	1	8
0	0	0	0	1	0	8
0	0	0	0	1	1	8
0	0	0	1	0	0	8
0	0	0	1	0	1	8
0	0	0	1	1	0	8
0	0	0	1	1	1	9
0	0	1	0	0	0	10
:	:	:	:	:	:	: Step = 1 :
1	1	1	1	1	0	64
1	1	1	1	1	1	65

13.11 Vertical Porch (R17H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

VBP7-VBP0: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line.

VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	Number of clock cycle of Hsync
0	0	0	0	0	0	0	0	Setting disable
0	0	0	0	0	0	0	1	Setting disable
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
0	0	0	0	0	1	0	0	4
0	0	0	0	0	1	0	1	5
:	:	:	:	:	:	:	:	: Step = 1 :
1	1	0	1	1	0	1	1	219
1	1	0	1	1	1	0	0	220
1	1	0	1	1	1	0	1	Setting disable
1	1	0	1	1	1	1	*	Setting disable
1	1	1	*	*	*	*	*	Setting disable

Remark *: Don't care

13.12 Power Supply Control 5 (R1EH)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	NOTP3	Dummy3	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

NOTP3: NOTP3 becomes "0" after power on reset and VCOMH voltage becomes programmed EEPROM value. When NOTP3 set to "1", setting of VCM5-VCM0 becomes valid and voltage of VCOMH can be adjusted.

VCM5-VCM0: Set the 262 K-color mode of VCOMH voltage if NOTP3 = "1". These bits amplify the VCOMH voltage 0.36 to 0.99 times the VLCD63 voltage.

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH Output
0	0	0	0	0	0	VLCD63 x 0.36
0	0	0	0	0	1	VLCD63 x 0.37
0	0	0	0	1	0	VLCD63 x 0.38
0	0	0	0	1	1	VLCD63 x 0.39
:	:	:	:	:	:	: Step = 0.01 :
1	1	1	1	1	0	VLCD63 x 0.98
1	1	1	1	1	1	VLCD63 x 0.99

13.13 Software Reset (R28H)

Register can be reset to its POR default values upon the following sequence are completed.

Step	Resister	Value	Internal Operation
1	R28H	0006	Idle
2	R28H	000E	Initialize register
3	R28H	0000	Reset is released.

Caution All other above settings of R28H are reserved. Therefore, please don't set up.

13.14 Gamma Control1 to 10 (R30H to R37H, R3AH, R3BH)

For more detail, refer to **14. GAMMA ADJUSTMENT FUNCTION**.

Reg.	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R30H	W	1	0	0	0	NOTP4	Dummy4	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
R31H	W	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
R32H	W	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
R33H	W	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
R34H	W	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
R35H	W	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
R36H	W	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
R37H	W	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
R3AH	W	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
R3BH	W	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00

NOTP4: NOTP4 becomes "0" after power on reset and gamma curve setting (R30H-R37H, R3AH, R3BH) becomes programmed EEPROM value. When NOTP4 set to "1", setting of R30H-R37H, R3AH, R3BH become valid and voltage of each gamma curve can be adjusted.

PKP52-PKP00: Micro-adjustment register for the positive polarity output
PRP12-PRP00: Gray-scale adjustment register for the positive polarity output
PKN52-PKN00: Micro-adjustment register for the negative polarity output
PRN12-PRN00: Gray-scale adjustment register for the negative polarity output
VRP14-VRP10: Amplitude adjustment register for the positive polarity output
VRP03-VRP00: Reference adjustment register for the positive polarity output
VRN14-VRN10: Amplitude adjustment register for the negative polarity output
VRN03-VRN00: Reference adjustment register for the negative polarity output

13.15 Power Supply Control 6 (R52H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DCSEL	VGHON	VCIX2ON	VCI2ON	VGLON	VL63ON	VCOMON	DCON	0	0	1	1	1	1	0	0

DCSEL: This flag selects power set-up mode as follows.

DCSEL = 0: Auto sequence mode OFF, VGHON/VCIX2ON/VCI2ON/VGLON/VL63ON are valid.

DCSEL = 1: Auto sequence mode

VGHON: When DCSEL=0, this flag is valid. VGH power supply circuit is control as follows.

VGHON = 0: Halt

VGHON = 1: Operate

VCIX2ON: When DCSEL = 0, this flag is valid. VCIX2 power supply circuit is control as follows.

VCIX2ON = 0: Halt

VCIX2ON = 1: Operate

VCI2ON: When DCSEL = 0, this flag is valid. Set the output voltage of VCIX2 as follows.

VCIX2ON = 0: VC [3:0] (R11H) is valid

VCIX2ON = 1: VC [3:0] (R11H) setting value –1 V

VGLON: When DCSEL = 0, this flag is valid. VGL power supply circuit is control as follows.

VGLON = 0: Halt

VGLON = 1: Operate

VL63ON: When DCSEL = 0, this flag is valid. VLCD63 regulator circuit is control as follows.

VL63ON = 0: Halt

VL63ON = 1: Operate

VCOMON: When DCSEL = 0, this flag is valid. Regulator circuit for COMMON output is control as follows.

VCOMON = 0: Halt

VCOMON = 1: Operate

Cautions 1. The case to set this register, don't change the IB7-IB0's value above-mentioned register value.

2. Above- mentioned R52H setting is not used except "EEROM data write sequence".

13.16 VGH OFF Setting (R54H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VGHOFF

VGHOFF: This flag control VGH output as follows.

VGHOFF = 0: Normal operation

VGHOFF = 1: VGH halt (VCIX2 voltage level is output).

13.17 EEPROM Mode Setting (R60H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	EP_READ	EP_WRITE	EP_PWR

EP_READ, EP_WRITE: READ/WRITE setting mode select of EEPROM. EEPROM setting mode is select by these bits as follow table. For more detail, refer to **22. EEPROM ACCESS**.

EP_READ	EP_WRITE	EEPROM Setting Mode
0	0	Normal operation
0	1	EEPROM Write setting
1	0	EEPROM Read setting
1	1	Setting disable

EP_PWR: Select power supply mode during “EEPROM write” as follow table. For more detail, refer to **22. EEPROM ACCESS**.

EP_PWR	Power Supply Mode
0	External power supply mode (supply to VGH/VGL pins by externally)
1	Internal power supply mode

13.18 EEPROM Operation Control (R61H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	IE2OPC2	IE2OPC1	IE2OPC0

IE2OPC2-IE2OPC0: Control the access to EEPROM as follow table. For more detail, refer to **22. EEPROM ACCESS**.

IE2OPC2	IE2OPC1	IE2OPC0	EEPROM Access Setting
0	0	0	NOP (Non operation)
0	0	1	WRITE (EEPROM write)
0	1	0	Reserved
0	1	1	Reserved
1	0	0	ERASE
1	0	1	NOP
1	1	0	READ (EEPROM read)
1	1	1	Reserved

<R> 13.19 EEPROM Monitor (R70H to R7DH)

Register No.	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
70H	R	1	There are no actual Registers. When these registers are read, value is '0'.							Parity	0	0	Dummy5	Dummy1	VRH3	VRH2	VRH1	VRH0
71H	R	1								Parity	Dummy6	Dummy2	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0
72H	R	1								Parity	Dummy7	Dummy3	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
73H	R	1								Parity	Dummy8	Dummy4	PKP12	PKP11	PKP10	PKP02	PKP01	PKP00
74H	R	1								Parity	0	PKP32	PKP31	PKP30	0	PKP22	PKP21	PKP20
75H	R	1								Parity	0	PKP52	PKP51	PKP50	0	PKP42	PKP41	PKP40
76H	R	1								Parity	0	PRP12	PRP11	PRP10	0	PRP02	PRP01	PRP00
77H	R	1								Parity	0	PKN12	PKN11	PKN10	0	PKN02	PKN01	PKN00
78H	R	1								Parity	0	PKN32	PKN31	PKN30	0	PKN22	PKN21	PKN20
79H	R	1								Parity	0	PKN52	PKN51	PKN50	0	PKN42	PKN41	PKN40
7AH	R	1								Parity	0	PRN12	PRN11	PRN10	0	PRN02	PRN01	PRN00
7BH	R	1								Parity	VRP12	VRP11	VRP10	0	VRP03	VRP02	VRP01	VRP00
7CH	R	1								Parity	VRN12	VRN11	VRN10	0	VRN03	VRN02	VRN01	VRN00
7DH	R	1								Parity	0	0	VRN14	VRN13	0	0	VRP14	VRP13

R70H-R7DH is a register which monitors content written to EEPROM.

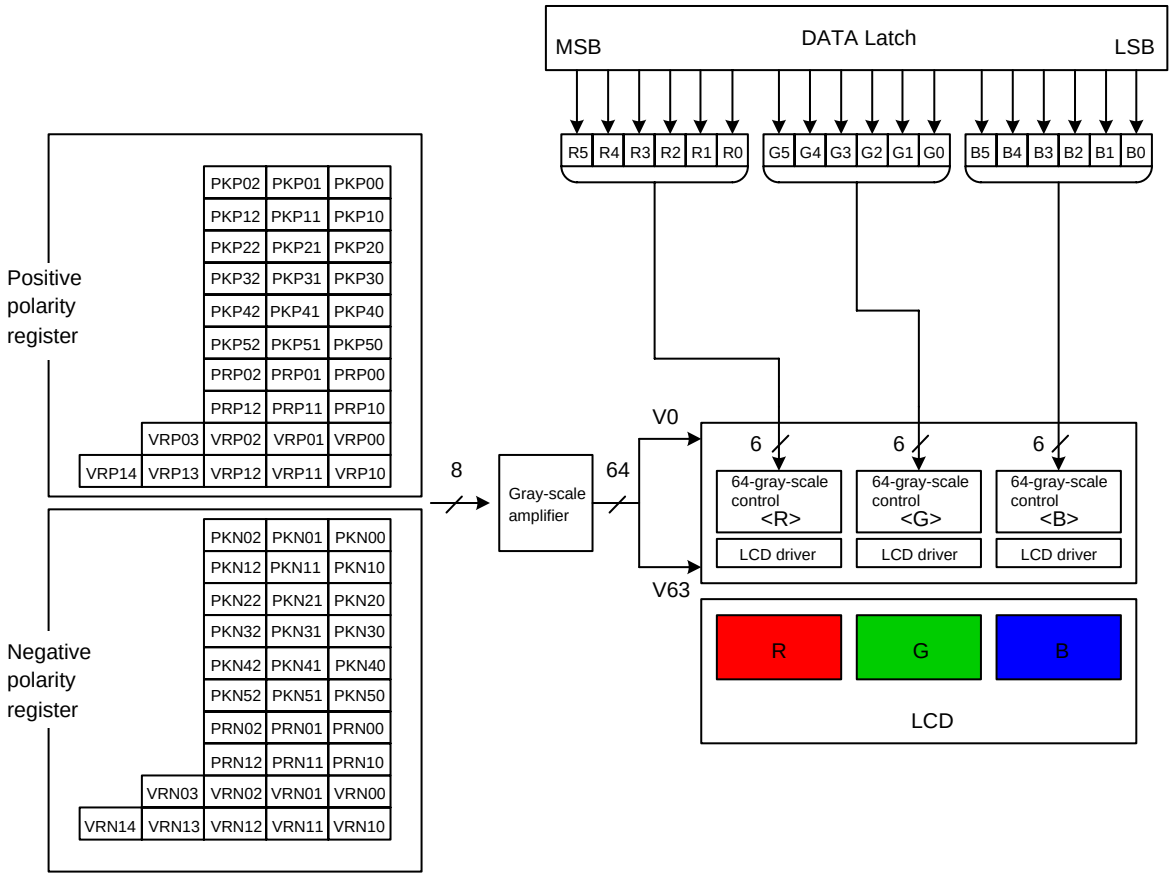
Parity bit of IB8 bit of instruction bit becomes 0 before written to EEPROM. Once it is written to EEPROM, these registers calculate parity.

14. GAMMA ADJUSTMENT FUNCTION

The μPD161608 provides the gamma adjustment function to display 262,144 colors simultaneously. The gamma adjustment executed by the gray-scale adjustment register and the micro-adjustment register that determines 8 gray-scale levels.

Furthermore, since the gray-scale adjustment register and the micro-adjustment register have the positive polarities and negative polarities, adjust them to match LCD panel respectively.

Figure 14–1. Gray-scale Control



15. STRUCTURE OF GRAY-SCALE AMPLIFIER

The structure of gray-scale amplifier is shown as below. 8-voltage-level (VINP0/VINP7-VINN0/VINN7) between VLCD63 and EXVR are determined by the gray-scale adjustment register and the micro adjustment register. Each level is split into 8 levels again by the internal ladder resistor network. As a result, gray-scale amplifier generates 64 voltage levels ranging from V0-V63 and outputs one of 64 levels. A gamma adjustment executed by the LCD panel respectively.

Figure 15–1. Structure of Gray-scale Amplifier

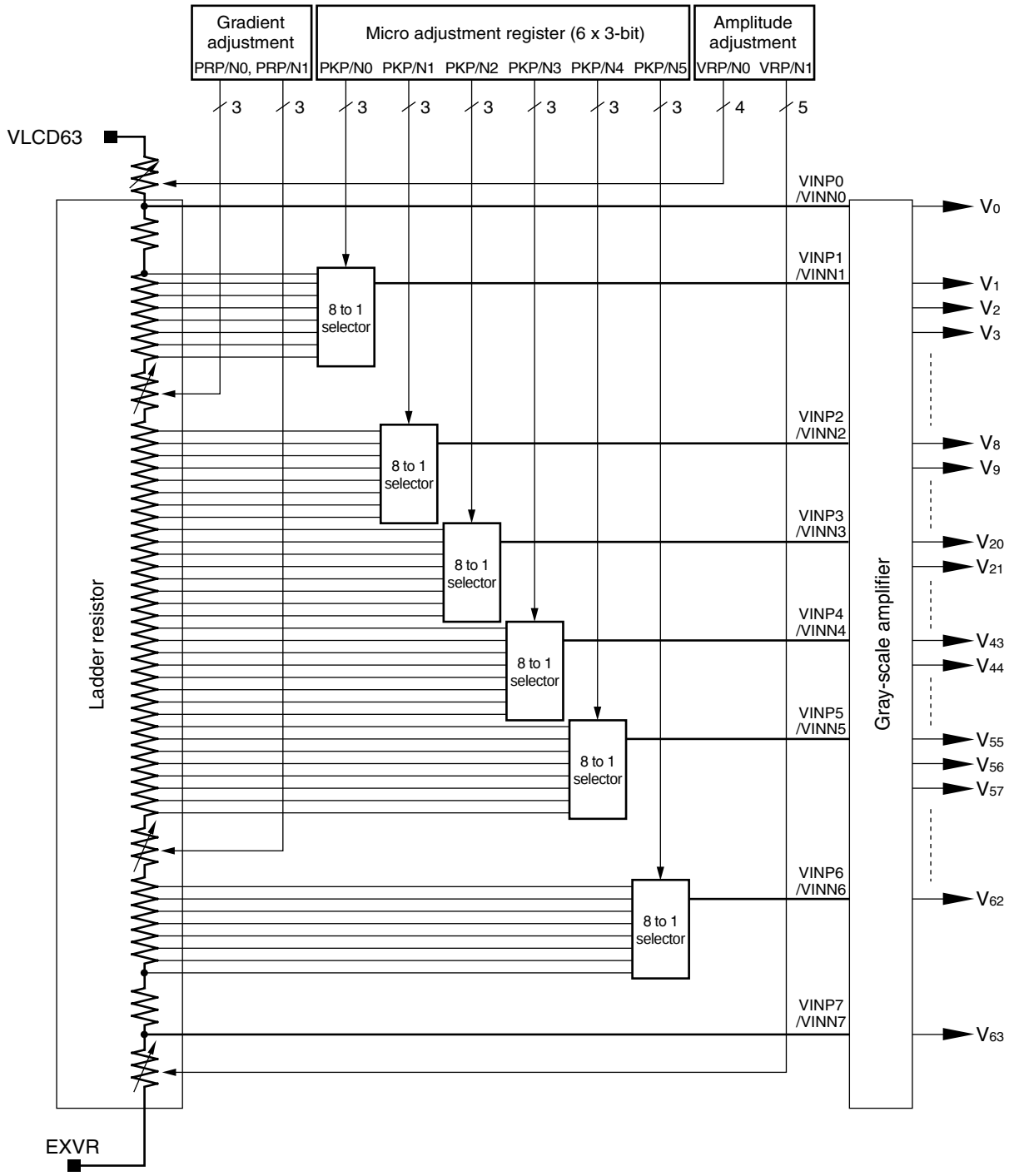
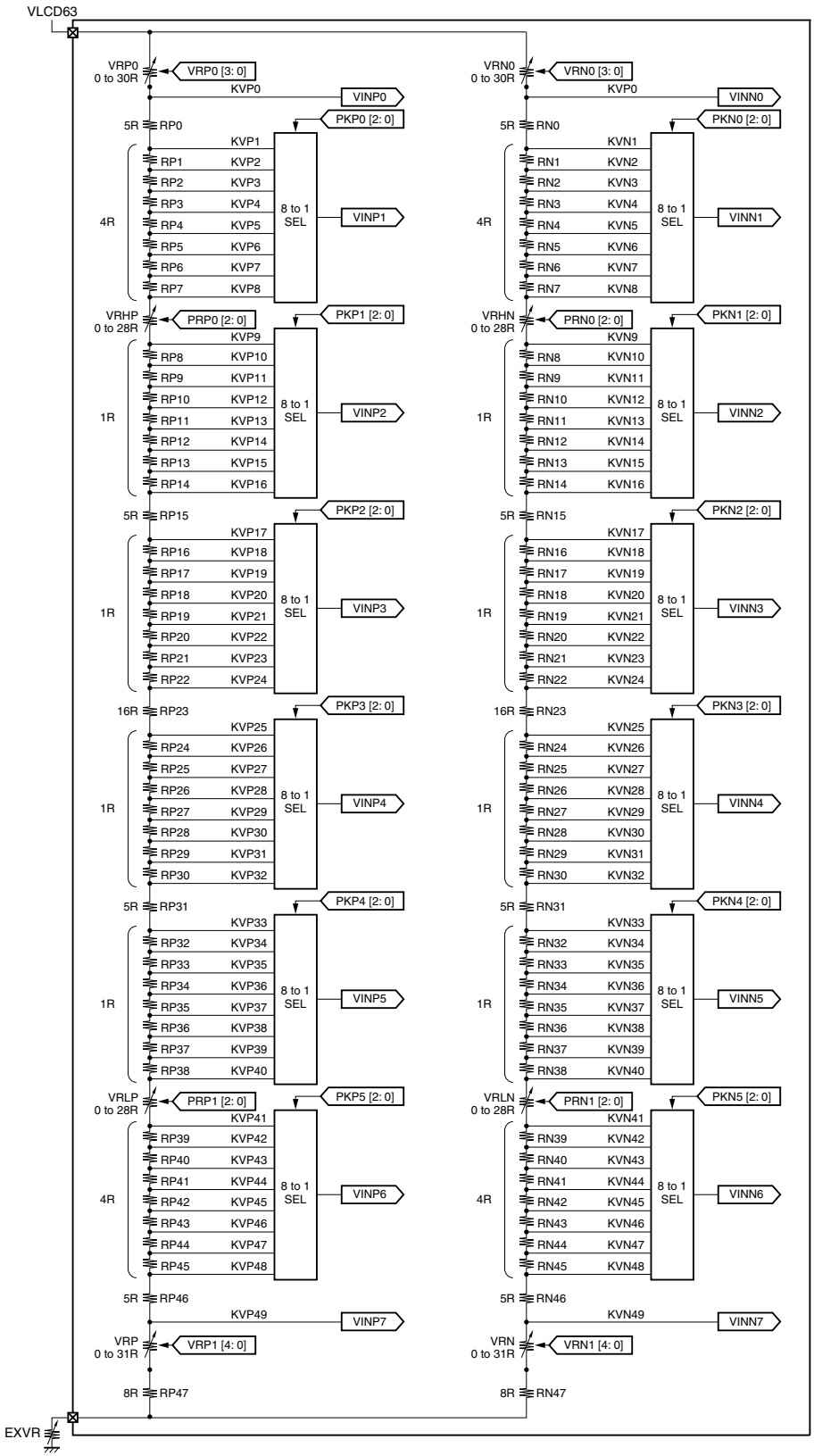


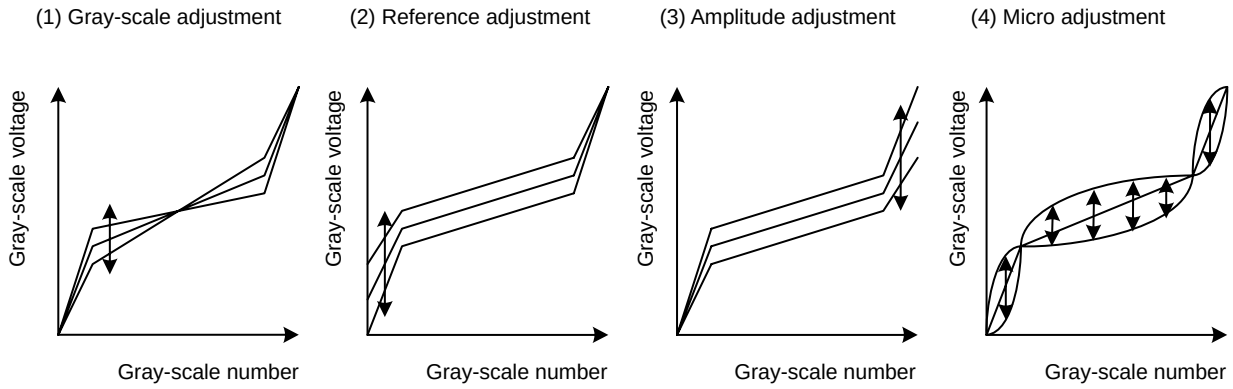
Figure 15–2. Structure of Resistor Ladder Network/8 to 1 Selector



16. GAMMA ADJUSTMENT REGISTER

The gamma adjustment register sets up the gray-scale voltage adjusting to the gamma specification of the LCD panel. This register can set positive/negative polarities independently. There are 3 types of register groups to adjust gray-scale and oscillation on number of the gray-scale, characteristics of the gray-scale voltage (But, R.G.B. is commonness). Following graphics indicate the operation of each adjusting register.

Figure 16–1. The Operation of Adjusting Register



16.1 Gray-scale Adjustment Resistor

The gray-scale adjustment resistors are used to adjust the gray-scale in the middle of the gray-scale characteristics for the voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistor (VRHP (N)/VRLP (N)) of the ladder resistor for the gray-scale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

16.2 Reference Adjustment Resistor

The Reference-adjusting resistor is to adjust reference of the gray-scale voltage. To accomplish the adjustment, it controls the variable resistor (VRP(N) 0) of the ladder resistor for the gray-scale voltage generator located at upper side of the ladder resistor.

16.3 Amplitude Adjustment Resistor

The amplitude-adjusting resistor is to adjust amplitude of the gray-scale voltage. To accomplish the adjustment, it controls the variable resistor (VRP(N) 1) of the ladder resistor for the gray-scale voltage generator located at lower side of the ladder resistor (Adjust upper side by input VLCD63 level). Also, there is an independent resistor on the positive/negative polarities as well as the gray-scale adjusting resistor.

16.4 Micro Adjustment Resistor

The micro adjustment resistor is to make subtle adjustment of the gray-scale voltage level. To accomplish the adjustment, it controls the each reference voltage level by the 8 to 1 selector towards the 8-leveled reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

Table 16–1. Gamma Adjusting Register

Register Group	Positive Polarity	Negative Polarity	Set-up Contents
Gray-scale adjustment	PRP02 to PRP00	PRN02 to PRN00	Variable resistor VRHP(N)
	PRP12 to PRP10	PRN12 to PRN10	Variable resistor VRLP(N)
Reference adjustment	VRP03 to VRP00	VRN03 to VRN00	Variable resistor VRP(N)0
Amplitude adjustment	VRP14 to VRP10	VRN14 to VRN10	Variable resistor VRP(N)1
Micro-adjustment	PKP02 to PKP00	PKN02 to PKN00	The voltage of gray-scale number 1 is selected by the 8 to 1 selector
	PKP12 to PKP10	PKN12 to PKN10	The voltage of gray-scale number 8 is selected by the 8 to 1 selector
	PKP22 to PKP20	PKN22 to PKN20	The voltage of gray-scale number 20 is selected by the 8 to 1 selector
	PKP32 to PKP30	PKN32 to PKN30	The voltage of gray-scale number 43 is selected by the 8 to 1 selector
	PKP42 to PKP40	PKN42 to PKN40	The voltage of gray-scale number 55 is selected by the 8 to 1 selector
	PKP52 to PKP50	PKN52 to PKN50	The voltage of gray-scale number 62 is selected by the 8 to 1 selector

17. LADDER RESISTOR / 8 TO 1 SELECTOR

The ladder resistor / 8 to 1 selector outputs the reference voltage of the gray-scale voltage. There are two ladder resistor networks including variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor network. The gamma resistor controls the variable and 8 to 1 resistors. Also, there is a pin connected to the external volume resistor. And it can compensate the dispersion of length between one panel to another.

17.1 Variable Resistor

There are 3 types of the variable resistors that is for the gray-scale adjustment (VRHP(N)/VRLP(N)), for reference adjustment (VRP(N)0), and for the amplitude adjustment (VRP(N)1). The resistance value is set by the gray-scale adjusting resistor (1), (2), reference adjustment resistor, and the oscillation-adjusting resistor as below.

Table 17–1. Gray-scale Adjustment (1)

Register Value PRP(N)0 [2:0]	Resistance Value VRHP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 17–2. Gray-scale Adjustment (2)

Register Value PRP(N)1 [2:0]	Resistance Value VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 17–3. Reference Adjustment

Register Value VRP(N)0 [3:0]	Resistance Value VRP(N)0
0000	0R
0001	2R
0010	4R
:	: Step = 1R :
1101	26R
1110	28R
1111	30R

Table 17–4. Amplitude Adjustment

Register Value VRP(N)1 [4:0]	Resistance Value VRP(N)1
00000	0R
00001	1R
00010	2R
:	: Step = 1R :
10110	22R
10111	23R
11000	24R
:	: Step = 1R :
11101	29R
11110	30R
11111	31R

18. THE 8 TO 1 SELECTOR

By the 8 to 1 selector, one of the voltage levels given by the ladder resistor network and the micro-adjusting register is selected. The 8 to 1 selector outputs one of the six types of reference voltages, the VINP(N)1 to VINP(N)6.

Following table explains the relationship between the micro-adjusting register and the selecting voltage.

Table 18–1. Relationship between Micro-adjusting Register and Selected Voltage

Register value	Selected Voltage					
PKP(N) [2:0]	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The gray-scale levels are determined by the following formulas listed in the next pages.

Table 18–2. Gamma Adjusting Voltage Formula (Positive Polarity)

Pins	Formula	Micro-adjusting Register Value	Reference Voltage
KVP0	VLCD63-ΔV*VRP0/SUMRP	–	VINP0
KVP1	VLCD63-ΔV*(VRP0+5R)/SUMRP	PKP02-00 = “000”	VINP1
KVP2	VLCD63-ΔV*(VRP0+9)/SUMRP	PKP02-00 = “001”	
KVP3	VLCD63-ΔV*(VRP0+13R)/SUMRP	PKP02-00 = “010”	
KVP4	VLCD63-ΔV*(VRP0+17R)/SUMRP	PKP02-00 = “011”	
KVP5	VLCD63-ΔV*(VRP0+21R)/SUMRP	PKP02-00 = “100”	
KVP6	VLCD63-ΔV*(VRP0+25R)/SUMRP	PKP02-00 = “101”	
KVP7	VLCD63-ΔV*(VRP0+29R)/SUMRP	PKP02-00 = “110”	
KVP8	VLCD63-ΔV*(VRP0+33R)/SUMRP	PKP02-00 = “111”	
KVP9	VLCD63-ΔV*(VRP0+33R+VRHP)/SUMRP	PKP12-10 = “000”	VINP2
KVP10	VLCD63-ΔV*(VRP0+34R+VRHP)/SUMRP	PKP12-10 = “001”	
KVP11	VLCD63-ΔV*(VRP0+35R+VRHP)/SUMRP	PKP12-10 = “010”	
KVP12	VLCD63-ΔV*(VRP0+36R+VRHP)/SUMRP	PKP12-10 = “011”	
KVP13	VLCD63-ΔV*(VRP0+37R+VRHP)/SUMRP	PKP12-10 = “100”	
KVP14	VLCD63-ΔV*(VRP0+38R+VRHP)/SUMRP	PKP12-10 = “101”	
KVP15	VLCD63-ΔV*(VRP0+39R+VRHP)/SUMRP	PKP12-10 = “110”	
KVP16	VLCD63-ΔV*(VRP0+40R+VRHP)/SUMRP	PKP12-10 = “111”	
KVP17	VLCD63-ΔV*(VRP0+45R+VRHP)/SUMRP	PKP22-20 = “000”	VINP3
KVP18	VLCD63-ΔV*(VRP0+46R+VRHP)/SUMRP	PKP22-20 = “001”	
KVP19	VLCD63-ΔV*(VRP0+47R+VRHP)/SUMRP	PKP22-20 = “010”	
KVP20	VLCD63-ΔV*(VRP0+48R+VRHP)/SUMRP	PKP22-20 = “011”	
KVP21	VLCD63-ΔV*(VRP0+49R+VRHP)/SUMRP	PKP22-20 = “100”	
KVP22	VLCD63-ΔV*(VRP0+50R+VRHP)/SUMRP	PKP22-20 = “101”	
KVP23	VLCD63-ΔV*(VRP0+51R+VRHP)/SUMRP	PKP22-20 = “110”	
KVP24	VLCD63-ΔV*(VRP0+52R+VRHP)/SUMRP	PKP22-20 = “111”	
KVP25	VLCD63-ΔV*(VRP0+68R+VRHP)/SUMRP	PKP32-30 = “000”	VINP4
KVP26	VLCD63-ΔV*(VRP0+69R+VRHP)/SUMRP	PKP32-30 = “001”	
KVP27	VLCD63-ΔV*(VRP0+70R+VRHP)/SUMRP	PKP32-30 = “010”	
KVP28	VLCD63-ΔV*(VRP0+71R+VRHP)/SUMRP	PKP32-30 = “011”	
KVP29	VLCD63-ΔV*(VRP0+72R+VRHP)/SUMRP	PKP32-30 = “100”	
KVP30	VLCD63-ΔV*(VRP0+73R+VRHP)/SUMRP	PKP32-30 = “101”	
KVP31	VLCD63-ΔV*(VRP0+74R+VRHP)/SUMRP	PKP32-30 = “110”	
KVP32	VLCD63-ΔV*(VRP0+75R+VRHP)/SUMRP	PKP32-30 = “111”	
KVP33	VLCD63-ΔV*(VRP0+80R+VRHP)/SUMRP	PKP42-40 = “000”	VINP5
KVP34	VLCD63-ΔV*(VRP0+81R+VRHP)/SUMRP	PKP42-40 = “001”	
KVP35	VLCD63-ΔV*(VRP0+82R+VRHP)/SUMRP	PKP42-40 = “010”	
KVP36	VLCD63-ΔV*(VRP0+83R+VRHP)/SUMRP	PKP42-40 = “011”	
KVP37	VLCD63-ΔV*(VRP0+84R+VRHP)/SUMRP	PKP42-40 = “100”	
KVP38	VLCD63-ΔV*(VRP0+85R+VRHP)/SUMRP	PKP42-40 = “101”	
KVP39	VLCD63-ΔV*(VRP0+86R+VRHP)/SUMRP	PKP42-40 = “110”	
KVP40	VLCD63-ΔV*(VRP0+87R+VRHP)/SUMRP	PKP42-40 = “111”	
KVP41	VLCD63-ΔV*(VRP0+87R+VRHP+VRLP)/SUMRP	PKP52-50 = “000”	VINP6
KVP42	VLCD63-ΔV*(VRP0+91R+VRHP+VRLP)/SUMRP	PKP52-50 = “001”	
KVP43	VLCD63-ΔV*(VRP0+95R+VRHP+VRLP)/SUMRP	PKP52-50 = “010”	
KVP44	VLCD63-ΔV*(VRP0+99R+VRHP+VRLP)/SUMRP	PKP52-50 = “011”	
KVP45	VLCD63-ΔV*(VRP0+103R+VRHP+VRLP)/SUMRP	PKP52-50 = “100”	
KVP46	VLCD63-ΔV*(VRP0+107R+VRHP+VRLP)/SUMRP	PKP52-50 = “101”	
KVP47	VLCD63-ΔV*(VRP0+111R+VRHP+VRLP)/SUMRP	PKP52-50 = “110”	
KVP48	VLCD63-ΔV*(VRP0+115R+VRHP+VRLP)/SUMRP	PKP52-50 = “111”	
KVP49	VLCD63-ΔV*(VRP0+120R+VRHP+VRLP)/SUMRP	–	VINP7

Remark SUMRP: Total of the positive polarity ladder resistance = VRP0 + 128R + VRHP + VRLP + VRP

SUMRN: Total of the negative polarity ladder resistance = VRN0 + 128R + VRHN + VRLN + VRN

ΔV: Potential difference between KV0 and KV49 = VLCD63*SUMRP*SUMRN/[SUMRP*SUMRN+EXVR*(SUMRP+SUMRN)]

Table 18–3. Gamma Voltage Formula (Positive Polarity)

Gray-scale Voltage	Formula	Gray-scale Voltage	Formula
V0	VINP0	V32	V43+(V20-V43)*(11/23)
V1	VINP1	V33	V43+(V20-V43)*(10/23)
V2	V8+(V1-V8)*(30/48)	V34	V43+(V20-V43)*(9/23)
V3	V8+(V1-V8)*(23/48)	V35	V43+(V20-V43)*(8/23)
V4	V8+(V1-V8)*(16/48)	V36	V43+(V20-V43)*(7/23)
V5	V8+(V1-V8)*(12/48)	V37	V43+(V20-V43)*(6/23)
V6	V8+(V1-V8)*(8/48)	V38	V43+(V20-V43)*(5/23)
V7	V8+(V1-V8)*(4/48)	V39	V43+(V20-V43)*(4/23)
V8	VINP2	V40	V43+(V20-V43)*(3/23)
V9	V20+(V8-V20)*(22/24)	V41	V43+(V20-V43)*(2/23)
V10	V20+(V8-V20)*(20/24)	V42	V43+(V20-V43)*(1/23)
V11	V20+(V8-V20)*(18/24)	V43	VINP4
V12	V20+(V8-V20)*(16/24)	V44	V55+(V43-V55)*(22/24)
V13	V20+(V8-V20)*(14/24)	V45	V55+(V43-V55)*(20/24)
V14	V20+(V8-V20)*(12/24)	V46	V55+(V43-V55)*(18/24)
V15	V20+(V8-V20)*(10/24)	V47	V55+(V43-V55)*(16/24)
V16	V20+(V8-V20)*(8/24)	V48	V55+(V43-V55)*(14/24)
V17	V20+(V8-V20)*(6/24)	V49	V55+(V43-V55)*(12/24)
V18	V20+(V8-V20)*(4/24)	V50	V55+(V43-V55)*(10/24)
V19	V20+(V8-V20)*(2/24)	V51	V55+(V43-V55)*(8/24)
V20	VINP3	V52	V55+(V43-V55)*(6/24)
V21	V43+(V20-V43)*(22/23)	V53	V55+(V43-V55)*(4/24)
V22	V43+(V20-V43)*(21/23)	V54	V55+(V43-V55)*(2/24)
V23	V43+(V20-V43)*(20/23)	V55	VINP5
V24	V43+(V20-V43)*(19/23)	V56	V62+(V55-V62)*(44/48)
V25	V43+(V20-V43)*(18/23)	V57	V62+(V55-V62)*(40/48)
V26	V43+(V20-V43)*(17/23)	V58	V62+(V55-V62)*(36/48)
V27	V43+(V20-V43)*(16/23)	V59	V62+(V55-V62)*(32/48)
V28	V43+(V20-V43)*(15/23)	V60	V62+(V55-V62)*(25/48)
V29	V43+(V20-V43)*(14/23)	V61	V62+(V55-V62)*(18/48)
V30	V43+(V20-V43)*(13/23)	V62	VINP6
V31	V43+(V20-V43)*(12/23)	V63	VINP7

Table 18–4. Gamma Adjusting Voltage Formula (Negative Polarity)

Pins	Formula	Micro-adjusting register value	Reference voltage
KVN0	VLCD63-ΔV*VRN0/SUMRN	–	VINN0
KVN1	VLCD63-ΔV*(VRN0+5R)/SUMRN	PKN02-00 = “000”	VINN1
KVN2	VLCD63-ΔV*(VRN0+9)/SUMRN	PKN02-00 = “001”	
KVN3	VLCD63-ΔV*(VRN0+13R)/SUMRN	PKN02-00 = “010”	
KVN4	VLCD63-ΔV*(VRN0+17R)/SUMRN	PKN02-00 = “011”	
KVN5	VLCD63-ΔV*(VRN0+21R)/SUMRN	PKN02-00 = “100”	
KVN6	VLCD63-ΔV*(VRN0+25R)/SUMRN	PKN02-00 = “101”	
KVN7	VLCD63-ΔV*(VRN0+29R)/SUMRN	PKN02-00 = “110”	
KVN8	VLCD63-ΔV*(VRN0+33R)/SUMRN	PKN02-00 = “111”	
KVN9	VLCD63-ΔV*(VRN0+33R+VRHN)/SUMRN	PKN12-10 = “000”	VINN2
KVN10	VLCD63-ΔV*(VRN0+34R+VRHN)/SUMRN	PKN12-10 = “001”	
KVN11	VLCD63-ΔV*(VRN0+35R+VRHN)/SUMRN	PKN12-10 = “010”	
KVN12	VLCD63-ΔV*(VRN0+36R+VRHN)/SUMRN	PKN12-10 = “011”	
KVN13	VLCD63-ΔV*(VRN0+37R+VRHN)/SUMRN	PKN12-10 = “100”	
KVN14	VLCD63-ΔV*(VRN0+38R+VRHN)/SUMRN	PKN12-10 = “101”	
KVN15	VLCD63-ΔV*(VRN0+39R+VRHN)/SUMRN	PKN12-10 = “110”	
KVN16	VLCD63-ΔV*(VRN0+40R+VRHN)/SUMRN	PKN12-10 = “111”	
KVN17	VLCD63-ΔV*(VRN0+45R+VRHN)/SUMRN	PKN22-20 = “000”	VINN3
KVN18	VLCD63-ΔV*(VRN0+46R+VRHN)/SUMRN	PKN22-20 = “001”	
KVN19	VLCD63-ΔV*(VRN0+47R+VRHN)/SUMRN	PKN22-20 = “010”	
KVN20	VLCD63-ΔV*(VRN0+48R+VRHN)/SUMRN	PKN22-20 = “011”	
KVN21	VLCD63-ΔV*(VRN0+49R+VRHN)/SUMRN	PKN22-20 = “100”	
KVN22	VLCD63-ΔV*(VRN0+50R+VRHN)/SUMRN	PKN22-20 = “101”	
KVN23	VLCD63-ΔV*(VRN0+51R+VRHN)/SUMRN	PKN22-20 = “110”	
KVN24	VLCD63-ΔV*(VRN0+52R+VRHN)/SUMRN	PKN22-20 = “111”	
KVN25	VLCD63-ΔV*(VRN0+68R+VRHN)/SUMRN	PKN32-30 = “000”	VINN4
KVN26	VLCD63-ΔV*(VRN0+69R+VRHN)/SUMRN	PKN32-30 = “001”	
KVN27	VLCD63-ΔV*(VRN0+70R+VRHN)/SUMRN	PKN32-30 = “010”	
KVN28	VLCD63-ΔV*(VRN0+71R+VRHN)/SUMRN	PKN32-30 = “011”	
KVN29	VLCD63-ΔV*(VRN0+72R+VRHN)/SUMRN	PKN32-30 = “100”	
KVN30	VLCD63-ΔV*(VRN0+73R+VRHN)/SUMRN	PKN32-30 = “101”	
KVN31	VLCD63-ΔV*(VRN0+74R+VRHN)/SUMRN	PKN32-30 = “110”	
KVN32	VLCD63-ΔV*(VRN0+75R+VRHN)/SUMRN	PKN32-30 = “111”	
KVN33	VLCD63-ΔV*(VRN0+80R+VRHN)/SUMRN	PKN42-40 = “000”	VINN5
KVN34	VLCD63-ΔV*(VRN0+81R+VRHN)/SUMRN	PKN42-40 = “001”	
KVN35	VLCD63-ΔV*(VRN0+82R+VRHN)/SUMRN	PKN42-40 = “010”	
KVN36	VLCD63-ΔV*(VRN0+83R+VRHN)/SUMRN	PKN42-40 = “011”	
KVN37	VLCD63-ΔV*(VRN0+84R+VRHN)/SUMRN	PKN42-40 = “100”	
KVN38	VLCD63-ΔV*(VRN0+85R+VRHN)/SUMRN	PKN42-40 = “101”	
KVN39	VLCD63-ΔV*(VRN0+86R+VRHN)/SUMRN	PKN42-40 = “110”	
KVN40	VLCD63-ΔV*(VRN0+87R+VRHN)/SUMRN	PKN42-40 = “111”	
KVN41	VLCD63-ΔV*(VRN0+87R+VRHN+VRLP)/SUMRN	PKN52-50 = “000”	VINN6
KVN42	VLCD63-ΔV*(VRN0+91R+VRHN+VRLP)/SUMRN	PKN52-50 = “001”	
KVN43	VLCD63-ΔV*(VRN0+95R+VRHN+VRLP)/SUMRN	PKN52-50 = “010”	
KVN44	VLCD63-ΔV*(VRN0+99R+VRHN+VRLP)/SUMRN	PKN52-50 = “011”	
KVN45	VLCD63-ΔV*(VRN0+103R+VRHN+VRLP)/SUMRN	PKN52-50 = “100”	
KVN46	VLCD63-ΔV*(VRN0+107R+VRHN+VRLP)/SUMRN	PKN52-50 = “101”	
KVN47	VLCD63-ΔV*(VRN0+111R+VRHN+VRLP)/SUMRN	PKN52-50 = “110”	
KVN48	VLCD63-ΔV*(VRN0+115R+VRHN+VRLP)/SUMRN	PKN52-50 = “111”	
KVN49	VLCD63-ΔV*(VRN0+120R+VRHN+VRLP)/SUMRN	~	VINN7

Remark SUMRP: Total of the positive polarity ladder resistance = VRP0 + 128R + VRHP + VRLP + VRP1

SUMRN: Total of the negative polarity ladder resistance = VRN0 + 128R + VRHN + VRLN + VRN1

ΔV: Potential difference between KV0 and KV49 = VLCD63*SUMRP*SUMRN/[SUMRP*SUMRN+EXVR*(SUMRP+SUMRN)]

Table 18–5. Gamma Voltage Formula (Negative Polarity)

Gray-scale Voltage	Formula	Gray-scale Voltage	Formula
V0	VINN0	V32	V43+(V20-V43)*(11/23)
V1	VINN1	V33	V43+(V20-V43)*(10/23)
V2	V8+(V1-V8)*(30/48)	V34	V43+(V20-V43)*(9/23)
V3	V8+(V1-V8)*(23/48)	V35	V43+(V20-V43)*(8/23)
V4	V8+(V1-V8)*(16/48)	V36	V43+(V20-V43)*(7/23)
V5	V8+(V1-V8)*(12/48)	V37	V43+(V20-V43)*(6/23)
V6	V8+(V1-V8)*(8/48)	V38	V43+(V20-V43)*(5/23)
V7	V8+(V1-V8)*(4/48)	V39	V43+(V20-V43)*(4/23)
V8	VINN2	V40	V43+(V20-V43)*(3/23)
V9	V20+(V8-V20)*(22/24)	V41	V43+(V20-V43)*(2/23)
V10	V20+(V8-V20)*(20/24)	V42	V43+(V20-V43)*(1/23)
V11	V20+(V8-V20)*(18/24)	V43	VINN4
V12	V20+(V8-V20)*(16/24)	V44	V55+(V43-V55)*(22/24)
V13	V20+(V8-V20)*(14/24)	V45	V55+(V43-V55)*(20/24)
V14	V20+(V8-V20)*(12/24)	V46	V55+(V43-V55)*(18/24)
V15	V20+(V8-V20)*(10/24)	V47	V55+(V43-V55)*(16/24)
V16	V20+(V8-V20)*(8/24)	V48	V55+(V43-V55)*(14/24)
V17	V20+(V8-V20)*(6/24)	V49	V55+(V43-V55)*(12/24)
V18	V20+(V8-V20)*(4/24)	V50	V55+(V43-V55)*(10/24)
V19	V20+(V8-V20)*(2/24)	V51	V55+(V43-V55)*(8/24)
V20	VINN3	V52	V55+(V43-V55)*(6/24)
V21	V43+(V20-V43)*(22/23)	V53	V55+(V43-V55)*(4/24)
V22	V43+(V20-V43)*(21/23)	V54	V55+(V43-V55)*(2/24)
V23	V43+(V20-V43)*(20/23)	V55	VINN5
V24	V43+(V20-V43)*(19/23)	V56	V62+(V55-V62)*(44/48)
V25	V43+(V20-V43)*(18/23)	V57	V62+(V55-V62)*(40/48)
V26	V43+(V20-V43)*(17/23)	V58	V62+(V55-V62)*(36/48)
V27	V43+(V20-V43)*(16/23)	V59	V62+(V55-V62)*(32/48)
V28	V43+(V20-V43)*(15/23)	V60	V62+(V55-V62)*(25/48)
V29	V43+(V20-V43)*(14/23)	V61	V62+(V55-V62)*(18/48)
V30	V43+(V20-V43)*(13/23)	V62	VINN6
V31	V43+(V20-V43)*(12/23)	V63	VINN7

Figure 18–1. Relationship between Input Data and Output Voltage

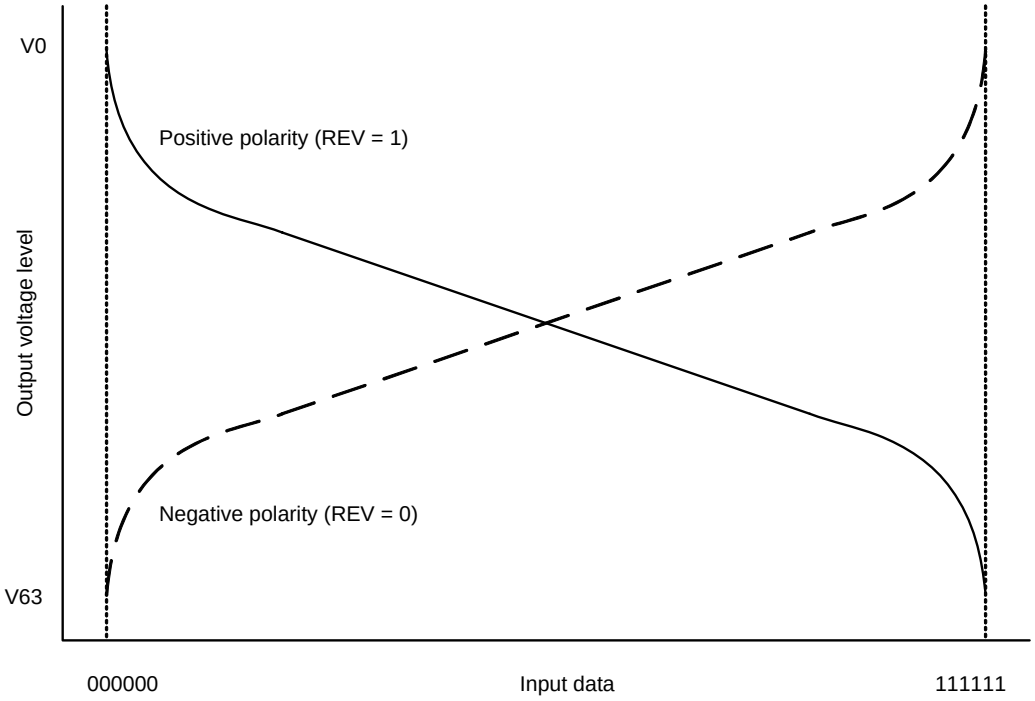
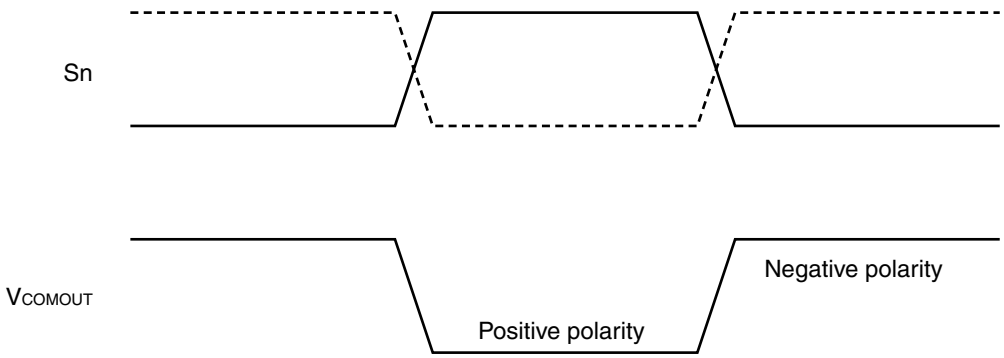


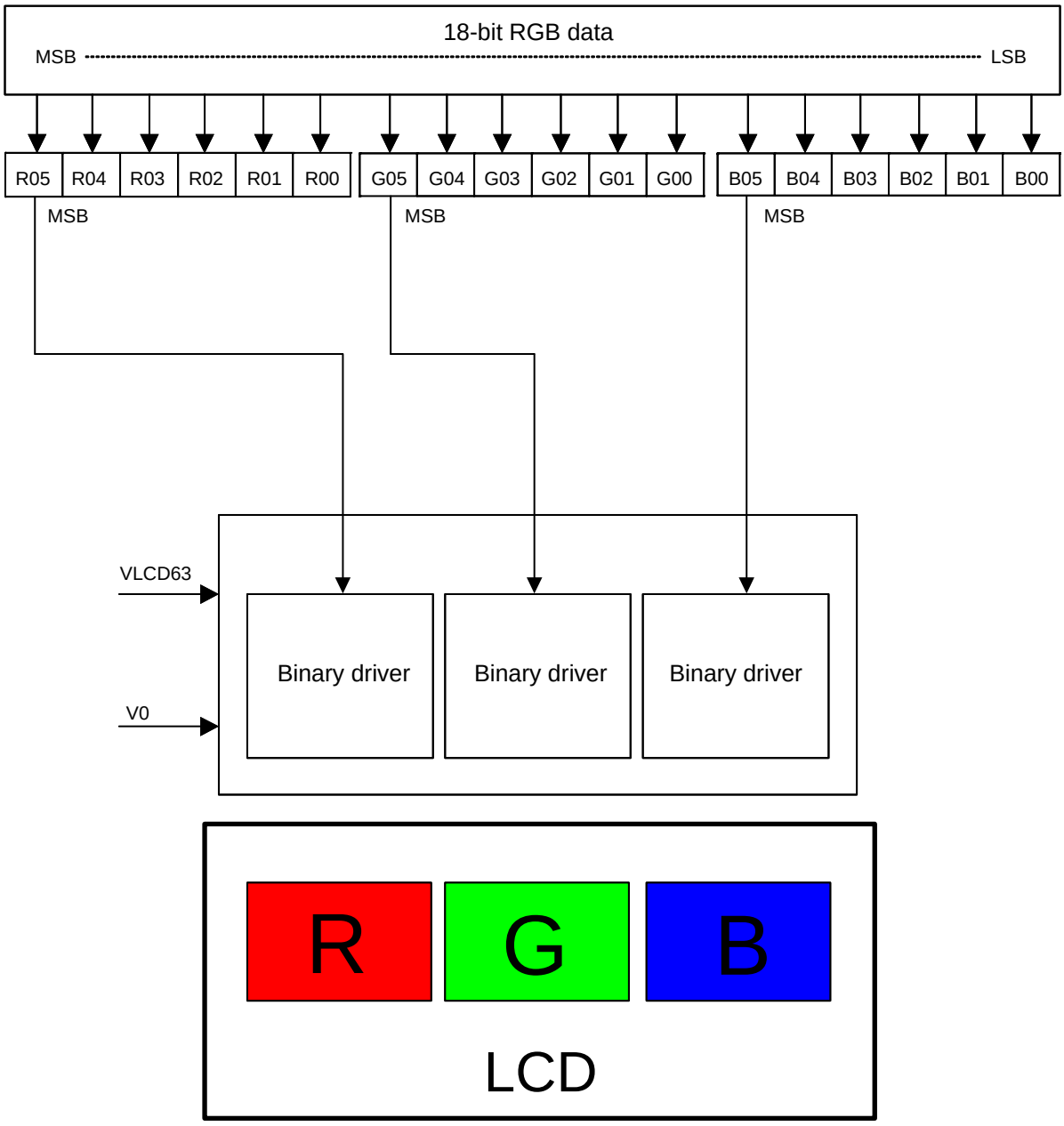
Figure 18–2. Relationship between Source Output and V_{COMOUT}



19. THE 8-COLOR DISPLAY MODE

The μPD161608 builds in 8-color display mode. Displaying the gray-scale levels in 8-color display mode, gray-scale amplifier and driver amplifier are halt. So that it attempts to lower power consumption.

Figure 19–1. 8-color Display Control

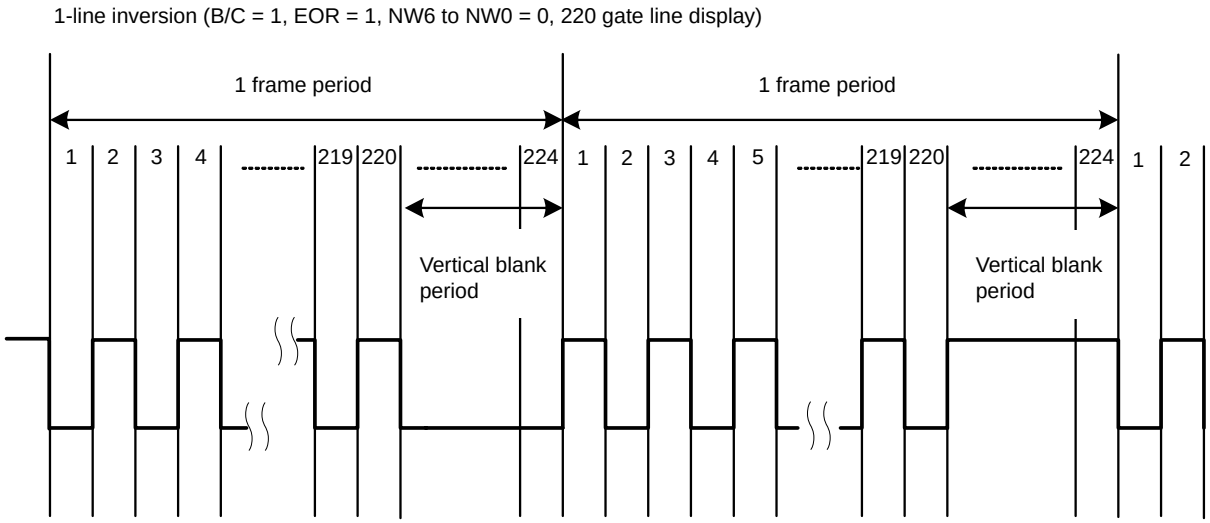


20. n-RASTER-ROW REVERSED AC DRIVER

The μPD161608 supports not only the LCD reversed AC drive in a one-frame unit but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 128 raster-rows. When a problem affecting display quality occurs, the n-raster-row reversed AC drive can improve the quality.

Determine the number of the raster-rows n (NW bit set value + 1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-row is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.

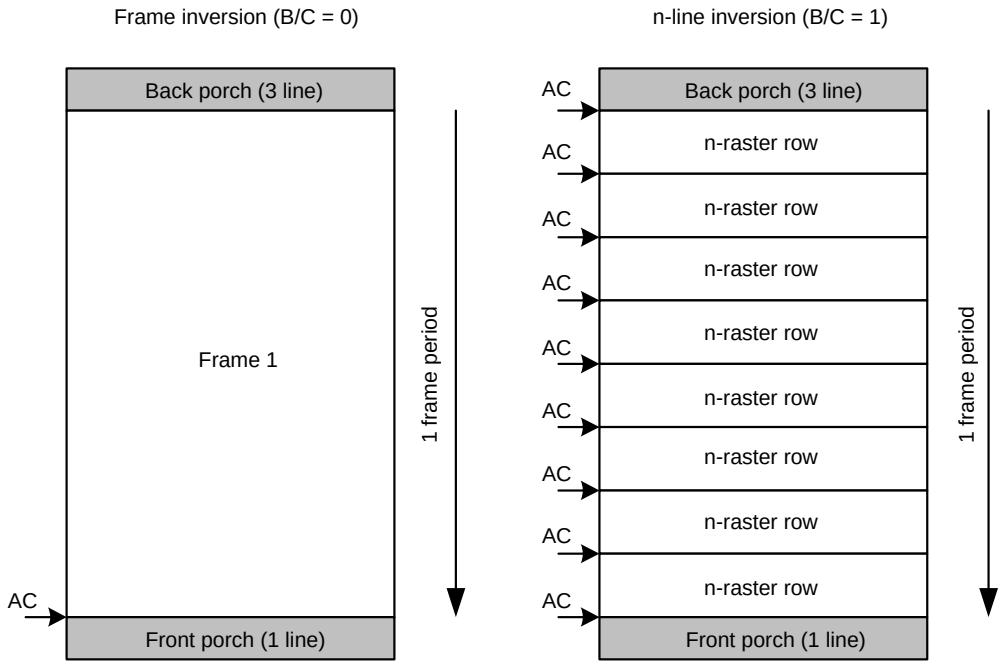
Figure 20–1. Example of an AC Signal under n-raster-row Reversed AC Drive



21. AC TIMING

Following diagram indicates the AC timing on the each AC drive method. After every 1 drawing, the AC timing is occurred on the reversed frame AC drive. After the AC timing, the blank (all outputs from the gate: VGL output) in 4H period is inserted. When the reversed n-raster-row is driving, a blank period of the 4H period is inserted after all screens are drawn.

Figure 21–1. AC Timing



22. EEPROM ACCESS

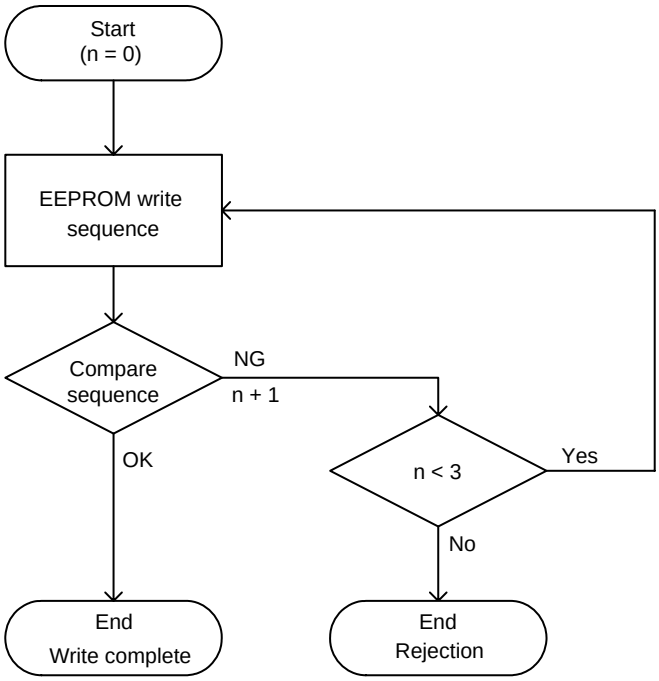
The μPD161608 builds in EEPROM for storing the internal register setting as following table. And μPD161608 can use the this EEPROM setting value as default value, when set each NOTP1 (R0DH), NOTP2 (R0EH), NOTP3 (R1EH), NOTP4 (R30H) bits to "0".

In addition, EEPROM built in the μPD161608 has a possibility that saved data may disappear, by irradiating UV light. Therefore, in case you perform UV irradiation especially at a mounting process, be careful to cope with shading etc.

Registers		Default in the case not to use EEPROM Note	
		Mode1	Mode2
R0DH	Power Control 3	0019H	001AH
R0EH	Power Control 4	7200H	7000H
R1EH	Power Control 5	0069H	0062H
R30H	Gamma Control 1	0800H	0800H
R31H	Gamma Control 2	0707H	0707H
R32H	Gamma Control 3	0406H	0406H
R33H	Gamma Control 4	0000H	0100H
R34H	Gamma Control 5	0103H	0103H
R35H	Gamma Control 6	0000H	0000H
R36H	Gamma Control 7	0707H	0707H
R37H	Gamma Control 8	0000H	0001H
R3AH	Gamma Control 9	0404H	1E00H
R3BH	Gamma Control 10	0006H	000FH

Note The case not to write any data EEPROM each NOTP1 (R0DH), NOTP2 (R0EH), NOTP3 (R1EH), NOTP4 (R30H) bits to "1", the μPD161608 use above-mentioned table value for each register's default value.

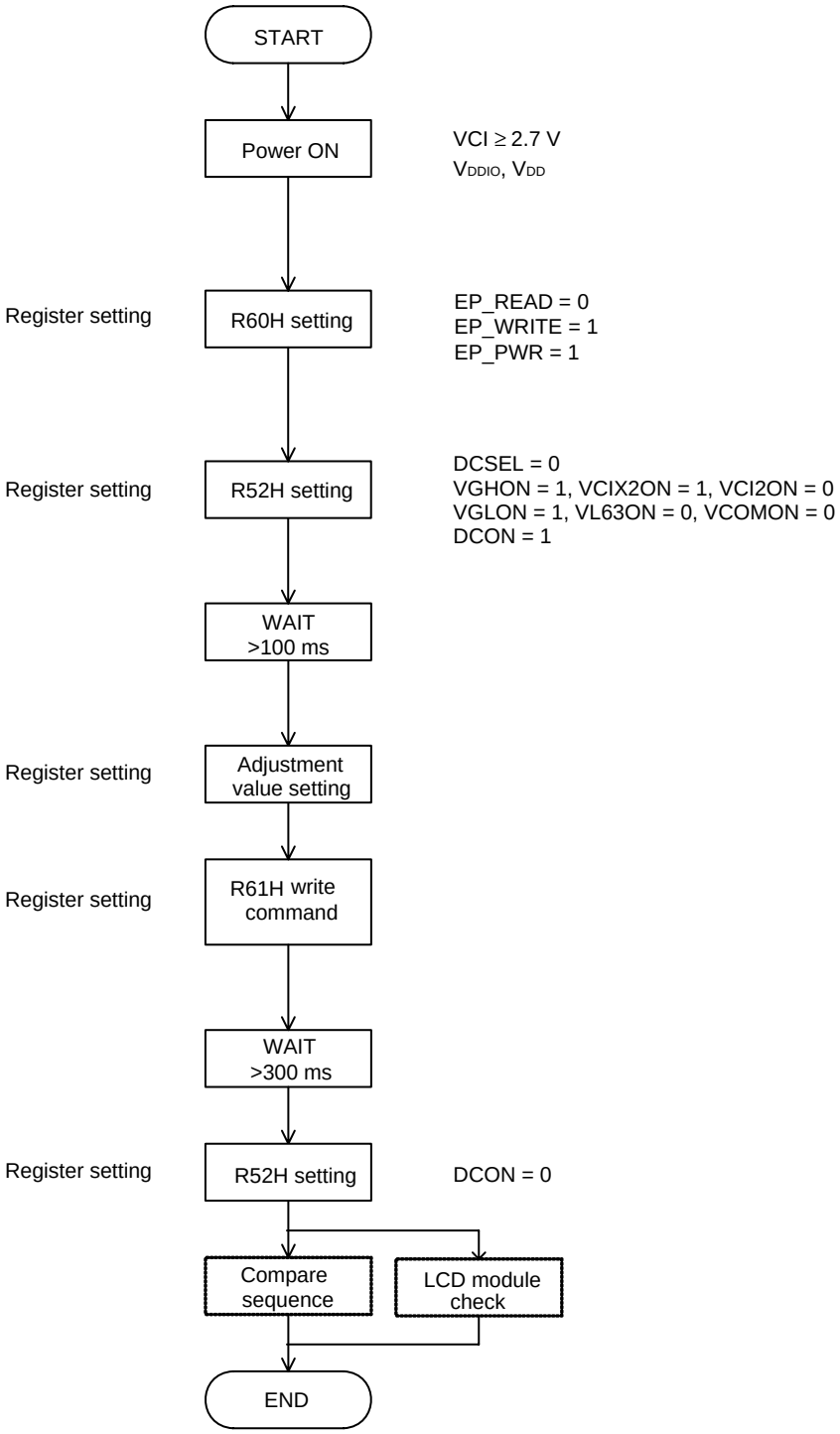
EEPROM access outline is shown as following figure.



22.1 EEPROM Erase/Write Sequence (Internal power supply mode)

The μPD161608 is able to select the power source for EEPROM erase/write. When EP_PWR (R60H) = 1, internal power supply mode is selected. In this mode, μPD161608 use the internal DC/DC converter output voltage for EEPROM operation.

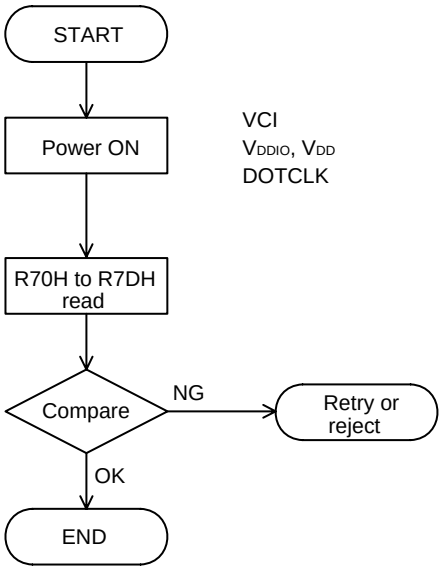
For more detail scheme, refer to following sequence.



22.2 EEPROM Compare Sequence (COMP)

The μPD161608 has the register (R70H-R7DH) which carries out the monitor of the contents of the EEPROM. By the following sequences, read the contents of R70H-R7DH and compare by comparing with the data which write. Correspondence of R70H-R7DH is shown in **13.19 EEPROM Monitor (R70H to R7DH)**.

For more detail scheme, refer to following sequence.



22.3 Initial Status before EEPROM Write

Serial Register map

Register Address	Register Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Value	
																		Mode1	Mode2
R0DH	Power Control (3)	0	0	0	0	0	0	0	0	0	0	NOTP1	Dummy1	VRH3	VRH2	VRH1	VRH0	0019H	001AH
R0EH	Power Control (4)	NOTP2	Dummy2	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0	7200H	7000H
R1EH	Power Control (5)	0	0	0	0	0	0	0	0	NOTP3	Dummy3	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	0069H	0062H
R30H	r-Control (1)	0	0	0	NOTP4	Dummy4	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00	0800H	0800H
R31H	r-Control (2)	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20	0707H	0707H
R32H	r-Control (3)	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40	0406H	0406H
R33H	r-Control (4)	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00	0000H	0100H
R34H	r-Control (5)	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00	0103H	0103H
R35H	r-Control (6)	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20	0000H	0000H
R36H	r-Control (7)	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40	0707H	0707H
R37H	r-Control (8)	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00	0000H	0001H
R3AH	r-Control (9)	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00	0404H	1E00H
R3BH	r-Control (10)	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00	0006H	000FH

EEPROM map

EEPROM Address	Register Name								D8 (Parity)	D7	D6	D5	D4	D3	D2	D1	D0	Value	
																		Mode1	Mode2
R00H	Power Control (3)								1	1	1	1	1	1	1	1	1	1FFH	1FFH
R01H	Power Control (4)								1	1	1	1	1	1	1	1	1	1FFH	1FFH
R02H	Power Control (5)								1	1	1	1	1	1	1	1	1	1FFH	1FFH
R03H	r-Control (1)								1	1	1	1	1	1	1	1	1	1FFH	1FFH
R04H	r-Control (2)								1	1	1	1	1	1	1	1	1	1FFH	1FFH
R05H	r-Control (3)								1	1	1	1	1	1	1	1	1	1FFH	1FFH
R06H	r-Control (4)								1	1	1	1	1	1	1	1	1	1FFH	1FFH
R07H	r-Control (5)								1	1	1	1	1	1	1	1	1	1FFH	1FFH
R08H	r-Control (6)								1	1	1	1	1	1	1	1	1	1FFH	1FFH
R09H	r-Control (7)								1	1	1	1	1	1	1	1	1	1FFH	1FFH
R0AH	r-Control (8)								1	1	1	1	1	1	1	1	1	1FFH	1FFH
R0BH	r-Control (9)								1	1	1	1	1	1	1	1	1	1FFH	1FFH
R0CH	r-Control (10)								1	1	1	1	1	1	1	1	1	1FFH	1FFH
R0DH	r-Control (9, 10)								1	1	1	1	1	1	1	1	1	1FFH	1FFH

<R> EEPROM Monitor register map

Register Address	Register Name	D15	D14	D13	D12	D11	D10	D9	D8 (Parity)	D7	D6	D5	D4	D3	D2	D1	D0	Value	
																		Mode1	Mode2
R70H	Power Control (3)	There are no actual Registers. When there registers are read, value is '0'.							0	0	0	Dummy5	Dummy1	VRH[3]	VRH[2]	VRH[1]	VRH[0]	0009H	000AH
R71H	Power Control (4)								0	Dummy6	Dummy2	VCOMG	VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]	0032H	0030H
R72H	Power Control (5)								0	Dummy7	Dummy3	VCM[5]	VCM[4]	VCM[3]	VCM[2]	VCM[1]	VCM[0]	0029H	0022H
R73H	r-Control (1)								0	Dummy8	Dummy4	PKP1[2]	PKP1[1]	PKP1[0]	PKP0[2]	PKP0[1]	PKP0[0]	0000H	0000H
R74H	r-Control (2)								0	0	PKP3[2]	PKP3[1]	PKP3[0]	0	PKP2[2]	PKP2[1]	PKP2[0]	0077H	0077H
R75H	r-Control (3)								0	0	PKP5[2]	PKP5[1]	PKP5[0]	0	PKP4[2]	PKP4[1]	PKP4[0]	0046H	0046H
R76H	r-Control (4)								0	0	PRP1[2]	PRP1[1]	PRP1[0]	0	PRP0[2]	PRP0[1]	PRP0[0]	0000H	0010H
R77H	r-Control (5)								0	0	PKN1[2]	PKN1[1]	PKN1[0]	0	PKN0[2]	PKN0[1]	PKN0[0]	0013H	0013H
R78H	r-Control (6)								0	0	PKN3[2]	PKN3[1]	PKN3[0]	0	PKN2[2]	PKN2[1]	PKN2[0]	0000H	0000H
R79H	r-Control (7)								0	0	PKN5[2]	PKN5[1]	PKN5[0]	0	PKN4[2]	PKN4[1]	PKN4[0]	0077H	0077H
R7AH	r-Control (8)								0	0	PRN1[2]	PRN1[1]	PRN1[0]	0	PRN0[2]	PRN0[1]	PRN0[0]	0000H	0001H
R7BH	r-Control (9)								0	VRP1[2]	VRP1[1]	VRP1[0]	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]	0084H	00C0H
R7CH	r-Control (10)								0	VRN1[2]	VRN1[1]	VRN1[0]	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]	0006H	000FH
R7DH	r-Control (9, 10)								0	0	0	VRN1[4]	VRN1[3]	0	0	VRP1[4]	VRP1[3]	0000H	0003H

22.4 Example of after EEPROM Write Status

The example that R1EH (Power control 5) register is set by the customer is shown below.

Serial Register map

R1EH is set by the customer.

Register Address	Register Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Value	
																		Mode1	Mode2
R0DH	Power Control (3)	0	0	0	0	0	0	0	0	0	0	NOTP1	Dummy1	VRH3	VRH2	VRH1	VRH0	0019H	001AH
R0EH	Power Control (4)	NOTP2	Dummy2	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0	7200H	7000H
R1EH	Power Control (5)	0	0	0	0	0	0	0	0	NOTP3	Dummy3	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	*	*
R30H	r-Control (1)	0	0	0	NOTP4	Dummy4	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00	0800H	0800H
R31H	r-Control (2)	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20	0707H	0707H
R32H	r-Control (3)	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40	0406H	0406H
R33H	r-Control (4)	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00	0000H	0100H
R34H	r-Control (5)	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00	0103H	0103H
R35H	r-Control (6)	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20	0000H	0000H
R36H	r-Control (7)	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40	0707H	0707H
R37H	r-Control (8)	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00	0000H	0001H
R3AH	r-Control (9)	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00	0404H	1E00H
R3BH	r-Control (10)	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00	0006H	000FH

<R> EEPROM map

Once EEPROM write command is executed, all register value are copied to EEPROM. And added calculated parity bits.

EEPROM Address	Register Name								D8 (Parity)	D7	D6	D5	D4	D3	D2	D1	D0	Value	
																		Mode1	Mode2
R00H	Power Control (3)								X	0	0	Dummy5	Dummy1	VRH[3]	VRH[2]	VRH[1]	VRH[0]	119H	11AH
R01H	Power Control (4)								X	Dummy6	Dummy2	VCOMG	VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]	072H	170H
R02H	Power Control (5)								X	Dummy7	Dummy3	VCM[5]	VCM[4]	VCM[3]	VCM[2]	VCM[1]	VCM[0]	*	*
R03H	r-Control (1)								X	Dummy8	Dummy4	PKP1[2]	PKP1[1]	PKP1[0]	PKP0[2]	PKP0[1]	PKP0[0]	140H	140H
R04H	r-Control (2)								X	0	PKP3[2]	PKP3[1]	PKP3[0]	0	PKP2[2]	PKP2[1]	PKP2[0]	077H	077H
R05H	r-Control (3)								X	0	PKP5[2]	PKP5[1]	PKP5[0]	0	PKP4[2]	PKP4[1]	PKP4[0]	146H	146H
R06H	r-Control (4)								X	0	PRP1[2]	PRP1[1]	PRP1[0]	0	PRP0[2]	PRP0[1]	PRP0[0]	110H	110H
R07H	r-Control (5)								X	0	PKN1[2]	PKN1[1]	PKN1[0]	0	PKN0[2]	PKN0[1]	PKN0[0]	113H	113H
R08H	r-Control (6)								X	0	PKN3[2]	PKN3[1]	PKN3[0]	0	PKN2[2]	PKN2[1]	PKN2[0]	000H	000H
R09H	r-Control (7)								X	0	PKN5[2]	PKN5[1]	PKN5[0]	0	PKN4[2]	PKN4[1]	PKN4[0]	077H	077H
R0AH	r-Control (8)								X	0	PRN1[2]	PRN1[1]	PRN1[0]	0	PRN0[2]	PRN0[1]	PRN0[0]	000H	101H
R0BH	r-Control (9)								X	VRP1[2]	VRP1[1]	VRP1[0]	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]	084H	0C0H
R0CH	r-Control (10)								X	VRN1[2]	VRN1[1]	VRN1[0]	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]	006H	00FH
R0DH	r-Control (9, 10)								X	0	0	VRN1[4]	VRN1[3]	0	0	VRP1[4]	VRP1[3]	000H	003H

<R> EEPROM Monitor register map

Register Address	Register Name	D15	D14	D13	D12	D11	D10	D9	D8 (Parity)	D7	D6	D5	D4	D3	D2	D1	D0	Value	
																		Mode1	Mode2
R70H	Power Control (3)								X	0	0	Dummy5	Dummy1	VRH[3]	VRH[2]	VRH[1]	VRH[0]	0119H	011AH
R71H	Power Control (4)								X	Dummy6	Dummy2	VCOMG	VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]	0072H	0170H
R72H	Power Control (5)								X	Dummy7	Dummy3	VCM[5]	VCM[4]	VCM[3]	VCM[2]	VCM[1]	VCM[0]	*	*
R73H	r-Control (1)								X	Dummy8	Dummy4	PKP1[2]	PKP1[1]	PKP1[0]	PKP0[2]	PKP0[1]	PKP0[0]	0140H	0140H
R74H	r-Control (2)								X	0	PKP3[2]	PKP3[1]	PKP3[0]	0	PKP2[2]	PKP2[1]	PKP2[0]	0077H	0077H
R75H	r-Control (3)								X	0	PKP5[2]	PKP5[1]	PKP5[0]	0	PKP4[2]	PKP4[1]	PKP4[0]	0146H	0146H
R76H	r-Control (4)								X	0	PRP1[2]	PRP1[1]	PRP1[0]	0	PRP0[2]	PRP0[1]	PRP0[0]	0110H	0110H
R77H	r-Control (5)								X	0	PKN1[2]	PKN1[1]	PKN1[0]	0	PKN0[2]	PKN0[1]	PKN0[0]	0113H	0113H
R78H	r-Control (6)								X	0	PKN3[2]	PKN3[1]	PKN3[0]	0	PKN2[2]	PKN2[1]	PKN2[0]	0000H	0000H
R79H	r-Control (7)								X	0	PKN5[2]	PKN5[1]	PKN5[0]	0	PKN4[2]	PKN4[1]	PKN4[0]	0077H	0077H
R7AH	r-Control (8)								X	0	PRN1[2]	PRN1[1]	PRN1[0]	0	PRN0[2]	PRN0[1]	PRN0[0]	0000H	0101H
R7BH	r-Control (9)								X	VRP1[2]	VRP1[1]	VRP1[0]	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]	0084H	00C0H
R7CH	r-Control (10)								X	VRN1[2]	VRN1[1]	VRN1[0]	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]	0006H	000FH
R7DH	r-Control (9, 10)								X	0	0	VRN1[4]	VRN1[3]	0	0	VRP1[4]	VRP1[3]	0000H	0003H

There are no actual Registers.
When there registers are read, value is '0'.

23. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	−0.5 to +3.6	V
Power supply voltage	V_{DDIO}	−0.5 to +6.0	V
Power supply voltage	VCI	−0.5 to +6.0	V
Power supply voltage	VLCD63	−0.5 to +6.0	V
Power supply voltage	VGH	−0.5 to +20.0	V
Power supply voltage	VGL	−20.0 to +0.5	V
Power supply voltage	VGH-VGL	−0.5 to +40.0	V
Input voltage	V_I	−0.5 to V_{DDIO}+0.5	V
Input current	I_I	±10	mA
Output current	I_O	±10	mA
Operating ambient temperature	T_A	−20 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = −20 to +70°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}	1.6		2.7	V
Power supply voltage	V_{DDIO}	1.6		3.3	V
Power supply voltage	VCI	2.5	2.8	3.3	V
Power supply voltage	VLCD63	3.6	5.0	5.5	V
Power supply voltage	VGH	10.0	13.75	16.5	V
Power supply voltage (EEPROM write)		10.50	10.75	11.00	V
Power supply voltage	VGL	−13.75	−11.0	−7.5	V
Power supply voltage (EEPROM write)		−11.00	−10.75	−10.50	V
Power supply voltage	VGH-VGL	17.5	24.75	30.25	V
Power supply voltage	VCIX2	5.0		5.5	V
Input voltage	V_{I1} **Note**	0		V_{DDIO}	V

Note Power supply system of V_{DD} pin

EEPROM Rewrite cycle

Characteristics	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Rewrite cycle	N_W		–	–	5	Cycle

DC Characteristics (V_{SS} = 0 V, T_A = –20 to +70°C)

Characteristics	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Note
Leakage Current	I_{VDDIOS}	REGVDD = "H", V_{DDIO} = 2.7 V			3	μA	1
		REGVDD = "L", V_{DDIO} = 3.3 V			10	μA	1
	I_{VCIS}	VCI = 3.3 V			5	μA	1
LCD driving voltage	ΔCOMH		–100		+100	mV	–
	ΔCOML		–100		+100	mV	–
	VGH	VCI = 2.775 V, BT [2:0] = 011	12.4	13.8	14.0	V	2
	VGL		–14.0	–13.8	–12.4	V	2
	VLCD63	TMB = H (Mode1)	4.26	4.35	4.44	V	5
	Δ VLCD63		–2		+2	%	–
Input high voltage	V_{IH}		0.8 x V_{DDIO}		V_{DDIO}	V	3
Input low voltage	V_{IL}		0		0.2 x V_{DDIO}	V	3
Output high voltage	V_{OH}	I_{OH} = –100 μA	V_{DDIO}–0.5		V_{DDIO}	V	4
Output low voltage	V_{OL}	I_{OL} = 100 μA	0.0		0.5	V	4
Input leakage current	I_{IL}	V_{IN} = V_{SS} or VCI	–1.0		1.0	μA	3
Output leakage current	I_{OL}	V_{IN} = V_{SS} or VCI	–3.0		3.0	μA	4
Regulator output voltage	RVDD		1.8	2.0	2.2	V	6

Notes 1. T_A = 25°C

2. Display OFF state

3. Applied pins for input voltage: RL, TB, BGR, REV, SHUT, CM, CSB, SQL, SDI, SPID, DOTCLK, ENABLE, RR [5:0], GG [5:0], BB [5:0], HSYNC, VSYNC, RESETB, REGVDD

4. Applied pin for output voltage: SDO

5. T_A = 70°C

6. REGVDD = L, V_{DD} = V_{DDIO} > 2.0 V

DC Characteristics for LCD driver output (V_{SS} = 0 V, T_A = –20 to +70°C)

Characteristics	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Note
1st step-up input voltage	VCI		2.5		3.3	V	–
1st step-up output efficiency	VCIX2	I_{LOAD} = 500 μA	95	99	–	%	–
2nd step-up input voltage	VCI		3.4		5.5	V	–
2nd step-up output efficiency	VGH	I_{LOAD} = 100 μA	90	95	–	%	–
	VGL	I_{LOAD} = 100 μA	90	95	–	%	–
3rd step-up input voltage	VCI		2.5		3.3	V	–
3rd step-up output efficiency	VCI2	I_{LOAD} = 100 μA	90	95	-	%	–
LCD gate driver output On resistance	R_{ON}	VGH = 13.775 V, VGL = –13.775 V		2	4	kΩ	1
LCD source driver high-level output current (Gradation output)	I_{HOG}	V_{SO} = 4.5 V, V_{SX} = 3.5 V			–50	μA	2
LCD source driver low-level output current (Gradation output)	I_{LOG}	V_{SO} = 0.5 V, V_{SX} = 1.5 V	50			μA	2
Output voltage deviation (Mean value)	ΔVo	4.2 V ≤ V_{SO}		±20	±55	mV	2
		0.8 V < V_{SO} < 4.2 V		±10	±30	mV	2
		V_{SO} ≤ 0.8 V		±20	±55	mV	2
LCD source driver output voltage range	V_{SO}		V_{SS} + 0.1		VCIX2 – 0.1	V	–
LCD source driver high-level output current (Binary output)	I_{HOB}	V_{SO} = 5.0 V, V_{SX} = 4.0 V			–100	μA	2
LCD source driver low-level output current (Binary output)	I_{LOB}	V_{SO} = 0.0 V, V_{SX} = 1.0 V	100			μA	2
LCD source driver delay	t_{SD}	VCIX2 = 5.5 V, VLCD63 = 5.0 V			35	μs	–
Current consumption during normal operation	I_{VCI}	No load		2.0		mA	3

Notes 1. T_A = 70°C

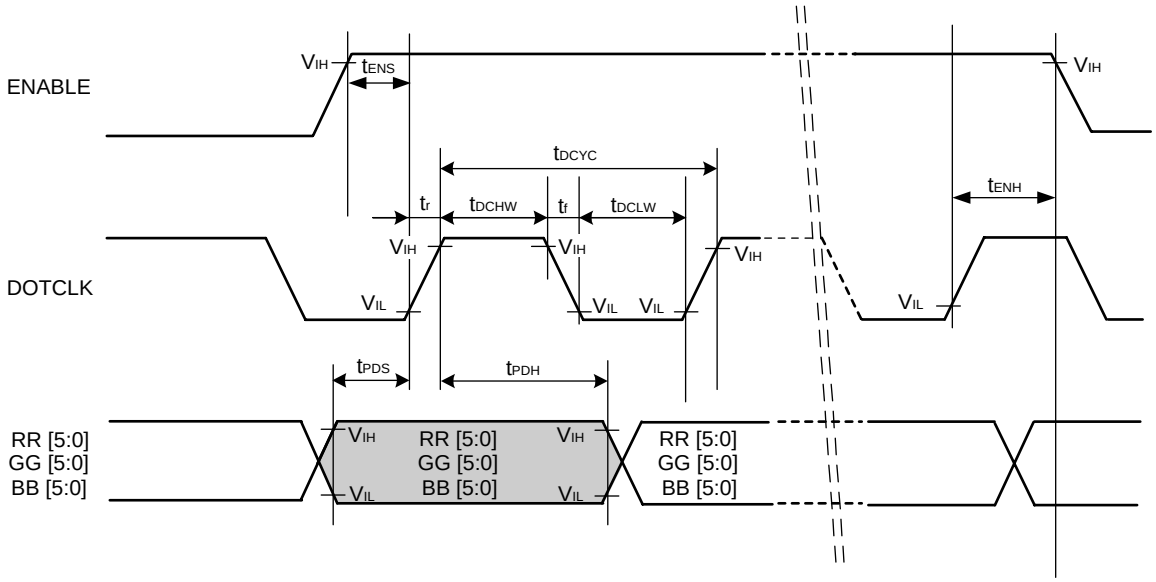
2. V_{SX} is the voltage applied to analog output pins S0 to S527. V_{SO} is the output voltage of analog output pins S0 to S527.

3. V_{DDIO} = V_{DD} = 1.875 V, REGVDD = V_{SS}, VCI = 2.775 V, CM = L (260-K color), REV = H,
RR [5:0] = GG [5:0] = BB [5:0] = 000000,
R01H-R03H, R0BH, R0DH-R0FH, R16H, R17H, R1EH, R30H-R37H, R3AH, R3BH are default value.
DOTCLK = 2.64 MHz TYP., no load, CX, CY, C1, C2, C3 = 0.1 μF

RGB Data Interface Characteristics (T_A = –20 to +70°C)

Characteristics	Symbol	MIN.	TYP.	MAX.	Unit
DOTCLK cycle time	t_{DCYC}	361	–	–	ns
DOTCLK pulse width high	t_{DCHW}	150	–	–	ns
DOTCLK pulse width low	t_{DCLW}	150	–	–	ns
ENABLE setup time	t_{ENS}	30	–	–	ns
ENABLE hold time	t_{ENH}	30	–	–	ns
PD data setup time	t_{PDS}	40	–	–	ns
PD data hold time	t_{PDH}	40	–	–	ns

Figure 23–1. AC Characteristics (RGB mode)



Clock Synchronized Serial Mode Characteristics (T_A = –20 to +70°C)

Characteristics	Symbol	MIN.	TYP.	MAX.	Unit
Serial clock cycle time (write)	t_{SYNC}	100	–	–	ns
Serial clock cycle time (read)	t_{SYNC}	300	–	–	ns
Serial clock rise/fall time	t_r, t_f	–	–	15	ns
Pulse width high for write	t_{SCHW}	35	–	–	ns
Pulse width high for read	t_{SCHR}	35	–	–	ns
Pulse width low for write	t_{SCLW}	35	–	–	ns
Pulse width low for read	t_{SCLR}	235	–	–	ns
Chip Select setup time	t_{CSS}	30	–	–	ns
Chip Select hold time	t_{CSH}	30	–	–	ns
Serial input data setup time	t_{SIDS}	30	–	–	ns
Serial input data hold time	t_{SIDH}	30	–	–	ns
Serial output data delay time	t_{SODD}	–	–	200	ns
Serial output data hold time	t_{SODH}	5	–	–	ns

Reset Timing Characteristics (T_A = –20 to +70°C)

Characteristics	Symbol	MIN.	TYP.	MAX.	Unit
Reset low pulse width	t_{RES}	10	–	–	μs
Reset release time	t_{REL}	10	–	–	μs

Caution Reset low pulse width shorter than 1 μs do not make reset. It means undesired short pulse such as glitch, bouncing noise or electrostatic discharge do not cause irregular system reset.

Figure 23–2. AC Characteristics (SPI mode)

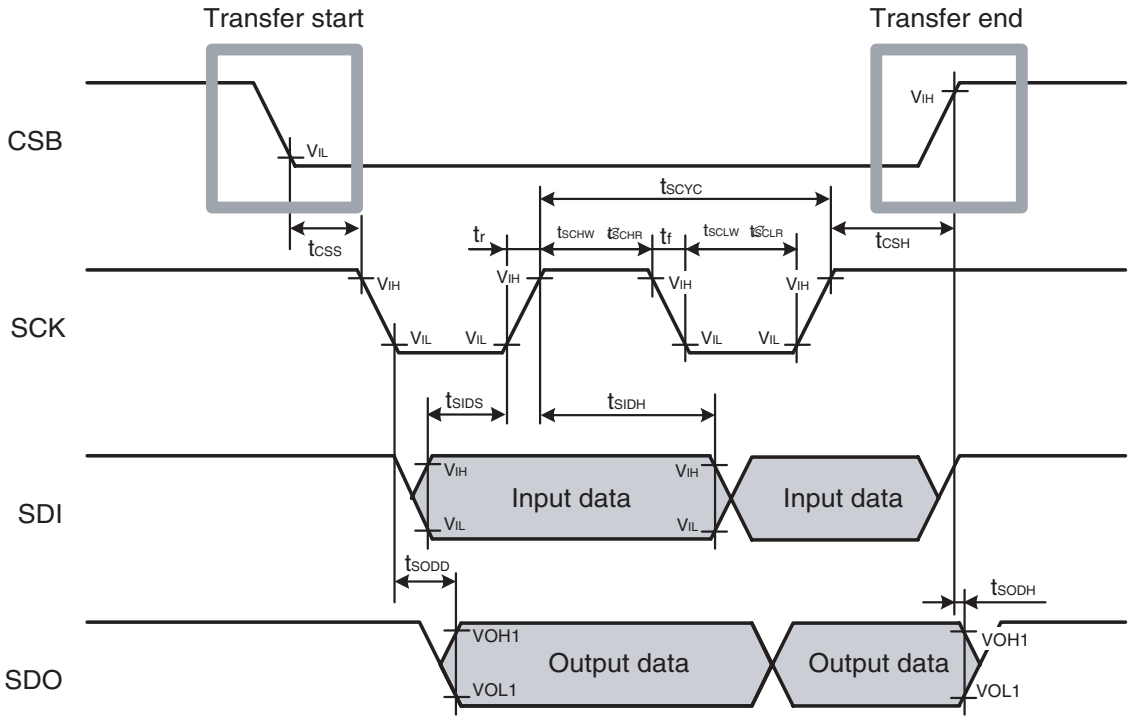


Figure 23–3. AC characteristics (RESET Mode)

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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