RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD16718

480/420-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

DESCRIPTION

The μPD16718 is a source driver for TFT-LCDs capable of dealing with displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ-corrected by an internal D/A converter and 7-by-2 external power modules. Because the output dynamic range is as large as V_{SS2} + 0.1 V to V_{DD2} – 0.1 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 57 MHz when driving at 2.5 V, this driver is applicable to SXGA+/UXGA-standard TFT-LCD panels.

FEATURES

- CMOS level input (2.5 to 3.6 V)
- 480/420 Outputs
- Input of 6 bits (gray scale data) by 6 dots
- Capable of outputting 64 values by means of 7-by-2 external power modules (14 units) and a D/A converter (R-DAC)
- Logic power supply voltage (V_{DD1}): 2.5 to 3.6 V
- Driver power supply voltage (V_{DD2}): 10.0 to 12.5 V
- Output dynamic range V_{SS2} + 0.1 V to V_{DD2} – 0.1 V
- High-speed data transfer: f_{CLK} = 57 MHz (internal data transfer speed when operating at V_{DD1} = 2.5 V
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output Voltage polarity inversion function (POL)
- Display data inversion function (capable of controlling by each input port) (POL21, POL22)
- Current consumption control function (LPC)
- TCP/COF package

★ ORDERING INFORMATION

Part Number	Package
μPD16718N-xxx	TCP (TAB package)
μPD16718NL-xxx	COF (Chip on Film) package

Remark Consult an our sales representative regarding the TCP/COF.

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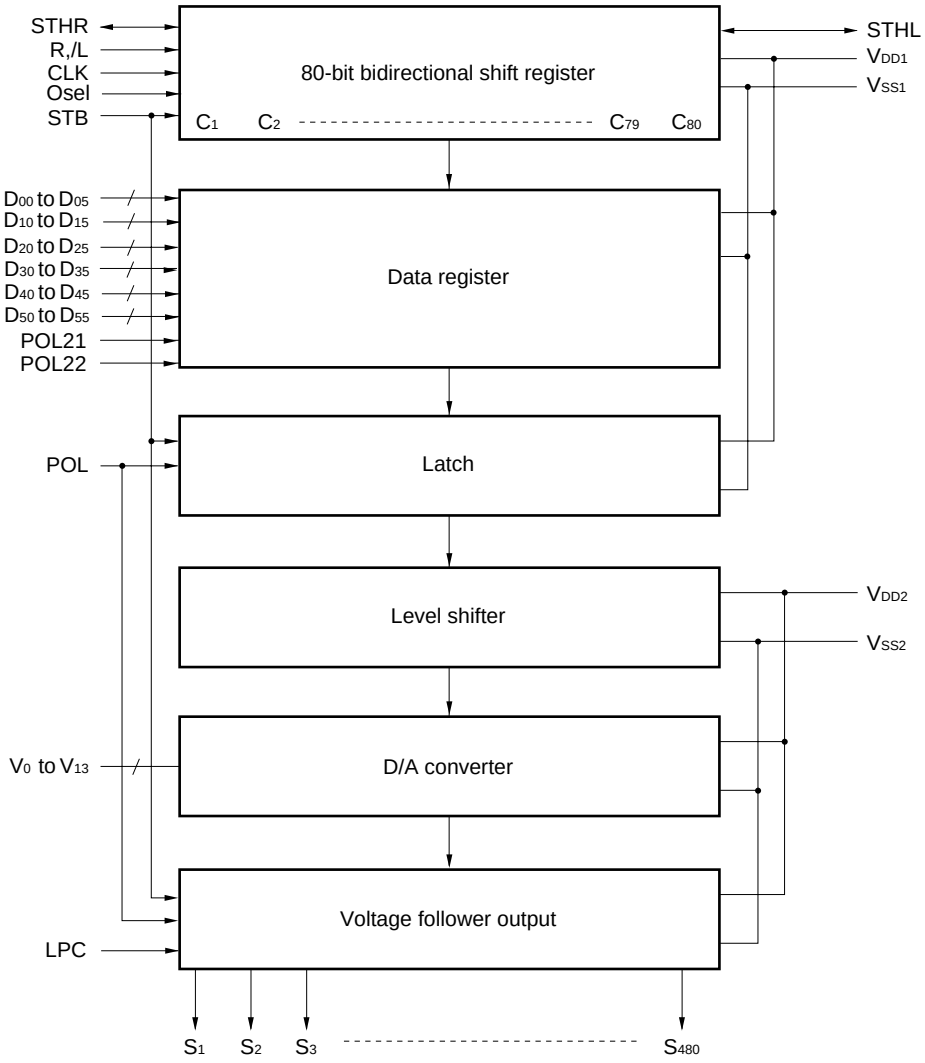
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

Document No. S15423EJ1V0DS00 (1st edition)
Date Published December 2001 NS CP(K)
Printed in Japan

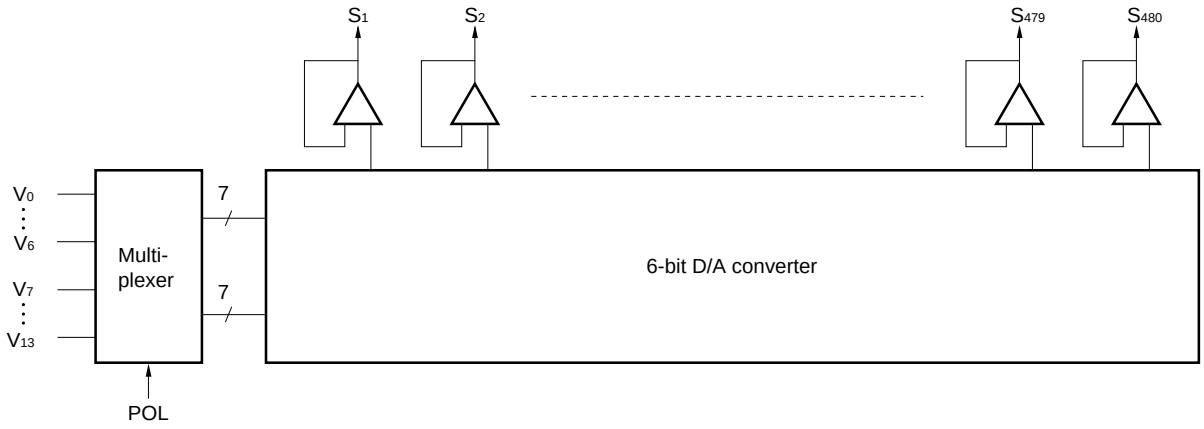
The mark ★ shows major revised points.

★ 1. BLOCK DIAGRAM

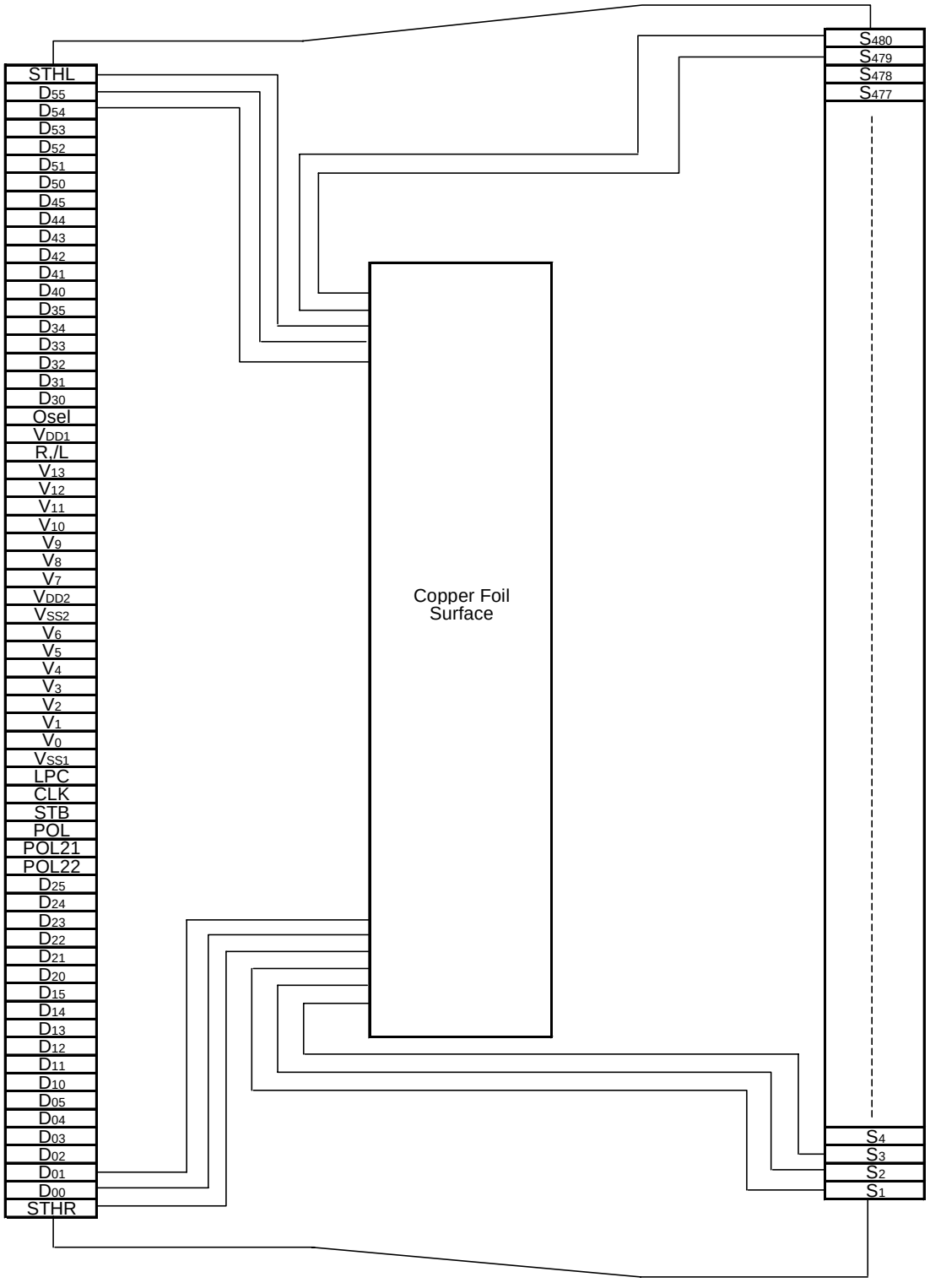


Remark /xxx indicates active low signal.

★ 2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD16718) (Copper Foil Surface, Face-up)



Remark This figure does not specify the TCP/COF package.

4. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	I/O	Description
S_1 to S_{480}	Driver	Output	The D/A converted 64-gray-scale analog voltage is output.
D_{00} to D_{05}	Display data	Input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D_{X0}: LSB, D_{X5}: MSB
D_{10} to D_{15}			
D_{20} to D_{25}			
D_{30} to D_{35}			
D_{40} to D_{45}			
D_{50} to D_{55}			
R,/L	Shift direction control	Input	Refers to the shift direction control. The shift directions of the shift registers are as follows. R,/L = H: STHR input, $S_1 \rightarrow S_{480}$, STHL output R,/L = L: STHL input, $S_{480} \rightarrow S_1$, STHR output This pin is pulled up to power supply V_{DD1} inside IC.
STHR	Right shift start pulse	I/O	These refer to the start pulse I/O pins when driver ICs are connected in cascade. Loading of display data starts when H is read at the rising edge of CLK. R,/L = H (right shift): STHR input, STHL output R,/L = L (left shift): STHL input, STHR output A high level should be input as the pulse of one cycle of the clock signal. If the start pulse input is more than 2 CLK, the first 1 CLK of the high-level input is valid.
STHL	Left shift start pulse	I/O	
CLK	Shift clock	Input	Refers to the shift register's shift clock input. The display data is loaded into the data register at the rising edge. At the rising edge of the 80(70) clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. If 82(72)-clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge. ( ) indicates 420 output.
STB	Latch	Input	The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity	Input	POL = L : The S_{2n-1} output uses V_0 to V_6 as the reference supply. The S_{2n} output uses V_7 to V_{13} as the reference supply. POL = H : The S_{2n-1} output uses V_7 to V_{13} as the reference supply. The S_{2n} output uses V_0 to V_6 as the reference supply. S_{2n-1} indicates the odd output: and S_{2n} indicates the even output. Input of the POL signal is allowed the setup time ($t_{POL-STB}$) with respect to STB's rising edge.
★ POL21, POL22	Data inversion	Input	Data inversion can invert when display data is loaded. POL21: Invert/not invert of display data D_{00} to D_{05}, D_{10} to D_{15}, D_{20} to D_{25}. POL22: Invert/not invert of display data D_{30} to D_{35}, D_{40} to D_{45}, D_{50} to D_{55}. POL21, POL22 = H: Display data is inverted inside the μPD16718. POL21, POL22 = L: Display data is not inverted.
Osel	Number of output pins select	input	Osel = H: driver output = 480 ch Osel = L or open: driver output = 420 ch (Output pins S_{211} to S_{270} are invalid) This pin is pulled down to power supply V_{DD1} inside IC.

(2/2)

Pin Symbol	Pin Name	I/O	Description
LPC	Low power control	Input	The current consumption is lowered by controlling the constant current source of the output amplifier and reduced V_{DD2} of normal current. LPC = H or open: Normal power mode LPC = L: Low power mode (about 3/4 of the normal current consumption) This pin is pulled up to the V_{DD1} power supply inside IC.
V_0 to V_{13}	γ-corrected power supplies	–	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} - 0.1\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 \geq V_7 > V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} \geq V_{SS2} + 0.1\ V$ and $0.45 \times V_{DD2} \leq V_6 = V_7 \leq 0.55 \times V_{DD2}$ or $V_{DD2} - 0.1\ V \geq V_6 > V_5 > V_4 > V_3 > V_2 > V_1 > V_0 \geq V_{13} > V_{12} > V_{11} > V_{10} > V_9 > V_8 > V_7 \geq V_{SS2} + 0.1\ V$ and $0.45 \times V_{DD2} \leq V_0 = V_{13} \leq 0.55 \times V_{DD2}$
V_{DD1}	Logic power supply	–	2.5 to 3.6 V
V_{DD2}	Driver power supply	–	10.0 to 12.5 V
V_{SS1}	Logic ground	–	Grounding
V_{SS2}	Driver ground	–	Grounding

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_{13} in that order. Reverse this sequence to shut down. (Simultaneous power application to V_{DD2} and V_0 to V_9 is possible.)

2. To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the γ-corrected power supply terminals (V_0, V_1, V_2, ···, V_{13}) and V_{SS2}.

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

This product incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches.

The ladder resistors (r0 to r62) are designed so that the ratio of LCD panel γ-compensated voltages to V_0' to V_{63}' and V_0'' to V_{63}'' is almost equivalent. For the 2 sets of seven γ-compensated power supplies, V_0 to V_6 and V_7 to V_{13}, respectively, input gray scale voltages of the same polarity with respect to the common voltage. When fine-gray scale voltage precision is not necessary, there is no need to connect a voltage follower circuit to the γ-compensated power supplies V_0 to V_6 and V_7 to V_{13}.

Figure 5–1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2}, common electrode potential V_{COM}, and γ-corrected voltages V_0 to V_{13} and the input data. Be sure to maintain the voltage relationships as follows:

$V_{DD2} - 0.1\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 \geq V_7 > V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} \geq V_{SS2} + 0.1\ V$ and

$0.45 \times V_{DD2} \leq V_6 = V_7 \leq 0.55 \times V_{DD2}$ or

$V_{DD2} - 0.1\ V \geq V_6 > V_5 > V_4 > V_3 > V_2 > V_1 > V_0 \geq V_{13} > V_{12} > V_{11} > V_{10} > V_9 > V_8 > V_7 \geq V_{SS2} + 0.1\ V$ and

$0.45 \times V_{DD2} \leq V_0 = V_{13} \leq 0.55 \times V_{DD2}$

positive side > $0.5\ V_{DD2} - 0.5V$, negative side > $0.5\ V_{DD2} + 0.5\ V$.

Figures 5–2 and 5–3 show the relationship between input data and output voltage. This driver IC is designed for only single-sided mounting

Figure 5–1. Relationship between Input Data and γ- corrected Power Supply

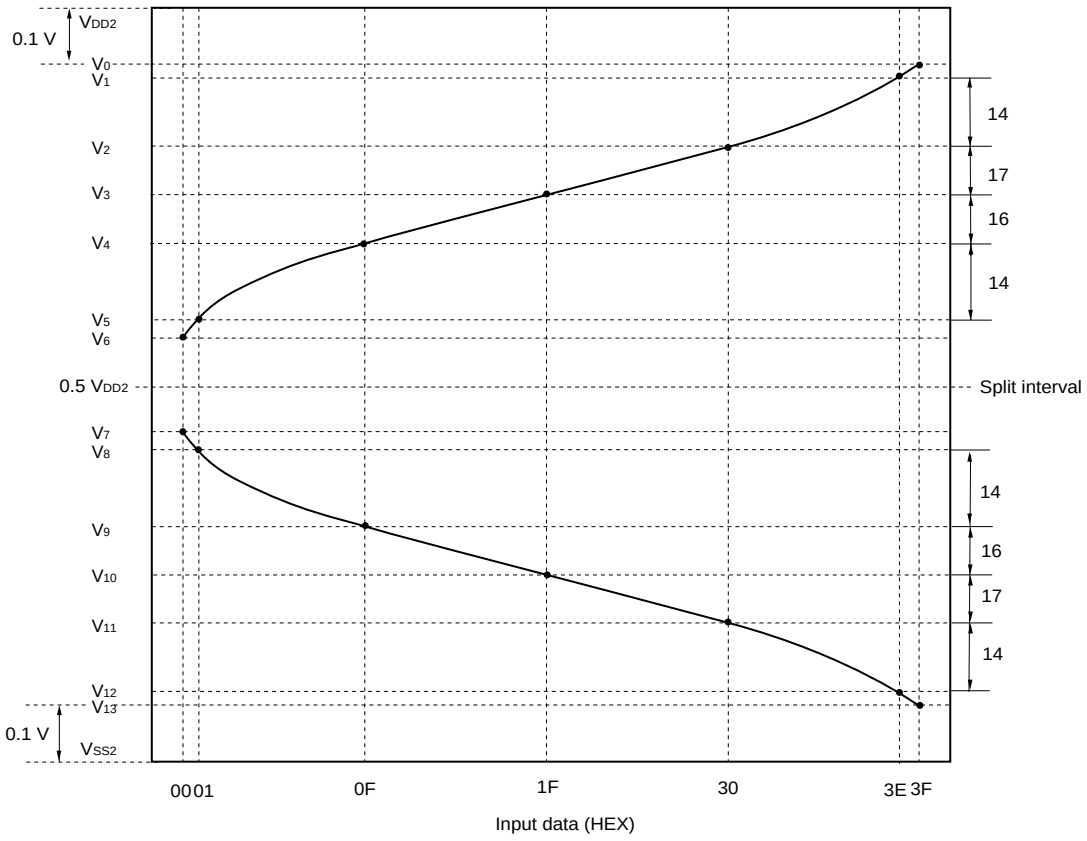
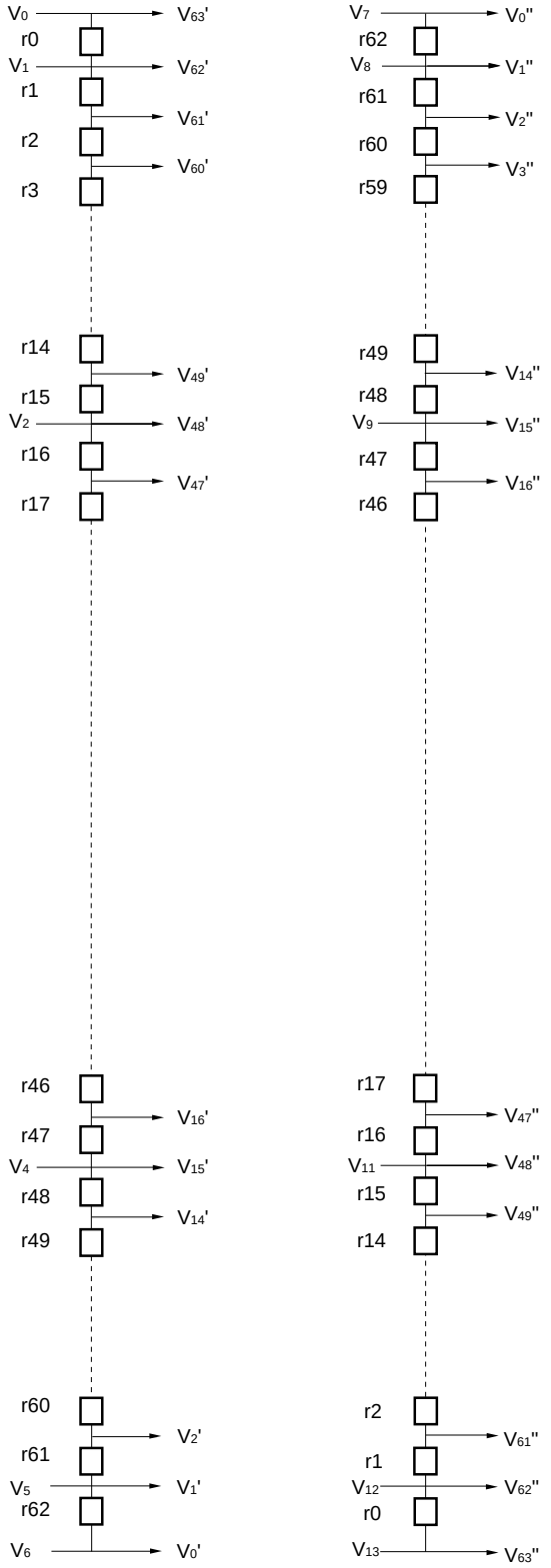


Figure 5–2. γ-corrected Voltages and Ladder Resistors Ratio



rn	Ratio
r0	7.0
r1	5.0
r2	5.0
r3	4.0
r4	3.0
r5	2.5
r6	2.5
r7	2.5
r8	2.0
r9	2.0
r10	1.8
r11	1.8
r12	1.7
r13	1.7
r14	1.7
r15	1.6
r16	1.6
r17	1.6
r18	1.6
r19	1.5
r20	1.5
r21	1.5
r22	1.5
r23	1.5
r24	1.5
r25	1.5
r26	1.5
r27	1.5
r28	1.5
r29	1.5
r30	1.5
r31	1.5
r32	1.5
r33	1.5
r34	1.5
r35	1.5
r36	1.5
r37	1.5
r38	1.5
r39	1.5
r40	1.5
r41	1.5
r42	1.5
r43	1.5
r44	1.5
r45	1.6
r46	1.6
r47	1.6
r48	1.7
r49	1.8
r50	1.9
r51	2.0
r52	2.1
r53	2.2
r54	2.3
r55	2.4
r56	2.5
r57	2.6
r58	2.7
r59	2.8
r60	2.9
r61	3.0
r62	5.0

Caution There is no connection between V_6 and V_7 terminal in the chip.

Figure 5–3. Relationship between Input Data and Output Voltage (POL21, POL22 = L)

(Output Voltage 1) $V_{DD2} - 0.1\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 \geq 0.5\ V_{DD2} - 0.5\ V$

(Output Voltage 2) $0.5\ V_{DD2} + 0.5\ V \geq V_7 > V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} \geq V_{SS2} + 0.1\ V$

Input Data	Output Voltage1					Output Voltage2				
00H	$V_{0'}$	V_6				$V_{0''}$	V_7			
01H	$V_{1'}$	V_5				$V_{1''}$	V_8			
02H	$V_{2'}$	$V_5+(V_4-V_5)\times$	3.0	/	32.9	$V_{2''}$	$V_9+(V_8-V_9)\times$	29.9	/	32.9
03H	$V_{3'}$	$V_5+(V_4-V_5)\times$	5.9	/	32.9	$V_{3''}$	$V_9+(V_8-V_9)\times$	27.0	/	32.9
04H	$V_{4'}$	$V_5+(V_4-V_5)\times$	8.7	/	32.9	$V_{4''}$	$V_9+(V_8-V_9)\times$	24.2	/	32.9
05H	$V_{5'}$	$V_5+(V_4-V_5)\times$	11.4	/	32.9	$V_{5''}$	$V_9+(V_8-V_9)\times$	21.5	/	32.9
06H	$V_{6'}$	$V_5+(V_4-V_5)\times$	14.0	/	32.9	$V_{6''}$	$V_9+(V_8-V_9)\times$	18.9	/	32.9
07H	$V_{7'}$	$V_5+(V_4-V_5)\times$	16.5	/	32.9	$V_{7''}$	$V_9+(V_8-V_9)\times$	16.4	/	32.9
08H	$V_{8'}$	$V_5+(V_4-V_5)\times$	18.9	/	32.9	$V_{8''}$	$V_9+(V_8-V_9)\times$	14.0	/	32.9
09H	$V_{9'}$	$V_5+(V_4-V_5)\times$	21.2	/	32.9	$V_{9''}$	$V_9+(V_8-V_9)\times$	11.7	/	32.9
0AH	$V_{10'}$	$V_5+(V_4-V_5)\times$	23.4	/	32.9	$V_{10''}$	$V_9+(V_8-V_9)\times$	9.5	/	32.9
0BH	$V_{11'}$	$V_5+(V_4-V_5)\times$	25.5	/	32.9	$V_{11''}$	$V_9+(V_8-V_9)\times$	7.4	/	32.9
0CH	$V_{12'}$	$V_5+(V_4-V_5)\times$	27.5	/	32.9	$V_{12''}$	$V_9+(V_8-V_9)\times$	5.4	/	32.9
0DH	$V_{13'}$	$V_5+(V_4-V_5)\times$	29.4	/	32.9	$V_{13''}$	$V_9+(V_8-V_9)\times$	3.5	/	32.9
0EH	$V_{14'}$	$V_5+(V_4-V_5)\times$	31.2	/	32.9	$V_{14''}$	$V_9+(V_8-V_9)\times$	1.7	/	32.9
0FH	$V_{15'}$	V_4				$V_{15''}$	V_9			
10H	$V_{16'}$	$V_4+(V_3-V_4)\times$	1.6	/	24.3	$V_{16''}$	$V_{10}+(V_9-V_{10})\times$	22.7	/	24.3
11H	$V_{17'}$	$V_4+(V_3-V_4)\times$	3.2	/	24.3	$V_{17''}$	$V_{10}+(V_9-V_{10})\times$	21.1	/	24.3
12H	$V_{18'}$	$V_4+(V_3-V_4)\times$	4.8	/	24.3	$V_{18''}$	$V_{10}+(V_9-V_{10})\times$	19.5	/	24.3
13H	$V_{19'}$	$V_4+(V_3-V_4)\times$	6.3	/	24.3	$V_{19''}$	$V_{10}+(V_9-V_{10})\times$	18.0	/	24.3
14H	$V_{20'}$	$V_4+(V_3-V_4)\times$	7.8	/	24.3	$V_{20''}$	$V_{10}+(V_9-V_{10})\times$	16.5	/	24.3
15H	$V_{21'}$	$V_4+(V_3-V_4)\times$	9.3	/	24.3	$V_{21''}$	$V_{10}+(V_9-V_{10})\times$	15.0	/	24.3
16H	$V_{22'}$	$V_4+(V_3-V_4)\times$	10.8	/	24.3	$V_{22''}$	$V_{10}+(V_9-V_{10})\times$	13.5	/	24.3
17H	$V_{23'}$	$V_4+(V_3-V_4)\times$	12.3	/	24.3	$V_{23''}$	$V_{10}+(V_9-V_{10})\times$	12.0	/	24.3
18H	$V_{24'}$	$V_4+(V_3-V_4)\times$	13.8	/	24.3	$V_{24''}$	$V_{10}+(V_9-V_{10})\times$	10.5	/	24.3
19H	$V_{25'}$	$V_4+(V_3-V_4)\times$	15.3	/	24.3	$V_{25''}$	$V_{10}+(V_9-V_{10})\times$	9.0	/	24.3
1AH	$V_{26'}$	$V_4+(V_3-V_4)\times$	16.8	/	24.3	$V_{26''}$	$V_{10}+(V_9-V_{10})\times$	7.5	/	24.3
1BH	$V_{27'}$	$V_4+(V_3-V_4)\times$	18.3	/	24.3	$V_{27''}$	$V_{10}+(V_9-V_{10})\times$	6.0	/	24.3
1CH	$V_{28'}$	$V_4+(V_3-V_4)\times$	19.8	/	24.3	$V_{28''}$	$V_{10}+(V_9-V_{10})\times$	4.5	/	24.3
1DH	$V_{29'}$	$V_4+(V_3-V_4)\times$	21.3	/	24.3	$V_{29''}$	$V_{10}+(V_9-V_{10})\times$	3.0	/	24.3
1EH	$V_{30'}$	$V_4+(V_3-V_4)\times$	22.8	/	24.3	$V_{30''}$	$V_{10}+(V_9-V_{10})\times$	1.5	/	24.3
1FH	$V_{31'}$	V_3				$V_{31''}$	V_{10}			
20H	$V_{32'}$	$V_3+(V_2-V_3)\times$	1.5	/	25.9	$V_{32''}$	$V_{11}+(V_{10}-V_{11})\times$	24.4	/	25.9
21H	$V_{33'}$	$V_3+(V_2-V_3)\times$	3.0	/	25.9	$V_{33''}$	$V_{11}+(V_{10}-V_{11})\times$	22.9	/	25.9
22H	$V_{34'}$	$V_3+(V_2-V_3)\times$	4.5	/	25.9	$V_{34''}$	$V_{11}+(V_{10}-V_{11})\times$	21.4	/	25.9
23H	$V_{35'}$	$V_3+(V_2-V_3)\times$	6.0	/	25.9	$V_{35''}$	$V_{11}+(V_{10}-V_{11})\times$	19.9	/	25.9
24H	$V_{36'}$	$V_3+(V_2-V_3)\times$	7.5	/	25.9	$V_{36''}$	$V_{11}+(V_{10}-V_{11})\times$	18.4	/	25.9
25H	$V_{37'}$	$V_3+(V_2-V_3)\times$	9.0	/	25.9	$V_{37''}$	$V_{11}+(V_{10}-V_{11})\times$	16.9	/	25.9
26H	$V_{38'}$	$V_3+(V_2-V_3)\times$	10.5	/	25.9	$V_{38''}$	$V_{11}+(V_{10}-V_{11})\times$	15.4	/	25.9
27H	$V_{39'}$	$V_3+(V_2-V_3)\times$	12.0	/	25.9	$V_{39''}$	$V_{11}+(V_{10}-V_{11})\times$	13.9	/	25.9
28H	$V_{40'}$	$V_3+(V_2-V_3)\times$	13.5	/	25.9	$V_{40''}$	$V_{11}+(V_{10}-V_{11})\times$	12.4	/	25.9
29H	$V_{41'}$	$V_3+(V_2-V_3)\times$	15.0	/	25.9	$V_{41''}$	$V_{11}+(V_{10}-V_{11})\times$	10.9	/	25.9
2AH	$V_{42'}$	$V_3+(V_2-V_3)\times$	16.5	/	25.9	$V_{42''}$	$V_{11}+(V_{10}-V_{11})\times$	9.4	/	25.9
2BH	$V_{43'}$	$V_3+(V_2-V_3)\times$	18.0	/	25.9	$V_{43''}$	$V_{11}+(V_{10}-V_{11})\times$	7.9	/	25.9
2CH	$V_{44'}$	$V_3+(V_2-V_3)\times$	19.5	/	25.9	$V_{44''}$	$V_{11}+(V_{10}-V_{11})\times$	6.4	/	25.9
2DH	$V_{45'}$	$V_3+(V_2-V_3)\times$	21.0	/	25.9	$V_{45''}$	$V_{11}+(V_{10}-V_{11})\times$	4.8	/	25.9
2EH	$V_{46'}$	$V_3+(V_2-V_3)\times$	22.6	/	25.9	$V_{46''}$	$V_{11}+(V_{10}-V_{11})\times$	3.2	/	25.9
2FH	$V_{47'}$	$V_3+(V_2-V_3)\times$	24.2	/	25.9	$V_{47''}$	$V_{11}+(V_{10}-V_{11})\times$	1.6	/	25.9
30H	$V_{48'}$	V_2				$V_{48''}$	V_{11}			
31H	$V_{49'}$	$V_2+(V_1-V_2)\times$	1.7	/	37.2	$V_{49''}$	$V_{12}+(V_{11}-V_{12})\times$	35.5	/	37.2
32H	$V_{50'}$	$V_2+(V_1-V_2)\times$	3.4	/	37.2	$V_{50''}$	$V_{12}+(V_{11}-V_{12})\times$	33.8	/	37.2
33H	$V_{51'}$	$V_2+(V_1-V_2)\times$	5.1	/	37.2	$V_{51''}$	$V_{12}+(V_{11}-V_{12})\times$	32.1	/	37.2
34H	$V_{52'}$	$V_2+(V_1-V_2)\times$	6.9	/	37.2	$V_{52''}$	$V_{12}+(V_{11}-V_{12})\times$	30.3	/	37.2
35H	$V_{53'}$	$V_2+(V_1-V_2)\times$	8.7	/	37.2	$V_{53''}$	$V_{12}+(V_{11}-V_{12})\times$	28.5	/	37.2
36H	$V_{54'}$	$V_2+(V_1-V_2)\times$	10.7	/	37.2	$V_{54''}$	$V_{12}+(V_{11}-V_{12})\times$	26.5	/	37.2
37H	$V_{55'}$	$V_2+(V_1-V_2)\times$	12.7	/	37.2	$V_{55''}$	$V_{12}+(V_{11}-V_{12})\times$	24.5	/	37.2
38H	$V_{56'}$	$V_2+(V_1-V_2)\times$	15.2	/	37.2	$V_{56''}$	$V_{12}+(V_{11}-V_{12})\times$	22.0	/	37.2
39H	$V_{57'}$	$V_2+(V_1-V_2)\times$	17.7	/	37.2	$V_{57''}$	$V_{12}+(V_{11}-V_{12})\times$	19.5	/	37.2
3AH	$V_{58'}$	$V_2+(V_1-V_2)\times$	20.2	/	37.2	$V_{58''}$	$V_{12}+(V_{11}-V_{12})\times$	17.0	/	37.2
3BH	$V_{59'}$	$V_2+(V_1-V_2)\times$	23.2	/	37.2	$V_{59''}$	$V_{12}+(V_{11}-V_{12})\times$	14.0	/	37.2
3CH	$V_{60'}$	$V_2+(V_1-V_2)\times$	27.2	/	37.2	$V_{60''}$	$V_{12}+(V_{11}-V_{12})\times$	10.0	/	37.2
3DH	$V_{61'}$	$V_2+(V_1-V_2)\times$	32.2	/	37.2	$V_{61''}$	$V_{12}+(V_{11}-V_{12})\times$	5.0	/	37.2
3EH	$V_{62'}$	V_1				$V_{62''}$	V_{12}			
3FH	$V_{63'}$	V_0				$V_{63''}$	V_{13}			

Caution There is no connection between V_6 and V_7 terminal in the chip.

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 6 bits × 2 RGBs (6 dots)

Input width: 36 bits (2-pixel data)

R,/L = H (Right shift)

Output	S_1	S_2	S_3	S_4	···	S_{479}	S_{480}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	···	D_{40} to D_{45}	D_{50} to D_{55}

R,/L = L (Left shift)

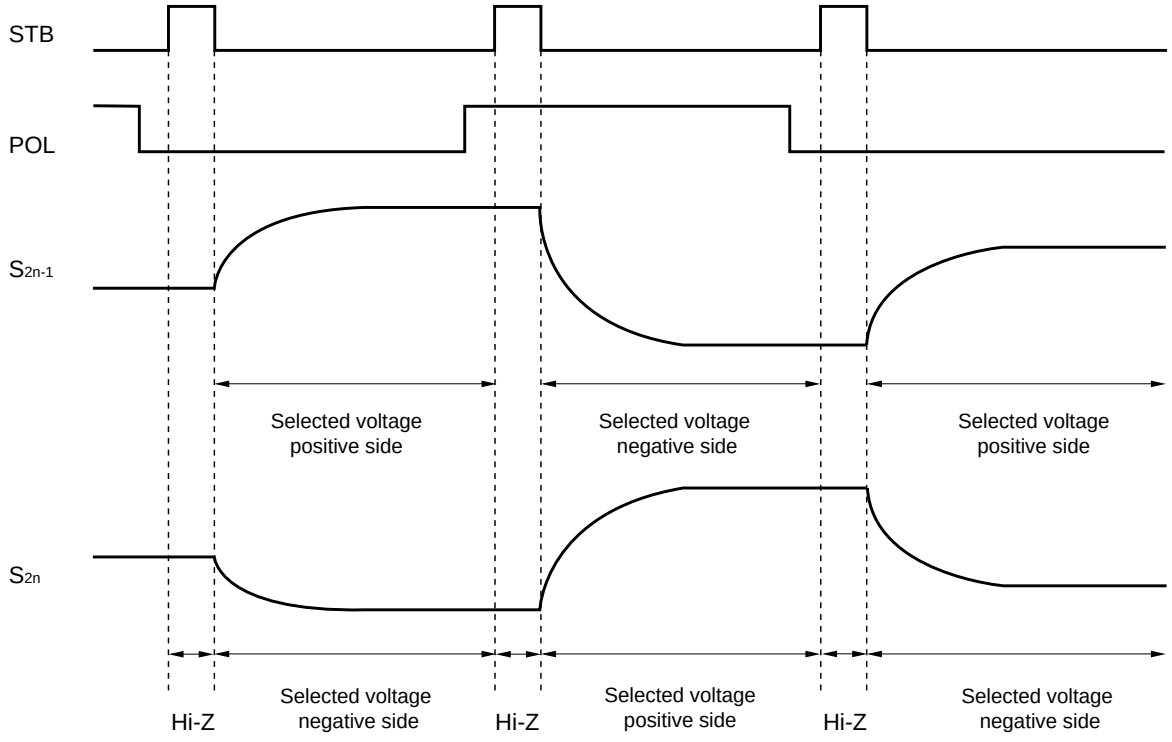
Output	S_1	S_2	S_3	S_4	···	S_{479}	S_{480}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	···	D_{40} to D_{45}	D_{50} to D_{55}

POL	S_{2n-1} Note	S_{2n} Note
L	V_0 to V_6	V_7 to V_{13}
H	V_7 to V_{13}	V_0 to V_6

Note S_{2n-1} (Odd output), S_{2n} (Even output)

★ 7. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.



8. CURRENT CONSUMPTION REDUCTION FUNCTION

The μPD16718 has a low power control function (LPC) which can switch the bias current of the output amplifier between two levels.

<Low power control function (LPC)>

The bias current of the output amplifier can be switched between two levels using this pin.

LPC = H or open: low power mode

LPC = L: normal power mode

The V_{DD2} of static current consumption can be reduced to two thirds of that in normal mode, input a stable DC current (V_{DD1}/V_{SS1}) to this pin.

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.5 to +4.0	V
Driver Part Supply Voltage	V_{DD2}	–0.5 to +17.0	V
Logic Part Input Voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Input Voltage	V_{I2}	–0.5 to V_{DD2} + 0.5	V
Logic Part Output Voltage	V_{O1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Output Voltage	V_{O2}	–0.5 to V_{DD2} + 0.5	V
Operating Ambient Temperature	T_A	–10 to +75	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –10 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}		2.5	3.3	3.6	V
Driver Part Supply Voltage	V_{DD2}		10.0	11.5	12.5	V
High-Level Input Voltage	V_{IH}		0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}		0		0.3 V_{DD1}	V
γ-Corrected Voltage	V_0 to V_{13}		0.1		V_{DD2} – 0.1	V
Driver Part Output Voltage	V_O		0.1		V_{DD2} – 0.1	V
Clock Frequency	f_{CLK}	V_{DD1} = 2.5 V			57	MHz

Electrical Characteristics (T_A = –10 to +75°C, V_{DD1} = 2.5 to 3.6 V, V_{DD2} = 10.0 to 12.5 V, V_{SS1} = V_{SS2} = 0 V, LPC = L)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Leak Current	I_{IL}	Except Osel, LPC, R,/L			±1.0	μA
Pull-up Resistance Value	R_{PU}	LPC, R,/L	100	190	500	kΩ
Pull-downResistance Value	R_{PD}	Osel	25	50	150	kΩ
High-Level Output Voltage	V_{OH}	STHR (STHL), I_{OH} = 0 mA	V_{DD1} – 0.1			V
Low-Level Output Voltage	V_{OL}	STHR (STHL), I_{OL} = 0 mA			0.1	V
γ-Corrected Resistance	I_γ	V_{DD2} = 12.5 V, V_0 to V_6 = V_7 to V_{13} = 5.0 V	8.7	14.5	20.3	kΩ
Driver Output Current	I_{VOH}	Vx = 11.0 V, V_{OUT} = 10.5 V[Note]		–50	–20	μA
	I_{VOL}	Vx = 0.5 V, V_{OUT} = 1.0 V[Note]	20	55		μA
Output Voltage Deviation	ΔV_O	V_O = 1.2 V to V_{DD2} – 1.2 V		±10	±20	mV
		V_O = 1.0 to 1.2 V V_O = V_{DD2} – 1.2 V to V_{DD2} – 1.0 V		±13	±25	mV
Output swing difference deviation	ΔV_{P-P1}	V_O = 5.4 V to V_{DD2} – 5.4 V		±5	±10	mV
	ΔV_{P-P2}	V_O = 1.9 to 5.4 V V_O = V_{DD2} – 5.4 V to V_{DD2} – 1.9 V		±8	±15	mV
	ΔV_{P-P3}	V_O = 1.0 to 1.9 V V_O = V_{DD2} – 1.0 V to V_{DD2} – 1.9 V		±15	±20	mV
Logic Part Dynamic Current Consumption	I_{DD1}	V_{DD1} = 3.3 V		0.6	11	mA
Driver Part Dynamic Current Consumption	I_{DD2}	V_{DD2} = 11.5 V, with no load, LPC = L		5.4	10	mA

Note V_X refers to the output voltage of analog output pins S_1 to S_{480}.

V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{480}.

Cautions 1. f_{STB} = 50 kHz, f_{CLK} = 40 MHz.

2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.

3. Refers to the current consumption per driver when cascades are connected under the assumption of UXGA single-sided mounting (10 units).

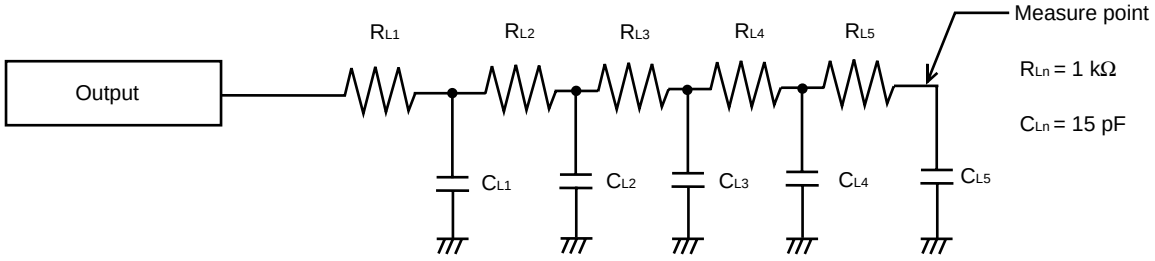
Electrical Characteristics (T_A = –10 to +75°C, V_{DD1} = 2.5 to 3.6 V, V_{DD2} = 10.0 to 12.5 V, V_{SS1} = V_{SS2} = 0 V, LPC = L)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 15 pF			15	ns
	t_{PKL1}				15	ns
Driver Output Delay Time	t_{PLH2} Note1	C_L = 75 pF, R_L = 5 kΩ		3.8	6	μs
	t_{PLH3} Note2			6.7	10	μs
	t_{PHL2} Note1			3.8	6	μs
	t_{PHL3} Note2			6.1	10	μs
Input Capacitance	C_{I1}	STHR (STHL) excluded, T_A = 25°C			10	pF
	C_{I2}	STHR (STHL),T_A = 25°C			15	pF

Notes 1. t_{PLH2}/t_{PHL2} are specified as the time it takes to reach the target voltage ±10% (condition: V_O = 0.1 to 12.4 V).

2. t_{PLH3}/t_{PHL3} are specified as the time it takes to reach the target voltage ±2% (condition: V_O = 0.1 to 12.4 V).

★ **<Measurement Condition>**



Timing Requirement (T_A = –10 to +75°C, V_{DD1} = 2.5 to 3.6 V, V_{SS1} = 0 V, $t_r = t_f$ = 5.0 ns)

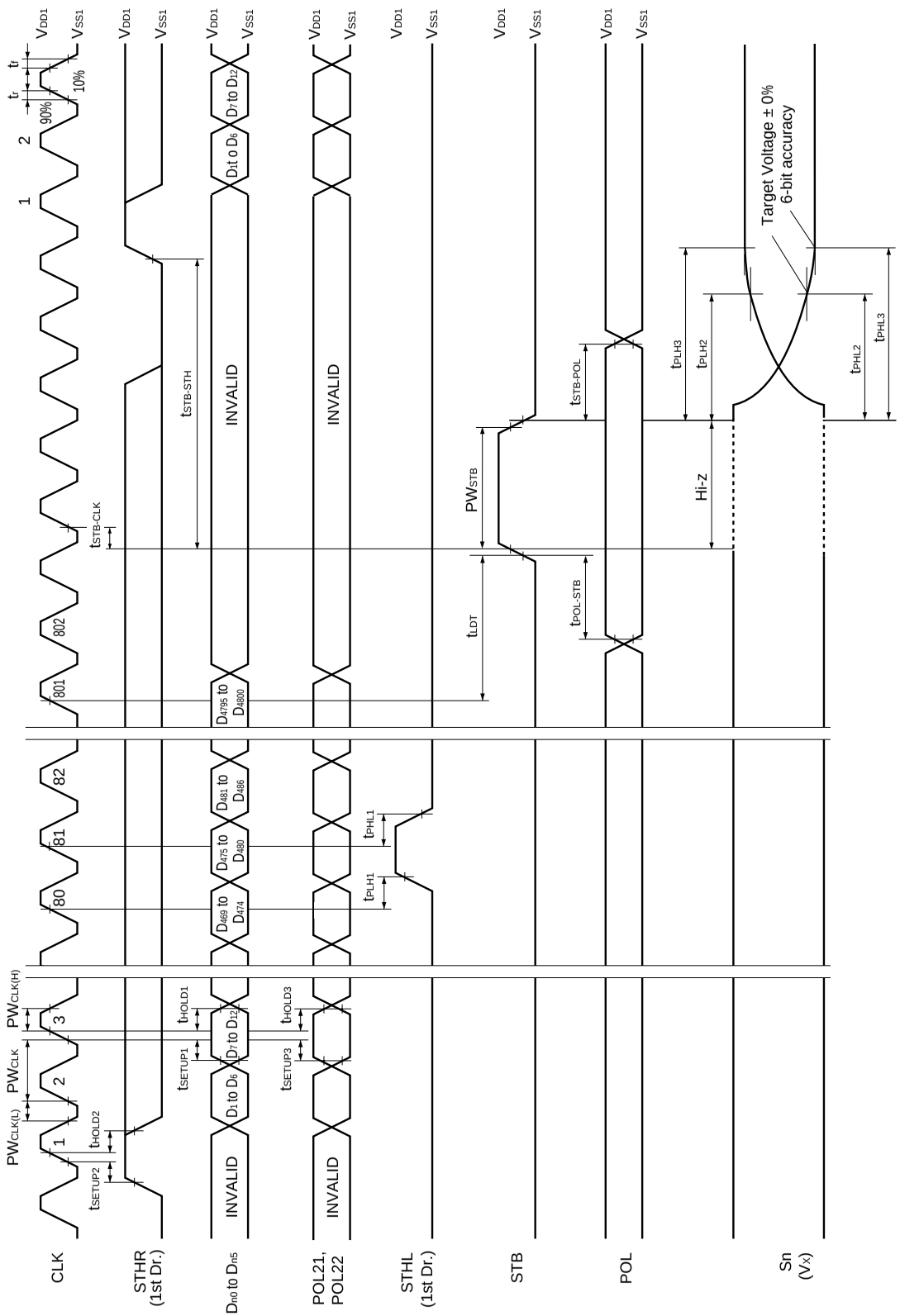
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		17			ns
Clock Pulse High Period	$PW_{CLK(H)}$		4			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		4			ns
Data Setup Time	t_{SETUP1}		3			ns
Data Hold Time	t_{HOLD1}		0			ns
Start Pulse Setup Time	t_{SETUP2}		3			ns
Start Pulse Hold Time	t_{HOLD2}		0			ns
POL21, POL22 Setup Time	t_{SETUP3}		3			ns
POL21, POL22 Hold Time	t_{HOLD3}		0			ns
STB Pulse Width	PW_{STB}		2			CLK
Last Data Timing	t_{LDT}		2			CLK
STB-CLK Time	$t_{STB-CLK}$	STB ↑ → CLK ↑	7			ns
Time between STB and Start Pulse	$t_{STB-STH}$	STB ↑ → STHR (STHL) ↑	2			CLK
POL-STB Time	$t_{POL-STB}$	POL ↑ or ↓ → STB ↑	–5			ns
STB-POL Time	$t_{STB-POL}$	STB ↓ → POL ↓ or ↑	6			ns

Remark Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

Phase-out/Discontinued

Switching Characteristics Waveform

Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.



10. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μPD16718.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

μPD16718N-xxx: TCP (TAB package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C: heating for 2 to 3 seconds: pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm^2 : time 3 to 5 seconds. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm^2 : time 30 to 40 seconds. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability / Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)