User's Manual

μPD720210

User's Manual: Hardware

ASSP (Four-port USB 3.0 Hub Controller)

Renesas Electronics
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Rev.2.00 May 2014

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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

PREFACE

Readers

This manual is intended for engineers who need to be familiar with the capability of the μPD720210 in order to develop application systems based on it.

Purpose

The purpose of this manual is to help users understand the hardware capabilities (listed below) of the μPD720210.

Configuration

This manual consists of the following chapters:

- Overview
- Pin function
- External ROM settings
- USB descriptor information
- Pin strapping
- Functions description
- Peripheral component connection

Guidance

Readers of this manual should already have a general knowledge of electronics, logic circuits, and microcomputers.

Notation

This manual uses the following conventions:

Data bit significance:	High-order bits on the left side; low-order bits on the right side
Active low:	XXXXB (Pin and signal names are suffixed with B.)
Note:	Explanation of an indicated part of text
Caution:	Information requiring the user's special attention
Remark:	Supplementary information
Numerical value:	Binary ... xxxx or xxxxb Decimal ... xxxx Hexadecimal ... xxxxh

Related Document

Use this manual in combination with the following document.
The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- μPD720210 Data Sheet: R19DS0070E

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μPD720210

ASSP (Four-port USB 3.0 Hub Controller)

R19UH0093EJ0200
Rev.2.00
May 26, 2014

1. Overview

The μPD720210 is a USB 3.0 hub controller that complies with the Universal Serial Bus (USB) Specification Revision 3.0 and operates at up to 5 Gbps. The device incorporates Renesas' market proven design expertise in USB 3.0 interface technologies and market proven USB 2.0 hub core. The device is fully compatible with all prior versions of USB spec and 100 % compatible with Renesas' industry standard USB 3.0 host controller. It comes in a small 76-pin QFN package and integrates several commonly required external components, making it ideally suited for applications with limited PCB space. In addition, μPD720210 incorporates Renesas' low-power technologies and supports all mainstream battery charging specifications.

1.1 Features

- Compliant with Universal Serial Bus 3.0 Specification Revision 1.0, which is released by USB Implementers Forum, Inc.
  - Supports the following speed data rate. : Low-speed (1.5 Mbps) / Full-speed (12 Mbps) / High-speed (480 Mbps) / SuperSpeed (5 Gbps)
  - Supports USB 3.0 link power management (U0/U1/U2/U3)
  - Supports USB 2.0 link power management (LPM: L0/L1/L2/L3)
- Configurable downstream port count of 2, 3, or 4
- Supports all VBUS control options
  - Individual or global over-current detection
  - Individual or ganged power control
- Supports USB 3.0/2.0 Compound (non-removable) devices by I/O pin configuration
- Supports clock output (24/12 MHz) for Compound (non-removal) device on downstream ports
- Supports Energy Star and EuP specifications for low-power PC peripherals and monitors
- Single 5V Power Supply
  - On chip LDO for 3.3 V from 5 V input and Switching Regulator for 1.05 V from 5 V input
- System clock: 24 MHz Crystal or Oscillator
- Supports USB Battery Charging Specification Revision 1.2 and other portable devices
  - DCP mode of BC 1.2
  - CDP mode of BC 1.2
  - China Mobile Phone Chargers
  - EU Mobile Phone Chargers
  - Apple iOS devices
  - Other major portable devices
- Supports SPI ROM for optional firmware and parameter data
- Small Footprint
  - Small and low pin count package with simple pin assignment for PCB layout
  - Integration of many peripheral components
  - Direct routing of all USB signal traces to connector pins using one layer of the PCB
- Self/Bus-Powered modes can be set by pin strapping
- Integrated termination resistors for USB
- Provides SUSPEND status output
- Supports Port Indicator control (only Green color)

1.2 Applications

Standalone Hub, Monitor-Hub, Docking Station, Integrated Hub, etc.

1.3 Ordering Information

Part Number	Package	Operating Temperature	Remark
μPD720210K8-BAF-A	76-pin QFN (9 × 9)	0 to +70°C	Lead-free product

1.4 Block Diagram

Figure 1-1. μPD720210 Block Diagram

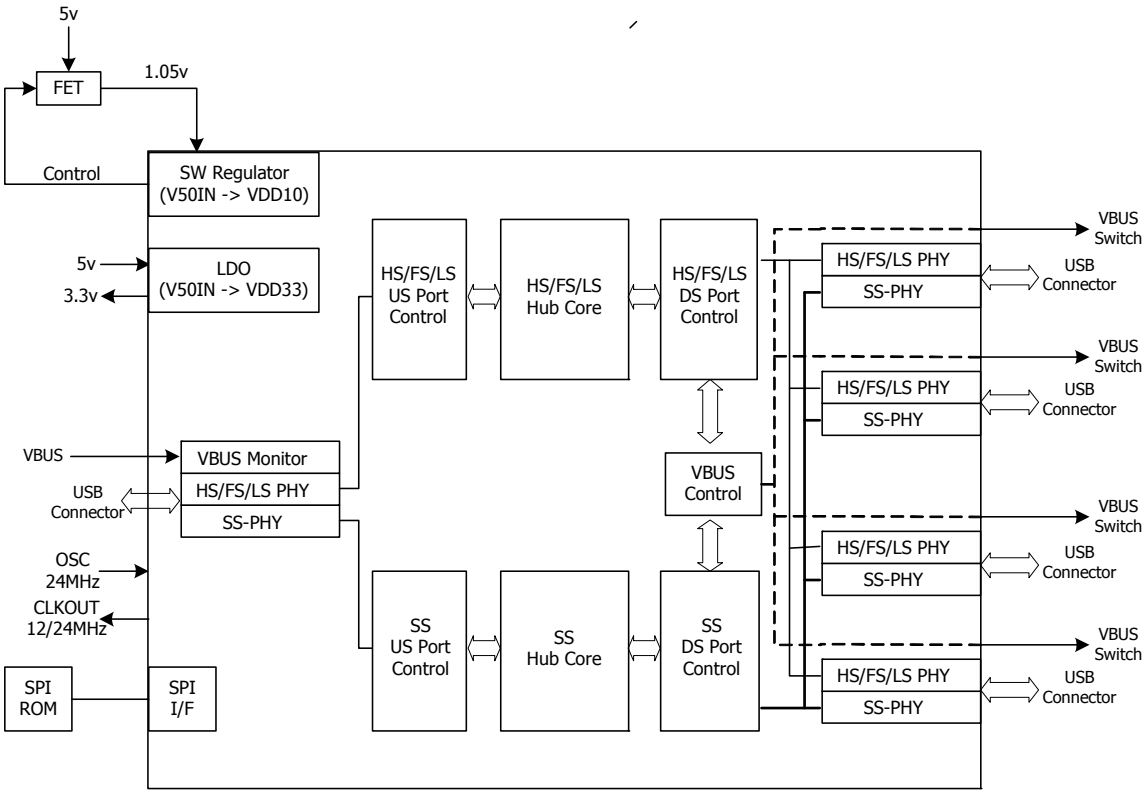


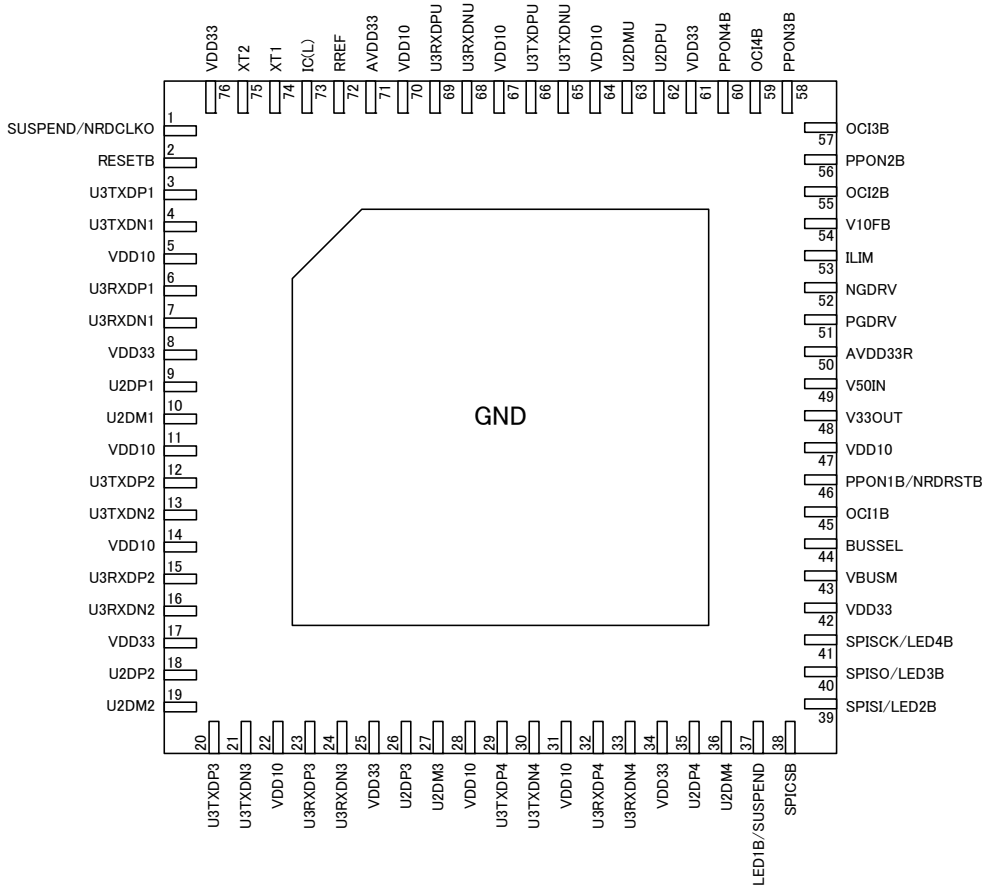
Table 1-1. Terminology

Block Name	Description
SS PHY	SuperSpeed transceiver
HS/FS/LS PHY	High-/Full-/Low-speed transceiver
VBUS Monitor	Monitors the VBUS voltage level of the upstream port.
SS US Port Control	Upstream port control logic for SuperSpeed
HS/FS/LS US Port Control	Upstream port control logic for High-/Full-/Low-speed
SS Hub Core	Central control logic for SS-Hub.
HS/FS/LS Hub Core	Central control logic for HS/FS/LS Hub.
SS DS Port Control	Downstream port control logic for SuperSpeed
HS/FS/LS DS Port Control	Downstream port control logic for HS/FS/LS
VBUS Control	Controls all the external port power switches
SPI Interface	Connected to external serial ROM which can hold the optional firmware and hub settings
SW-Regulator	Switching regulator control logic to output 1.05 V power from 5 V input, utilizing the external transistor
LDO	Integrated Low Drop Out regulator to output 3.3 V power from 5 V input.

1.5 Pin Configuration

- **76-pin QFN (9 × 9)**
  μPD720210K8-BAF-A

Figure 1-2. Pin Configuration of μPD720210 (Top View)



2. Pin Function

This section describes each pin function.
Strapping information in the tables shows how the pin can be used to configure the functional settings of this controller when the pin is pulled up/down, as detected at the end of chip reset. Refer to Chapter 5 for a complete description of all available pin strap settings. Also refer to Section 3.4 for a list of chip configuration settings available via external SPI ROM (optional).

2.1 Power Supply

Pin Name	Pin No.	I/O Type	Function
VDD10	5, 11, 14, 22, 28, 31, 47, 64, 67, 70	Power	1.05 V power supply for Core Logic
VDD33	8, 17, 25, 34, 42, 61, 76	Power	3.3 V power supply for IO buffer
AVDD33	71	Power	3.3 V power supply for Analog circuit
V50IN	49	Power	LDO Regulator 5 V Input Need to be connected to GND, when integrated LDO is not used.
V33OUT	48	Power	LDO 3.3 V Output 15 kΩ and 4.7 μF are required between this pin and GND, when integrated LDO is not used.
AVDD33R	50	Power	SW Regulator 3.3 V Input
NGDRV	52	-	SW Regulator Nch FET Control (Note)
PGDRV	51	-	SW Regulator Pch FET Control (Note)
ILIM	53	-	SW Regulator Current Sense
V10FB	54	-	SW Regulator Output Monitor

Note: See section 7.10 for important information about the selection of FET.

2.2 Analog Interface

Pin Name	Pin No.	I/O Type	Function
RREF	72	-	Reference Voltage Input for USB 2.0 RREF must be connected to a 1.6 kΩ resistor with a tolerance of +/- 1%. It is strongly recommended to use a single resistor for 1.6 kΩ, versus the combined resistance with multiple resistors to achieve this value and tolerance.

2.3 System Clock

Pin Name	Pin No.	I/O Type	Function
XT1	74	IN	External Oscillator Input Connect to 24 MHz crystal. This pin can be a 3.3 V Oscillator input as well.
XT2	75	OUT	External Oscillator Output Connect to 24 MHz crystal When using single-ended clock input to XT1, this pin should be left open.

2.4 System Interface Pins

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>I/O Type</th><th>Active Level</th><th>Function</th></tr>
<tr><td>SUSPEND/NRDCLKO</td><td>1</td><td>OUT</td><td>High/NA</td><td>SUSPEND Output or CLKOUT depending on pin strap setting of SPICSB and OCI1B.
SUSPEND is Suspend state output
1: in suspend state
0: not in suspend state
[Note]
SUSPEND/NRDCLKO output level is Hi-z till this pin function is configured as SUSPEND output or clock output for non-removable device
<table>
<tr><th>SPICSB</th><th>OCI1B</th><th>Pin Function</th></tr>
<tr><td rowspan="2">Low</td><td>Low</td><td>NRDCLKO</td></tr>
<tr><td>High</td><td>SUSPEND</td></tr>
<tr><td>High</td><td>X</td><td>Depends on Serial ROM setting</td></tr>
</table></td></tr>
<tr><td>VBUSM</td><td>43</td><td>IN</td><td>High</td><td>Upstream Port VBUS Monitor
Divide VBUS to 3.3V and connect to VBUSM</td></tr>
<tr><td>BUSSEL</td><td>44</td><td>IN</td><td>N/A</td><td>Power Mode Select Input
0: Bus-power setting
1: Self-power setting</td></tr>
<tr><td>LED1B/SUSPEND</td><td>37</td><td>OUT</td><td>Low</td><td>When the external ROM is not used (SPICSB is low), LED1B/SUSPEND is used as LED function for LED1B pin for port1 with the following pin strap settings. When the external ROM is used (SPICSB is high) and SUSPEND function is enabled in the ROM Writing Tool, LED1B/SUSPEND is used as SUSPEND function. If the SUSPEND function is not enabled, this pin is not functional (Hi-Z).
[Function]
LED1B is LED control output signal to indicate port enable. Note that μPD720210 supports only Green Color of port indicator.
0: Port is enabled
Hi-Z: Port is disabled
Suspend state is shown by the following pin level.
1: in suspend state
0: not in suspend state
<table>
<tr><th>SPICSB</th><th>SPISCK/ LED4B</th><th>SPISO/ LED3B</th><th>SPISI/ LED2B</th><th>LED1B/ SUSPEND</th><th>Pin Function</th></tr>
<tr><td>Low</td><td>High</td><td>High</td><td>High</td><td>High</td><td>LED1B</td></tr>
<tr><td>Low</td><td colspan="3">Others</td><td>High</td><td>Reserved (Hi-Z)</td></tr>
<tr><td>Low</td><td>X</td><td>X</td><td>X</td><td>Low</td><td>Reserved (Hi-Z)</td></tr>
<tr><td>High</td><td>X</td><td>X</td><td>X</td><td>X</td><td>SUSPEND or Hi-Z</td></tr>
</table>
[Pin strapping option]
- LED function (Refer to Chapter 5.1.2)
- Battery Charging mode (Refer to Chapter 5.1.6)
- Address length of external ROM (Refer to Chapter 5.1.8)</td></tr>
<tr><td>RESETB</td><td>2</td><td>IN</td><td>Low</td><td>Chip Reset Input</td></tr>
</table>

2.5 USB Port Control Pins

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>I/O Type</th><th>Active Level</th><th>Function</th></tr>
<tr><td>OCI1B</td><td>45</td><td>IN</td><td>Low</td><td>[Function]
Over Current Input
0: Over-current condition is detected.
1: Non over-current condition is detected.
[Pin strapping option]
<table><tr><td>OCI1B</td><td>Pin Function</td></tr><tr><td>High</td><td>Removable device setting and Over current input.</td></tr><tr><td>Low</td><td>Non-Removable setting.</td></tr></table>This pin is used to select non-removable setting.</td></tr>
<tr><td>OCI2B, OCI3B, OCI4B</td><td>55, 57, 59</td><td>IN</td><td>Low</td><td>[Function]
Over Current Input
0: Over-current condition is detected.
1: Non over-current condition is detected.
[Pin strapping option]
<table><tr><td>OCIXB</td><td>Pin Function</td></tr><tr><td>High</td><td>Removable device setting and Over Current Input.</td></tr><tr><td>Low</td><td>Non-Removable setting.</td></tr></table>This pin is used to select non-removable setting.</td></tr>
<tr><td>PPON1B/NRDRSTB</td><td>46</td><td>I/O</td><td>Low</td><td>[Function]
Port Power Control or NRDRSTB (Non-Removable Device Reset) depending on pin strap setting of this pin.
<table><tr><td>PPON1B/NRDRSTB</td><td>Pin Function</td></tr><tr><td>High</td><td>PPON1B</td></tr><tr><td>Low</td><td>NRDRSTB</td></tr></table>PPON1B is a Port Power Control signal
0: Power supply for VBUS is on.
1: Power supply for VBUS is off.
NRDRSTB is a reset signal for Non-Removable device.</td></tr>
<tr><td>PPON2B</td><td>56</td><td>I/O</td><td>Low</td><td>[Function]
This pin is a Port Power Control signal.
0: Power supply for VBUS is on.
1: Power supply for VBUS is off.
[Pin strapping option]
This pin is used for pin strapping option:
Gang/Individual Power Control of all ports.
<table><tr><td>PPON2B</td><td>Gang/Individual Mode</td></tr><tr><td>High</td><td>Individual</td></tr><tr><td>Low</td><td>Gang</td></tr></table></td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>I/O Type</th><th>Active Level</th><th>Function</th></tr>
<tr><td>PPON3B, PPON4B</td><td>58, 60</td><td>I/O</td><td>Low</td><td>[Function]
These pins are a Port Power Control signal.
0: Power supply for VBUS is on.
1: Power supply for VBUS is off.
[Pin strapping option]
These pins are used for pin strapping options to select Number of ports.
<table>
<tr><th>PPON4B</th><th>PPON3B</th><th>Number of ports</th></tr>
<tr><td>Low</td><td>Low</td><td>2 ports setting
Port 3 & 4 are not used.</td></tr>
<tr><td>Low</td><td>High</td><td>3 ports setting
Port 4 is not used</td></tr>
<tr><td>High</td><td>Low</td><td>Prohibit setting</td></tr>
<tr><td>High</td><td>High</td><td>All ports are used</td></tr>
</table>
</td></tr>
</table>

2.6 USB Data Pins

Pin Name	Pin No.	I/O Type	Function
U3TXDN1, U3TXDN2, U3TXDN3, U3TXDN4	4, 13, 21, 30	OUT	USB 3.0 Downstream Transmit data D- signal for SuperSpeed
U3TXDNU	65	OUT	USB 3.0 Upstream Transmit data D- signal for SuperSpeed
U3TXDP1, U3TXDP2, U3TXDP3, U3TXDP4	3, 12, 20, 29	OUT	USB 3.0 Downstream Transmit data D+ signal for SuperSpeed
U3TXDPU	66	OUT	USB 3.0 Upstream Transmit data D+ signal for SuperSpeed
U3RXDN1, U3RXDN2, U3RXDN3, U3RXDN4	7, 16, 24, 33	IN	USB 3.0 Downstream Receive data D- signal for SuperSpeed
U3RXDNU	68	IN	USB 3.0 Upstream Receive data D- signal for SuperSpeed
U3RXDP1, U3RXDP2, U3RXDP3, U3RXDP4	6, 15, 23, 32	IN	USB 3.0 Downstream Receive data D+ signal for SuperSpeed
U3RXDPU	69	IN	USB 3.0 Upstream Receive data D+ signal for SuperSpeed
U2DN1, U2DN2, U2DN3, U2DN4	10, 19, 27, 36	I/O	USB 2.0 Downstream D- signal for High-/Full-/Low-speed
U2DNU	63	I/O	USB 2.0 Upstream D- signal for High-/Full-/Low-speed
U2DP1, U2DP2, U2DP3, U2DP4	9, 18, 26, 35	I/O	USB 2.0 Downstream D+ signal for High-/Full-/Low-speed
U2DPU	62	I/O	USB 2.0 Upstream D+ signal for High-/Full-/Low-speed

2.7 SPI Interface

Pin Name	Pin No.	I/O Type	Active Level	Function
SPISCK/LED4B	41	I/O	N/A	[Function] External serial ROM Clock Output or LED output, depending on pin strap setting. [Pin strapping option] This pin is used for pin strapping option to select the below functions. - LED function (Refer to Chapter 5.1.2) - Battery Charging mode (Refer to Chapter 5.1.6)
SPICSB	38	I/O	Low	[Function] External serial ROM Chip Select [Pin strapping option] This pin is used for pin strap option to select the below functions. - External SPI ROM (Refer to Chapter 5.1.1) - LED function (Refer to Chapter 5.1.2) - Address length of external ROM (Refer to Chapter 5.1.8)
SPISO/LED3B	40	I/O	N/A	[Function] External serial ROM Data Input (to be connected to Serial Data Output pin of the external ROM) or LED output, depending on pin strap setting. [Pin strapping option] This pin is used for pin strap option to select the below functions. - LED function (Refer to Chapter 5.1.2) - Battery Charging mode (Refer to Chapter 5.1.6) - Address length of external ROM (Refer to Chapter 5.1.8)
SPISI/LED2B	39	I/O	N/A	[Function] External serial ROM Data Output (to be connected to Serial Data input pin of the external ROM) or LED output, depending on pin strap setting. [Pin strapping option] This pin is used for pin strap option to select the below functions. - LED function (Refer to Chapter 5.1.2) - Battery Charging mode (Refer to Chapter 5.1.6) - Address length of external ROM (Refer to Chapter 5.1.8)

2.8 Test Pin

Pin Name	Pin No.	I/O Type	Active Level	Function
IC(L)	73	IN	High	Test Pin to be connected to GND

3. External ROM Settings

3.1 Overview

μPD720210 can connect the external SPI ROM by option.
Using the external SPI ROM has the following advantages.

- PID/VID can be set as needed by the μPD720210 ROM Writing Tool for Windows (W210ROMTOOL.exe). Otherwise the PID and VID are fixed (default) values.
- Some functions have more features than pin strapping. These features are can be set by the μPD720210 ROM Writing Tool for Windows (W210ROMTOOL.exe).
- The internal firmware can be updated.

If not using the external SPI ROM, the functions of μPD720210 are determined by pin strapping.
The configuration parameters cannot be changed.
Refer to Chapter 3.4 for the default values of configuration parameters.

3.2 Supported ROMs

Table 3-1 below shows the External ROM Information & Parameter which μPD720210 supports. To access the External ROM, the software must set the ROM parameter before accessing the External ROM.

Table 3-1. External SPI ROM Information

Vendor	Product Name
SPI EEPROM	
RENESAS	R1EX25064ASA00A
RENESAS	R1EX25064ATA00A
SPI Serial Flash ROM	
Macronix	MX25L512E
Winbond	W25X05CL
Numonyx	M25P05-P
Chingis	Pm25LD512C2
Adesto Technologies	AT25DF512C, AT25F512B
EON	EN25F05
AMIC	A25L512

3.3 ROM Contents

The external ROM should contain the firmware and the parameter values. The μPD720210 ROM Writing Tool for Windows (W210ROMTOOL.exe) provided by Renesas can set up the external ROM contents correctly reflecting the operator's choice

3.4 Configurable Items

The following configurable Items can be set by the μPD720210 ROM Writing Tool for Windows (W210ROMTOOL.exe). Default value is the initial value of μPD720210.

Category	Item Name	Description	Default Value
Device Descriptor	<USB 3.0>		
	Vendor ID	Vendor ID (Note 1)	045Bh
	Product ID	USB 3.0 Hub Product ID (Note 1)	0210h
	bcdDevice	USB 3.0 Hub Device version (Note 1)	0100h
	<USB 2.0>		
	Product ID	USB 2.0 Hub Product ID (Note 1)	0209h
Hub Descriptor	Number of ports	Number of downstream facing ports (Note 2)	011b (4 ports)
	Gang/Individual Power	Gang or Individual VBUS switching mode on downstream (Note 2)	1 (Individual)
	PwrOn2PwrGood time	Power on to PowerGood Time (Value x 100 ms)	1 (100ms) (Power Control)
	Device Removable Port 1	Port 1 Device Removable setting (Note 2)	1 (Removable)
	Device Removable Port 2	Port 2 Device Removable setting (Note 2)	1 (Removable)
	Device Removable Port 3	Port 3 Device Removable setting (Note 2)	1 (Removable)
	Device Removable Port 4	Port 4 Device Removable setting (Note 2)	1 (Removable)
BC Mode	BC Mode Port 1	Port 1 Battery Charging Mode	SDP only
	BC Mode Port 2	Port 2 Battery Charging Mode	SDP only
	BC Mode Port 3	Port 3 Battery Charging Mode	SDP only
	BC Mode Port 4	Port 4 Battery Charging Mode	SDP only
	PPOFF_MODE	Time delay before turning on VBUS when changing the BC mode (Note 1)	0b (400 ms)
Pin Usage Settings	SUSPEND/NRDCLKO Pin Usage	SUSPEND/NRDCLKO pin function (Suspend output, or CLKOUT) (Note 1)	0 (Suspend State)
	LED1B/SUSPEND Pin Usage	LED1B/SUSPEND pin function (None, or Suspend output) (note1)	1b (None)
Clock Output Function's Additional Settings	Output Clock Control	CLKOUT control (Controllable, or Unstoppable) (Note 1)	1 (Unstoppable)
	Output Clock Frequency	CLKOUT Frequency (12 MHz, or 24 MHz) (Note 1)	0 (24 MHz)
	Port1 Non-Removable-Device type	Non-Removable Device Type (Hub, or other) (Note 1)	0 (USB3Hub)
Other Settings	USB2.0 LPMENABLE	USB 2.0 LPM Enable (Note 1)	1 (Enabled)
	USB3.0 U2 Disable	USB 3.0 U2 line state disable (Note 1)	1 (Disabled)
	USB3.0 U1 Disable	USB 3.0 U1 line state disable (Note 1)	1 (Disabled)
	SSC ON/OFF	Select SSC mode	1 (SSC on)
	Low Power Mode during Suspend	Select Low Power Mode during Suspend	Disable

Note1: This setting is for the external ROM only. When external ROM is not used, default is used.
Note2: This setting MUST reflect (be the same as) the setting in Pin Strapping options.

3.5 Low Power Mode during Suspend

This mode can be reduce the power consumption of μPD720210 during Suspend (U3 State) where the μPD720210 is disabled from signaling a remote wakeup due to a connect or disconnect event.
By enabling this mode, the power consumption during Sleep state decreases in the Windows8 and Windows8.1 environments.
To use this mode, need to connect the external SPI ROM.
The parameter can be set by the μPD720210 ROM Writing Tool for Windows (W210ROMTOOL.exe).

4. USB Descriptor Information

4.1 SuperSpeed Descriptors

4.1.1 Device Descriptor

Table 4-1. Device Descriptor

Field Name	Size(Byte)	Value	Description
bLength	1	12h	Size of Descriptor (18 bytes)
bDescriptorType	1	01h	Descriptor type (DEVICE)
bcdUSB	2	0300h	USB Specification Release Number (3.00)
bDeviceClass	1	09h	Class Code (HUB CLASS)
bDeviceSubClass	1	00h	Sub Class Code (USB spec defined)
bDeviceProtocol	1	03h	Protocol Code (USB spec defined, for USB 3)
bMaxPacketSize0	1	09h	Endpoint 0 Max Packet Size (2^9 = 512 bytes)
idVendor	2	045Bh	Vendor ID (Renesas Electronics)(Note 1)
idProduct	2	0210h	Product ID (μPD720210 • USB 3)(Note 1)
bcdDevice	2	0100h	Device release number (“01.00”)(Note 1)
iManufacturer	1	00h	Index of string descriptor (No descriptor)
iProduct	1	00h	Index of string descriptor (No descriptor)
iSerialNumber	1	00h	Index of string descriptor (No descriptor)
bNumConfigurations	1	01h	Number of possible configuration (1)

Note 1: The value can be overridden by external ROM setting

4.1.2 BOS Descriptor

Table 4-2. BOS Descriptor

Field Name	Size(Byte)	Value	Description
bLength	1	05h	Size of Descriptor (5 bytes)
bDescriptorType	1	0Fh	Descriptor type (BOS)
wTotalLength	2	002Ah	Total descriptor length (42 bytes)
bNumDeviceCaps	1	03h	Number of device capability descriptor (3)

Table 4-3. USB 2.0 Extension

Field Name	Size(Byte)	Value	Description
bLength	1	07h	Size of Descriptor (7 bytes)
bDescriptorType	1	10h	Descriptor type (DEVICE CAPABILITY)
bDeviceCapabiltiyType	1	02h	Device Capability Type (USB 2.0 EXTENSION)
bmAttributes	4	0000_0002h	Supported device capability (Note 1) (LPM Enable=1)

Note 1: The Bit[1] value can be overridden by external ROM setting

Table 4-4. SuperSpeed Device Capabilities

Field Name	Size(Byte)	Value	Description
bLength	1	0Ah	Size of Descriptor (10 bytes)
bDescriptorType	1	10h	Descriptor type (DEVICE CAPABILITY)
bDeviceCapabiltiyType	1	03h	Device Capability Type (SUPERSPEED_USB)
bmAttributes	1	00h	Supported device capability (LTM = 0)
wSpeedsSupported	2	000Eh	Speeds Supported (FS = 1, HS = 1, SS = 1)
bFunctionalitySupport	1	01h	Lowest Speed (FS)
bU1DevExitLat	1	0Ah	U1 Device Exit Latency (Less Than 10 μs)
wU2DevExitLat	2	000Ah	U2 Device Exit Latency (Less Than 10 μs)

Table 4-5. Container ID

Field Name	Size(Byte)	Value	Description
bLength	1	14h	Size of Descriptor (20 bytes)
bDescriptorType	1	10h	Descriptor type (DEVICE CAPABILITY)
bDeviceCapabiltiyType	1	04h	Device Capability Type (CONTAINER_ID)
bReserved	1	00h	Reserved
ContainerID	16	0h	UUID (Note 1)

Note 1: The value can be overridden by External ROM setting

4.1.3 Configuration Descriptor

Table 4-6. Configuration Descriptor

Field Name	Size(Byte)	Value	Description
bLength	1	09h	Size of Descriptor (9 bytes)
bDescriptorType	1	02h	Descriptor type (CONFIGURATION)
wTotalLength	2	001Fh	Total descriptor length (31bytes)
bNumInterfaces	1	01h	Number of Interfaces supported (1)
bConfigurationValue	1	01h	Configuration value (1)
iConfiguration	1	00h	Index of string descriptor (No descriptor)
bmAttributes	1	E0h	Self-powered Remote Wakeup supported
bMaxPower	1	00h	0mA

Table 4-7. Interface Descriptor

Field Name	Size(Byte)	Value	Description
bLength	1	09h	Size of Descriptor (9 bytes)
bDescriptorType	1	04h	Descriptor type (INTERFACE)
bInterfaceNumber	1	00h	Number of this interface (0)
bAlternateSetting	1	00h	Alternate Setting (0)
bNumEndpoints	1	01h	Number of endpoints (1)
bInterfaceClass	1	09h	Class Code (HUB CLASS)
bInterfaceSubClass	1	00h	Subclass Code (USB spec defined)
bInterfaceProtocol	1	00h	Protocol Code (USB spec defined)
iInterface	1	00h	Index of string descriptor (No descriptor)

Table 4-8. Endpoint Descriptor

Field Name	Size(Byte)	Value	Description
bLength	1	07h	Size of Descriptor (7 bytes)
bDescriptorType	1	05h	Descriptor type (ENDPOINT)
bEndpointAddress	1	81h	Address of endpoint (IN, Endpoint1)
bmAttributes	1	13h	Endpoint Attributes (Notification Interrupt)
wMaxPacketSize	2	02h	Maximum packet size this endpoint (2)
bInterval	1	8h	Interval for data transfer (2^(8-1)*125 μs)

Table 4-9. Endpoint Companion Descriptor

Field Name	Size(Byte)	Value	Description
bLength	1	06h	Size of Descriptor (6 bytes)
bDescriptorType	1	30h	Descriptor type (SUPERSPEED_USB_ENDPOINT_COMPANION)
bMaxBurst	1	00h	Maximum number of packets in burst (0 = 1)
bmAttributes	1	00h	Endpoint Attributes (Reserved for Interrupt)
wBytesPerInterval	2	02h	Total number of bytes in service interval (2)

4.1.4 Hub Descriptor

Table 4-10. Hub Descriptor

Field Name	Size(Byte)	Value	Description
bLength	1	0Ch	Size of Descriptor (12 bytes)
bDescriptorType	1	2Ah	Descriptor type (HUB)
bNbrPorts	1	04h	Number of downstream facing ports (4 port) (Note 1)
wHubCharacteristics	2	09h	Hub Characteristics (Individual Power Switching, Not part of a compound device, Individual Over current protection)(Note 2)
bPwrOn2PwrGood	1	32h	Time from Power on to Power Good (100 ms) (Note 3)
bHubContrCurrent	1	32h	Maximum current of Hub Controller (aCurrentUnit(4mA)*32h = 200 mA)
bHubHdrDecLat	1	01h	Hub Packet Header Decode Latency (0.1 μs)
wHubDelay	2	012Ch	Average delay of forwarding packet (300 ns)
DeviceRemovable	2	0000h	Removable device attached (All 4 downstream ports are removable) (Note 4)

Note 1: The value can be overridden by ROM setting or Strap pin setting
Note 2: Bit[3], Bit[2], Bit[0] = The value can be overridden by ROM setting
Note 3: The value can be overridden by ROM setting or Strap pin setting (32h or 00h)
Note 4: Bit[4:1] = The value can be overridden by ROM setting or Strap pin setting

4.2 High Speed Standard Descriptor

4.2.1 Device Descriptor

Table 4-11. Device Descriptor

Field Name	Size	Value	Description
bLength	1	12h	Descriptor Length (18 bytes)
bDescriptorType	1	01h	Device
bcdUSB	2	0210h	USB 2.0 compliant, LPM support
bDeviceClass	1	09h	Hub Class
bDeviceSubClass	1	00h	USB Spec. define
bDeviceProtocol	1	01h	Single TT
bMaxPacketSize0	1	40h	Max 64 bytes
idVendor	2	045Bh	(Note 1)
idProduct	2	0209h	(Note 1)
bcdDevice	2	0100h	(Note 1)
iManufacturer	1	00h	No string
iProduct	1	00h	No string
iSerialNumber	1	00h	No string
bNumConfigurations	1	01h	Number of configurations

Note 1: The value can be overridden by ROM setting

4.2.2 BOS Descriptor

Table 4-12. BOS Descriptor

Field Name	Size	Value	Description
bLength	1	05h	Descriptor Length (5 bytes)
bDescriptorType	1	0Fh	BOS Descriptor Type
wTotalLength	2	002Ah	Descriptor Total Length(42 bytes)
bNumDeviceCaps	1	03h	Number of device capability

Table 4-13. USB 2.0 Extension

Field Name	Size	Value	Description
bLength	1	07h	Descriptor Length (7 bytes)
bDescriptorType	1	10h	DEVICE CAPABILITY Descriptor Type
bDevCapabilityType	1	02h	USB 2.0 Extension
bmAttributes	4	00000002h	Support LPM: LPM_EN=1 (Note 1)

Note 1: The Bit[1] value can be overridden by External ROM setting

Table 4-14. SuperSpeed USB

Field Name	Size	Value	Description
bLength	1	0Ah	Descriptor Length (10 bytes)
bDescriptorType	1	10h	DEVICE CAPABILITY Descriptor Type
bDevCapabilityType	1	03h	SuperSpeed USB
bmAttributes	1	00h	LTM Unsupported
wSpeedSupported	2	000Eh	Support FS, HS, SS
bFunctionalitySupport	1	01h	Full Speed
bU1DevExitLat	1	0Ah	U1 Device Exit Latency
wU2DevExitLat	2	000Ah	U2 Device Exit Latency

Table 4-15. Container ID

Field Name	Size	Value	Description
bLength	1	14h	Descriptor Length (20 bytes)
bDescriptorType	1	10h	DEVICE CAPABILITY Descriptor Type
bDevCapabilityType	1	04h	Container ID
bReserved	1	00h	Reserved
bmAttributes	16	UUID[127:0]	128-bit UUID (Note 1)

Note 1: The value can be generated and set by ROM Writing Tool

4.2.3 Device Qualifier Descriptor

Table 4-16. Device Qualifier Descriptor

Field Name	Size	Value	Description
bLength	1	0Ah	Descriptor Length (10 bytes)
bDescriptorType	1	06h	Device Qualifier
bcdUSB	2	0210h	USB 2.0 compliant, LPM support
bDeviceClass	1	09h	Hub Class
bDeviceSubClass	1	00h	USB Spec. define
bDeviceProtocol	1	00h	USB Spec. define
bMaxPacketSize0	1	40h	Max 64bytes
bNumConfigurations	1	01h	Number of configuration
bReserved	1	00h	Reserved

4.2.4 Configuration Descriptor

Table 4-17. Configuration Descriptor

Field Name	Size	Value	Description
bLength	1	09h	Descriptor Length (9 bytes)
bDescriptorType	1	02h	Configuration
wTotalLength	2	0019h	Descriptor Total Length(25 bytes)
bNumInterfaces	1	01h	1 interface
bConfigurationValue	1	01h	Configuration Value is 1
iConfiguration	1	00h	No String
bmAttributes	1	E0h	Self-powered Remote Wakeup supported
bMaxPower	1	00h	0mA

4.2.5 Interface Descriptor (combined with Configuration Descriptor)

Table 4-18. Interface Descriptor

Field Name	Size	Value	Description
bLength	1	09h	Descriptor Length (9 bytes)
bDescriptorType	1	04h	Interface
bInterfaceNumber	1	00h	
bAlternateSetting	1	00h	
bNumEndpoints	1	01h	1 Endpoint
bInterfaceClass	1	09h	
bInterfaceSubClass	1	00h	
bInterfaceProtocol	1	00h	
iInterface	1	00h	No String

4.2.6 Endpoint Descriptor (combined with Configuration Descriptor)

Table 4-19. Endpoint Descriptor

Field Name	Size	Value	Description
bLength	1	07h	Descriptor Length (7 bytes)
bDescriptorType	1	05h	Endpoint
bEndpointAddress	1	81h	EP1 IN
bmAttributes	1	03h	Interrupt
wMaxPacketSize	2	0001h	Max 1 byte data
bInterval	1	0Ch	

4.2.7 Other Speed Configuration Descriptor

Table 4-20. Other Speed Configuration Descriptor

Field Name	Size	Value	Description
bLength	1	09h	Descriptor Length (9 bytes)
bDescriptorType	1	07h	Other Speed Configuration
wTotalLength	2	0019h	Descriptor Total Length (25 bytes)
bNumInterfaces	1	01h	1 interface
bConfigurationValue	1	01h	Configuration Value is 1
iConfiguration	1	00h	No String
bmAttributes	1	E0h	Self-powered Remote Wakeup supported
bMaxPower	1	00h	0mA

4.2.8 Interface Descriptor (combined with Other Speed Configuration Descriptor)

Table 4-21. Interface Descriptor

Field Name	Size	Value	Description
bLength	1	09h	Descriptor Length (9 bytes)
bDescriptorType	1	04h	Interface
bInterfaceNumber	1	00h	
bAlternateSetting	1	00h	
bNumEndpoints	1	01h	1 Endpoint
bInterfaceClass	1	09h	
bInterfaceSubClass	1	00h	
bInterfaceProtocol	1	00h	
iInterface	1	00h	No String

4.2.9 Endpoint Descriptor (combined with Other Speed Configuration Descriptor)

Table 4-22. Endpoint Descriptor

Field Name	Size	Value	Description
bLength	1	07h	Descriptor Length (7 bytes)
bDescriptorType	1	05h	Endpoint
bEndpointAddress	1	81h	EP1 IN
bmAttributes	1	03h	Interrupt
wMaxPacketSize	2	0001h	Max 1 byte data
bInterval	1	FFh	

4.2.10 Class Specified Hub Class Descriptor

Table 4-23. Class Specified Hub Class Descriptor

Field Name	Size	Value	Description
bDescLength	1	09h	Descriptor Length(9 bytes)
bDescriptorType	1	29h	Hub Class
bNbrPorts	1	04h	4 downstream facing ports(Note 1)
wHubCHaracteristics	2	00A9h	
		01b(D1:D0)	Individual port power switching(Note 1)
		0b(D2)	Not compound device(Note 2)
		01b(D4:D3)	Individual overcurrent protection(Note 1)
		01b(D6:D5) 00b(D6:D5)	TT Think Time is 16 FS bit time(Note 3)
		1b(D7) 0b(D7)	Support Port Indicator
bPwrOn2PwrGood	1	32h 00h	100ms 0ms(Note 1)
bHubContrCurrent	1	64h	Hub Control Current
DeviceRemovable	1	00h	All downstream port is removable(Note 1)
PortPwrCtrlMask	1	FFh	

Note 1: The value can be overridden by ROM setting or Strap Pin setting
Note 2: When one or more available port(s) is non-removable, the value is set to 1b
Note 3: Bit[7:5] = 000b, when FS_ONLY_MODE = 1b

4.3 Full Speed Standard Descriptor

4.3.1 Device Descriptor

Table 4-24. Device Descriptor

Field Name	Size	Value	Description
bLength	1	12h	Descriptor Length (18 bytes)
bDescriptorType	1	01h	Device
bcdUSB	2	0210h	USB 2.0 compliant, LPM support
bDeviceClass	1	09h	Hub Class
bDeviceSubClass	1	00h	USB Spec. define
bDeviceProtocol	1	00h	USB Spec. define
bMaxPacketSize0	1	40h	Max 64bytes
idVendor	2	045Bh	(Note 1)
idProduct	2	0209h	(Note 1)
bcdDevice	2	0100h	(Note 1)
iManufacturer	1	00h	No string
iProduct	1	00h	No string
iSerialNumber	1	00h	No string
bNumConfigurations	1	01h	Number of configurations

Note 1: The value can be overridden by ROM setting

4.3.2 BOS Descriptor

Table 4-25. BOS Descriptor

Field Name	Size	Value	Description
bLength	1	05h	Descriptor Length (5 bytes)
bDescriptorType	1	0Fh	BOS Descriptor Type
wTotalLength	2	002Ah	Descriptor Total Length (42 bytes)
bNumDeviceCaps	1	03h	Number of device capabilities

4.3.2.1 USB 2.0 Extension

Table 4-26. USB 2.0 Extension

Field Name	Size	Value	Description
bLength	1	07h	Descriptor Length (7 bytes)
bDescriptorType	1	10h	DEVICE CAPABILITY Descriptor Type
bDevCapabilityType	1	02h	USB 2.0 Extension
bmAttributes	4	00000002h	Supported device capability (LPM_Enable=1) (Note.1)

Note 1: the Bit[1] value can be overridden by External ROM setting

4.3.2.2 SuperSpeed USB

Table 4-27. SuperSpeed USB

Field Name	Size	Value	Description
bLength	1	0Ah	Descriptor Length (10 bytes)
bDescriptorType	1	10h	DEVICE CAPABILITY Descriptor Type
bDevCapabilityType	1	03h	SuperSpeed USB
bmAttributes	1	00h	LTM Unsupported
wSpeedSupported	2	000Eh	Support FS, HS, SS
bFunctionalitySupport	1	01h	Full Speed
bU1DevExitLat	1	0Ah	U1 Device Exit Latency
wU2DevExitLat	2	000Ah	U2 Device Exit Latency

4.3.2.3 Container ID

Table 4-28. Container ID

Field Name	Size	Value	Description
bLength	1	14h	Descriptor Length (20 bytes)
bDescriptorType	1	10h	DEVICE CAPABILITY Descriptor Type
bDevCapabilityType	1	04h	Container ID
bReserved	1	00h	Reserved
bmAttributes	16	UUID[127:0]	128-bit UUID (Note 1)

Note 1: The value can be overridden by External ROM setting

4.3.3 Device Qualifier Descriptor

Table 4-29. Device Qualifier Descriptor

Field Name	Size	Value	Description
bLength	1	0Ah	Descriptor Length (10 bytes)
bDescriptorType	1	06h	Device Qualifier
bcdUSB	2	0210h	USB 2.0 compliant, LPM support
bDeviceClass	1	09h	Hub Class
bDeviceSubClass	1	00h	USB Spec. define
bDeviceProtocol	1	01h	Single TT
bMaxPacketSize0	1	40h	Max 64 bytes
bNumConfigurations	1	01h	Number of configurations
bReserved	1	00h	Reserved

4.3.4 Configuration Descriptor

Table 4-30. Configuration Descriptor

Field Name	Size	Value	Description
bLength	1	09h	Descriptor Length (9 bytes)
bDescriptorType	1	02h	Configuration
wTotalLength	2	0019h	Descriptor Total Length (25 bytes)
bNumInterfaces	1	01h	1 interface
bConfigurationValue	1	01h	Config Value is 1
iConfiguration	1	00h	No String
bmAttributes	1	0Eh	Self-powered Remote Wakeup supported
bMaxPower	1	00h	0mA

4.3.5 Interface Descriptor (combined with Configuration Descriptor)

Table 4-31. Interface Descriptor

Field Name	Size	Value	Description
bLength	1	09h	Descriptor Length (9 bytes)
bDescriptorType	1	04h	Interface
bInterfaceNumber	1	00h	
bAlternateSetting	1	00h	
bNumEndpoints	1	01h	1 Endpoint
bInterfaceClass	1	09h	
bInterfaceSubClass	1	00h	
bInterfaceProtocol	1	00h	
iInterface	1	00h	No String

4.3.6 Endpoint Descriptor (combined with Configuration Descriptor)

Table 4-32. Endpoint Descriptor

Field Name	Size	Value	Description
bLength	1	07h	Descriptor Length (7 bytes)
bDescriptorType	1	05h	Endpoint
bEndpointAddress	1	81h	EP1 IN
bmAttributes	1	03h	Interrupt
wMaxPacketSize	2	0001h	Max 1 byte data
bInterval	1	FFh	

4.3.7 Other Speed Configuration Descriptor

Table 4-33. Other Speed Configuration Descriptor

Field Name	Size	Value	Description
bLength	1	09h	Descriptor Length (9 bytes)
bDescriptorType	1	07h	Other Speed Configuration
wTotalLength	2	0019h	Descriptor Total Length(25 bytes)
bNumInterfaces	1	01h	1 interface
bConfigurationValue	1	01h	Configuration Value is 1
iConfiguration	1	00h	No String
bmAttributes	1	E0h	Self-powered Remote Wakeup supported
bMaxPower	1	00h	0mA

4.3.8 Interface Descriptor (combined with Other Speed Configuration Descriptor)

Table 4-34. Interface Descriptor

Field Name	Size	Value	Description
bLength	1	09h	Descriptor Length (9 bytes)
bDescriptorType	1	04h	Interface
bInterfaceNumber	1	00h	
bAlternateSetting	1	00h	
bNumEndpoints	1	01h	1 Endpoint
bInterfaceClass	1	09h	
bInterfaceSubClass	1	00h	
bInterfaceProtocol	1	00h	
iInterface	1	00h	No String

4.3.9 Endpoint Descriptor (combined with Other Speed Configuration Descriptor)

Table 4-35. Endpoint Descriptor

Field Name	Size	Value	Description
bLength	1	07h	Descriptor Length (7 bytes)
bDescriptorType	1	05h	Endpoint
bEndpointAddress	1	81h	EP1 IN
bmAttributes	1	03h	Interrupt
wMaxPacketSize	2	0001h	Max 1 byte data
bInterval	1	0Ch	

5. Pin Strapping

5.1 Pin Strapping Settings

Some pins are used to set the configuration of the chip functions, by being pulled up or down at the end of chip reset (RESETB). The list of the configurations is shown Table 5-1.
The below pins are associated with the strapping setting. The details of each pin refer to Chapter 2.
SPICSB, SPISI/LED2B, SPISO/LED3B, SPISCK/LED4B
OCI1B, OCI2B, OCI3B, OCI4B, PPON1B/NRDRSTB, PPON2B, PPON3B, PPON4B
LED1B/SUSPEND, SUSPEND/NRDCLKO

Caution: The level of each pin is sampled just after reset, and used for the configuration as follows. Signal Name in the tables refers to the level of the pin latched at the end of reset. These pins should be either pulled up or pulled down for the expected function of the hub. In the following tables, pull-up is shown as "1", pull-down is "0". "X" represents "Don't Care".

Table 5-1. Pin Strapping Setting

No	Configuration	w/ the external SPI ROM	w/o the external SPI ROM
1	Using SPI ROM	Refer to 5.1.1	
2	LED function	Don't care (Note 4) (LED function is disabled)	Refer to 5.1.2
3	Number of ports	Refer to 5.1.3 (Note 1)	
4	Non-Removable ports setting	Refer to 5.1.4 (Note 1)	Refer to 5.1.4
5	Gang/Individual settings, and PowerOn2PowerGood setting	Refer to 5.1.5 (Note 1)	Refer to 5.1.5
6	Battery Charging setting	Refer to 5.1.6 (Note 2)	Refer to 5.1.6
7	GIO(SUSPEND/NRDCLKO) pin usage	Refer to 5.1.7 (Note 2)	Refer to 5.1.7
8	Address length of External ROM	Refer to 5.1.8 (Note 3)	Not applicable (Note 4)
9	PPON1B Output function	Refer to 5.1.9 (Note 3)	Refer to 5.1.9

(Note1) This parameter value needs to be set the same as the strap pin setting by the μPD720210 ROM Writing Tool for Windows (W210ROMTOOL.exe)
(Note2) This parameter value can be set arbitrarily by the μPD720210 ROM Writing Tool for Windows (W210ROMTOOL.exe) regardless of the strap pin setting.
(Note3) This parameter value cannot be set controlled by the μPD720210 ROM Writing Tool for Windows (W210ROMTOOL.exe) Strap pin setting is required.
(Note4) Need to connect pull-up or pull-down.

The details of each configuration are as below. The "No" column in each table below refers to the configuration case listed in Table 5-1.

5.1.1 External SPI ROM

This configuration sets whether the external SPI ROM is used or not.

[Pin Strapping Setting]

Table 5-2. External SPI ROM

No	Configuration	SPICSB	Definition
1	External SPI ROM	0	No SPI ROM
		1	SPI ROM attached

5.1.2 LED function

This configuration sets whether the LED function is used or not.

[Pin Strapping Setting]

Table 5-3. LED Function

No	Configuration	SPISCB	SPISCK/ LED4B	SPISO/ LED3B	SPISI/ LED2B	LED1B/ SUSPEND	Definition
2	LED function	0	1	1	1	1	LED function enable
		0	Others				LED function disable
		1	X	X	X	X	LED function disable

[Note]
LED function is not available in the following case.
1. Using the external ROM

2. Battery charging mode is set to CDP, CDP+DCP, CDP+FVO2 or CDP+Auto. (Refer to 5.1.6)

5.1.3 Number of ports

This configuration sets the Number of ports.

[Pin Strapping Setting]

Table 5-4. Number of Ports

No	Configuration	PPON4B	PPON3B	Definition
3	Number of ports	0	0	2 ports Port 4 and Port3 are not used.
		0	1	3 ports Port 4 is not used.
		1	0	Prohibited setting
		1	1	4 ports All ports are used.

5.1.4 Non-Removable Ports

This configuration sets the mode of Port 1 to Port 4. Port 1 to Port 4 can be set to Non-removable or removable.

[Pin Strapping Setting]

Table 5-5. Non-Removable Ports

No	Configuration	OCI4B	OCI3B	OCI2B	OCI1B	Definition
4	Non-Removable	0	X	X	X	Port4 Non-Removable OCI4B pin not used
		X	0	X	X	Port3 Non-Removable OCI3B pin not used
		X	X	0	X	Port2 Non-Removable OCI2B pin not used
		X	X	X	0	Port1 Non-Removable OCI1B pin not used (See also 5.1.7. NRDCLKO)

[Note]

1. When Port 1 is set to Non-Removable mode under Gang mode, the over current detection cannot be available.

5.1.5 Gang / Individual Port Power Control

This configuration sets whether power control is Gang mode or Individual mode.

[Pin Strapping Setting]

Table 5-6. Gang / Individual Port Power Control

No	Configuration	PPON2B	Definition
5	Gang/Individual control and PowerOn2PowerGood value	0	Gang PowerOn-to-PowerGood=0ms No VBUS on/off switch
		1	Individual PowerOn-to-PowerGood=100ms Use VBUS on/off switch

[Note]

1. Over current can only detect by OCI1B pin, when Gang mode is set.

5.1.6 Battery Charging mode

This configuration sets the Battery Charging mode.

[Pin Strapping Setting]

Table 5-7. Battery Charging Mode

No	Configuration	SPISCK/ LED4B	SPISO/ LED3B	SPISI/ LED2B	LED1B/ SUSPEND	Definition
6	Battery Charging Function This table is effective, when SPICSB =0 When SPICSB =1 All ports are initially SDP The mode can be changed by setting the parameter in the external SPI ROM.	1	1	1	1	SDP
				1	0	CDP (1)
				0	1	CDP (2)
				0	0	CDP (3)
		1	0	1	1	SDP
				1	0	CDP+DCP (1)
				0	1	CDP+DCP (2)
				0	0	CDP+DCP (3)
		0	1	1	1	SDP
				1	0	CDP+FVO2 (1)
				0	1	CDP+FVO2 (2)
				0	0	CDP+FVO2 (3)
		0	0	1	1	SDP
				1	0	CDP+Auto (1)
				0	1	CDP+Auto (2)
				0	0	CDP+Auto (3)

(1) All removable ports support Battery Charging.
(2) The removable port with the biggest number supports Battery Charging.
(3) The removable port with the smallest number supports Battery Charging.

[Note]

1. To use Battery Charging mode, set Individual mode. (Refer to 5.1.5)

2. When Battery charging mode (CDP etc) is used, LED function is not available.

5.1.7 GIO function

This configuration sets the GIO pin function. GIO pin output can be set to CLKOUT signal or SUSPEND signal. The CLKOUT function is intended for use by a non-removable device that needs a 24 MHz clock, without having to use a dedicated 24 MHz oscillator for the downstream device. Likewise, NRDRSTB (5.1.9) is also intended for such a device.

[Pin Strapping Setting]

Table 5-8. GIO Function

No	Configuration	SPICSB	OCI1B	Definition
7	GIO(SUSPEND/NRDCLKO) pin function	0	0	CLKOUT Output
		0	1	Suspend Output
		1	X	ROM Setting

[Note]

1. SUSPEND/NRDCLKO output level is Hi-Z till this pin function is configured SUSPEND output or clock output for non-removable device.
2. When use the CLKOUT output mode, SUSPEND/NRDCLKO pin needs to be set Pull-down.
3. When use the Suspend output mode, SUSPEND/NRDCLKO pin needs to be set Pull-up.
4. When External ROM is used and the clock output function is used, the frequency of the clock output can be set to 12MHz or 24MHz using the μPD720210 ROM Writing Tool for Windows.

5.1.8 Address length of External ROM

This configuration sets the address length of the external ROM, when the external SPI ROM is used.

[Pin Strapping Setting]

Table 5-9. Address Length of External ROM

No	Configuration	SPISCB	SPISO/ LED3B	SPISI/ LED2B	LED1B/ SUSPEND	Definition
8	Address length of Ext SPI ROM	0	X	X	X	Non external SPI ROM
		1	0	1	1	24bit (1)
		1	Others			16bit (2)

(1) Only SPI Serial Flash ROM is supported.
(2) Only SPI EEPROM is supported.

5.1.9 PPON1B Output function

This configuration sets the PPON1B pin function.

[Pin Strapping Setting]

Table 5-10. PPON1B Output Function

No	Configuration	PPON1B/ NRDRSTB	Definition
9	PPON1B/NRDRSTB Output	0	Port1 Non Removable Device Reset
		1	Port1 PPONB

6. Functions Description

6.1 Battery Charging

μPD720210 supports the USB Battery Charging Function. It is possible to permit devices to draw VBUS current in excess of the original USB2.0 specification for charging on the downstream port of μPD720210. This function complies with Battery Charging Specification Rev1.2.

- All of the μPD720210 downstream ports support SDP, CDP, DCP, and FVO1/2 mode. (Note 1)
- It is possible to select one Battery charging mode.
- It is possible to set the Battery charging mode on the one port with the biggest number among available ports.
- VBUS must be controlled by PPONxB in each port respectively.
- Auto mode can also charge other portable devices which do not support USB Battery Charging spec.

SDP: Standard Downstream Port (no Battery Charging support)
CDP: Charging Downstream Port (as defined in BC1.2)
DCP: Dedicated Charging Port (as defined in BC1.2)
Auto: This mode can detect DCP mode and FVO1 mode automatically.
FVO: Fixed Voltage Output. (D+ and D- are pulled up at the pre-defined voltage)
The difference of FVO1 and FVO2 is the level of fixed voltage output.

Note 1: FVO1 mode is supported when using the external SPI ROM.

6.1.1 Battery Charging Mode

[Without the external SPI ROM]

μPD720210 supports the Battery charging modes shown in Table 6-1.

In this case, modes are set by pin strapping.

Table 6-1. Battery Charging Mode

SPISCK/ LED4B	SPISO/ LED3B	SPISI/ LED2B	LED1B/ SUSPEND	Battery Charging port type		Support port
				During operation	No connection to host/ Suspend state	
1	1	1	1	SDP		(1)
		1	0	CDP		(1)
		0	1	CDP		(2)
		0	0	CDP		(3)
1	0	1	1	SDP		(1)
		1	0	CDP	DCP	(1)
		0	1	CDP	DCP	(2)
		0	0	CDP	DCP	(3)
0	1	1	1	SDP		(1)
		1	0	SDP	FVO2	(1)
		0	1	SDP	FVO2	(2)
		0	0	SDP	FVO2	(3)
0	0	1	1	SDP		(1)
		1	0	CDP	Auto	(1)
		0	1	CDP	Auto	(2)
		0	0	CDP	Auto	(3)

(1) All removable ports among variable ones support Battery Charging.
(2) The port with the biggest number among variable ones supports Battery Charging.
(3) The port with the smallest number among variable ones supports Battery Charging.

Note 1: To enable Battery charging function under S3/S4/S5, μPD720210 must remain powered under S3/S4/S5. When the power is supplied only in S0 and S3, the charging function is only available in those power states.

Note 2: When “wake on connect function” and “wake on disconnect function” are enabled, BC modes are not available, because these functions need to detect device attach or detach.

[With the external SPI ROM]

μPD720210 supports the Battery charging modes shown in Table 6-2.

In this case, modes can be set by the μPD720210 ROM Writing Tool for Windows (W210ROMTOOL.exe).

From Port 1 to Port 4 can be set individually regardless the pin strapping.

Table 6-2. Battery Charging Mode

Battery Charging port type	
During operation	No connection to host/ Suspend state
SDP (Battery Charging is disable.)	
CDP only	
CDP	DCP
CDP	FVO2
CDP	Auto
CDP	FVO1

Boot conditions of each BC mode are the following. The following conditions must all be met.

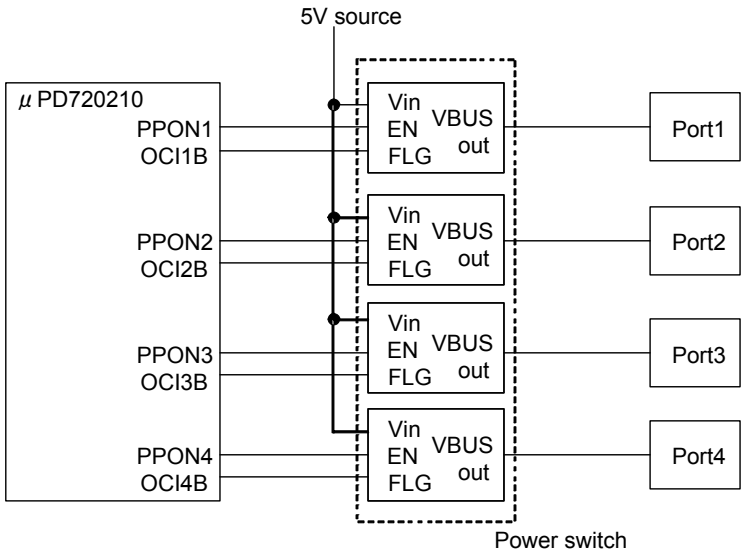
[CDP]
- Over current does not occur.
- Local Power Source of Get Hub Status is not set. (This means that Local power supply is good)

[DCP / FVO1 / FVO2]
- Over current does not occur.
- DEVICE_REMOTE_WAKEUP Feature of USB2.0 Hub is not set.
- Function Remote Wake of USB3.0 Hub is not set or Conn_RWEnable, Disconn_RWEnable and OC_RWEnable are not set.
- Local Power Source of Get Hub Status is not set. (This means that Local power supply is good)

6.1.2 HW configuration requirement

Some Battery charging functions change the port type in each device state. VBUS shall be cut off temporarily when the charging port is changed, as required by the Battery Charging Specification. Thus, VBUS shall be controlled by a power switch controlled by PPONxB for each port. And it is recommended to use power switches having the VBUS discharge function.

Figure 6-1. VBUS Control Configuration with Battery Charging Function

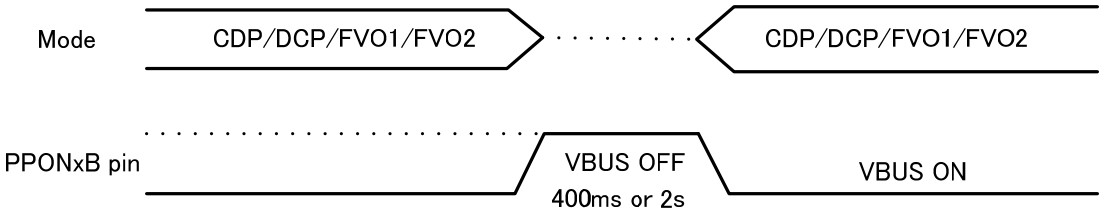


6.1.3 Downstream port VBUS control

VBUS of Downstream port set to OFF in the below case.

- When mode is changed from CDP to DCP, FVO1 or FVO2 mode.
- When BC mode is changed to another BC mode.

Figure 6-2. Downstream Port VBUS Control



6.2 Remote Wake Up function

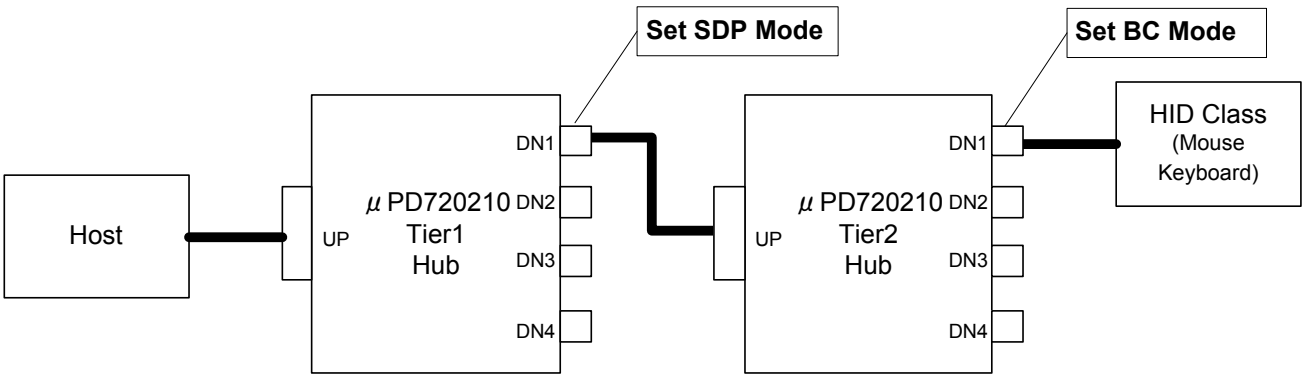
6.2.1 Remote Wake Up function

μPD720210 supports the Remote Wake Up function in all BC modes. When a Full-Speed device or Low-Speed device is connected to the downstream port and enumerated by the system, and then μPD720210 transitions to the suspend state, the PPONxB of a downstream port in BC mode is not asserted, to keep VBUS so that μPD720210 can accept the Remote Wake Up signal from the device. Once the device is removed during the suspend state, the BC mode of the port is changed as shown Table 6-2.

When μPD720210 is used as Tier 1 Hub such as in Figure 6-3, a downstream port to which a Tier 2 hub is connected should be set to SDP mode to enable Remote Wake Up function.

Note: Remote Wake Up function is not available when a downstream port to which a Tier 2 hub is connected is in BC mode.

Figure 6-3. Remote Wake Up Function



6.3 Clock Output Function

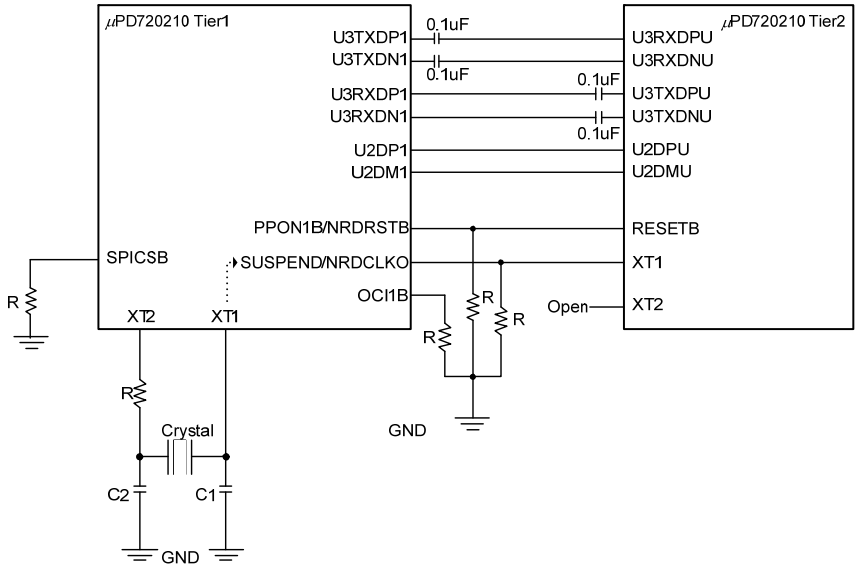
μPD720210 can provide the 24MHz or 12MHz reference clock and reset signal to a non-removable device. This section describes the clock output function for the non-removable device connected to the downstream port1 (Port1) of the μPD720210.

6.3.1 Clock Output Usage

SUSPEND/NRDCLKO pin can output a reference clock for a non-removable device connected to Port 1 by setting the pin strapping or the External ROM. Refer to section 5.1.4 and section 5.1.7 for the pin strapping setting and section 6.3.3 for the External ROM settings. Note that when this function is used, this pin needs a pull-down resistor.
Also PPON1B/NRDRSTB pin can output a reset signal to the non-removable device. Refer to section 5.1.9. Note that when this function is used, the pin needs a pull-down resistor.
Figure 6-4 shows the cascade connection of μPD720210 on the same board. With this configuration, a crystal circuit and a reset circuit for Tier2 are removed. The clock output timing of SUSPNED/NRDCLKO and the reset timing of PPON1B/NRDRSTB are shown in μPD720210 Data Sheet (R19DS0070E).

Note1: When the clock output function is used, SUSPEND/NRDCLKO pin cannot be used for the suspend signal function.
Note2: The clock output function must not be used for Port2 Non-Removable device.

Figure 6-4. Clock Output Usage (without External ROM)



6.3.2 Clock Output Function Settings

Table 6-3 shows the clock output function settings. These settings can be changed with the ROM Writing Tool for Windows. When the External ROM is not used, all of the settings are in default value except for the Pin Function, depending on the pin strapping setting (Refer to section 5.1.7.

Table 6-3. Clock Output Function Settings

Configuration item	Description	Default Setting
Pin Function	SUSPEND/NRDCLKO pin can be set to the suspend signal function or the clock output function.	SUSPEND
Clock Output Control	This setting controls the behavior of the Clock Output. Mode 1 : Unstoppable When this mode is set, the Clock Output does not stop by the timing when RESETB is asserted. Mode 2: Controllable When this mode is set, the Clock Output stops in suspend state. Refer to section 6.3.3 Clock Output Control for more detail.	Unstoppable
Output Clock Frequency	This setting controls the frequency of the Output Clock, 24MHz or 12MHz.	24MHz
Port 1 Non-Removable-Device Type	μPD720210 needs to know whether the non-Removable device is a USB3 Hub or not, to control the clock when the Output Clock Control is “Controllable”. When the Output Clock Control is unstoppable, this setting is not available.	USB3 Hub

6.3.3 Clock Output Function Control

When “Output Clock Control” is set to the controllable clock output, μPD720210 stops the clock output during the suspend state. Table 6-4 shows the stop condition of the clock output. Table 6-5 shows the start condition of the clock output after stopping the clock output.

Table 6-4. Clock Output Stop Condition

Non-Removable device	Condition for stopping the clock output
USB 3.0 Hub	Both USB 3.0 hub portion and USB 2.0 hub portion in the Non-removable device transitions to the suspend state.
Not USB3.0 Hub	Non-removable device transitions to the suspend state.

Table 6-5. Clock Output Start Condition

Non-Removable device	Condition for starting the clock output
USB 3.0 Hub	Satisfy any one of the following conditions (1) USB 3.0 hub portion in the Non-removable device transitions to not suspend state. (2) USB2.0 hub portion in the Non-removable device transitions to not suspend state. (3) USB2.0 Upstream port of the μPD720210 transitions to not suspend state.
USB 3.0 device (except USB 3.0 Hub)	Satisfy the following condition (1) USB 3.0 hub portion in the Non-removable device transitions to not suspend state.
USB 2.0 device	Satisfy any one of the following conditions (1) USB2.0 hub portion in the Non-removable device transitions to not suspend state. (2) USB2.0 Upstream port of the μPD720210 transitions to not suspend state.

7. Peripheral Component Connection

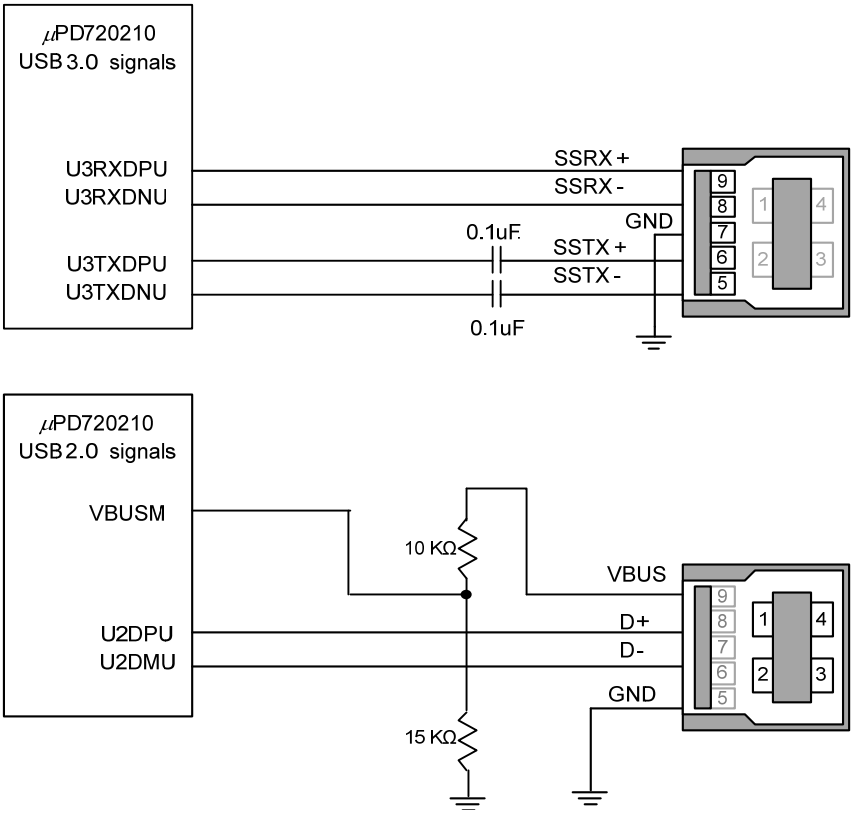
7.1 Unused Pin Connection

Table 7-1. Unused Pin Connection

Pin	Direction	Connection Method
U2DPx	I/O	Connect to GND, directly or through a resistor
U2DMx	I/O	Connect to GND, directly or through a resistor
U3TXDPx	O	Open
U3TXDNx	O	Open
U3RXDPx	I	Connect to GND, directly or through a resistor
U3RXDNx	I	Connect to GND, directly or through a resistor
SUSPEND/ NRDCLKO	O	Open
XT2	O	Open
IC(L)	I	Connect to GND, directly or through a resistor

7.2 USB Upstream Port Connection

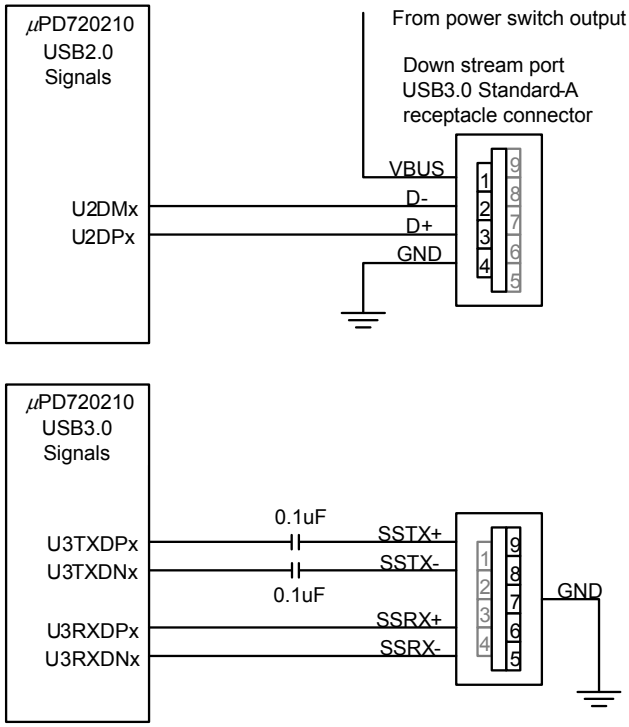
Figure 7-1. USB Upstream Port Connection



Remark: The maximum capacitance that can be placed on VBUS line should be less than 10 μF for the inrush current limiting requirement specified by USB 3.0 specification. Please see section 11.4.4.1 in USB 3.0 specification for details.

7.3 USB Downstream Port Connection

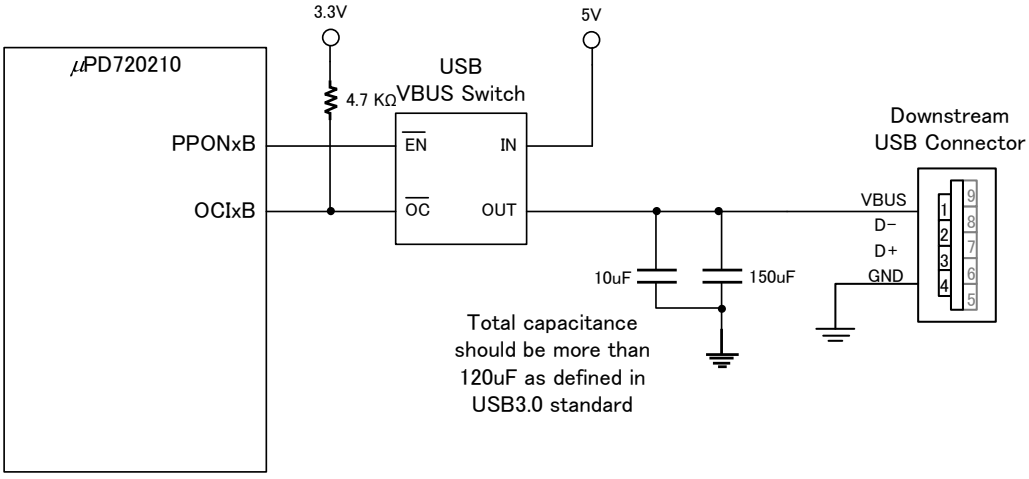
Figure 7-2. USB Downstream Port Connection



7.4 VBUS Power Switching Connection

7.4.1 USB Power Switch

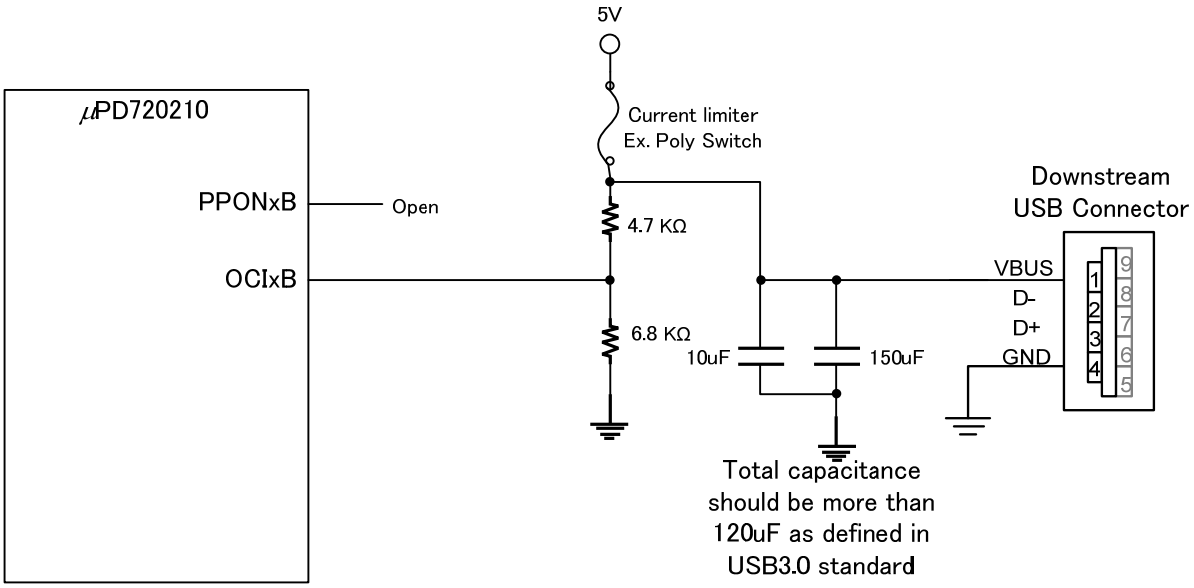
Figure 7-3. VBUS Switch Connection



Remark: The 3.3 V that pulls up OCIxB must be the same 3.3 V supplied to the μPD720210.
Remark: Total capacitance of VBUS should be no less than 120 μF. See 11.4.4.1 of USB 3.0 Specification.

7.4.2 Current Limiter

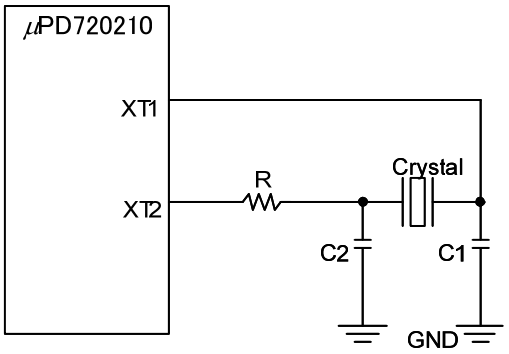
Figure 7-4. VBUS Current Limiter Connection



Remark: Total capacitance of VBUS should be no less than 120 μF. See 11.4.4.1 of USB 3.0 Specification.

7.5 Crystal Connection

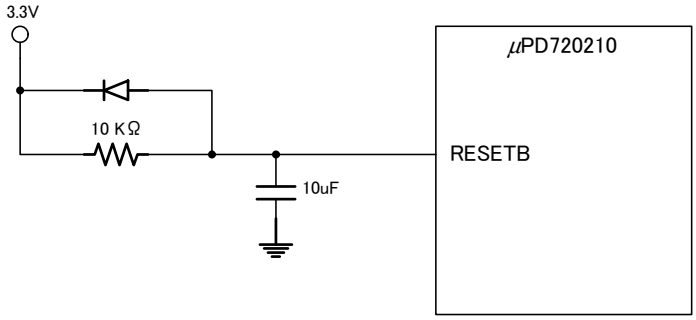
Figure 7-5. Crystal Connection



Remark: Clock shall be 24 MHz within 100 ppm. Moreover optimal crystal parameters and RC component values may be affected by the PCB layout.

7.6 RESET Connection

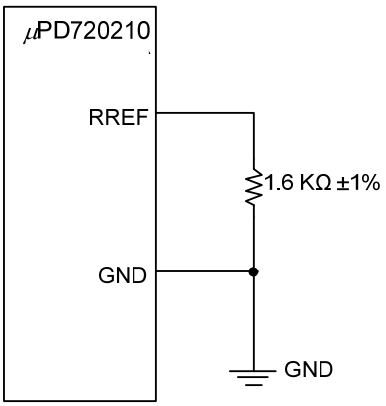
Figure 7-6. Reset Connection



Remark: The power-on-reset should be longer than 10 ms.

7.7 RREF Connection

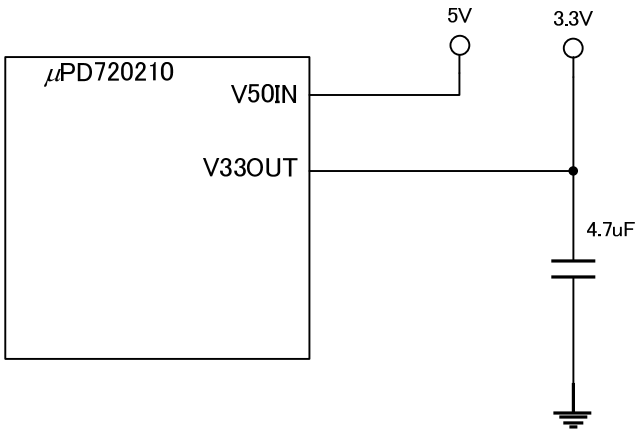
Figure 7-7. RREF Connection



Remark: The board layout should minimize the total path length from RREF through the resistor to GND and path length to GND. GND must be stable.
Due to analog sensitivity, 1.60 kΩ within ±1% must be used, and two or more resistors in series or parallel should not be used in place of a single 1.60 kΩ resistor.

7.8 Internal LDO (5V → 3.3V) Connection (in use)

Figure 7-8. Internal LDO Connection in use

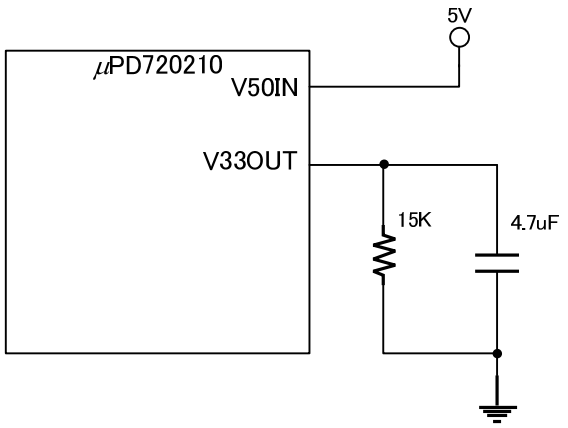


Remark: 4.7 μF capacitor is required, and the capacitor should be placed close to V33OUT pin.

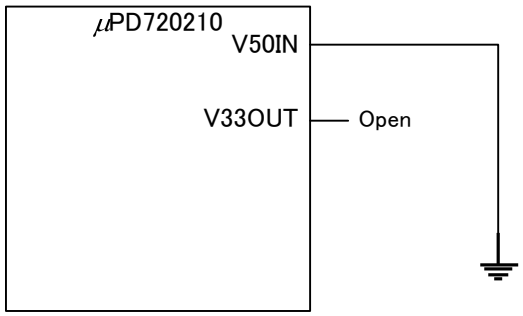
7.9 Internal LDO (5 V → 3.3 V) Connection (out of use)

Figure 7-9. Internal LDO Connection out of use

Case 1:
Internal Switching Regulator is used.

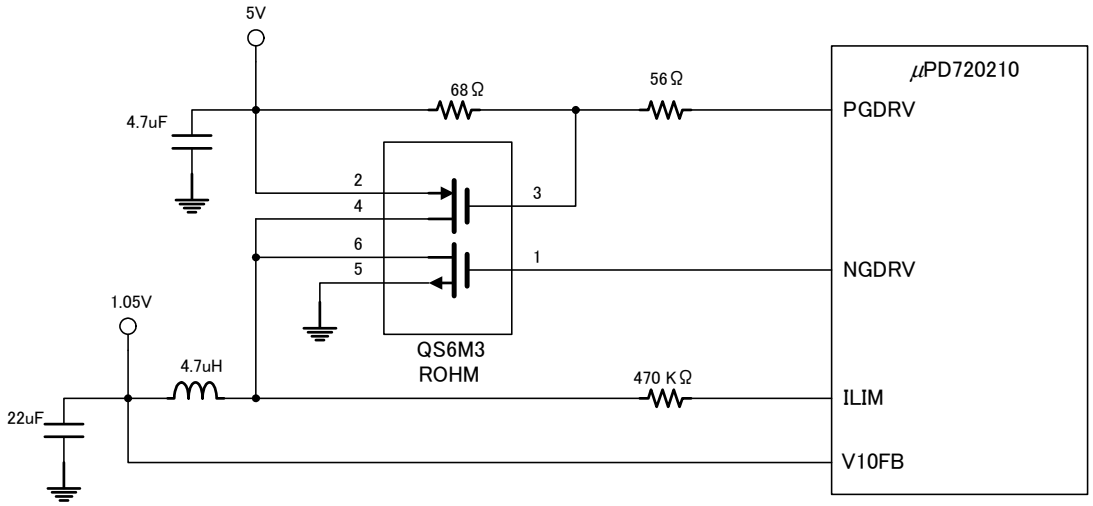


Case 2:
Internal Switching Regulator is NOT used.



7.10 Internal Switching Regulator (5 V → 1.05 V) Connection (in use)

Figure 7-10. Internal Switching Regulator Connection in use



It is necessary to use the correct Field Effect Transistor (FET) for the part of this switching regulator. The requirements for this FET are as follows.

1) Pch Vt: <2.5V
2) P-ch gate capacitance (Ciss): <270pF
3) Switching Period (On Time: Td+Tr, OffTime: Td+Tf) Nch<30ns, Pch<65ns
4) P-N One package, Single Die
5) Maximum Power Dissipation (Pd): >1.5W
6) Drain Current (Id): Continuous >1.5A
7) On Resistance (Rds): <170mOHM (Vgs=4.5V)

Remark: Recommended part for FET is QS6M3 (ROHM). Renesas is unaware of any other acceptable alternative device to the identified FET.

Important:

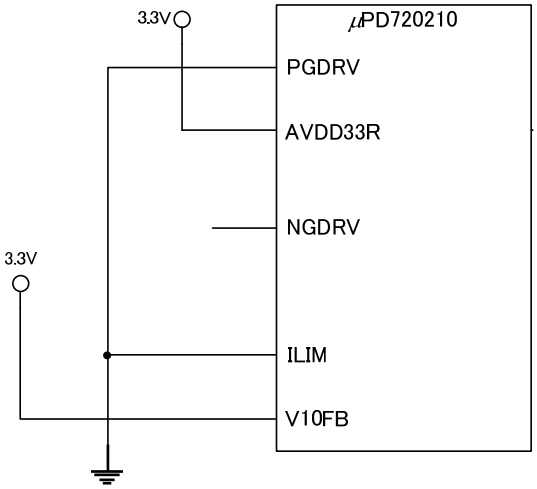
Please note that there is no known acceptable alternate device for the ROHM QS6M3 transistor noted in the μPD720210 User's Manual, as shown in the excerpt above. The reason is that this transistor carries the main load current for the 1.05V power used by the μPD720210 and may become excessively hot if an alternate transistor type is used. The heating can be severe enough to cause discoloration of the circuit board and possible damage to the end product and property unless the specified transistor is used as shown.

The only alternative is to use an external 1.05V switching regulator instead of the on-chip regulator, as shown in the μPD720210 User's Manual, Section 7.11.

"Notwithstanding anything to the contrary, Renesas shall not be responsible for any loss or damage resulting from Customer's use or incorporation of any components, including any FET, used in the Customer's design, system or end product. Customer is solely responsible for any and all decisions concerning its design, the components used therein, its assembly and functionality."

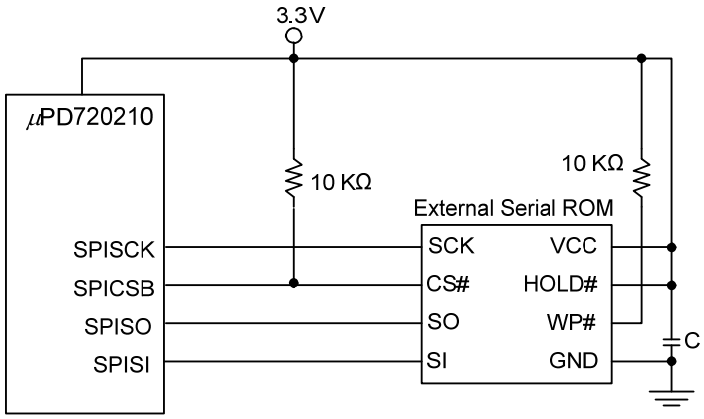
7.11 Internal Switching Regulator (5 V → 1.05 V) Connection (out of use)

Figure 7-11. Internal Switching Regulator Connection out of use



7.12 External Serial ROM Connection

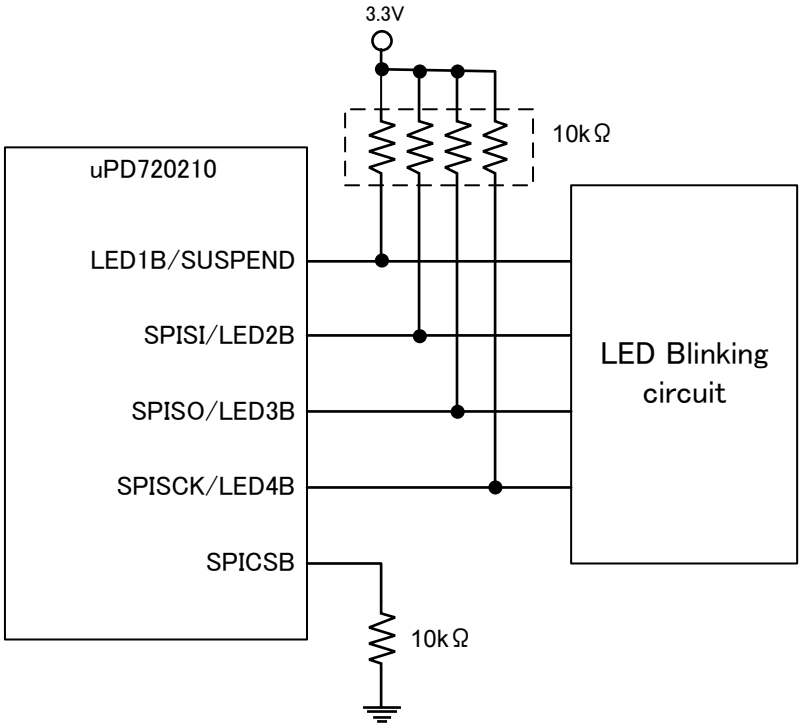
Figure 7-12. External Serial ROM Connection



Remark: Recommended Serial ROMs are refer to Chapter 3.2.
Remark: SPISCK signal has to be pulled up as in Figure 7-12, when the external ROM is used. Other pins are also used for some function settings. See Chapter 5. “Pin Strapping” for more details.

7.13 LED Control Connection

Figure 7-13. LED Control Connection



REVISION HISTORY	μPD720210 User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 26, 2012	-	Document promoted from Preliminary to v1.00. (Document No. R19UH0093E)
2.00	May. 26. 2014	-	Modified the overall chapter.

μPD720210 User's Manual: Hardware

Publication Date: Rev. 1.00 Sep 26, 2012
Rev. 2.00 May 26, 2014

Published by: Renesas Electronics Corporation

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

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