μPD8279
PROGRAMMABLE KEYBOARD/ DISPLAY INTERFACE

Description

The μPD8279 is a programmable keyboard and display input/output device providing the user with the ability to display data on alphanumeric segment displays or simple indicators. The display RAM can be programmed to function as a 16 x 8-bit or dual 16 x 4-bit memory and can be loaded or read by the host processor. The display can be loaded with right or left entry with an auto-increment of the display RAM address.

The keyboard interface provides a scanned signal to a 64 contact key matrix expandable to 128. General sensors or strobed keys may also be used. Keystrokes are stored in an 8 character FIFO and can be either 2 key lockout or N key rollover. Keyboard entries generate an interrupt to the processor.

Features

- ☐ Programmable by processor
- ☐ 32 hex or 16 alphanumeric displays
- ☐ 64 expandable to 128 keyboard
- ☐ Simultaneous keyboard and display
- ☐ 8 character keyboard—FIFO
- ☐ 2 key lockout or N key rollover
- ☐ Contact debounce
- ☐ Programmable scan timer
- ☐ Interrupt on key entry
- ☐ Single +5 V ±10% power supply
- ☐ Fully compatible with 8080A, 8085A, μPD780 (Z80®)

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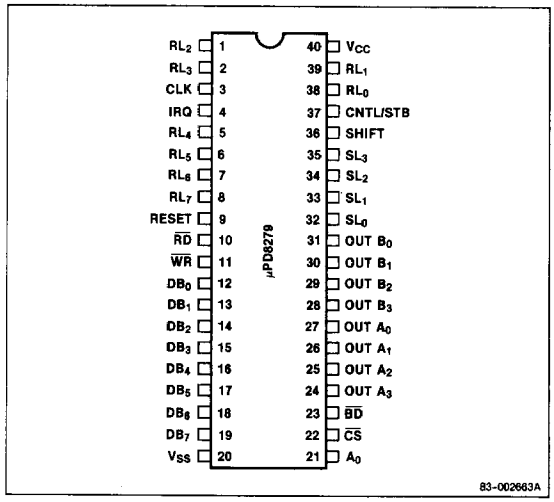
Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD8279C-2	40-pin plastic DIP	5 MHz
μPD8279C-5	40-pin plastic DIP	3 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1,2,5,6,7,8,38,39	RL_0-RL_7	Return lines
3	CLK	Clock input
4	IRQ	Interrupt request
9	RESET	Reset input
10	$\overline{RD}$	Read input
11	$\overline{WR}$	Write input
12-19	DB_0-DB_7	Data bus
20	V_{SS}	Ground reference
21	A_0	Buffer address
22	$\overline{CS}$	Chip select
23	$\overline{BD}$	Blank display output
24-27	OUT A_0-OUT A_3	Display A outputs
28-31	OUT B_0-OUT B_3	Display B outputs
32-35	SL_0-SL_3	Scan lines
36	Shift	Shift input
37	CNTL/STB	Control/strobe input
40	V_{CC}	+5 V input

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Pin Functions

RL_0-RL_7 (Return Lines)

Return line inputs which are connected to the scan lines through the keys or sensor switches. They have active internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the strobed input mode.

CLK (Clock)

Clock from system used to generate internal timing.

IRQ (Interrupt Request)

In a keyboard mode, the interrupt line is high when there is data in the FIFO/sensor RAM. The interrupt line goes low with each FIFO/sensor RAM read and returns high if there is still information in the RAM. In the sensor mode, the interrupt line goes high whenever a change in a sensor is detected.

RESET (Reset)

A high signal on this pin resets the μPD8279.

$\overline{RD}$ (Read Input)

Input read allows the data buffers to send data to the external bus.

$\overline{WR}$ (Write Input)

Input write allows the data buffers to receive data from the external bus.

DB_0-DB_7 (Data Bus)

Bidirectional data bus. All data and commands between the processor and the μPD8279 are transmitted on these lines.

OUT A_0-OUT A_3 (Display A Outputs)

Output port for the 16 x 4 display refresh registers. The output data is synchronized to the scan lines (SL_0-SL_3) for multiplexed digit displays. Ports A and B may be blanked independently and may also be considered as one 8-bit port.

OUT B_0-OUT B_3 (Display B Outputs)

Output port for the 16 x 4 display refresh registers. The output data is synchronized to the scan lines (SL_0-SL_3) for multiplexed digit displays. Ports A and B may be blanked independently and may also be considered as one 8-bit port.

SL_0-SL_3 (Scan Lines)

Scan lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).

A_0 (Buffer Address)

A high on this line indicates the signals in or out are interpreted as a command or status. A low indicates that they are data.

$\overline{CS}$ (Chip Select)

A low on this pin enables the interface functions to receive or transmit.

$\overline{BD}$ (Blank Display Output)

This output is used to blank the display during digit switching or by a display blanking command.

SHIFT (Shift)

The shift input status is stored along with the key position on key closure in the scanned keyboard modes. It has an active internal pullup to keep it high until a switch closure pulls it low.

CNTL/STB (Control/Strobe Input)

For keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into the FIFO in strobed input mode (rising edge). It has an active internal pullup to keep it high until a switch closure pulls it low.

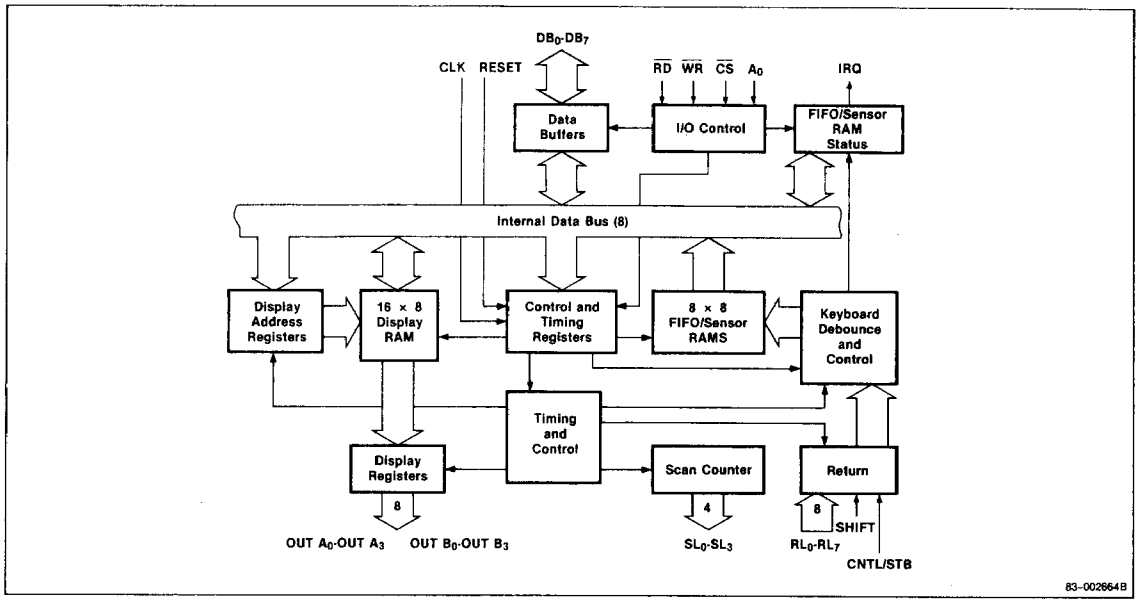
V_{SS} (Ground Reference)

Ground.

V_{CC} (Power Supply)

+5 V power supply input.

Block Diagram



Functional Description

The μPD8279 has two basic functions: 1) to control displays to output and 2) to control a keyboard for input. Its specific purpose is to unburden the host processor from monitoring keys and refreshing displays. The μPD8279 is designed to directly interface with the microprocessor bus. The microprocessor must program the operating mode to the μPD8279 as follows:

Output Modes

- 8 or 16 character display
- Right or left entry display formats

Input Modes

- Scanned keyboard with encoded (8 x 8 key keyboard) or decoded (4 x 8 key keyboard) scan lines.
- Scanned sensor matrix with encoded (8 x 8 matrix switches) or decoded (4 x 8 matrix switches) scan lines.
- Strobed input with data on return lines during control line strobe being transferred to FIFO.

Block Diagram

Following is a description of each section of the μPD8279. See the block diagram for functional reference.

I/O Control and Data Buffers

Communication to and from the μPD8279 is performed by selecting $\overline{CS}$, A_0, $\overline{RD}$ and $\overline{WR}$. The type of information written or read by the processor is selected by A_0. A logic 0 states that information is data while a 1 selects command or status. $\overline{RD}$ and $\overline{WR}$ select the direction by which the transfer occurs through the data buffers. When the chip is deselected ($\overline{CS}$ = 1) the bidirectional data buffers are in a high impedance state. This enables the μPD8279 to be tied directly to the processor bus.

Timing Registers and Timing Control

The timing registers store the display and keyboard modes and other conditions programmed by the processor. The timing control contains the timing counter chain. One counter is a divide-by-N scaler, which may be programmed to match the processor cycle time. The scaler is programmed with a value between 2 and 31 to divide the external clock input by N to yield the internal clock frequency. A value which scales the internal frequency to 100 kHz gives a 5.1 ms scan time and 10.3 ms switch debounce. The other counters divide down to make key, row matrix, and display scans.

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Scan Counter

The scan counter can operate in either the encoded or decoded mode. In the encoded mode, the counter provides a count which must be decoded to provide the scan lines. In the decoded mode, the counter provides a 1 out of 4 decoded scan. In the encoded mode, the scan lines are active high, and in the decoded mode, they are active low.

Return Buffers, Keyboard Debounce and Control

The eight return lines are buffered and latched by the return buffers. In the keyboard mode these lines are scanned to sample for key closures in each row. If the debounce circuit senses a closure, about 10 ms are timed out and a check is performed again. If the switch is still pressed, the address of the switch matrix plus the status of shift and control are written into the FIFO. In the scanned sensor mode, the contents of return lines are sent directly to the sensor RAM (FIFO) each key scan. In the strobed mode, the transfer takes place on the rising edge of CNTL/STB.

FIFO/Sensor RAM and Status

This section is a dual purpose 8 x 8 RAM. In strobe or keyboard mode it is a FIFO. Each entry is pushed into the FIFO and read in order. Status keeps track of the number of entries in the FIFO. Too many reads or writes to the FIFO will be treated as an error condition. The status logic generates an IRQ whenever the FIFO has an entry. In the sensor mode the memory is a sensor RAM which detects changes in the status of a sensor. If a change occurs, the IRQ is generated until the change is acknowledged.

Display Address Registers and Display RAM

The display address register contains the address of the word being read or written by the processor, as well as the word being displayed. This address may be programmed to autoincrement after each read or write. The display RAM may be read by the processor any time after the mode and address is set. Data entry to the display RAM may be set to either right or left entry.

Command Operation

The commands programmable to the μPD8279 via the data bus with $\overline{CS}$ active (0) and A_0 high are as follows:

Keyboard/Display Mode Set

0	0	0	D	D	K	K	K

Display Mode:

D	D	
0	0	Eight 8-bit character display—left entry
0	1(1)	Sixteen 8-bit character display—left entry
1	0	Eight 8-bit character display—right entry
1	1	Sixteen 8-bit character display—right entry

Note:

(1) Power on default condition.

Keyboard Mode:

K	K	K	
0	0	0	Encoded scan—2 key lockout
0	0	0	Decoded scan—2 key lockout
0	1	0	Encoded scan—N key rollover
0	1	1	Decoded scan—N key rollover
1	0	0	Encoded scan—sensor matrix
1	0	1	Decoded scan—sensor matrix
1	1	0	Strobed input, encoded display scan
1	1	1	Strobed input, decoded display scan

Program Clock

0	0	1	P	P	P	P	P

Where PPPPP is the prescaler value between 2 and 31. This prescaler divides the external clock by PPPPP to develop its internal frequency. After reset, a default value of 31 is generated.

Read FIFO/Sensor RAM

0	1	0	A_1	X	A	A	A	$A_0 = 0$

A_1 is the autoincrement flag. AAA is the row to be read by the processor. The read command is accomplished with ($\overline{CS}$ • RD • $\overline{A0}$) by the processor. If A_1 is 1, the row select counter will be incremented after each read. Note that autoincrementing has no effect on the display.

Read Display RAM

0	1	1	A_1	X	A	A	A	$A_0 = 0$

Where A_1 is the autoincrement flagg and AAAA is the character which the processor is about to read.

Write Display RAM

1	0	0	A_1	A	A	A	A

Where AAAA is the character the processor is about to write.

Display Write Inhibit Blanking

1	0	1	X	IW	IW	BL	BL
				A	B	A	B

Where IWA and IWB are inhibit writing nibble A and B respectively, while BLA and BLB are used for blanking. When using the display as a dual 4-bit, it is necessary to mask one of the 4-bit halves to eliminate interaction between the two halves. This in accomplished with the IW flags. The BL flags allow the programmer to blank either half of the display independently. To blank a display formatted as a single 8-bit, it is necessary to set both BLA and BLB. Default after a reset is all zeros. All signals are active high (logic 1).

Clear

1	1	0	C_D	C_D	C_D	C_F	C_A

Where:

C_D	C_D	C_D	
1	0	X	All zeros
1	1	0	AB = 20H
1	1	1	All ones
0	X	X	Disable clear display

This command is used to clear the display RAM, the FIFO, or both. The C_D options allow the user the ability to clear the display RAM to either all zeros or all ones. Clearing the display takes one complete display scan. During this time the processor can't write to the display RAM.

If the C_F bit is set to logic 1, the FIFO status is cleared, the FIFO empty flag is set, and IRQ is cleared. The sensor matrix mode RAM pointer will then be set to row 0.

C_A, the clear all bit, has the combined effect of C_F and C_D; it uses the C_D clearing code on the display RAM and also clears FIFO status. It also resynchronizes the internal timing chain.

End Interrupt/Error Mode Set

1	1	1	E	X	X	X	X

In the sensor matrix mode, this instruction clears IRQ and allows writing into RAM. In N key rollover, setting the E bit to 1 allow for operating in the special error mode. See description of FIFO status.

FIFO Status

D_U	S/E	O	U	F	N	N	N

Where:

- DU = Display unavailable because a clear display or clear all command is in progress.
- S/E = Sense error flag due to multiple closure of switch matrix.
- O = FIFO overrun since an attempt was made to push too many characters into the FIFO.
- U = FIFO underrun. An indication that the processor tried to read an empty FIFO.
- F = FIFO full flag.
- NNN = The number of characters presently in FIFO.

The FIFO status is read with A_0 high and $\overline{CS}$, $\overline{RD}$ active low.

If the C_D or C_A command has not completed its clearing, the display is not available. The S/E flags are used to show an error in multiple closures has occurred. The O or U, overrun or underrun, flags occur when too many characters are written into the FIFO or the processor tries to read an empty FIFO. F is an indication that the FIFO is full and NNN is the number of characters in the FIFO.

Data Read

Data can be read during A_0 = 0 and when $\overline{CS}$, $\overline{RD}$ are active low. The source of data is determined by the read display or read FIFO commands.

Data Write

Data is written to the chip when A_0, $\overline{CS}$, and $\overline{WR}$ are active low. Data will be written into the display RAM with its address selected by the latest read or write display command.

Data Format

CNTL	SH	SCAN	RET

In the scanned key mode, the characters in the FIFO correspond to the above format where CNTL and SH are the most significant bits and the SCAN and return lines are the scan and column counters.

RL_7	RL_6	RL_5	RL_4	RL_3	RL_2	RL_1	RL_0

In the sensor matrix mode, the data corresponds directly to the row of the sensor RAM being scanned. Shift and control (SH, CNTL) are not used in this mode.

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Command Word Summary

0	0	0	D	D	K	K	K	Keyboard display mode set
0	0	1	P	P	P	P	P	Load program clock
0	1	0	A_1	X	A	A	A	Read FIFO/sensor RAM
0	1	1	A_1	A	A	A	A	Read display RAM
1	0	0	A_1	A	A	A	A	Write display RAM
1	0	1	X	IW A	IW B	BL A	BL B	Display write inhibit/blanking
1	1	0	C_D	C_D	C_D	C_F	C_A	Clear
1	1	1	E	X	X	X	X	End interrupt/error mode set
D_U	S/E	0	U	F	N	N	N	FIFO status

Absolute Maximum Ratings

T_A = 25°C

Power supply voltage, V_{DD}	−0.5 V to +7.0 V(1)
Power dissipation, P_D	1.0 W
Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Note:

(1) With respect to V_{SS}.

Comment: Exposing the device to stresses above those listed in the absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Capacitance

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I	5		10	pF	$V_I = V_{CC}$
Output capacitance	C_O	10		20	pF	$V_O = V_{CC}$

DC Characteristics

T_A = 0°C to +70°C; V_{CC} = 5 V ±10%; V_{SS} = 0 V

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
Input high voltage for return lines	V_{IH1}	2.2		V	
Input high voltage for other lines	V_{IH2}	2.0		V	
Input low voltage for return lines	V_{IL1}	−0.5	1.4	V	
Input low voltage for other lines	V_{IL2}	−0.5	0.8	V	
Output high voltage on interrupt line	IRQ pin	+3.5		V	I_{OH} = −50 μA
	others	+2.4		V	I_{OH} = −400 μA
Output low voltage	V_{OL}		0.45	V	I_{OL} = 2.2 mA
Input current on shift, control and return lines	I_{IL1}		+10	μA	$V_I = V_{CC}$
			−100	μA	V_I = 0 V
Input leakage current for other lines	I_{IL2}		±10	μA	$V_I = V_{CC}$ to 0 V
Output float leakage	I_{OFL}		±10	μA	$V_O = V_{CC}$ to 0 V
Power supply current	I_{CC}		120	mA	

AC Characteristics

T_A = 0°C to +70°C; V_{CC} = 5 V ±10%; V_{SS} = 0 V

Parameter	Symbol	μPD8279-5 Limits Min	μPD8279-5 Limits Max	μPD8279-2 Limits Min	μPD8279-2 Limits Max	Unit	Test Conditions
Read							
Address stable before $\overline{\text{read}}$	t_{AR}	0		0		ns	
Address hold time for $\overline{\text{read}}$	t_{RA}	0		0		ns	
$\overline{\text{Read}}$ pulse width	t_{RR}	250		200		ns	
Data delay from $\overline{\text{read}}$	t_{RD}		150		140	ns	C_L = 150 pF
Address to data valid	t_{AD}		250		250	ns	C_L = 150 pF
$\overline{\text{Read}}$ to data floating	t_{DF}	10	100	10	100	ns	
Read cycle time	t_{RCY}	1000		200		ns	
Write							
Address stable before $\overline{\text{write}}$	t_{AW}	0		0		ns	
Address hold time for $\overline{\text{write}}$	t_{WA}	0		0		ns	
$\overline{\text{Write}}$ pulse width	t_{WW}	250		200		ns	
Data set up time for $\overline{\text{write}}$	t_{DW}	150		150		ns	
Data hold time for $\overline{\text{write}}$	t_{WD}	0		0		ns	
Write cycle time	t_{WCY}	1000		200		ns	
Other							
Clock pulse width	$t_{\phi W}$	120		70		ns	
Clock period	t_{CY}	320		200		ns	

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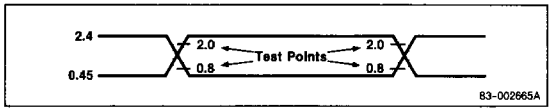
General Timing

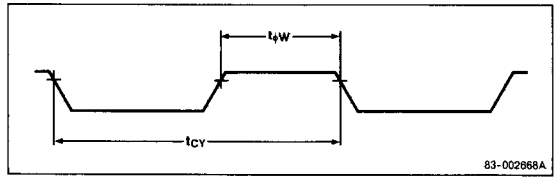
Keyboard scan time	5.1 ms
Keyboard debounce time	10.3 ms
Key scan time	80 μs
Display scan time	10.3 ms
Digit-on time	480 μs
Blanking time	160 μs
Internal clock cycle	10 μs

Timing Waveforms

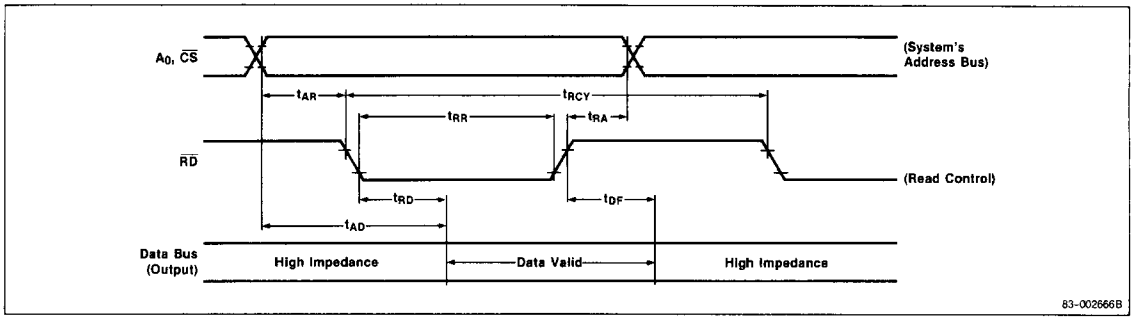
AC Test Input



Clock Input



Read



Write