uS5651P

ADC Prefilter with Analog Multiplexer

General Description

The uS5651P is an ADC prefilter with analog multiplexer, which output is used mainly by the analog to digital converter (ADC) of GPU/ASIC for voltage and current monitoring. This device has four input channels, and each channel has an independent voltage and current monitoring input. This part senses the voltage across the shunt resistor for current monitoring. The voltage and current information of each channel is processed and scaled then sent to a differential output via a multiplexer. The multiplexer selects which channel to be the signal source in a switching manner. The operating mode, switching sequence, scaling factor and other parameters are set by the I^2C register. The device operates with 3.3V VCC supply voltage, and it is available in a WQFN4x4-32L package.

Features

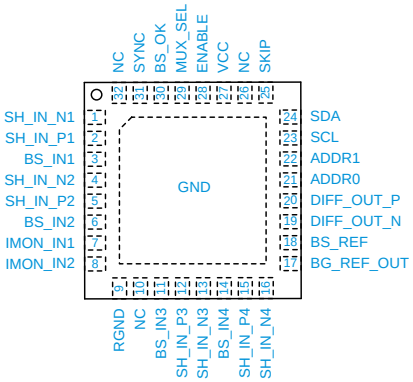
- 4 Channel Bus Voltage Monitoring Inputs, Up to 30V
- 4 Channel Shunt Current Monitoring Inputs with 5V to 30V Operating Voltage
- 2.8V to 3.8V VCC Supply Voltage
- Differential Output via Analog Multiplexer with Single Bit MUX Select
- Selectable I^2C Device Address by Resistor Strap
- Adjustable Scaling Factors and Operating Parameters by I^2C Registers
  - Active Channel
  - Alternating Mode
  - Offset Voltage
  - Common Mode Voltage
  - Voltage Gain (Bus Gain)
  - Current Gain (Shunt Gain)
- Open-Drain Bus OK Indicator
- Device Enable Control
- Two IMON Analog Inputs
- Reference GND Input
- Stand-Alone and Dual Device Operation Mode
- Low Profile WQFN4x4-32L Package
- RoHS Compliant and Halogen Free

Ordering Information

Order Number	Package Type	Top Marking
uS5651PQKI	WQFN4x4-32L	uS5651P

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



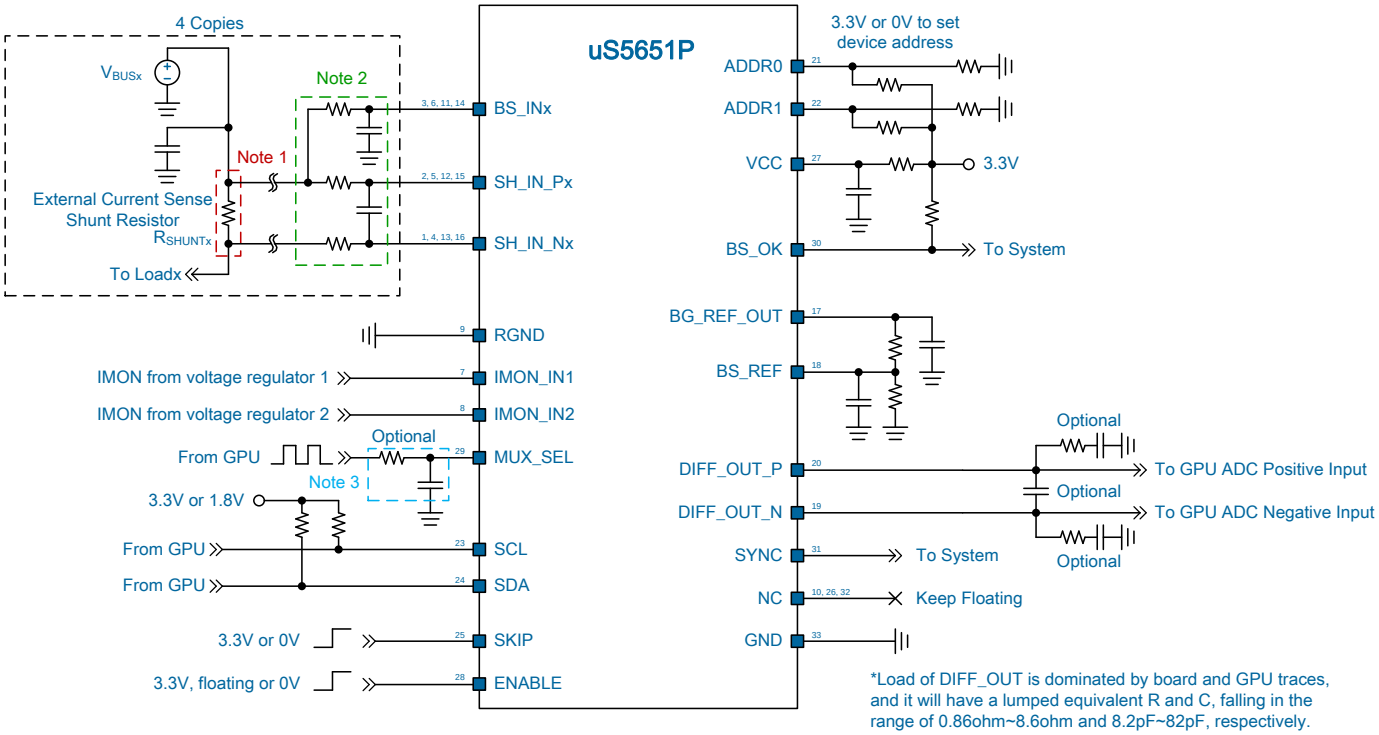
Applications

- Computers
- Power Management
- Battery Chargers
- Power Supplies
- Test Equipments

uS5651P

Typical Application Circuit

4-Channel Stand-Alone Mode



Note 1: Use Kelvin connection for external current sense shunt resistor.

Note 2: Local RC filter at BS_Inx input, and local RCR filter at SH_IN_Px and SH_IN_Nx input are required for noise filtering.

Note 3: Recommend to reserve RC circuit at MUX_SEL and DIFF_OUT pins for noise filtering when necessary.

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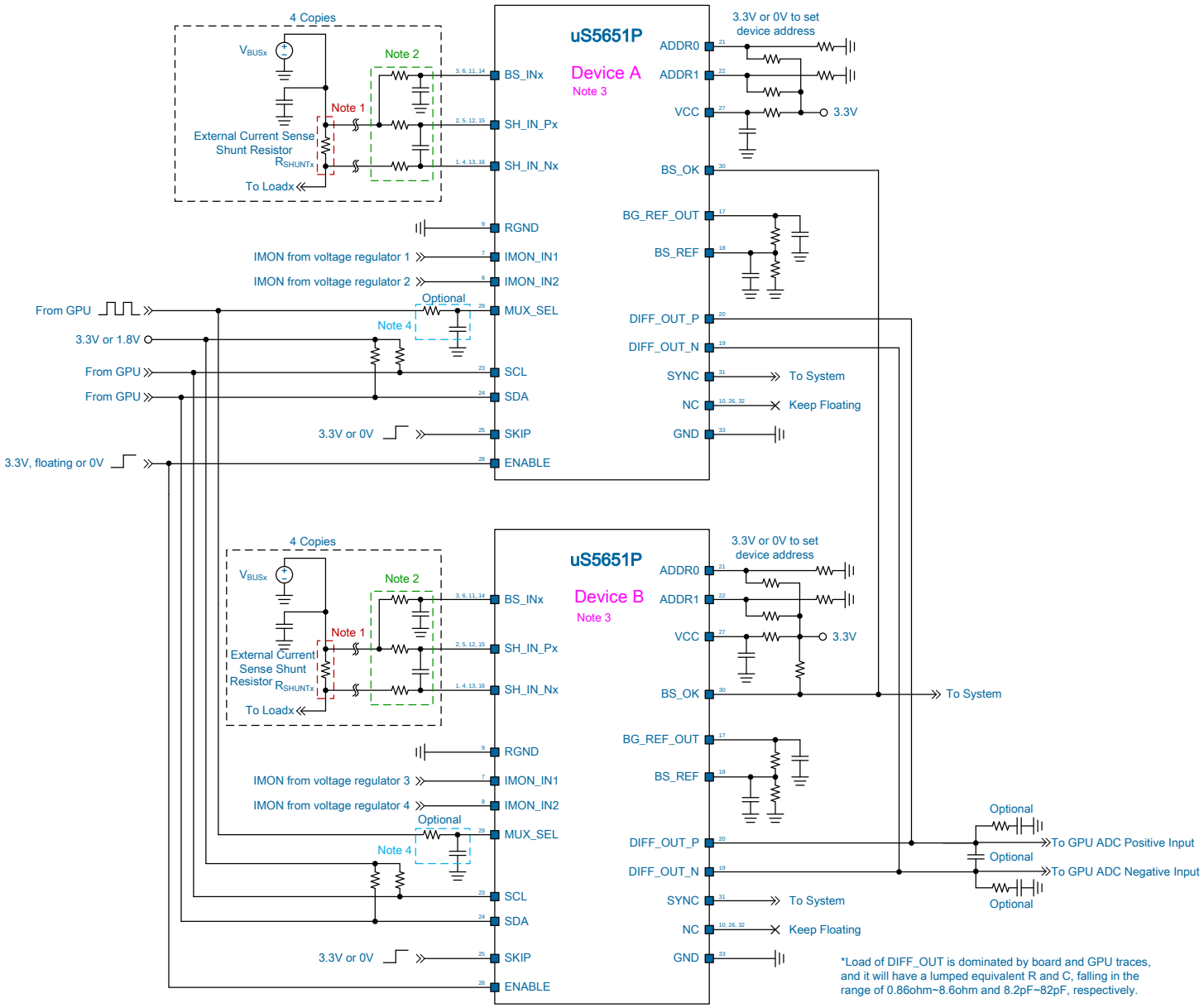
Typical Application Circuit

8-Channel Dual Device Mode



Note 1: Use Kelvin connection for external current sense shunt resistor.

Note 2: Local RC filter at BS_INx input, and local RCR filter at SH_IN_Px and SH_IN_Nx input are required for noise filtering.

Note 3: Register 0x05h of each device need to be programmed to activate dual device mode operation.

Note 4: Recommend to reserve RC circuit at MUX_SEL and DIFF_OUT pins for noise filtering when necessary.

Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
1	SH_IN_N1	AI	**Negative Node of Current Monitoring Input for Channel 1.**Connect to the external current sense shunt resistor with Kelvin connection for current sense. If not used, see related section for pin connection of unused channel.
2	SH_IN_P1	AI	**Positive Node of Current Monitoring Input for Channel 1.** Connect to the external current sense shunt resistor with Kelvin connection for current sense. If not used, see related section for pin connection of unused channel.
3	BS_IN1	AI	**Bus Voltage Sense Input for Channel 1.** Connect to the same point as SH_IN_P1. If not used, see related section for pin connection of unused channel.
4	SH_IN_N2	AI	**Negative Node of Current Monitoring Input for Channel 2.** Connect to the external current sense shunt resistor with Kelvin connection for current sense. If not used, see related section for pin connection of unused channel.
5	SH_IN_P2	AI	**Positive Node of Current Monitoring Input for Channel 2.** Connect to the external current sense shunt resistor with Kelvin connection for current sense. If not used, see related section for pin connection of unused channel.
6	BS_IN2	AI	**Bus Voltage Sense Input for Channel 2.** Connect to the same point as SH_IN_P2. If not used, see related section for pin connection of unused channel.
7	IMON_IN1	AI	**Voltage Regulator IMON Input 1.** Connect to the total output current signal of voltage regulator 1.
8	IMON_IN2	AI	**Voltage Regulator IMON Input 2.** Connect to the total output current signal of voltage regulator 2.
9	RGND	AI	**Ground Reference Channel Input.** Connect to the ground near this device. The device will use this as an input and mux it through signal channel.
10, 26, 32	NC	--	**Do not connect to any circuit.** These pins must be left floating.
11	BS_IN3	AI	**Bus Voltage Sense Input for Channel 3.** Connect to the same point as SH_IN_P3. If not used, see related section for pin connection of unused channel.
12	SH_IN_P3	AI	**Positive Node of Current Monitoring Input for Channel 3.** Connect to the external current sense shunt resistor with Kelvin connection for current sense. If not used, see related section for pin connection of unused channel.

Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
13	SH_IN_N3	AI	**Negative Node of Current Monitoring Input for Channel 3.** Connect to the external current sense shunt resistor with Kelvin connection for current sense. If not used, see related section for pin connection of unused channel.
14	BS_IN4	AI	**Bus Voltage Sense Input for Channel 4.** Connect to the same point as SH_IN_P4. If not used, see related section for pin connection of unused channel.
15	SH_IN_P4	AI	**Positive Node of Current Monitoring Input for Channel 4.** Connect to the external current sense shunt resistor with Kelvin connection for current sense. If not used, see related section for pin connection of unused channel.
16	SH_IN_N4	AI	**Negative Node of Current Monitoring Input for Channel 4.** Connect to the external current sense shunt resistor with Kelvin connection for current sense. If not used, see related section for pin connection of unused channel.
17	BG_REF_OUT	AO	**Bandgap Reference Voltage Output.** Connect a MLCC to this pin for noise decoupling. BG_REF_OUT is the voltage source for resistor voltage divider for BS_REF input. It is recommended to use MLCC of 100nF minimum for noise decoupling.
18	BS_REF	AI	**Reference Input for the BS_OK Comparator.** Connect a resistor voltage divider from BG_REF_OUT to this pin to set the reference voltage for bus-ready comparator (for BS_OK). Recommend to add a MLCC to this pin for noise decoupling.
19	DIFF_OUT_N	AO	**Negative Output Node of Differential Amplifier.** Connect this pin to the GPU ADC negative input pin. It is recommended to reserve RC circuit for noise decoupling when necessary.
20	DIFF_OUT_P	AO	**Positive Output Node of Differential Amplifier.** Connect this pin to the GPU ADC positive input pin. It is recommended to reserve RC circuit for noise decoupling when necessary.
21	ADDR0	DI	**Device Address Setting 0.** Logic state of this pin determines the I^2C address of this device. See I^2C Device Bus Address Setting table for detail.
22	ADDR1	DI	**Device Address Setting 1.** Logic state of this pin determines the I^2C address of this device. See I^2C Device Bus Address Setting table for detail.
23	SCL	DI	**I^2C Clock Input.** This pin receives serial bus clock signal input (3.3V or 1.8V logic).
24	SDA	DI/DO	**I^2C Data Input.** This pin is input or output of serial bus data signal (3.3V or 1.8V logic).

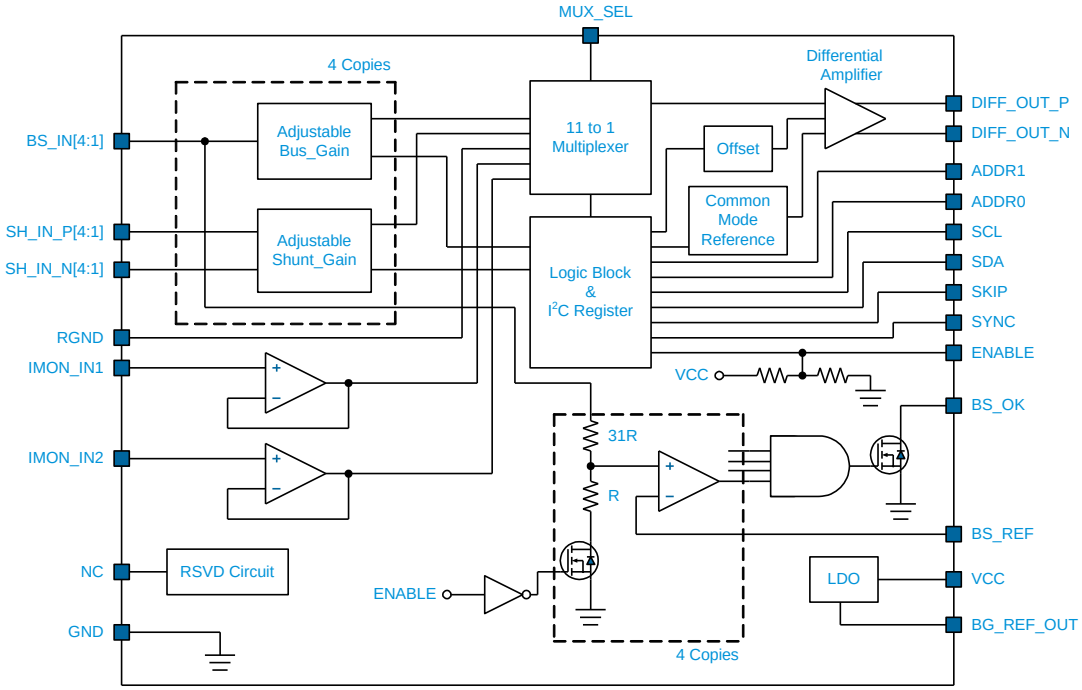
Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
25	SKIP	DI	**Mask for BS_OK.** See table of logic state of ENABLE, SKIP, BS_INx and BS_OK for detail.
27	VCC	AI	**Supply Input for the Device.** Connect this pin to a 3.3V voltage source with a MLCC of 1uF minimum.
28	ENABLE	DI	**Enable Control (Active Low)**. Logic state of this pin enable/disable the device. Note that this pin is active low, which means logic state low to this pin enables this device to full function state.
29	MUX_SEL	DI	**Multiplexer Selection Input.** The multiplexer selects which channel to be the signal source per MUX_SEL clock input. It is recommended to reserve RC circuit for noise filtering. It is recommended to reserve RC filter at MUX_SEL input for noise filtering.
30	BS_OK	DO	**Bus OK Indication.** This pin is an open-drain output. Connect this pin to a voltage source with a pull-up resistor.
31	SYNC	DO	**Synchronous Output.** This pin outputs a pulse for the first MUX_SEL period in every MUX_SEL sequence.
Exposed Pad		--	**Ground.** The exposed pad is the ground of the device, and it must be soldered to a large PCB and connected to GND.

Note: AI=Analog Input; AO=Analog Output; DI=Digital Input; DO=Digital Output

uS5651P

Functional Block Diagram



Functional Description

Device Enable Control

Input logic state of ENABLE pin controls the disable/enable of this device. Note that the ENABLE function is **active low**, which is different from the pin name convention. There are three logic levels for ENABLE function as shown in the table below.

Table 1. Logic Input State of ENABLE and Operation Mode

Input Logic State of ENABLE	Description
Low	**Enabled and fully functional.**
Tri-state	**Enabled but with limited function.** Only BG_REF_OUT and BS_OK comparators are functional. All other functions are disabled to reduce power consumption. The differential amplifier output (DIFF_OUT_P/N) is in high impedance state, and MUX_SEL logic input is ignored.
High	**Disabled.** The device is disabled and in standby mode. All functions are turned off to minimize power consumption.

I²C Device Address Setting

The uS5651P has I²C interface for function setting. Logic state of ADDR0 and ADDR1 determines the I²C address of this device. It is recommended to use VCC or ground for address setting logic input. See Table 2 for device address setting.

Table 2. I²C Device Address Setting

ADDR1 Input	ADDR0 Input	I²C Device Address Bit[7:1]
GND	GND	0110100 (68h)
GND	VCC	0110101 (6Ah)
VCC	GND	0110110 (6Ch)
VCC	VCC	0110111 (6Eh)

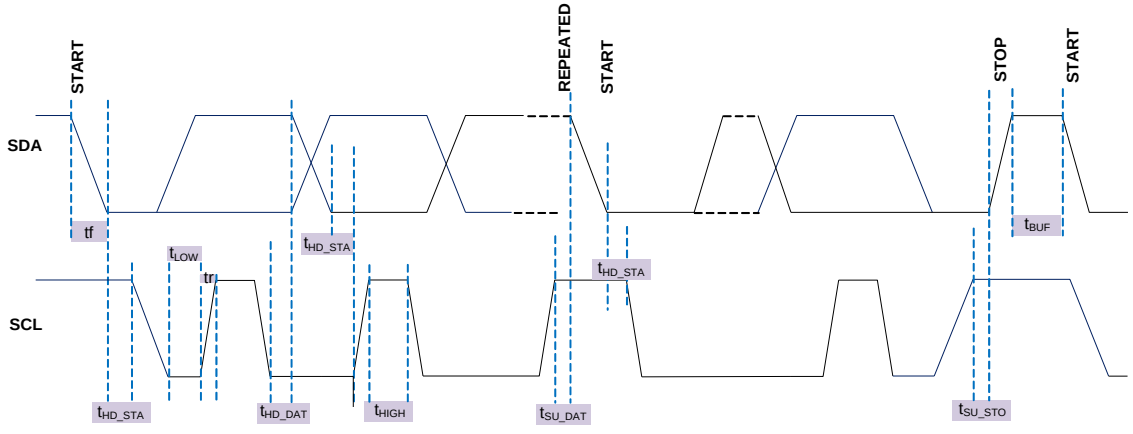
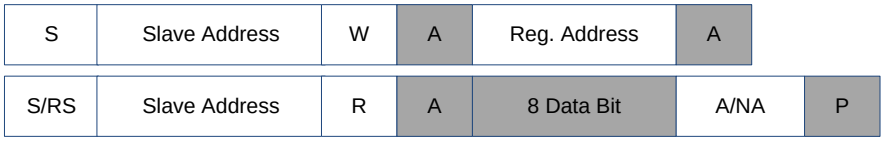


Figure 1. I²C Bus Timing Diagram

Functional Description

Read Data:



From Master to Slave

From Slave to Master

Slave address: 7 bit Reg. address: 8 bit
W: 1'b0, R:1'b1
S: Start, P: Stop, RS: Restart
A: ACK (SDA low)
NA: Not ACK (SDA high)

Write Data:

From Master to Slave

From Slave to Master

Slave address: 7 bit Reg. address: 8 bit
W: 1'b0, R:1'b1
S: Start, P: Stop
A: ACK (SDA low)
NA: Not ACK (SDA high)

Figure 2. I^2C Read/Write Protocol Format

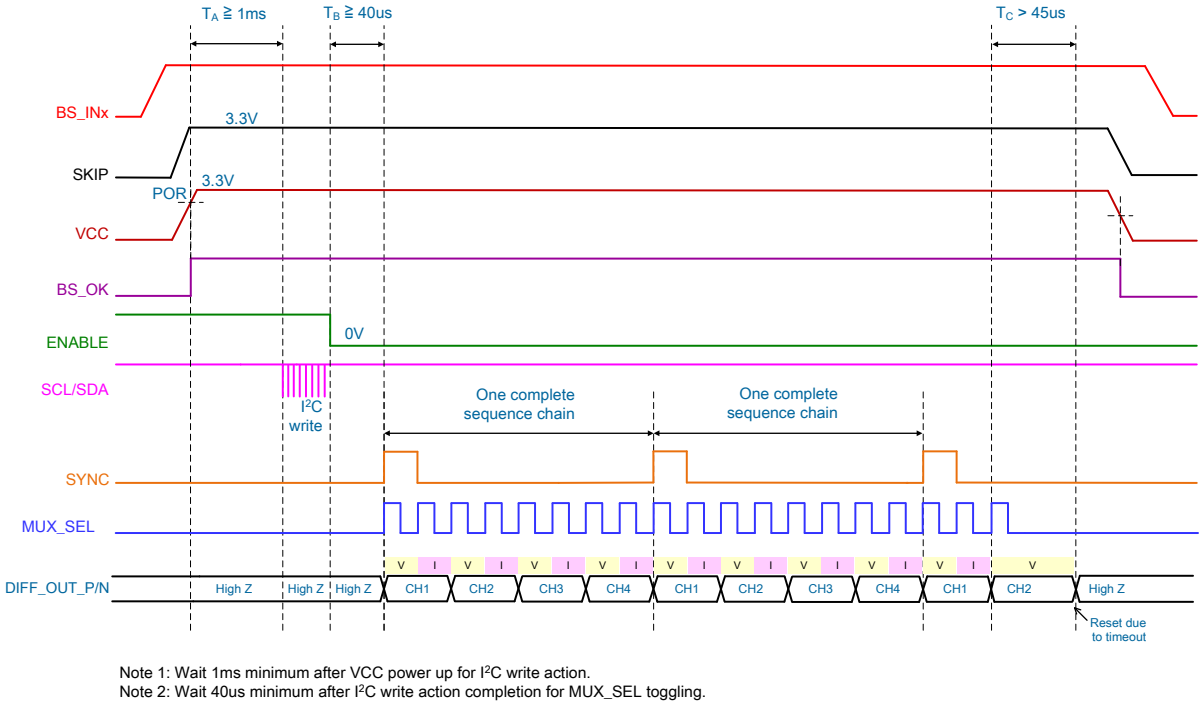
Table 3. Timing Requirements of I^2C Interface

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{I2C}	--	400	kHz
Repeated Hold Time START Condition	t_{HD_STA}	0.26	--	us
Data Hold Time	t_{HD_DAT}	0	--	us
LOW Period of SCL Clock	t_{LOW}	0.5		us
HIGH Period of SCL Clock	t_{HIGH}	0.26	--	us
Setup Time for Repeated START Condition	t_{SU_STA}	0.26	--	us
Data Setup Time	t_{SU_DAT}	50		ns
Setup Time for STOP Condition	t_{SU_STO}	0.26	--	us
Bus Free Time between STOP and START Condition	t_{BUF}	0.5	--	us
Rise Time for Both SDA and SCL Signals	t_r	--	120	ns
Fall Time for Both SDA and SCL Signals	t_f	--	120	ns

Functional Description

Power up Sequence

Once the device is enabled and its VCC rises above the POR threshold, it starts to operate. The timing relation between VCC, BS_IN, BS_OK and MUX_SEL is shown in the Figure 3. For I^2C writing timing, a delay time of 1ms (T_A) minimum is required after VCC POR. It is required to wait for at least 1ms after VCC POR to write data into registers. This is to ensure all the internal circuits are ready to receive I^2C command. As for MUX_SEL timing, a delay time of 40us (T_B) minimum is required after ENABLE go low (device enabled) to MUX_SEL toggling. It is required to wait for at least 40us after ENABLE go low to toggle MUX_SEL. This delay time is to ensure all the circuits are ready for operation mode transition. Note that the MUX_SEL has a timeout of 45us (T_C) maximum, therefore the device will go back to the initial state of output sequence if MUX_SEL stays high or low longer than timeout.



Note 1: Wait 1ms minimum after VCC power up for I^2C write action.
Note 2: Wait 40us minimum after I^2C write action completion for MUX_SEL toggling.

Figure 3. Timing Relation between VCC, BS_IN, BS_OK and MUX_SEL.

Shunt Current Monitoring

The input for shunt current monitoring function comes in a pin pair (SH_IN_P and SH_IN_N). An external current sense shunt resistor is required to convert current signal to voltage signal for channel current sensing. In each channel, a differential amplifier senses the voltage across the external shunt resistor, amplifying the sensed voltage with a ratio Shunt_Gain. The amplified signal is fed to a multiplexer then sent to the single to differential amplifier and outputs (DIFF_OUT_P and DIFF_OUT_N) to GPU. The ADC of the GPU then receives the shunt current information. For shunt current monitoring, the output of differential amplifier is as follows.

$$V_{DIFF\_OUT} = I \times R_{SENSE} \times Shunt\_Gain$$

Functional Description

I is the shunt current, R_{SENSE} is the resistance of current sense shunt resistor, and Shunt_Gain is the amplification ratio. The Shunt_Gain value is adjustable in register 0x20h~0x23h. Table 4 lists the Shunt_Gain register content.

Note that the PCB trace routing between the external current sense shunt resistor and SH_IN_P/N pins should be Kelvin connection. Also, the BS_IN pin should be tied to the same point as SH_IN_P.

Table 4. Shunt_Gain Register Content

Shunt_Gain Register (0x20h, 0x21h, 0x22h, 0x23h) Content, bit[7:6] and bit0 are fixed=0					
Bit[5:1]	**Hex (include bit7, bit6 & bit0)**	**Shunt_Gain**	**Bit[5:1]**	**Hex (include bit7, bit6 & bit0)**	**Shunt_Gain**
00000	00(default)	2.000	10000	20	7.212
00001	02	2.167	10001	22	7.813
00010	04	2.348	10010	24	8.465
00011	06	2.544	10011	26	9.172
00100	08	2.756	10100	28	9.937
00101	0A	2.986	10101	2A	10.767
00110	0C	3.235	10110	2C	11.665
00111	0E	3.505	10111	2E	12.639
01000	10	3.798	11000	30	13.694
01001	12	4.115	11001	32	14.837
01010	14	4.458	11010	34	16.075
01011	16	4.830	11011	36	17.417
01100	18	5.233	11100	38	18.870
01101	1A	5.670	11101	3A	20.445
01110	1C	6.143	11110	3C	22.151
01111	1E	6.656	11111	3E	24.000

Bus Voltage Monitoring and BS_OK

The bus voltage monitoring function has a single input pin (BS_IN). The BS_IN is internally connected to a resistor voltage divider with adjustable dividing ratio of 1/Bus_Gain. The Bus_Gain is adjustable in register 0x10h~0x13h. Table 5 lists the Bus_Gain register content. The BS_IN input is scaled down and fed to a multiplexer then sent to a single to differential amplifier and outputs (DIFF_OUT_P and DIFF_OUT_N) to GPU. The common mode voltage of the differential amplifier is determined by register 0x08h with 675mV as default setting. The analog to digital converter (ADC) of the GPU then receives the bus voltage information.

For bus voltage monitoring, the output of differential amplifier is $V_{DIFF\_OUT}=V_{BS\_IN}$ / *Bus_Gain*, where Bus_Gain is the denominator, meaning it is an attenuation factor.

Functional Description

Table 5. Bus_Gain (Attenuation Factor) Register Content

Bus_Gain (Attenuation Factor) Register (0x10h, 0x11h, 0x12h, 0x13h) Content, bit[7:6] and bit0 are fixed=0					
Bit[5:1]	**Hex (include bit7, bit6 & bit0)**	**Bus_Gain (Attenuation Factor)**	**Bit[5:1]**	**Hex (include bit7, bit6 & bit0)**	**Bus_Gain (Attenuation Factor)**
00000	00(default)	64.000	10000	20	15.300
00001	02	58.524	10001	22	13.991
00010	04	53.517	10010	24	12.794
00011	06	48.939	10011	26	11.700
00100	08	44.752	10100	28	10.699
00101	0A	40.923	10101	2A	9.783
00110	0C	37.422	10110	2C	8.946
00111	0E	34.220	10111	2E	8.181
01000	10	31.292	11000	30	7.481
01001	12	28.615	11001	32	6.841
01010	14	26.167	11010	34	6.256
01011	16	23.928	11011	36	5.720
01100	18	21.881	11100	38	5.231
01101	1A	20.009	11101	3A	4.783
01110	1C	18.297	11110	3C	4.374
01111	1E	16.732	11111	3E	4.000

Operating independently from the multiplexer, the uS5651P have comparators for each bus inputs and VCC. The BS_IN input is internally connected to another voltage divider (fixed as 1/32). In each channel, a comparator compares (1/32) downscaled bus voltage with BS_REF (divided from BG_REF_OUT) to indicate whether the bus voltage is good for operation. When the (1/32) downscaled bus voltage of all active channels are higher than BS_REF, VCC is higher than a threshold (for BS_OK) and the SKIP pin is logic High, the BS_OK (open-drain) is set to high impedance state (BS_OK=High) to indicate bus voltage is good. Note that the Bus_Gain setting in I^2C registers does not affect the BS_OK function since they are operated independently.

Functional Description

ENABLE, SKIP and BS_INx

The BS_OK function provides an indication that all the effective bus voltage inputs are above the user-defined level. BS_OK keeps low if any of the active bus voltage inputs fall below the user-defined level. In addition, the SKIP pin provides a flexibility to modify the logic of ENABLE, BS_IN and BS_OK. The complete logic table of ENABLE, BS_IN, BS_OK and SKIP is as Table 6. The SKIP pin is used to provide power to hold BS_OK=Low in the absence of VCC.

Table 6. Logic State of ENABLE, SKIP, BS_INx and BS_OK

VCC	ENABLE	BS_INx	SKIP	BS_OK	Note
L	L	X	L	H (open drain)	No power is provided to the device.
L	L	X	H	L	Enabled. SKIP pin provides power to hold BS_OK
H	H	X	L	H (open drain)	Disable state (standby mode).
H	H	X	H	L	Disable state (standby mode).
H	L High Z	L	H	L	Fully functional. Enabled but with limited function.
H	L High Z	H	H	H (open drain)	Fully functional. Enabled but with limited function.
H	L High Z	X	L	H (open drain)	Fully functional. Enabled but with limited function.
L=Low, H=High, X=Don’t care, High Z=High impedance state					

Voltage Regulator IMON Monitoring

The uS5651P provides two analog input channels for voltage regulator IMON signal monitoring. IMON_IN1 and IMON_IN2 are connected to the total output current signal of voltage regulators. The input of IMON_IN1 and IMON_IN2 are fed to the multiplexer through a unity gain voltage buffer. The ADC of the GPU then receives the voltage regulator total output current information.

Reference Ground (RGND) Monitoring

The RGND pin is treated as a reference ground input (RGND) of device. The uS5651P uses RGND as an input and mux it through signal chain, and the corresponding output at DIFF_OUT_P/N denotes the offset error of the differential amplifier. The GPU is then able to get the information of differential amplifier offset error, which can be used for offset cancellation when needed.

Functional Description

I²C Register and Function Setting

Most of the functions of the device are controlled by registers. Table 7 shows the register map. Operation of each main function is described in the following sections.

Table 7. Register Map

Register Address	Register Name	Bit	Type	Description	Default Value		New Value Takes Effect
0x00h	Vendor ID	7:0	R	Vendor specific ID	4E		--
0x01h	Device ID	7:0	R		2E		--
0x04h	Active Channel	7	R/W	Ground Reference	0(disable)	0F	At next timeout
		6	--	Don't care	0		--
		5	R/W	IMON Channel 2	0(disable)		At next timeout
		4	R/W	IMON Channel 1	0(disable)		At next timeout
		3	R/W	Channel 4 Voltage & Current	1(enable)		At next timeout
		2	R/W	Channel 3 Voltage & Current	1(enable)		At next timeout
		1	R/W	Channel 2 Voltage & Current	1(enable)		At next timeout
		0	R/W	Channel 1 Voltage & Current	1(enable)		At next timeout
0x05h	MUL_SEL Skip	7:4	R/W	Pulses to skip at start of cycle (operated as Device B in dual device mode)	0 (no pulse to skip)	00	At next timeout
		3:0	R/W	Pulses to skip at start of cycle (operated as Device A in dual device mode)	0 (no pulse to skip)		At next timeout
0x06h	Alternating Mode	7	R/W	Bit7=1: Enable alternating mode Bit7=0: No alternating	0 (No alternating)	00	At next timeout
		6:0	--	Don't care	0		--
0x07h	Offset Voltage	7:4	--	Don't care	0	00	--
		3:0	R/W	1111= -375mV …… 0001= -25mV 0000= 0mV	0(0mV)		At next timeout
0x08	Common Mode Voltage	7:4	--	Don't care	0	07	--
		3:0	R/W	1111= 875mV …… 0001= 525mV 0000= 500mV	7 (675mV)		At next timeout
0x0F	Timeout	7	R/W	Bit7=1: Disable timeout Bit7=0: Enable timeout	0 (Enable timeout)	00	
		6:0	--	Don't care	0		--

Functional Description

Table 7. Register Map (cont.)

Register Address	Register Name	Bit	Type	Description	Default Value		New Value Takes Effect
0x10	Bus_Gain 1	5:1	R/W	See Table 5(2)	00(64)		At next timeout
0x11	Bus_Gain 2	5:1	R/W		00(64)		At next timeout
0x12	Bus_Gain 3	5:1	R/W		00(64)		At next timeout
0x13	Bus_Gain 4	5:1	R/W		00(64)		At next timeout
0x20	Shunt_Gain 1	5:1	R/W	See Table 4(2)	00(2)		At next timeout
0x21	Shunt_Gain 2	5:1	R/W		00(2)		At next timeout
0x22	Shunt_Gain 3	5:1	R/W		00(2)		At next timeout
0x23	Shunt_Gain 4	5:1	R/W		00(2)		At next timeout
0x24	Lock	7:2	--	Don't care	00	0	--
		1	R/W	Bit1=1: Lock interface write action Bit1=0: Allow interface write action		0 (allow write)	Immediately
		0	R/W	Bit1=1: Lock interface read and write action Bit1=0: Allow interface read and write action		0 (allow read and write)	Immediately

Note 1: R=Read, R/W=Read and Write

Note 2: For Bus_Gain and Shunt_Gain registers, bit [7:6] and bit 0 are always 0.

MUX_SEL and Multiplexer Output Sequence

A differential amplifier outputs a scaled bus voltage and shunt current (in the form of voltage) for active channels. These voltage and current information are sent to DIFF_OUT_P and DIFF_OUT_N via a multiplexer.

The multiplexer selection is done through a single bit digital input clock MUX_SEL. The device monitors the input and cycle the output in a fixed sequence. The sequence starts with the bus voltage of first enumerated and active channel before changing to its shunt. It then cycles likewise through the bus/shunt pairs in order of enumeration repeating itself after the shunt of the last active channel has been passed through the multiplexer. The multiplexer repeats the cycle indefinitely until either a timeout condition is detected or device is disabled. The multiplexer default output sequence is shown in Table 8.

Table 8. Multiplexer Default Output Sequence

MUX_SEL clock cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Differential Output	High Z	Ch1 Bus V	Ch1 Shunt I	Ch2 Bus V	Ch2 Shunt I	Ch3 Bus V	Ch3 Shunt I	Ch4 Bus V	Ch4 Shunt I	Ch1 Bus V	Ch1 Shunt I	Ch2 Bus V	Ch2 Shunt I	Ch3 Bus V	Ch3 Shunt I	Ch4 Bus V	Ch4 Shunt I
Register setting: 0x04h=0F(default, IMON1, IMON2, RGND are off), 0x05h=00(default, no pulse to skip), 0x06h=00(default, no alternating)																	

			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
register	value (hex)	value(bin)	RGND	RSVD	IMON2	IMON1	CH4 (V&I)	CH3 (V&I)	CH2 (V&I)	CH1 (V&I)
0x04h	0F	00001111	OFF	X	OFF	OFF	ON	ON	ON	ON

Functional Description

Active Channel Configuration (0x04h)

The device can be configured to work with a reduced channel. Register 0x04h determines which channel is active and to be monitored. The default setting of 0x04h is 0F, which means only CH1~CH4 are active and its voltage and current signals are the output.

Table 9 and Table 10 are examples of the multiplexer output sequence with reduced channel.

Table 9. An Example of Multiplexer Output Sequence with Reduced Channel

MUX_SEL clock cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Differential Output	High Z	Ch1 Bus V	Ch1 Shunt I	Ch3 Bus V	Ch3 Shunt I	Ch1 Bus V	Ch1 Shunt I	Ch3 Bus V	Ch3 Shunt I	Ch1 Bus V	Ch1 Shunt I	Ch3 Bus V	Ch3 Shunt I	Ch1 Bus V	Ch1 Shunt I	Ch3 Bus V	Ch3 Shunt I
Register setting: 0x04h=05(Ch2, Ch4, IMON1, IMON2, RGND are off), 0x05h=00(default, no pulse to skip), 0x06h=00(default, no alternating)																	

			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
register	value (hex)	value(bin)	RGND	RSVD	IMON2	IMON1	CH4 (V&I)	CH3 (V&I)	CH2 (V&I)	CH1 (V&I)
0x04	05	00000101	OFF	X	OFF	OFF	OFF	ON	OFF	ON

Table 10. Another Example of Multiplexer Output Sequence with Reduced Channel

MUX_SEL clock cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Differential Output	High Z	Ch1 Bus V	Ch1 Shunt I	Ch2 Bus V	Ch2 Shunt I	Ch3 Bus V	Ch3 Shunt I	Ch4 Bus V	Ch4 Shunt I	IMON2	RGND	Ch1 Bus V	Ch1 Shunt I	Ch2 Bus V	Ch2 Shunt I	Ch3 Bus V	Ch3 Shunt I	Ch4 Bus V	Ch4 Shunt I	IMON2	RGND
Register setting: 0x04h=AF(IMON1 is off), 0x05h=00(default, no pulse to skip), 0x06h=00(default, no alternating)																					

			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
register	value (hex)	value(bin)	RGND	RSVD	IMON2	IMON1	CH4 (V&I)	CH3 (V&I)	CH2 (V&I)	CH1 (V&I)
0x04	AF	10101111	ON	X	ON	OFF	ON	ON	ON	ON

Dual Device (MUX_SEL Skips) Mode (0x05h)

The uS5651P can be configured to work in one of three modes of operation: stand-alone, as device-A, or as device-B per register 0x05h (MUX_SEL Skips) setting. The default setting of 0x05h is 00, which means stand-alone mode operation with no pulse to skip. In stand-alone mode, the device cycles through channels based on active channel configuration in register 0x04h. There is no skip pulse in either start or end of cycles. As device-A mode, the device respond to the first set of clock cycle and then go into high impedance, waiting specified amount of cycles programmed in 0x05h bit [3:0].

While device-B skips the start of cycles programmed in 0x05 bit [7:4], then responds to the subsequent clocks. With the capability of specifying different skip cycles for two devices, asymmetric channel configuration is achieved. Table 11 shows an example of multiplexer output sequence of dual device mode with asymmetric channel configuration. When in dual device mode, one device is configured as device-A, and the other is configured as device-B, both share the MUX_SEL and DIFF_OUT lines on the PCB as shown in the typical application circuit section.

Functional Description

Table 11. An Example of Multiplexer Output Sequence of Dual Device Mode

MUX_SEL clock cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Device- A Differential Output	High Z	Ch1 Bus V	Ch1 Shunt I	Ch2 Bus V	Ch2 Shunt I	Ch3 Bus V	Ch3 Shunt I	IMON1	IMON2	RGND	High Z	High Z	High Z	High Z	High Z	Ch1 Bus V	Ch1 Shunt I
Device- B Differential Output	High Z	High Z	High Z	High Z	High Z	High Z	High Z	High Z	High Z	High Z	Ch1 Bus V	Ch1 Shunt I	Ch3 Bus V	Ch3 Shunt I	RGND	High Z	High Z
Device-A register setting: 0x04h=B7(CH4 is off), 0x05h=05(as device-A, 5 pulses to skip), 0x06h=00(default, no alternating) Device-B register setting: 0x04h=85(CH2, CH4, IMON1, IMON2 are off), 0x05h=90(as device-B, 9 pulses to skip), 0x06h=00(default, no alternating)																	

			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
register	value (hex)	value(bin)	RGND	RSVD	IMON2	IMON1	CH4 (V&I)	CH3 (V&I)	CH2 (V&I)	CH1 (V&I)
0x04	B7	10110111	ON	X	ON	ON	OFF	ON	ON	ON
0x04	85	10000101	ON	X	OFF	OFF	OFF	ON	OFF	ON

Alternating Mode (0x06h)

The device can be configured to work in alternating differential polarity mode (alternating mode), which is set by register 0x06h. In alternating mode, the polarity of the input signal to the differential amplifier and its output is reversed. The polarity reversal technique is often used to cancel potential offset error of the differential amplifier.

Figure 4 shows the simplified input and output diagram of the differential amplifier. V_{DM} is the differential input signal, V_{OFS_ERR} is the offset error of the differential amplifier, V_{DIFF_OUT} is the output, S1 and S2 are switches used to reverse the polarity. The result of first measurement with S1 turned on is

$V_{DIFF\_OUT}(S_1) = V_{DIFF\_OUT\_P} - V_{DIFF\_OUT\_N} = V_{DM} + (V_{OFS\_ERR})$ (Eq. 1)

The result of second measurement with S2 turned on (reversed input and output polarity) is

$V_{DIFF\_OUT}(S_2) = V_{DIFF\_OUT\_P} - V_{DIFF\_OUT\_N} = V_{DM} + (-V_{OFS\_ERR})$ (Eq. 2)

Add Eq. 2 and Eq. 1 yields the final result,

$V_{DIFF\_OUT}(S_1+S_2) = 2*V_{DM}$ (Eq. 3)

The polarity reversal technique effectively removes the offset error. When the device works in alternating mode, the polarity changes in an alternating way as described above. With the alternating mode, the GPU is able to get more accurate voltage/current reporting from the device.

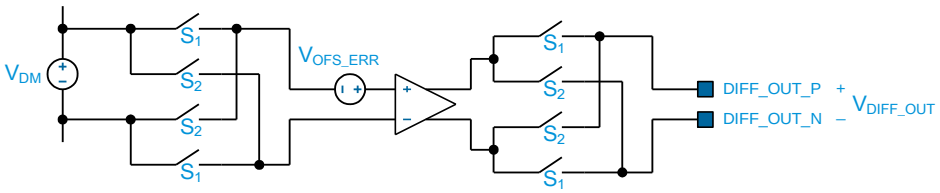


Figure 4. Polarity Reversal in Alternating Mode

When alternating mode is enabled, the N channel device will first output N pairs of differential signal, then each channel signal become reversed differential output. If the reference ground channel is enabled, the reference ground channel is also reversed in alternating mode. Table 12 is an example of multiplexer output sequence of stand-alone application with alternating mode enabled. Table 13 is an example of multiplexer output sequence of dual device application with alternating mode enabled.

Functional Description

Table 12. An Example of Multiplexer Output Sequence of Stand-Alone Mode with Alternating Mode Enabled

MUX_SEL clock cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
Differential Output	High Z	Ch1 Bus V	Ch1 Shunt I	Ch2 Bus V	Ch2 Shunt I	Ch3 Bus V	Ch3 Shunt I	Ch4 Bus V	Ch4 Shunt I	IMON2	RGND	Ch1 Bus V Reversed	Ch1 Shunt I Reversed	Ch2 Bus V Reversed	Ch2 Shunt I Reversed	Ch3 Bus V Reversed	Ch3 Shunt I Reversed	Ch4 Bus V Reversed	Ch4 Shunt I Reversed	IMON2 Reversed	RGND Reversed	Ch1 Bus V	Ch1 Shunt I
Register setting: 0x04h=AF(IMON1 is off), 0x05h=00(default, no pulse to skip), 0x06h=80(bit7=1, enable alternating mode)																							

			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
register	value (hex)	value(bin)	RGND	RSVD	IMON2	IMON1	CH4 (V&I)	CH3 (V&I)	CH2 (V&I)	CH1 (V&I)
0x04	AF	10101111	ON	X	ON	OFF	ON	ON	ON	ON

Table 13. An Example of Multiplexer Output Sequence of Dual Device Mode with Alternating Mode Enabled

MUX_SEL clock cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
Device- A Differential Output	High Z	Ch1 Bus V	Ch1 Shunt I	Ch2 Bus V	Ch2 Shunt I	Ch3 Bus V	Ch3 Shunt I	IMON2	RGND	High Z	High Z	High Z	High Z	High Z	Ch1 Bus V Reversed	Ch1 Shunt I Reversed	Ch2 Bus V Reversed	Ch2 Shunt I Reversed	Ch3 Bus V Reversed	Ch3 Shunt I Reversed	IMON2 Reversed	RGND Reversed	High Z	High Z	High Z	High Z	High Z	Ch1 Bus V	Ch1 Shunt I
Device- B Differential Output	High Z	High Z	High Z	High Z	High Z	High Z	High Z	High Z	High Z	Ch1 Bus V	Ch1 Shunt I	Ch3 Bus V	Ch3 Shunt I	RGND	High Z	High Z	High Z	High Z	High Z	High Z	High Z	High Z	Ch1 Bus V Reversed	Ch1 Shunt I Reversed	Ch3 Bus V Reversed	Ch3 Shunt I Reversed	RGND Reversed	High Z	High Z
Device-A register setting: 0x04h=A7(IMON1, CH4 are off), 0x05h=05(as device-A, 5 pulses to skip), 0x06h=80(bit7=1, enable alternating mode)																													
Device-B register setting: 0x04h=85(CH2, CH4, IMON1, IMON2 are off), 0x05h=80(as device-B, 8 pulses to skip), 0x06h=80(bit7=1, enable alternating mode)																													

			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
register	value (hex)	value(bin)	RGND	RSVD	IMON2	IMON1	CH4 (V&I)	CH3 (V&I)	CH2 (V&I)	CH1 (V&I)
0x04	A7	10100111	ON	X	ON	OFF	OFF	ON	ON	ON
0x04	85	10000101	ON	X	OFF	OFF	OFF	ON	OFF	ON

Offset Voltage for Differential Output (0x07h)

Besides the common mode reference voltage, an additional offset voltage can be applied to the differential amplifier output. The offset voltage for differential output is set in register 0x07h, in the range of -375mV to 0mV, -25mV/step, and the default setting is 00(0mV).

Common Mode Reference Voltage of Differential Output (0x08h)

The common mode reference voltage of the differential output is generated internally and it can be adjusted in register 0x08h. The range of common mode reference voltage is between 500mV to 875mV, 25mV/step, and the default setting is 07(675mV).

Timeout and Reset (0x0Fh)

The multiplexer has a timeout function. The enable/disable of timeout function is controlled by register 0x0Fh bit7, and the default of timeout function is enabled (0x0Fh bit7=0). The timeout function is triggered by keeping the input to MUX_SEL at logic state high or logic state low longer than the timeout period (45us maximum). After the timeout is triggered, the device turns the output of DIFF_OUT_P/N to high impedance state, and the operation of device is interrupted. The output sequence will be reset to the initial state, which means the output will start from CH1_Bus V (default setting) upon the next coming MUX_SEL clock rising edge. If the timeout function is disabled (by setting register 0x0Fh bit7=1), the timeout will not be triggered even if the input to MUX_SEL is kept at logic high or logic low over 45us. In this condition, the operation of the device is not interrupted, and the device will keep the output at the latest state per output sequence chain before the next coming MUX_SEL clock rising edge.

As stated in the above, the triggering of timeout function will reset the output sequence. In addition to the timeout function, toggling the ENABLE pin will also reset the output sequence, which means the output will start from CH1_Bus V (default setting) upon the next coming MUX_SEL clock rising edge.

Functional Description

Connection for Unused Channel

In some applications, not all channels are required. For example, when there are only two channels are physically available, there will be two unused channels. For unused BS_IN, SH_IN_P and SH_IN_N, it is recommended to tie them together to active Bus. The unused IMON or RGND must be shorted to GND. The available pin connections for unused channel are listed in Table 14.

Table 14. Pin Connection for Unused Channel

Pin Name	Pin Connection
BS_INx	Tied to adjacent active BS_IN
SH_IN_Px	Tied to adjacent active BS_IN
SH_IN_Nx	Tied to adjacent active BS_IN
IMON_INx	Short to GND
RGND	Short to GND
Note: For each unused channel, all the three pins (BS_INx, SH_IN_Px and SH_IN_Nx) of that channel should be at the same voltage (e.g. BS_IN3=SH_IN_P3=SH_IN_N3=active BS_IN).	

Filter to Inputs

The uS5651P senses the voltage at one node of the external current sense shunt resistor for voltage reporting, and senses the voltage difference across the two nodes of the same shunt resister for current reporting. The current sense shunt resistor is connected to the load, which is usually the power input of a multi-phase buck converter.

During the operation, the buck converter has load current transients, and its power input experiences current transient events as well. The transient current flows through parasitic components on the PCB trace and the shunt resistor, creating voltage perturbation at the inputs to uS5651P. To ensure normal operation, slight filtering at the inputs of uS5651P is usually required. Figure 5 shows the input filtering of uS5651P. An RC filter locally to the BS_INx pin, and an RCR filter locally to the input pair of SH_IN_Px and SH_IN_Nx pins are required. Since adding RCs to the shunt input pairs affects the sensing accuracy and response time, there is a trade-off in adding these RCs. Use R=51ohm and C=100nF as a start point. It is recommended to keep R unchanged, and increase C when necessary.

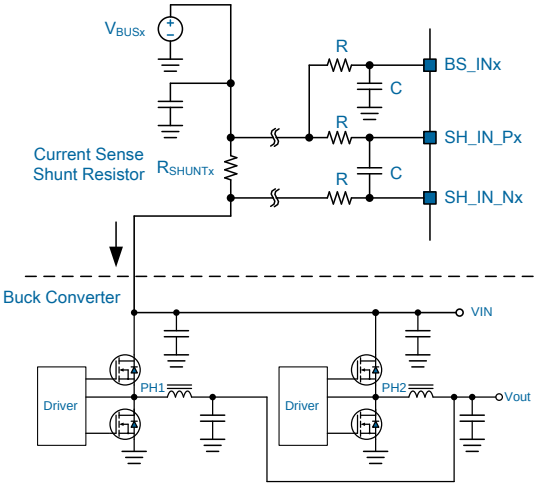


Figure 5. Filter to Inputs

Absolute Maximum Rating

Supply Input Voltage, VCC ---------- -0.3V to +6V
BS_IN_Px, SH_IN_Px, SH_IN_Nx ---------- -0.3V to +30V
DIFF_OUT_P, DIFF_OUT_N ---------- -0.3V to +1.8V
Other Pins ---------- -0.3V to +6V
Junction Temperature ---------- 150 °C
Lead Temperature (Soldering, 10 sec) ---------- 260 °C
ESD Rating (Note 2)
HBM (Human Body Model) ---------- 1kV
CDM (Charged Device Model) ---------- 1kV

Thermal Information

Package Thermal Resistance (Note 3)
WQFN4x4-32L θ_{JA} ---------- 37 °C/W
WQFN4x4-32L θ_{JC} ---------- 20 °C/W
Power Dissipation, P_D @ T_A = 25 °C
WQFN4x4-32 L ---------- 1W

Recommended Operation Conditions

(Note 4)
Supply Input Voltage, VCC ---------- 2.8V to 3.8V
SDA, SCL Valid Operation Range ---------- 1.8V to 3.3V
Operating Voltage (SH_IN_Px, SH_IN_Nx) ---------- 5V to 26V
Operating Junction Temperature Range ---------- -40 °C to 105 °C
Operating Ambient Temperature Range ---------- -40 °C to 85 °C

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of *JEDEC 51-3* thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(VCC = 3.3V, T_A = 25℃, unless specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Multiplexer Settling						
Multiplexer Settling Error @100ns(1)	$V_{ERR\_DIFF\_OUT\_100}$	Rising edge of MUX_SEL when DIFF_OUT is within settling error	--	--	9.325	mV
Multiplexer Settling Error @300ns(1)	$V_{ERR\_DIFF\_OUT\_300}$		--	--	3.125	mV
Multiplexer Select						
MUX_SEL Timeout Reset(1)	$T_{MUX\_SEL\_TIMEOUT}$		--	--	45	us
MUX_SEL Valid Period(1)	$T_{MUX\_SEL\_H}$		0.185	--	11	us
MUX_SEL Supported Clock Frequency(1)	F_{MUX_SEL}		--	--	5.5	MHz
MUX_SEL Logic High Input(1)	$V_{IH\_MUX\_SEL}$		0.945	--	--	V
MUX_SEL Logic Low Input(1)	$V_{IL\_MUX\_SEL}$		--	--	0.405	V
SDA, SCL						
I^2C Input High Voltage(1)	V_{IH_I2C}		0.945	--	--	V
I^2C Input Low Voltage(1)	V_{IL_I2C}		--	--	0.405	V
BS_OK Function						
BS_OK Low Resistance	$R_{ON\_BS\_OK}$		--	9	20	Ω
BS_OK Comparator Input (BS_REF) Voltage Range	V_{BS_REF}		100	--	800	mV
BS_REF Input Leakage Current	$I_{LEAK\_BS\_REF}$	BS_REF input voltage = 800mV	--	--	100	nA
BS_OK Comparator Input (BS_IN) Divider Ratio(1)			--	1/32	--	
BS_OK Comparator Hysteresis(1)	$V_{HYS\_BS\_OK}$		--	20	--	mV
VCC POR Threshold for BS_OK Comparator	$V_{VCCPOR\_BS\_OK}$		2.6	--	2.8	V
VCC POR Hysteresis for BS_OK Comparator	$V_{VCCHYS\_BS\_OK}$		--	150	--	mV
BG_REF_OUT						
BG_REF_OUT Voltage	$V_{BG\_REF\_OUT}$	VCC=2.8V~3.8V	--	1.3	--	V
BG_REF_OUT Source Current	$I_{BG\_REF\_OUT\_MAX}$		--	40	--	uA
Shunt Monitor						
Shunt Offset Voltage(2)	$V_{SH\_IN\_OFS}$		-2	--	2	mV
Shunt Offset Voltage Drift(1)	$V_{SH\_IN\_OFSDFT}$	T_A = -40°C~105°C	-6	--	6	mV
Shunt CMRR(1)			80	--	--	dB
Shunt Current Gain Range	Shunt_Gain		2	--	24	
Shunt Current Gain Tolerance(2)			--	--	0.6	%

Electrical Characteristics

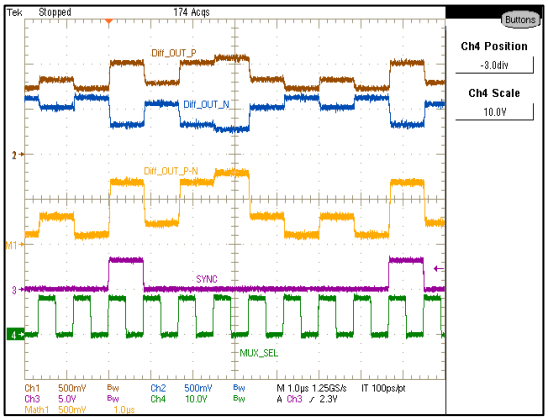
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Bus Input Voltage Monitor						
Bus Offset Voltage(2)	$V_{BS\_IN\_OFS}$		-2	--	2	mV
Bus Offset Voltage Drift(1)	$V_{BS\_IN\_OFSDFT}$	T_A = -40°C~105°C	-6	--	6	mV
Bus Voltage Dividing Ratio			1/64	--	1/4	
Bus Gain Tolerance(2)			-1	--	1	%
Enable						
Enable Tri-state Input Resistance	R_{ENABLE}		100	--	--	kΩ
Enable Logic High Input	V_{IH_ENABLE}		0.945	--	--	V
Enable Logic Low Input	V_{IL_ENABLE}		--	--	0.405	V
Standby or Limited Function to Full Functional Delay Time	T_{DLY}		--	--	40	us
SKIP						
SKIP Logic High Input	V_{IH_SKIP}		1.8	--	--	V
SKIP Logic Low Input	V_{IL_SKIP}		--	--	0.8	V
IMON						
IMON Input Leakage Current	I_{LEAK_IMON}	IMON input voltage = 800mV	--	--	100	nA
IMON Offset Voltage	V_{IMON_OFS}	IMON = 0V	-2	--	2	mV
RGND						
RGND Input Leakage Current	I_{LEAK_RGND}	RGND input voltage = 800mV	--	--	100	nA
RGND Offset Voltage	V_{RGND_OFS}	RGND = 0V	-2	--	2	mV
Address Setting						
ADDR0/1 Logic High Input	V_{IH_ADDR}		0.945	--	--	V
ADDR0/1 Logic Low Input	V_{IL_ADDR}		--	--	0.405	V
Input Leakage Current	I_{LEAK_ADDR}	ADDR0/1 input voltage = 3.3V	--	--	100	nA
VCC						
VCC Supply Current at Full Functional Mode	I_{VCC_FF}	ENABLE = 0V, default setting	--	2.8	--	mA
VCC Supply Current at Limited Function Mode	I_{VCC_LF}	ENABLE = floating	--	300	--	uA
VCC Supply Current at Standby Mode	I_{VCC_STBY}	ENABLE = 3.3V	--	250	--	uA
BS_IN						
BS_IN Current in Standby Mode	$I_{BS\_IN\_STBY}$	BS_IN Voltage = 26V	--	--	2	uA
BS_IN Current in Limited Mode	$I_{BS\_IN\_LF}$		--	--	100	uA
BS_IN Current in Full Functional Mode	$I_{BS\_IN\_FF}$		--	--	600	uA
BS_IN Current When VCC Floating	$I_{BS\_IN\_VCCFLT}$		--	--	2	uA
SH_IN						
SH_IN_N Current in Standby/Limited Mode	$I_{SH\_IN\_N\_STBY}$	BS_IN Voltage = 26V, SH_IN_P = SH_IN_N Voltage = 26V	--	--	2	uA
SH_IN_P Current in Standby Mode	$I_{SH\_IN\_P\_STBY}$		--	--	2	uA
SH_IN_P Current in Limited Mode	$I_{SH\_IN\_P\_LF}$		--	--	2	uA

Note: (1) Guaranteed by design
(2) Limit/tolerance may loosen for some high input voltage condition measurements due to tester limitation

uS5651P

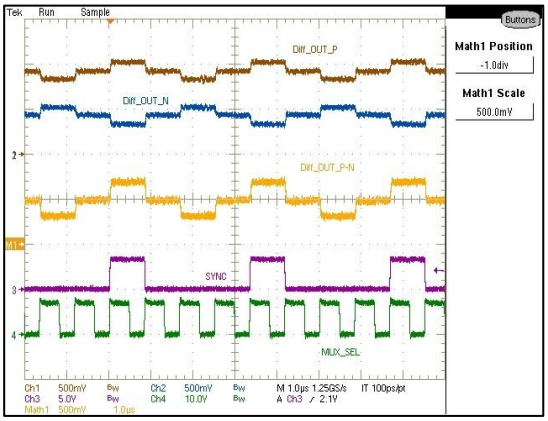
Typical Operation Characteristics

Default Operation (CH1 to CH4 are Active)



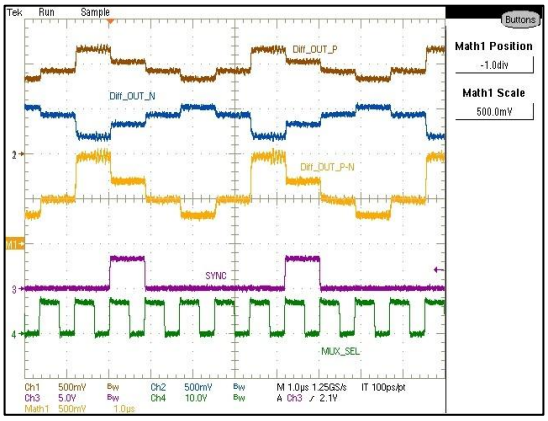
BS_INx=20V, SH_IN_Px to SH_IN_Nx=50mV, x=1~4, 0x10h=0x11h=12, 0x12h=0x13h=00, 0x20h=16, 0X21h=34, 0x22h=0x23h=00

Reduced Channel Operation (CH1&CH3 are Active)



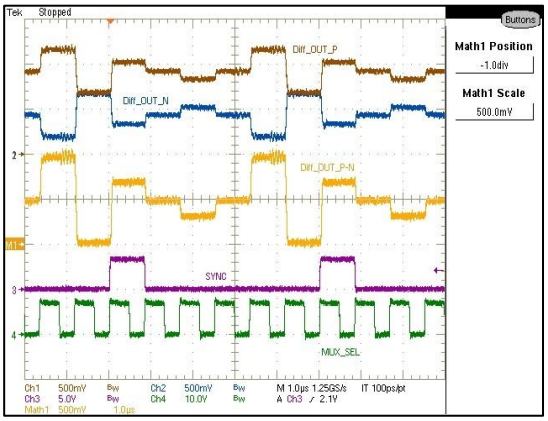
BS_INx=20V, SH_IN_Px to SH_IN_Nx=100mV, x=1,3, 0x10h=12, 0x12h=00, 0x20h=0x22h=16

Operation with CH1, CH3 and IMON2 Enabled



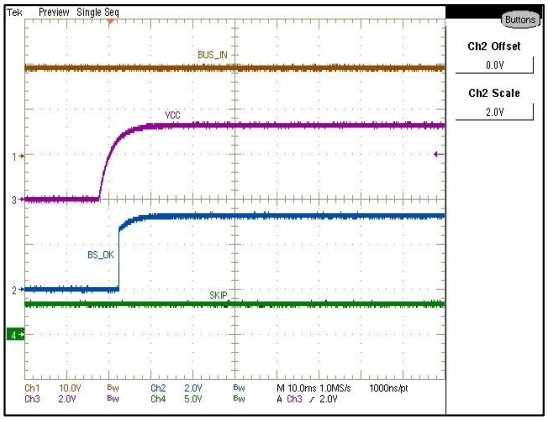
BS_INx=20V, SH_IN_Px to SH_IN_Nx=100mV, x=1,3, IMON_IN2=1V, 0x10h=12, 0x12h=00, 0x20h=0x22h=16

Operation with CH1, CH3, IMON1 and RGND Enabled



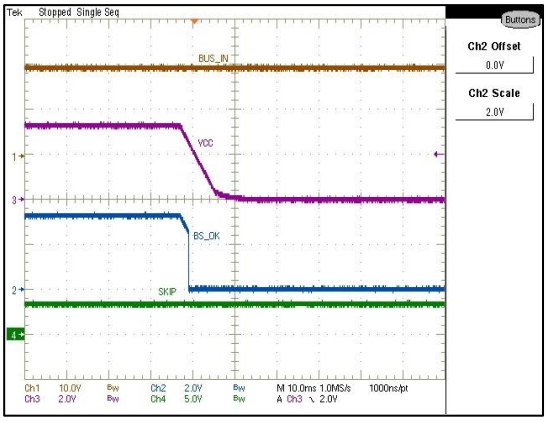
BS_INx=20V, SH_IN_Px to SH_IN_Nx=100mV, x=1,3, IMON_IN1=1V, RGND=0V, 0x10h=12, 0x12h=00, 0x20h=0x22h=16

VCC Power On



BS_INx=20V, x=1~4, Skip=H

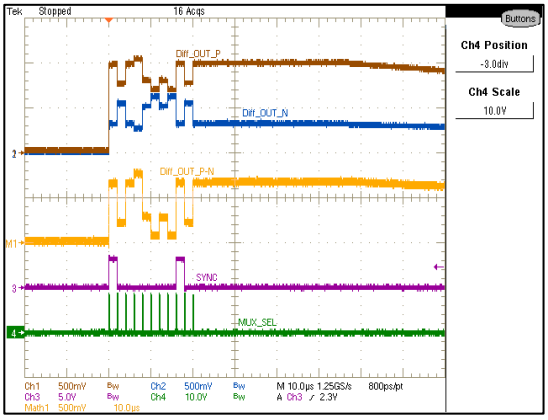
VCC Power Off



BS_INx=20V, x=1~4, Skip=H

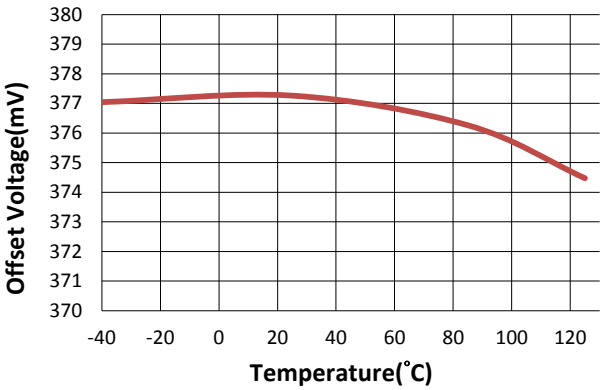
Typical Operation Characteristics

MUX_SEL Timeout

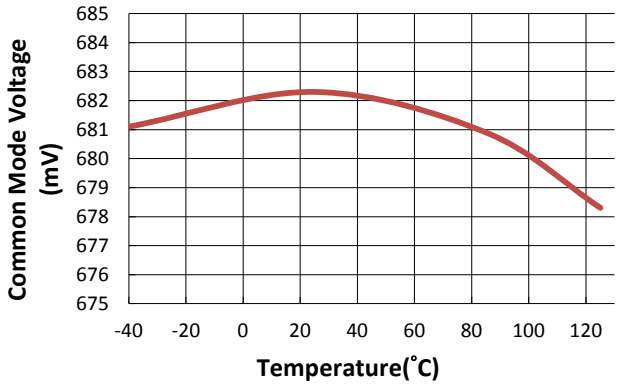


BS_INx=20V, SH_IN_Px to SH_IN_Nx=50mV, x=1~4,
0x10h=0x11h=12, 0x12h=0x13h=00, 0x20h=16, 0X21h=34, 0x22h=0x23h=00

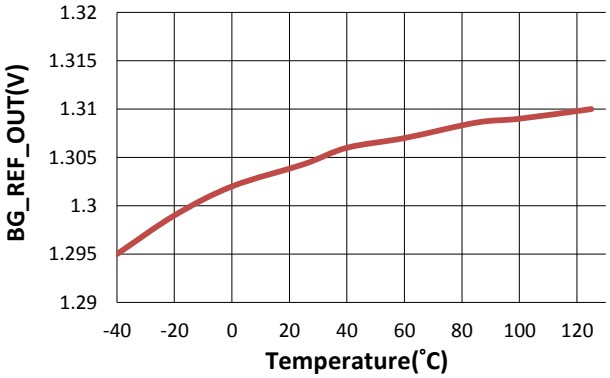
Offset Voltage vs. Temperature



Common Mode Voltage vs. Temperature



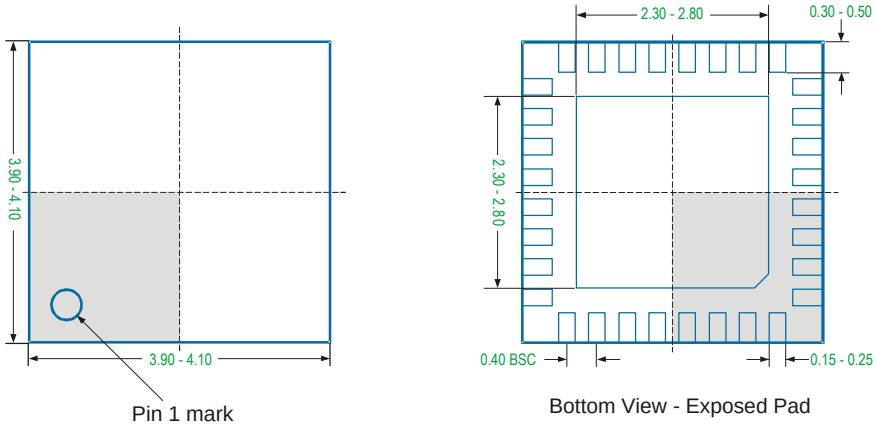
BG_REF_OUT Voltage vs. Temperature



uS5651P

Package Information

WQFN4x4-32L



Note

1. Package Outline Unit Description:
   MIN: Minimum dimension specified.
   NOM: Nominal. Provided as a general value.
   MAX: Maximum dimension specified.
   BSC: Basic. Represents theoretical exact dimension or dimension target.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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