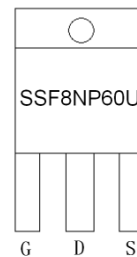
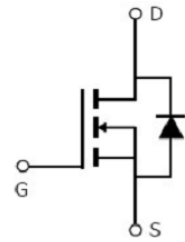


Main Product Characteristics:

V_{DSS}	600V
$R_{DS(on)}$	0.73Ω (typ.)
I_D	8A ①


TO-220

Marking and pin Assignment

Schematic diagram
Features and Benefits:

- High dv/dt and avalanche capabilities
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance


Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application (adaptor, lighting, charger etc.) and a wide variety of other applications.

Absolute max Rating:

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V	8 ①	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V	4.9 ①	
I_{DM}	Pulsed Drain Current ②	32	
P_D @TC = 25°C	Power Dissipation ③	62.5	W
	Linear Derating Factor	0.5	W/°C
V_{DS}	Drain-Source Voltage	600	V
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy @ L=22.5mH	45	mJ
I_{AS}	Avalanche Current @ L=22.5mH	2	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

Thermal Resistance

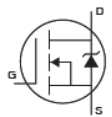
Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	2.0	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10\text{s}$) ④	—	62	$^{\circ}\text{C/W}$

Electrical Characterizes @ $T_A=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	600	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	0.73	0.85	Ω	$V_{GS}=10\text{V}, I_D = 1\text{A}$
		—	1.54	—		$T_J = 125^{\circ}\text{C}$
		—	0.78	1.0	Ω	$V_{GS}=10\text{V}, I_D = 2.8\text{A}$
		—	1.76	—		$T_J = 125^{\circ}\text{C}$
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
		—	2.5	—		$T_J = 125^{\circ}\text{C}$
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 600\text{V}, V_{GS} = 0\text{V}$
		—	—	50		$T_J = 125^{\circ}\text{C}$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 30\text{V}$
		—	—	-100		$V_{GS} = -30\text{V}$
Q_g	Total gate charge	—	12	—	nC	$I_D = 4.6\text{A},$ $V_{DS}=480\text{V},$ $V_{GS} = 10\text{V}$
Q_{gs}	Gate-to-Source charge	—	2.1	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	5.3	—		
$t_{d(on)}$	Turn-on delay time	—	9.8	—	ns	$V_{GS}=10\text{V}, V_{DS} = 300\text{V},$ $R_{GEN}=25\Omega, I_D = 4.6\text{A}$
t_r	Rise time	—	14	—		
$t_{d(off)}$	Turn-Off delay time	—	29	—		
t_f	Fall time	—	14	—		
C_{iss}	Input capacitance	—	344	—	pF	$V_{GS} = 0\text{V}$ $V_{DS} = 100\text{V}$ $f = 1\text{MHz}$
C_{oss}	Output capacitance	—	19	—		
C_{rss}	Reverse transfer capacitance	—	3.0	—		

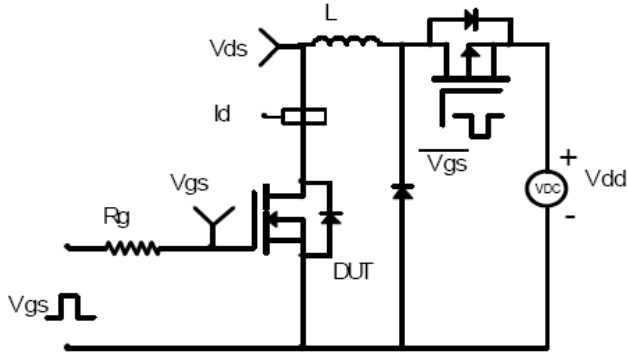
Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	8 ①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)	—	—	32	A	
V_{SD}	Diode Forward Voltage	—	0.83	1.2	V	$I_S=2.8\text{A}, V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	181	—	nS	$T_J = 25^{\circ}\text{C}, I_F = 4.6\text{A},$ $di/dt = 100\text{A}/\mu\text{s}$
Q_{rr}	Reverse Recovery Charge	—	1.0	—	μC	

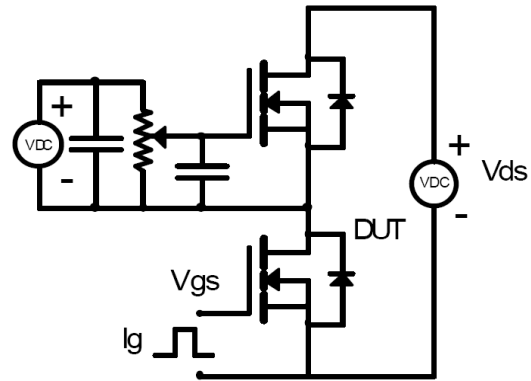


Test circuits and Waveforms

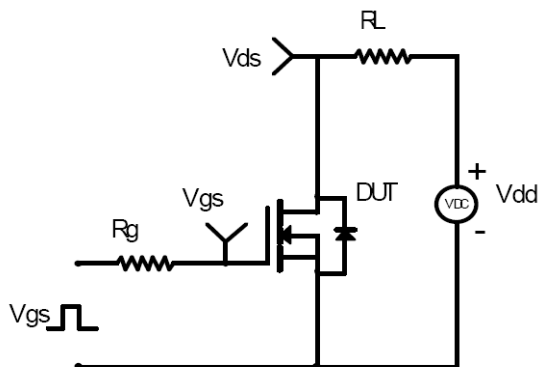
EAS Test Circuit:



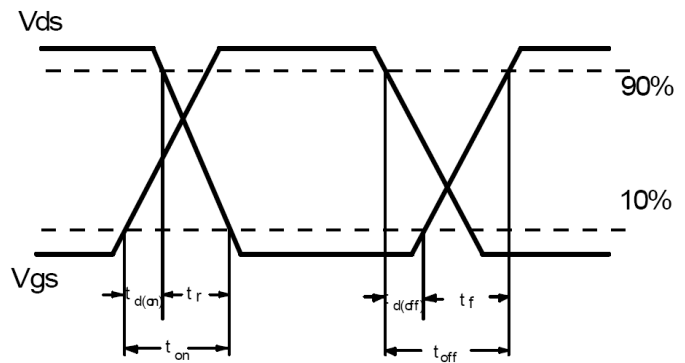
Gate charge test circuit:



Switching Time Test Circuit:



Switching Waveforms:



Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Typical electrical and thermal characteristics

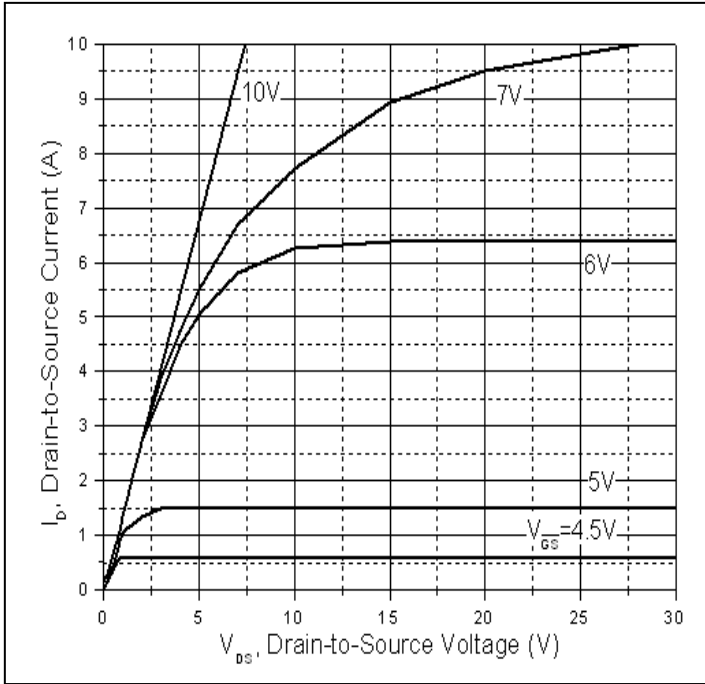


Figure 1: Typical Output Characteristics

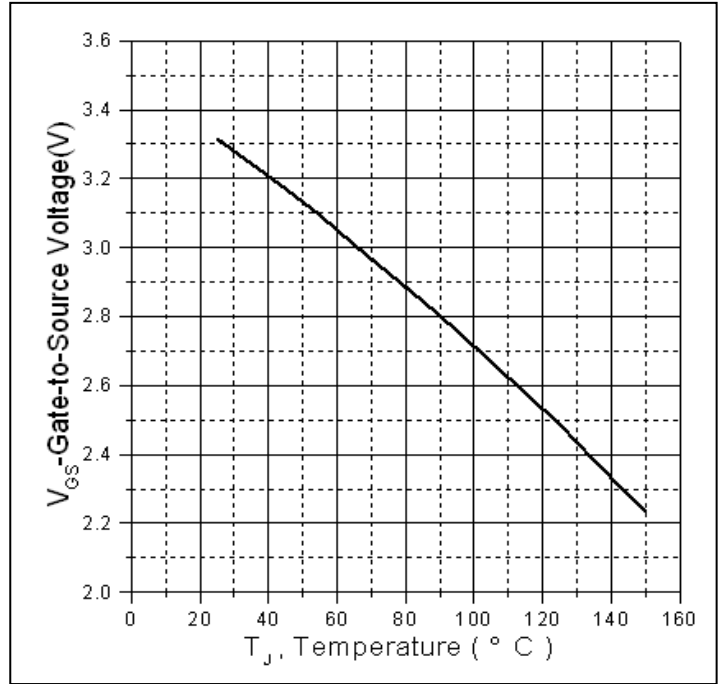


Figure 2: Gate to source cut-off voltage

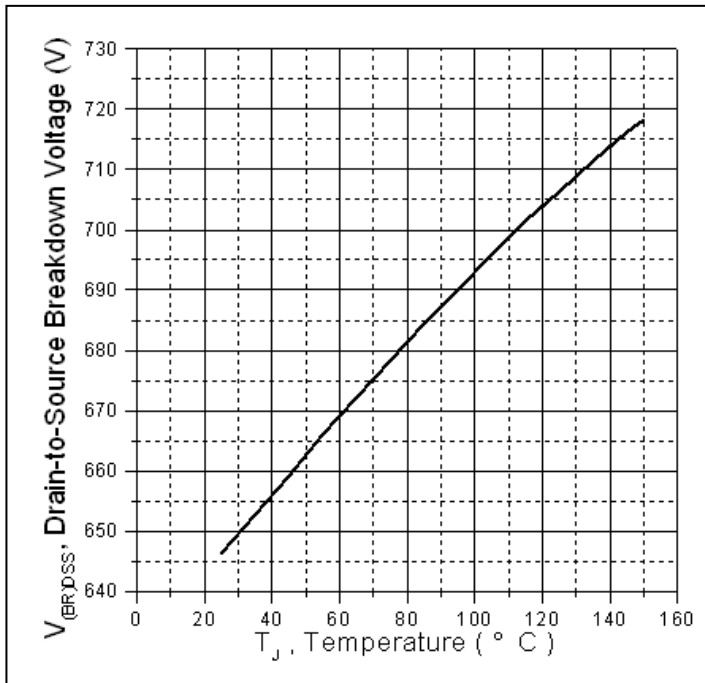


Figure 3: Drain-to-Source Breakdown Voltage Vs. Case Temperature

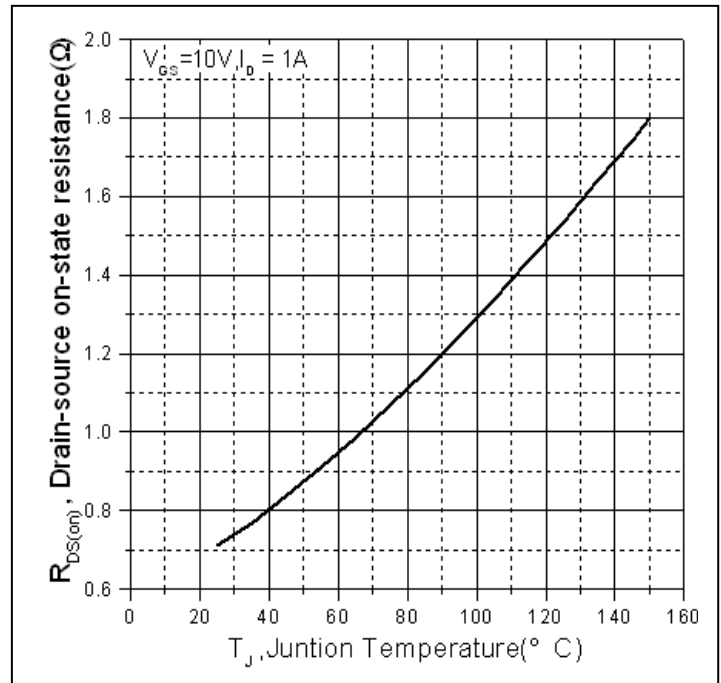


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

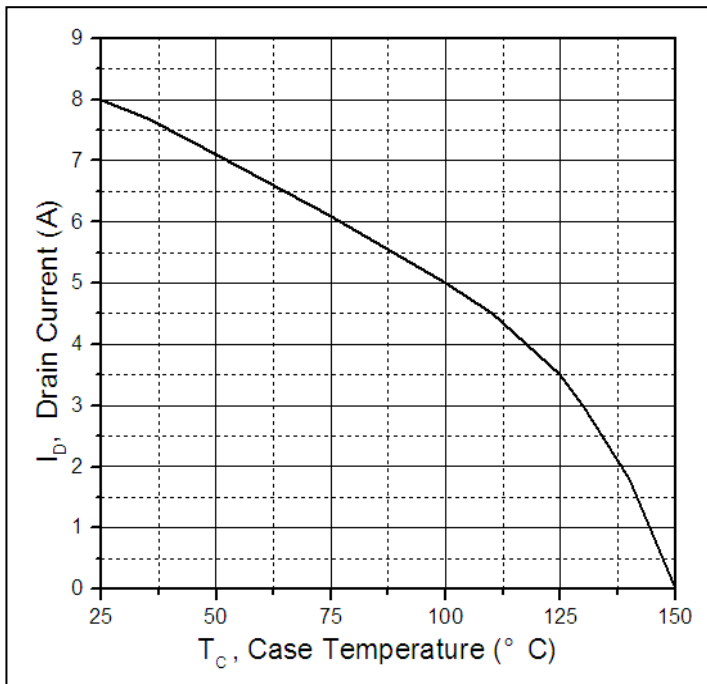


Figure 5. Maximum Drain Current Vs. Case Temperature

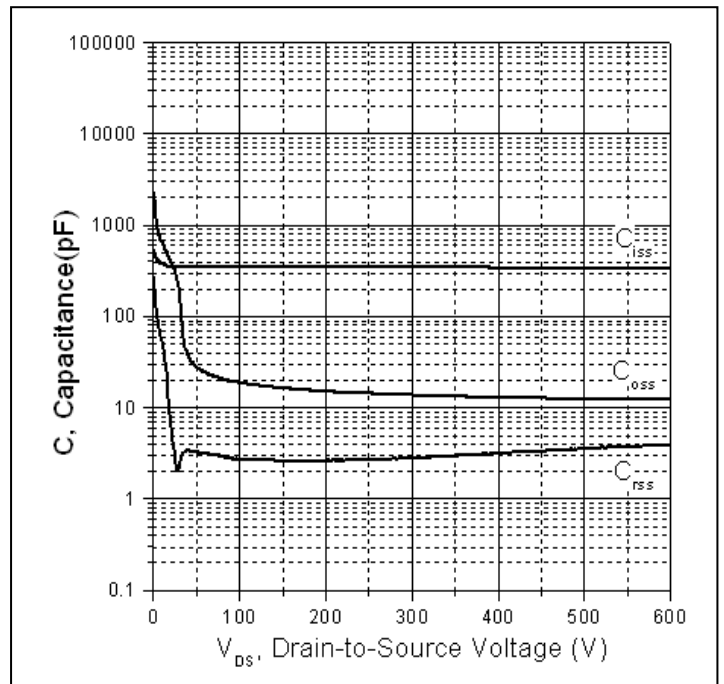


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

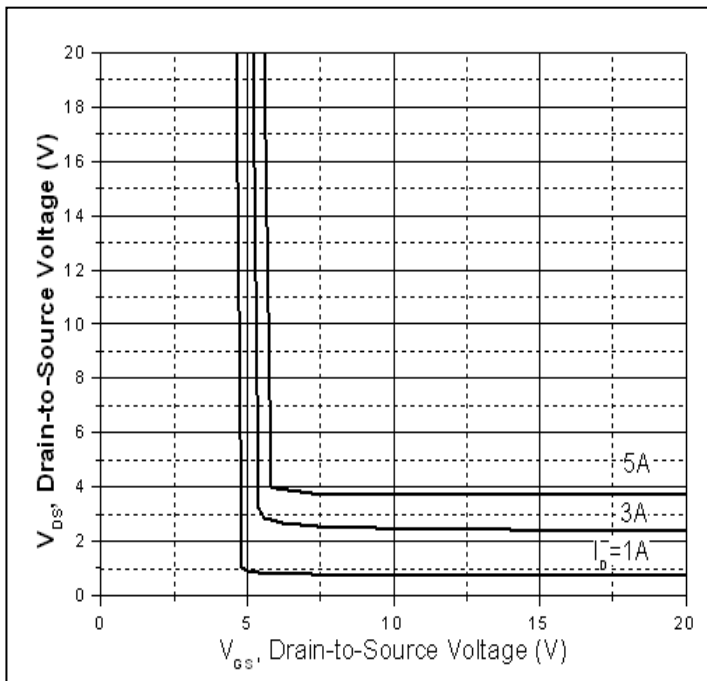


Figure7. Drain-to-Source Voltage Vs. Gate-to-Source Voltage

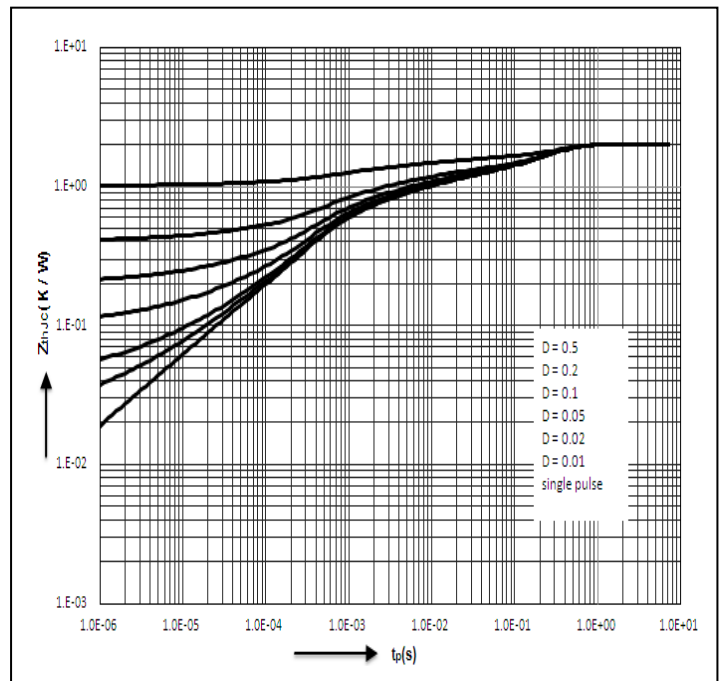
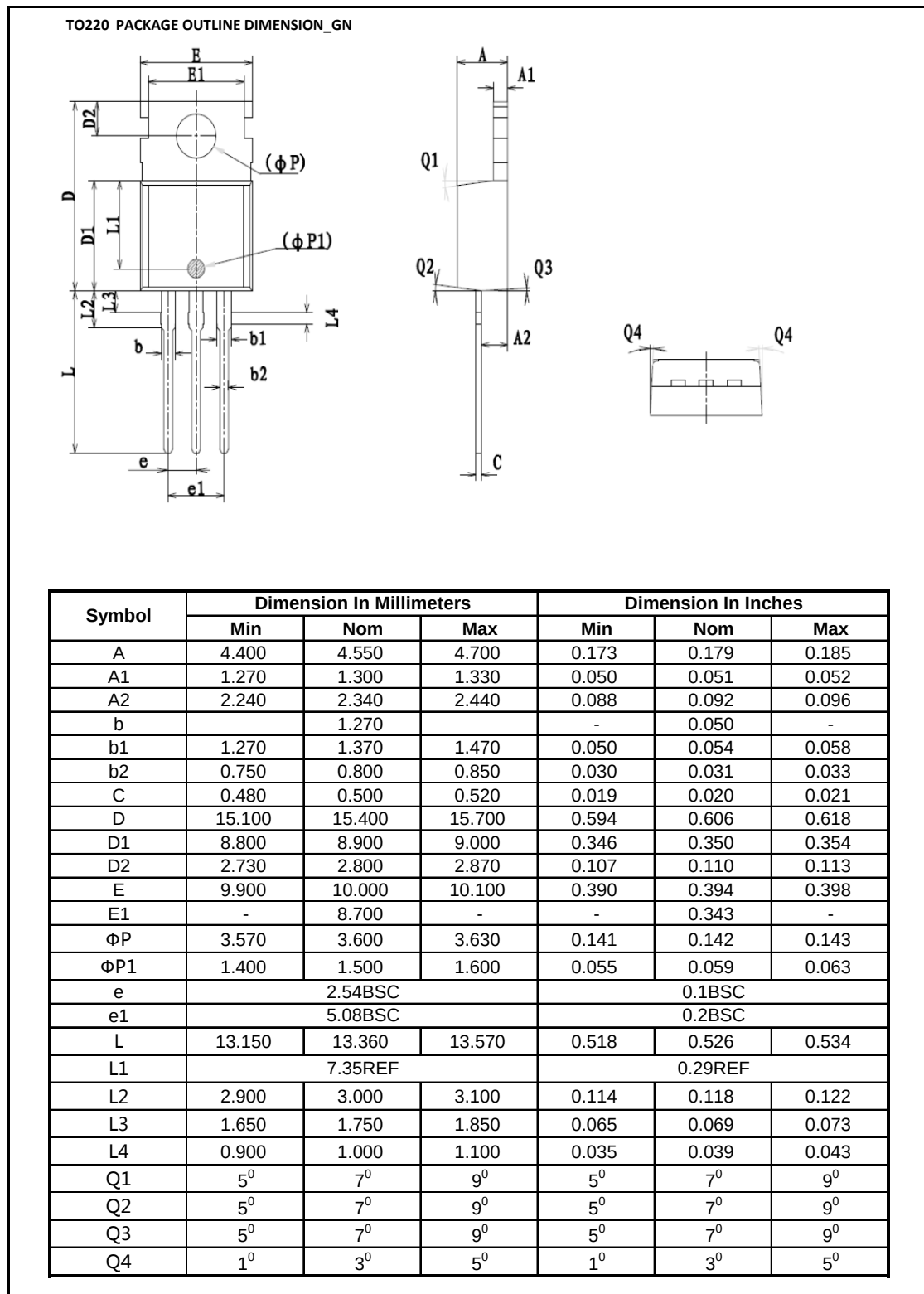


Figure8. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data:


Ordering and Marking Information**Device Marking: SSF8NP60U****Package (Available)****TO-220****Operating Temperature Range****C : -55 to 150 °C****Devices per Unit**

Package Type	Units/ Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-220	50	20	1000	6	6000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 150°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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