

Power Amplifier 37.0 - 40.0 GHz

Rev. V3

Features

- Linear Power Amplifier
- On-Chip Power Detector
- Output Power Adjust
- 27.0 dB Small Signal Gain
- +27.0 dBm P1dB Compression Point
- +38.0 dBm OIP3
- Lead-Free 7 mm 16-lead SMD Package
- RoHS* Compliant and 260°C Reflow Compatible

Description

The MAAP-011170 is a four stage 37-40 GHz packaged GaAs MMIC power amplifier that has a small signal gain of 27 dB with a +38 dBm Output Third Order Intercept. The amplifier contains an integrated, temperature compensated, on-chip power detector. This MMIC uses M/A-COM Technology Solutions' GaAs pHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity.

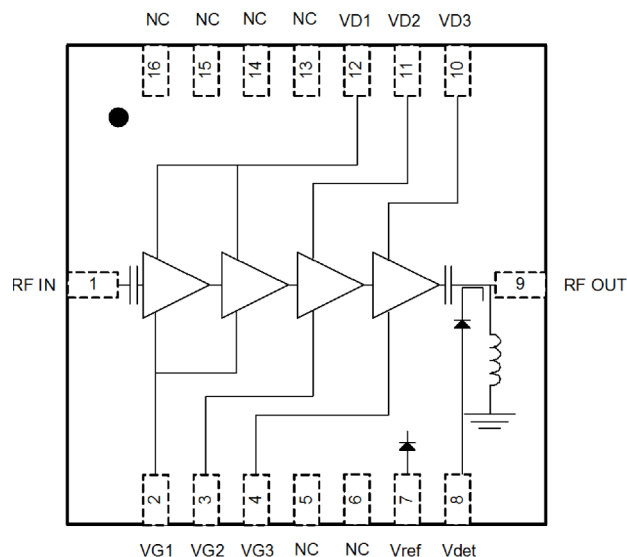
The device comes in a RoHS compliant 7x7mm Surface Mount Package offering excellent RF and thermal properties. This device has been designed for use in 38 GHz Point-to-Point Microwave Radio applications.

Ordering Information ¹

Part Number	Package
MAAP-011170	bulk quantity
MAAP-011170-TR1000	tape and reel
MAAP-011170-000SMB	evaluation module

1. Reference Application Note M513 for reel size information.

Functional Schematic



Pin Configuration ²

Pin No.	Function	Pin No.	Function
1	RF Input	9	RF Output
2	Gate Bias, Stage 1	10	Drain Bias, Stage 3
3	Gate Bias, Stage 2	11	Drain Bias, Stage 2
4	Gate Bias, Stage 3	12	Drain Bias, Stage 1
5-6	Not Connected	13,14	Not Connected
7	Detector Reference Output	15	Not Connected
8	Detector Output	16	Not Connected

2. The exposed pad centered on the package bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EC.

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Electrical Specifications: 37-40 GHz (Ambient Temperature T = 25°C)

Parameter	Units	Min.	Typ.	Max.
Input Return Loss (S11)	dB	-	12.0	-
Output Return Loss (S22)	dB	-	12.0	-
Small Signal Gain (S21)	dB	21	27.0	30
Gain Flatness (ΔS_{21})	dB	-	+/-1.0	-
Reverse isolation (S12)	dB	-	50	-
Output Power for 1dB Compression Point (P1dB)	dBm	-	27.0	-
PSat	dBm		28.0	
Output IMD3 with Pout (scl) = 14 dBm	dBc	43.0	48.0	-
Output IP3	dBm	35.5	+38.0	-
Vdiff @ Pout (scl) = 0 dBm	mV		25.0	
Vdiff @ Pout (scl) = 25 dBm	mV		1500	
Vdiff slope @ Pout (scl) = 0 dBm	mV/dB		5.0	
Drain Bias Voltage (Vd)	VDC	-	4.0	4.0
Gate Bias Voltage (Vg)	VDC	-1.0	-0.3	-0.1
Supply Current (Id1) (Vd=4.0V, Vg=-0.3V)	mA	-	1000	1200

Absolute Maximum Ratings

Parameter	Absolute Max.
Supply Voltage (Vd)	+4.3 V
Gate Bias Voltage (Vg)	-1.5 V < Vg < 0 V
Input Power (Pin)	15 dBm
Max. Operating Junction/Channel Temp	175°C
Continuous Power Dissipation (Pdiss) at 85 °C	7.0 W

Parameter	Absolute Max.
Operating Temperature (Ta)	-40°C to +85°C
Storage Temperature (Tstg)	-65°C to +150°C
Mounting Temperature	260°C
ESD Min. - Human Body Model (HBM)	Class 1A
MSL Level	MSL3

- Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.
- For saturated performance it recommended that the sum of (2*Vdd + abs (Vgg)) <9V

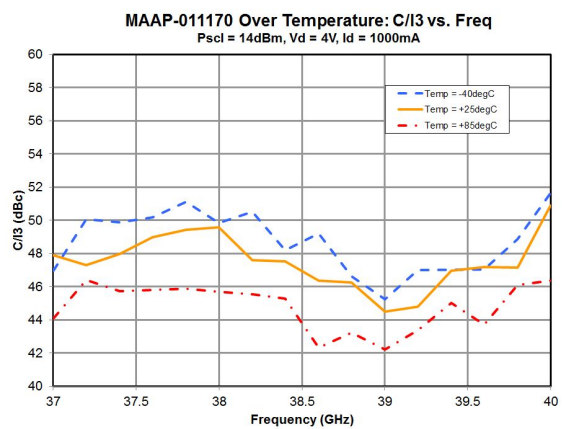
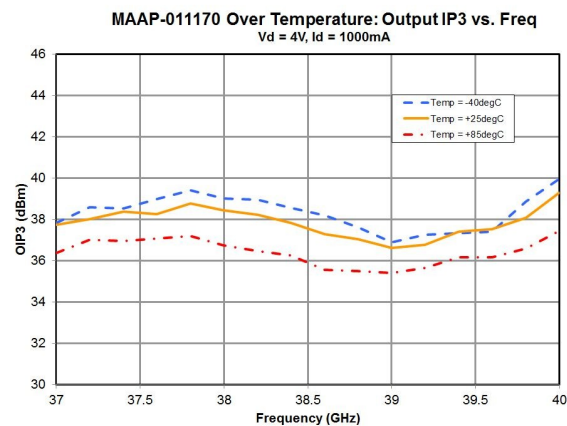
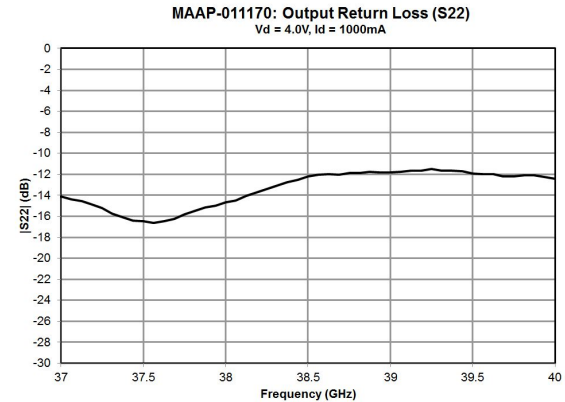
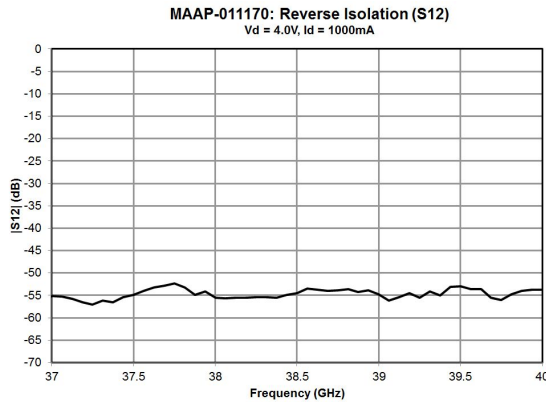
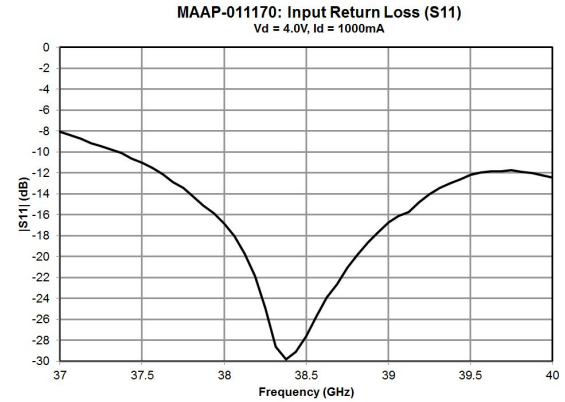
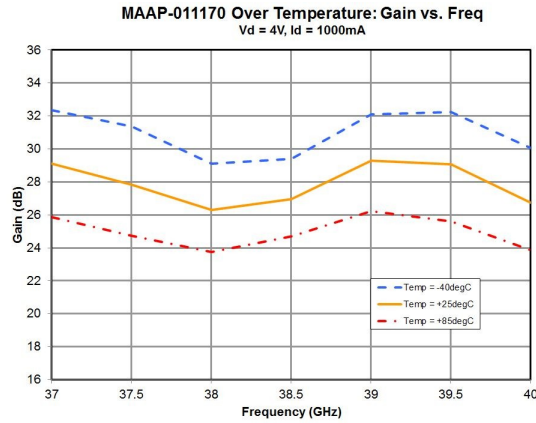
Thermal and Reliability Information: Tbase = 85°C , Vd = 4V

Parameter	Test Conditions		Rating
Thermal Resistance	Id = 1A	Pdiss = 4W	12°C/W
Channel Temperature	Id = 1A	Pdiss = 4W	135°C
Median Lifetime	Id = 1A	Pdiss = 4W	4 E+7 Hours

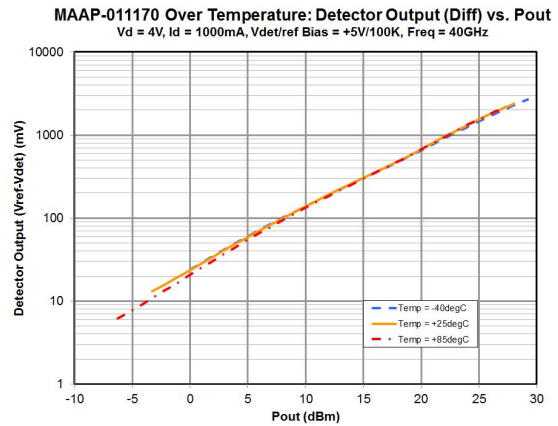
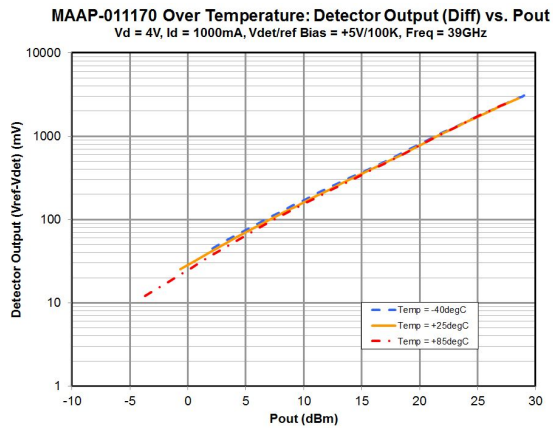
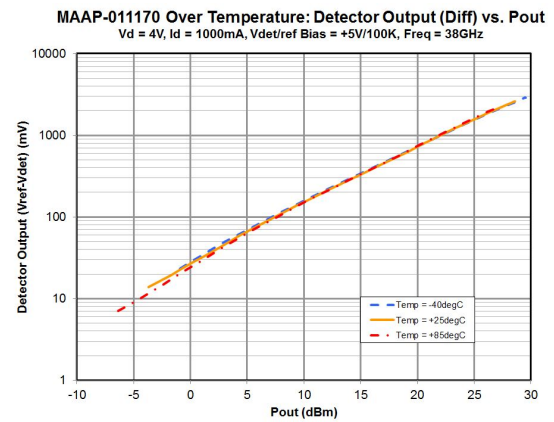
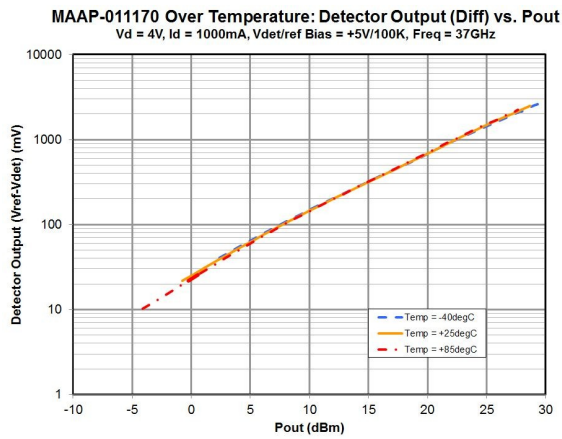
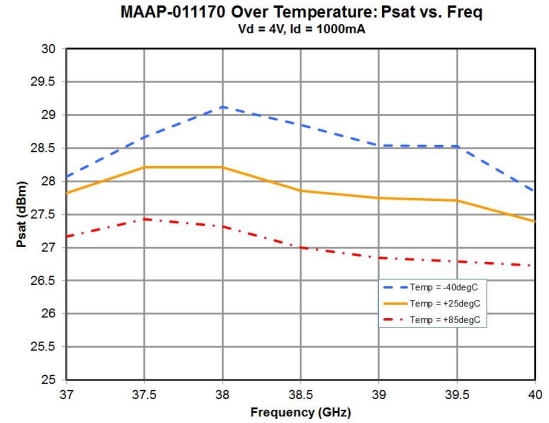
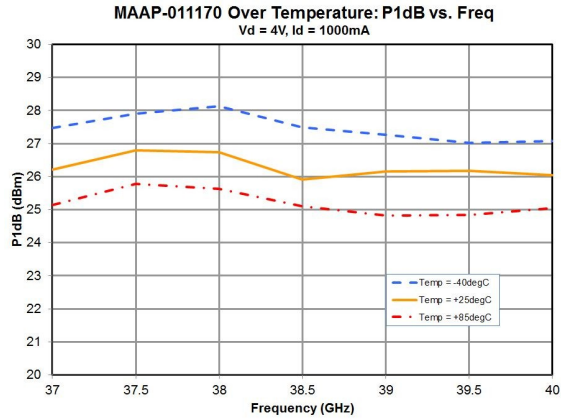
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Typical Performance Curves



Typical Performance Curves (cont.)



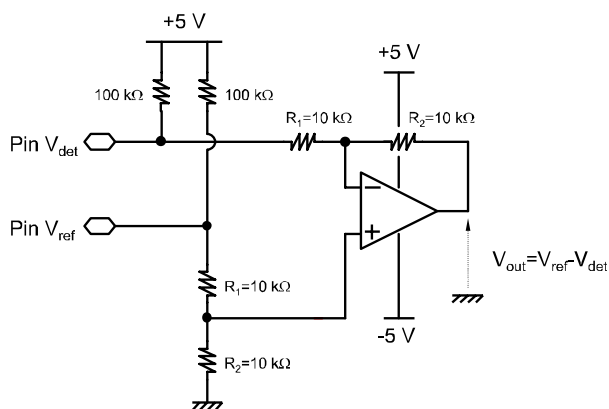
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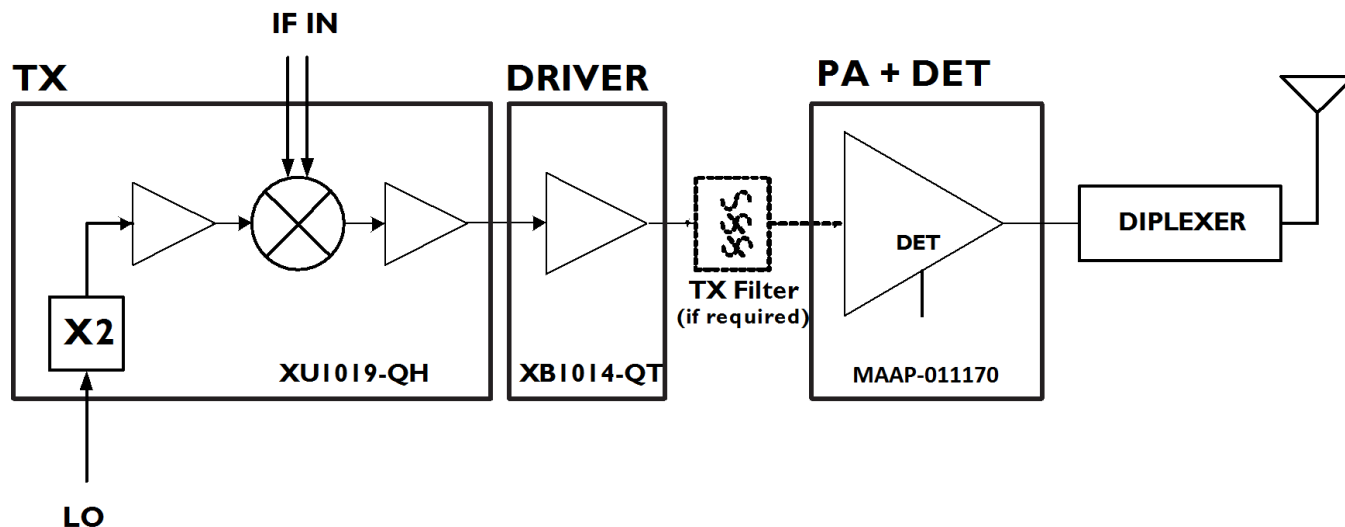
App Note [1] Biasing - It is recommended to bias the amplifier with $V_d=4.0$ V and $I_d=1000$ mA. It is also recommended to use active biasing to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.3 V. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Bias Arrangement - Each DC pin ($V_{d1,2,3}$ and $V_{g1,2,3}$) needs to have DC bypass capacitance (10 nF/ 1 μ F) as close to the package as possible.

App Note [3] Power Detector - As shown in the schematic below, the power detector is implemented by providing $+5$ V bias and measuring the difference in output voltage with standard op-amp in a differential mode configuration.



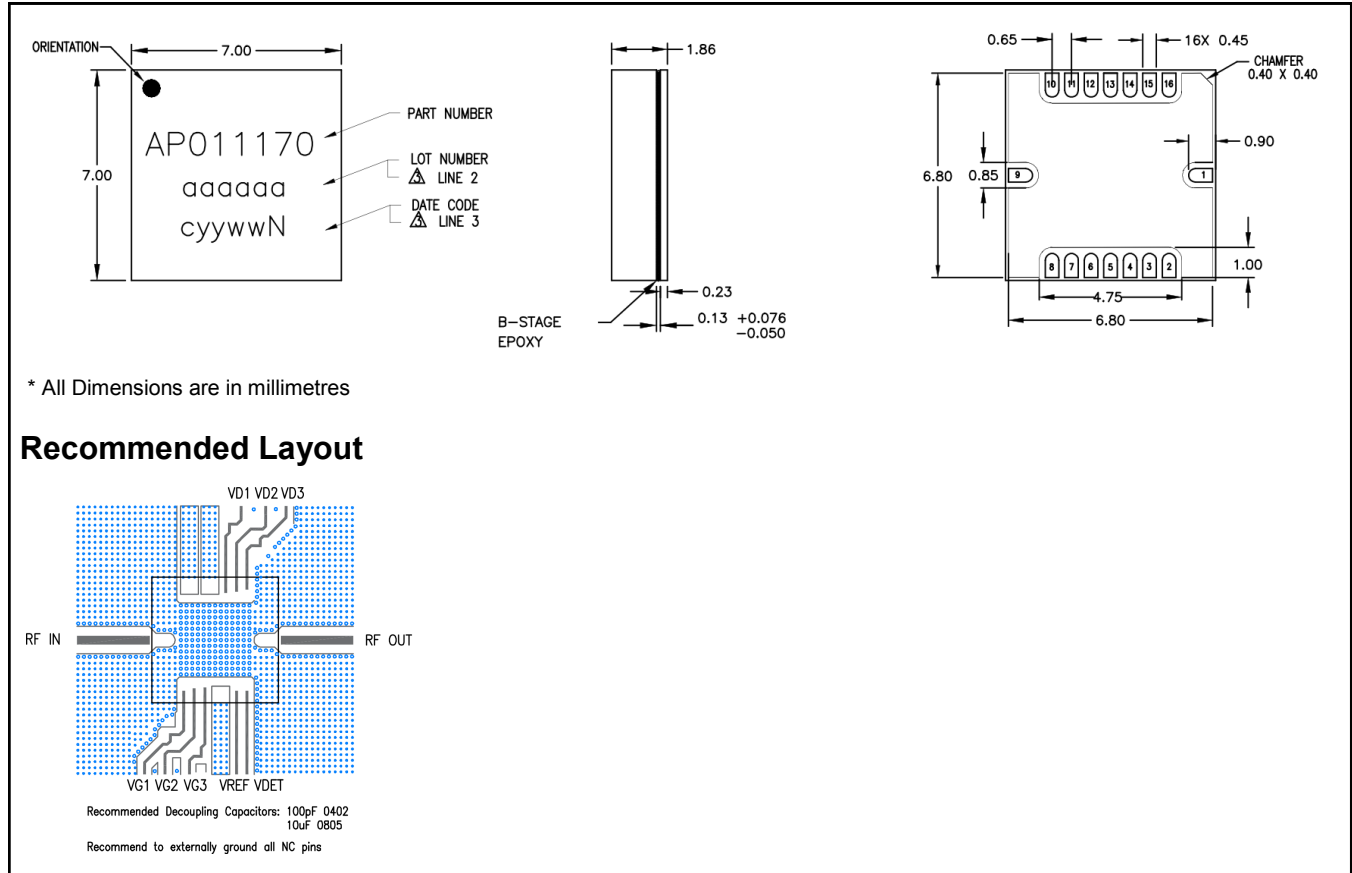
Typical Application



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Lead-Free 7 mm 16-Lead SMD[†]



[†] Reference Application Note S2083 for lead-free solder reflow recommendations.
Plating is matte gold/nickel over copper.