# MAAP-015035

## Power Amplifier, 12 W
## 8.5 - 11.5 GHz

Rev. V1

### Features

- 12 W X-Band Power Amplifier
- 36 dB Small Signal Gain
- 41 dBm Saturated Pulsed Output Power
- 40% Power Added Efficiency
- On Chip Gate Bias Circuit
- 100% On-wafer DC & RF Power Tested
- 100% Visual Inspection to MIL-STD-833
- Bare Die

### Description

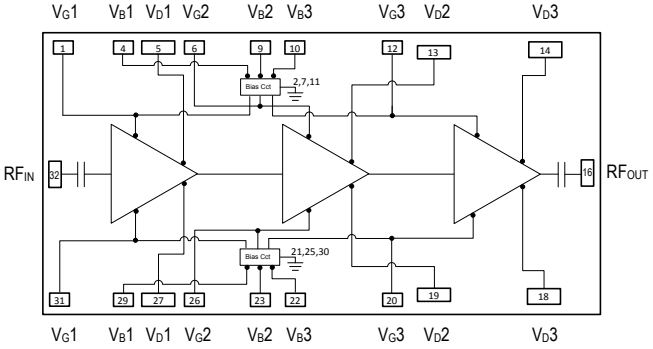
The MAAP-015035 is a three stage 8.5 - 11.5 GHz GaAs pHEMT MMIC power amplifier capable of achieving a saturated pulsed output power of 41 dBm and a small signal gain of 36 dB. The gate terminals of the power amplifier can be biased directly using a direct gate voltage or using an on chip gate bias circuit. The chip includes surface passivation for added protection and reliability

This device is well suited for communication and radar applications.

### Ordering Information

| Part Number | Package |
|---|---|
| MAAP-015035-DIE | Die in Vacuum release gel pack |

### Functional Schematic




### Pad Configuration

| Pad No. | Function | Pad No. | Function |
|---|---|---|---|
| 1 | $V_G1$ | 17 | GND |
| 2 | Bias Circuit GND | 18 | $V_D3$ |
| 3 | GND | 19 | $V_D2$ |
| 4 | $V_B1$ | 20 | $V_G3$ |
| 5 | $V_D1$ | 21 | Bias Circuit GND |
| 6 | $V_G2$ | 22 | $V_B3$ |
| 7 | Bias Circuit GND | 23 | $V_B2$ |
| 8 | GND | 24 | GND |
| 9 | $V_B2$ | 25 | Bias Circuit GND |
| 10 | $V_B3$ | 26 | $V_G2$ |
| 11 | Bias Circuit GND | 27 | $V_D1$ |
| 12 | $V_G3$ | 28 | $V_B1$ |
| 13 | $V_D2$ | 29 | GND |
| 14 | $V_D3$ | 30 | Bias Circuit GND |
| 15 | GND | 31 | $V_G1$ |
| 16 | $RF_{OUT}$ | 32 | $RF_{IN}$ |

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.





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## Power Amplifier, 12 W
## 8.5 - 11.5 GHz



### Electrical Specifications:

**Freq. = 8.5 - 11.5 GHz, $T_A$ = +25°C, Duty Cycle = 5%, Pulse = 5µs, $P_{IN}$ = 8 dBm, $V_G$ = -0.9V**

| Parameter | Units | Min. | Typ. | Max. |
|---|---|---|---|---|
| Gain (Large Signal) | dB | 32 | 33 | — |
| Gain | dB | — | 36 | — |
| Gain Flatness | dB | — | 1 | — |
| Input Return Loss | dB | — | 12 | — |
| Output Return Loss | dB | — | 10 | — |
| Saturated Output Power | dBm | 40 | 41 | — |
| Power Added Efficiency<br>8.5 - 9.0 GHz<br>9.0 - 10.0 GHz<br>10.0 - 11.5 GHz | % | — | <br>35<br>40<br>40 | — |
| Drain Bias Voltage | V | — | 8.0 | — |
| Drain Current | A | 2.5 | 3 | 5.5 |

### Absolute Maximum Ratings[1,2]

| Parameter | Absolute Maximum |
|---|---|
| Input Power | +12 dBm |
| Drain Voltage | +8.5 V |
| Gate Voltage | -2.0 V < $V_G$ < -0.7 V |
| Bias Voltage | -6.5 V < $V_B$ < -4.5 V |
| Drain Current | 6 A |
| Gate Current (Direct Bias) | 30 mA |
| Gate Current (On Chip Bias) | 180 mA |
| Operating Temperature | -40°C to +85°C |
| Junction Temperature[3,4] | +175°C |

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.
3. Operating at nominal conditions with $T_J \leq$ +175°C will ensure MTTF > 1 x $10^6$ hours.
4. Junction Temperature ($T_J$) = $T_A$ + Θjc * (V * I)
   Typical thermal resistance (Θjc) = 6.8°C/W.
   a) For $T_A$ = 25°C,
   $T_J$ = 175°C @ 8 V, 2.76 A
   b) For $T_A$ = 85°C,
   $T_J$ = 175°C @ 8 V, 1.65 A

### Handling Procedures

Please observe the following precautions to avoid damage:

### Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.





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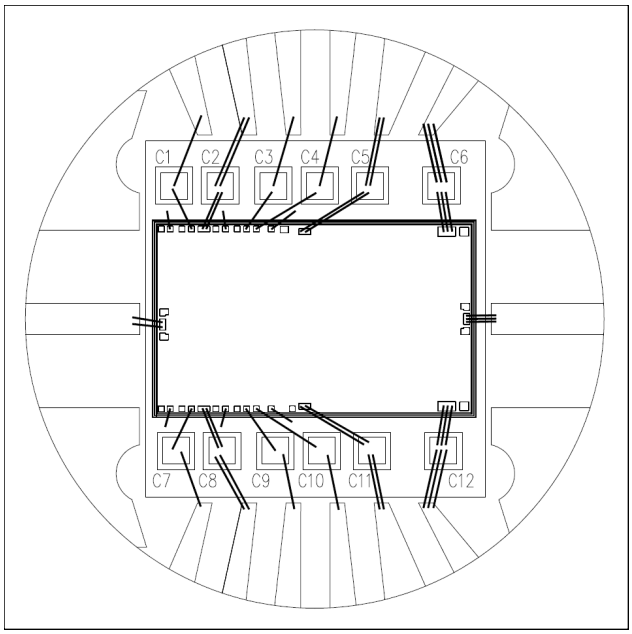
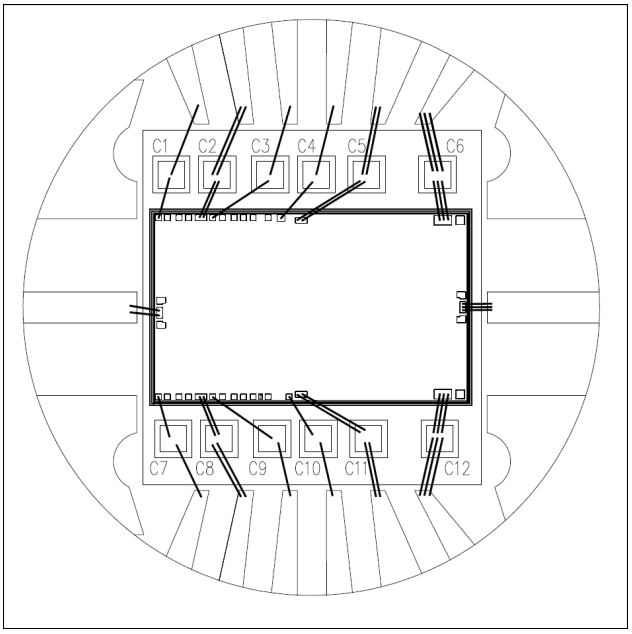
## Bonding Diagram - On Chip Bias[5]

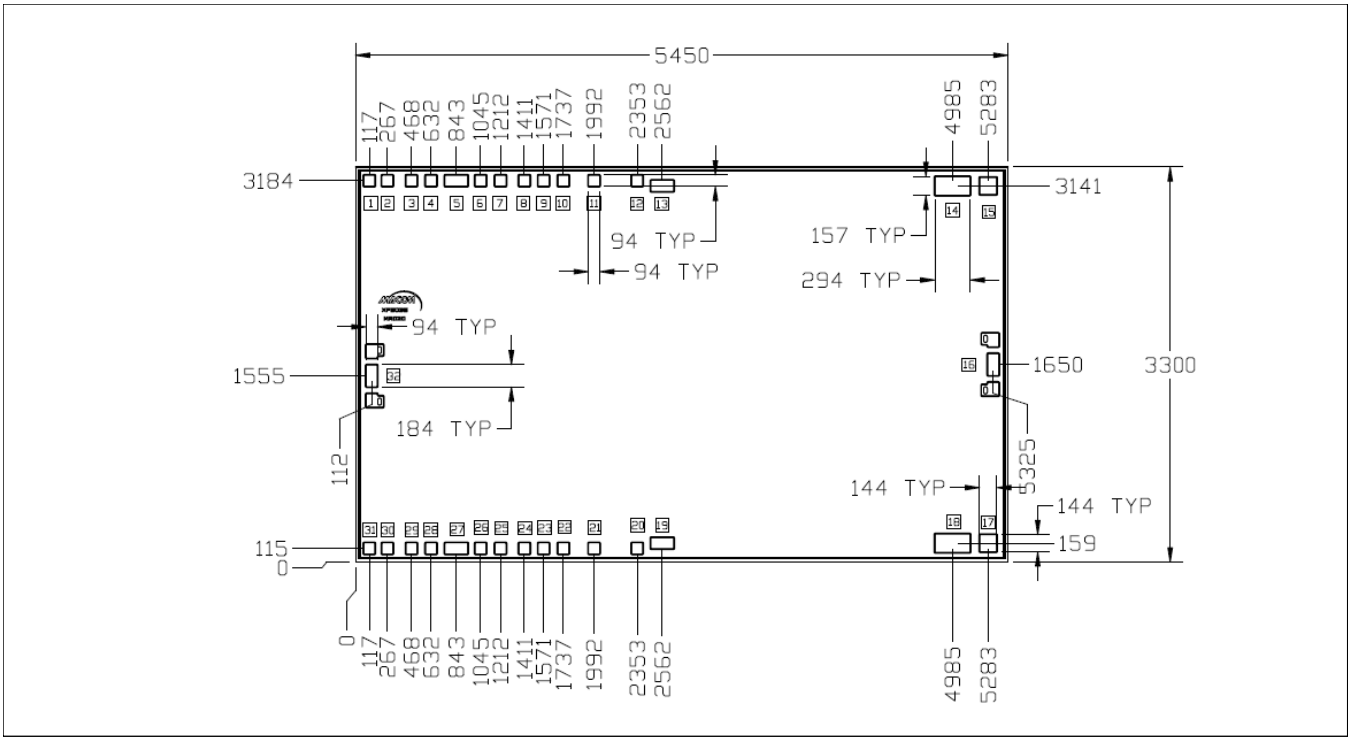



## Bonding Diagram - Direct Gate Bias[5]




5. Components C1 - C12 are all 100 pF chips.

## *MMIC Bare Die*





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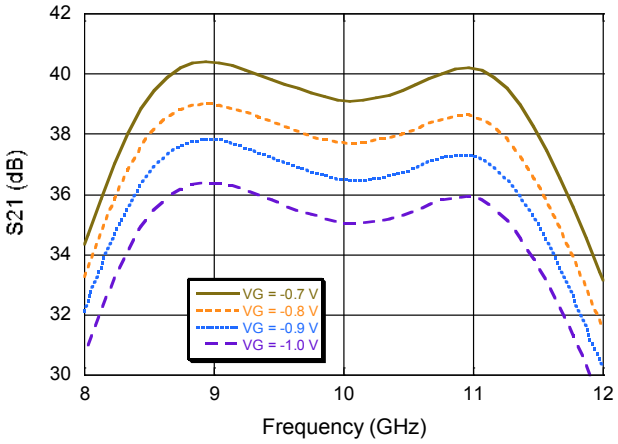
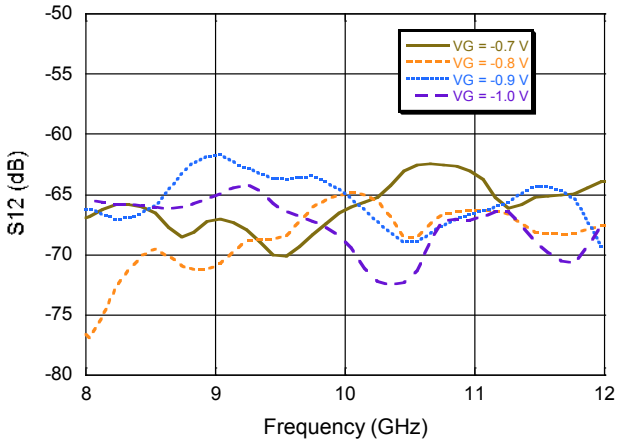
## Typical Pulsed Performance Curves over Gate Voltage

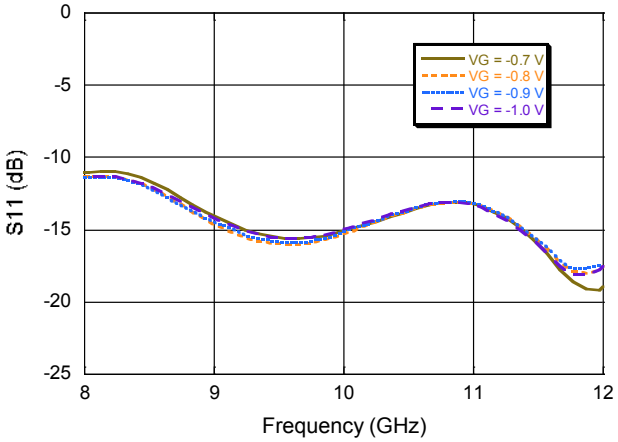
***Gain vs. Frequency***



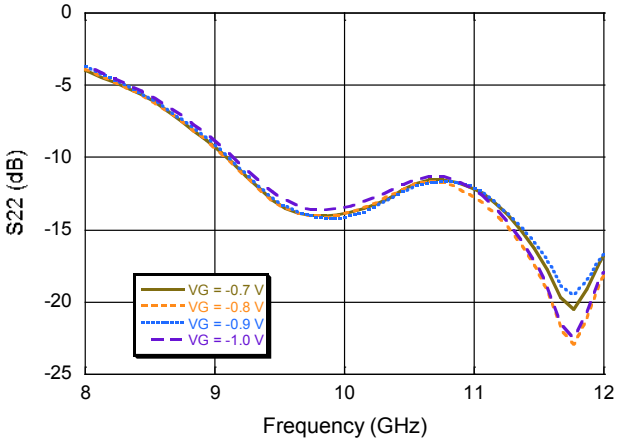

***Reverse Isolation vs. Frequency***




***Input Return Loss vs. Frequency***

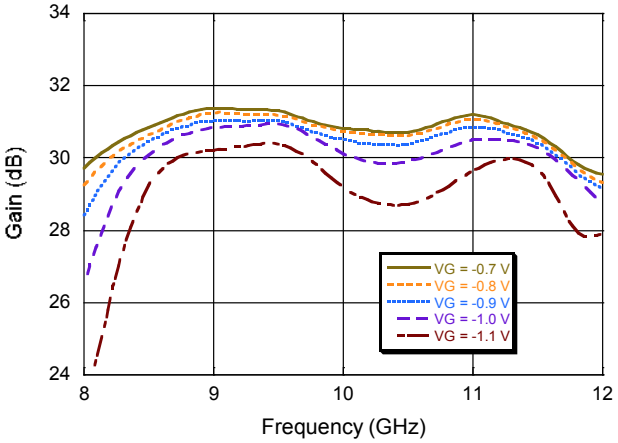



***Output Return Loss vs. Frequency***

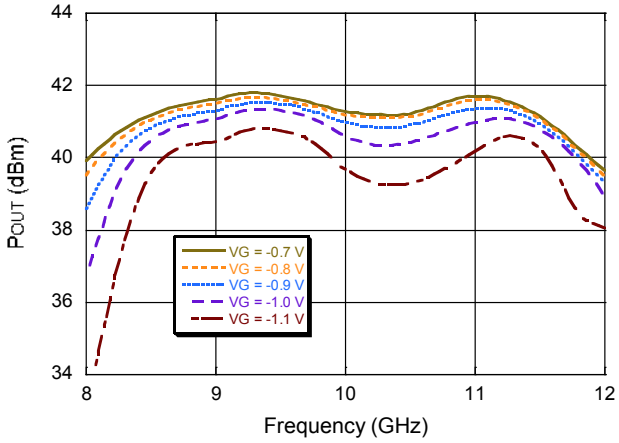


## Typical Pulsed Performance Curves over Gate Voltage: $P_{IN}$ = 10 dBm

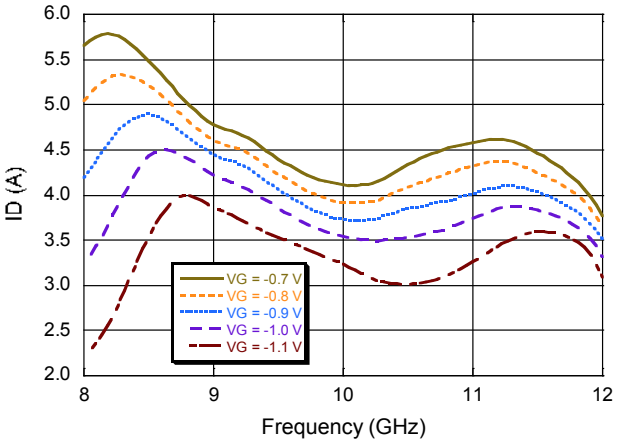
***Gain vs. Frequency***



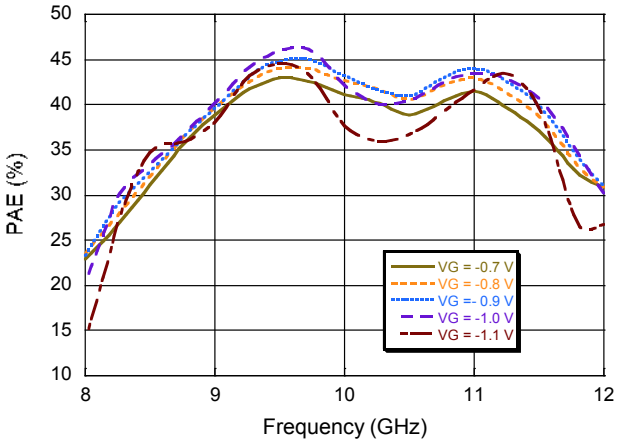

***Output Power vs. Frequency***




***Drain Current vs. Frequency***




***PAE vs. Frequency***





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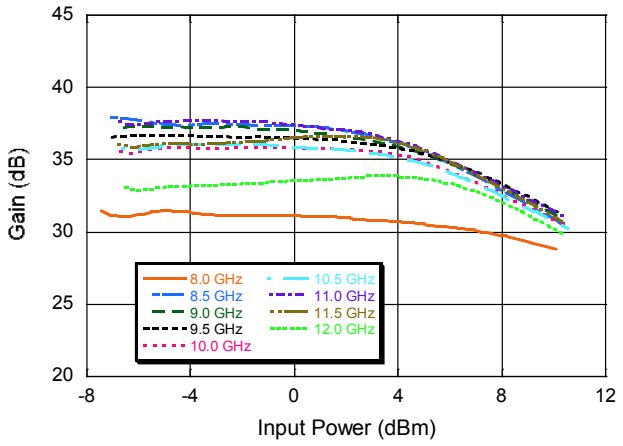
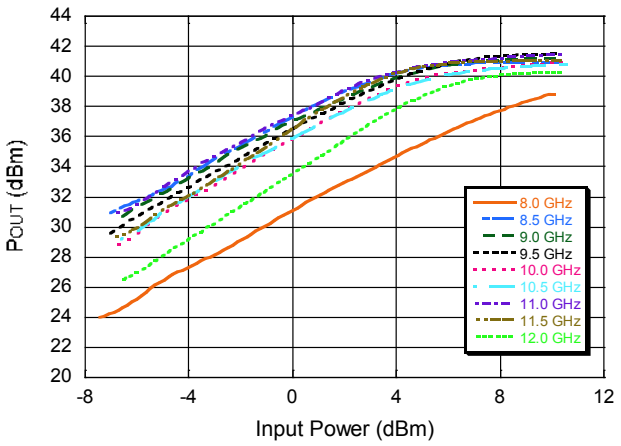
## Typical Pulsed Performance Curves over Frequency: VG = -0.9 V

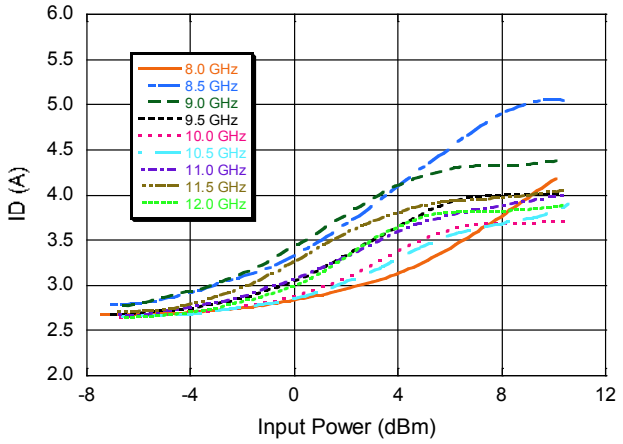
***Gain vs. Input Power***



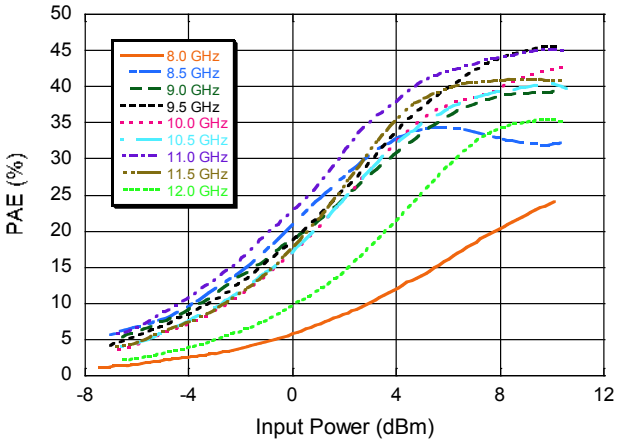

***Output Power vs. Input Power***



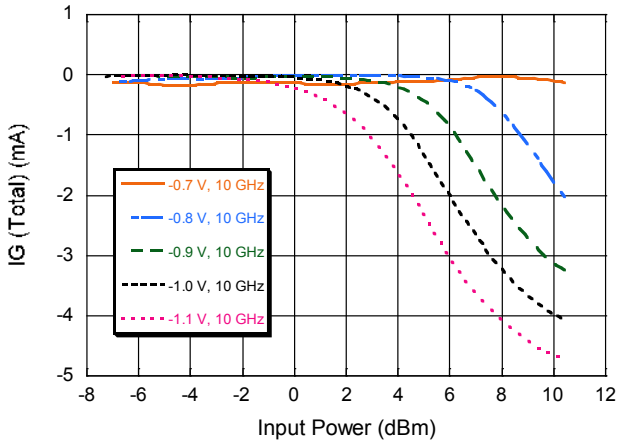

***Drain Current vs. Input Power***




***PAE vs. Input Power***

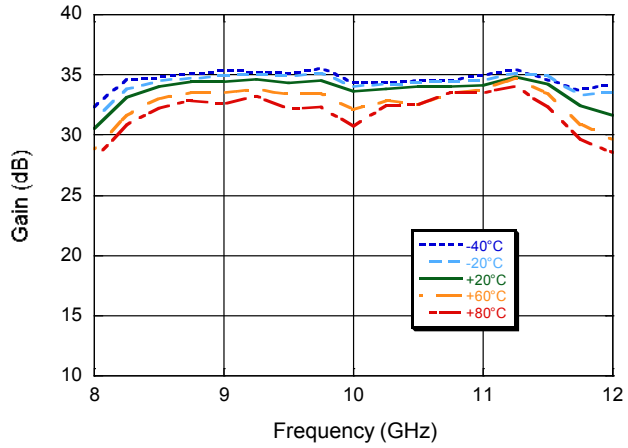



***Gate Current vs. Input Power***

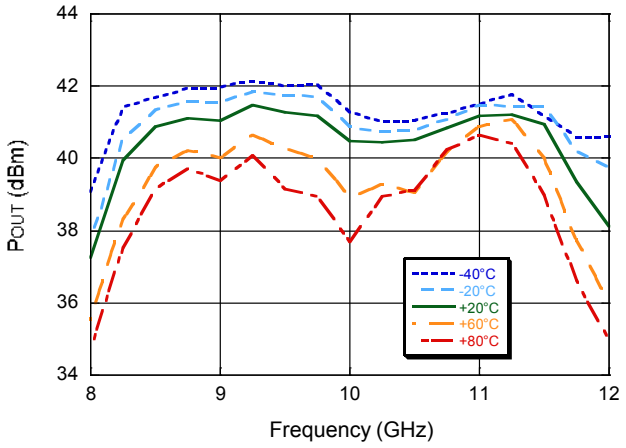


## Typical Pulsed Performance Curves over Temperature: VG = -0.9 V, $P_{IN}$ = 7 dBm

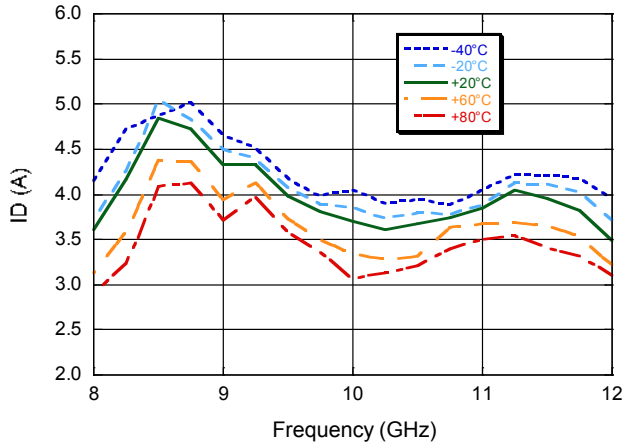
***Gain vs. Frequency***



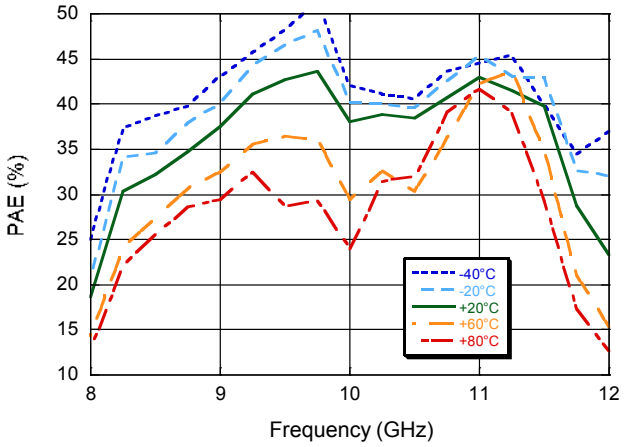

***Output Power vs. Frequency***




***Drain Current vs. Frequency***

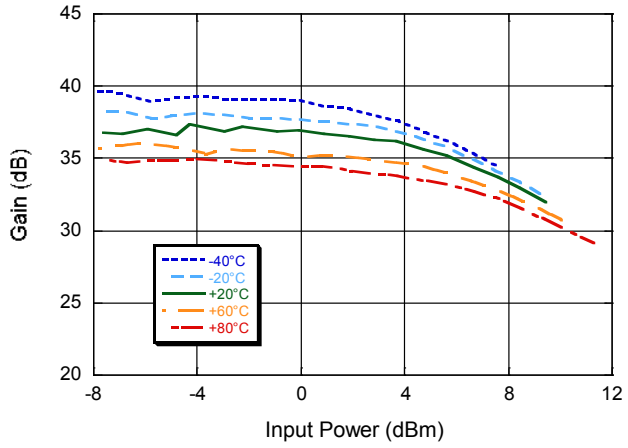



***PAE vs. Frequency***

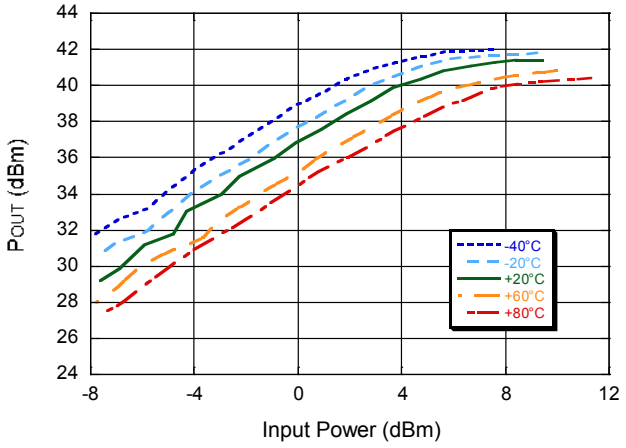


## Typical Pulsed Performance Curves over Temperature at 9 GHz, VG = -0.9 V

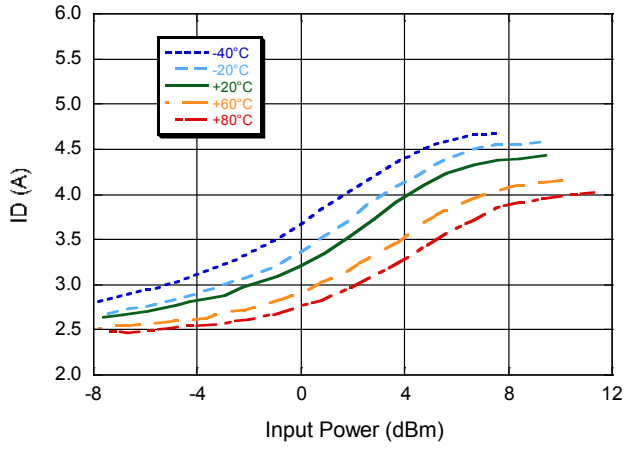
***Gain vs. Input Power***



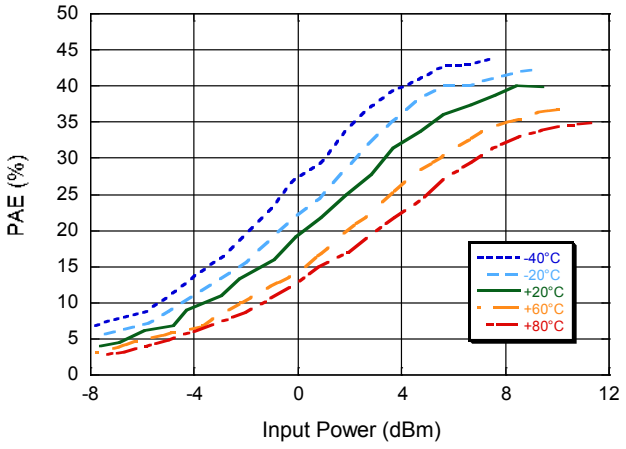

***Output Power vs. Input Power***




***Drain Current vs. Input Power***

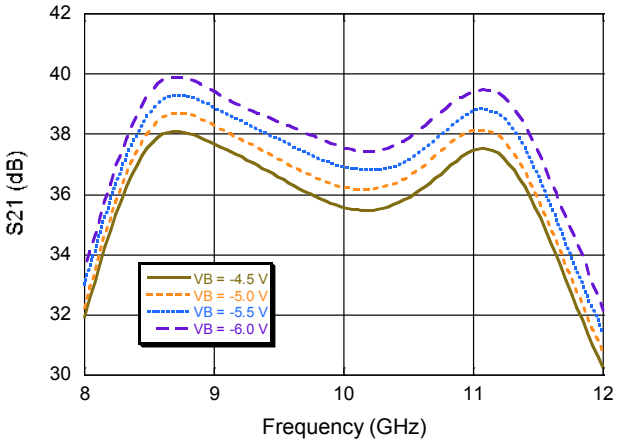



***PAE vs. Input Power***

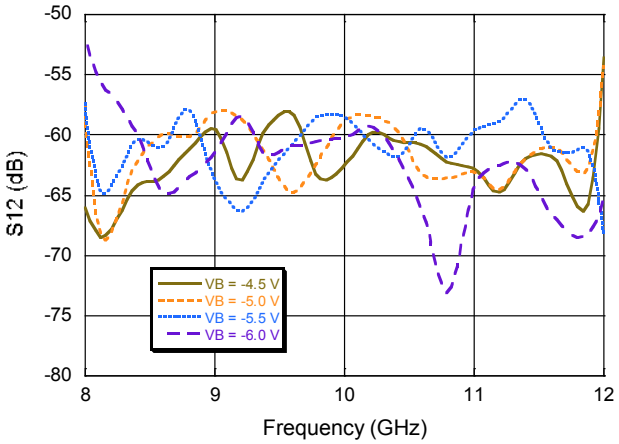


## Typical Pulsed Performance Curves over Bias Circuit Voltage

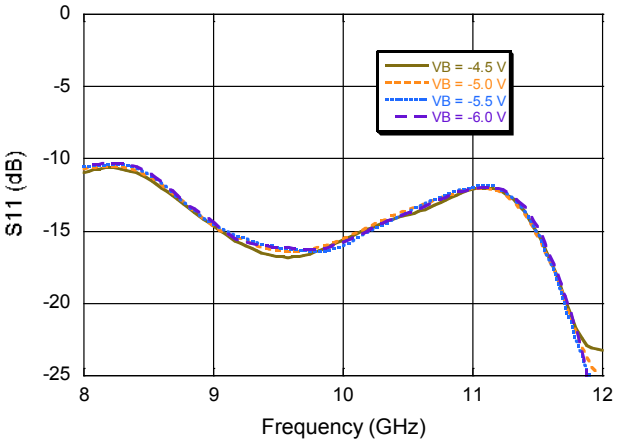
***Gain vs. Frequency***



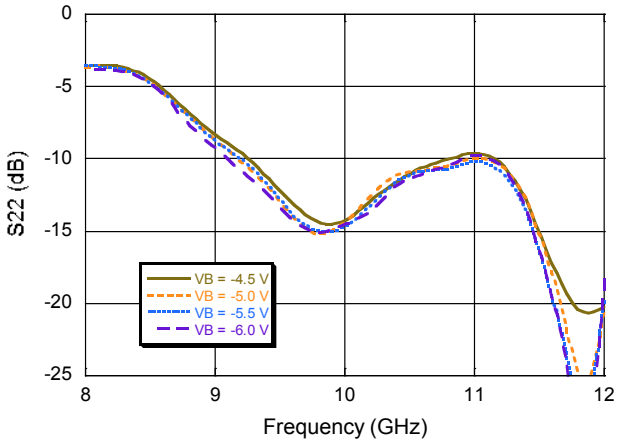

***Reverse Isolation vs. Frequency***




***Input Return Loss vs. Frequency***




***Output Return Loss vs. Frequency***





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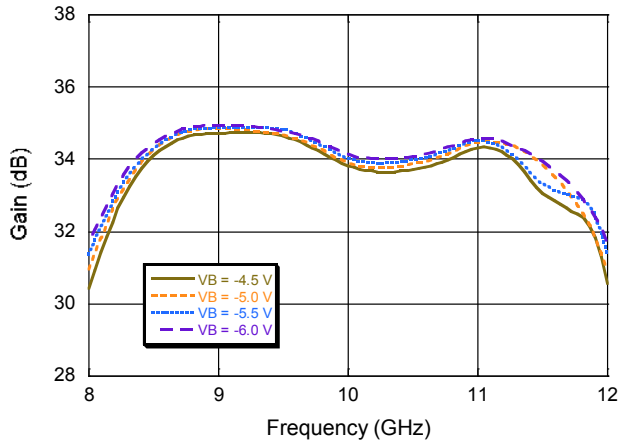
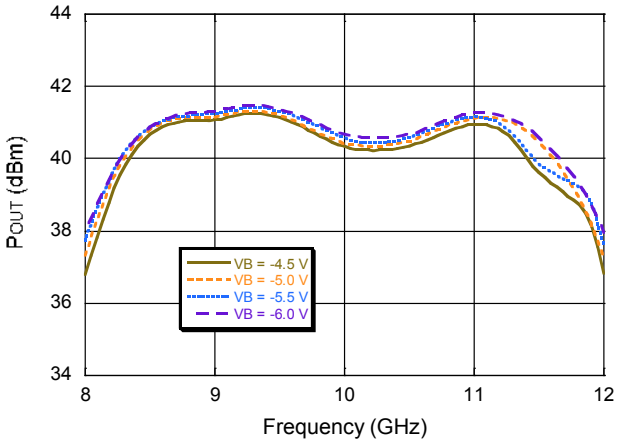
## Typical Pulsed Performance Curves over Bias Circuit Voltage : $P_{IN}$ = 7 dBm

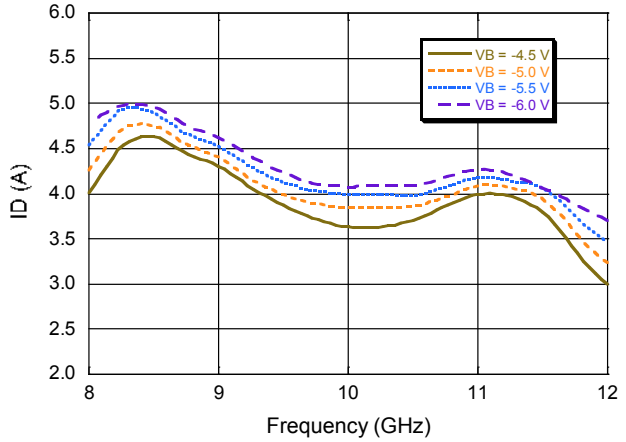
***Gain vs. Frequency***



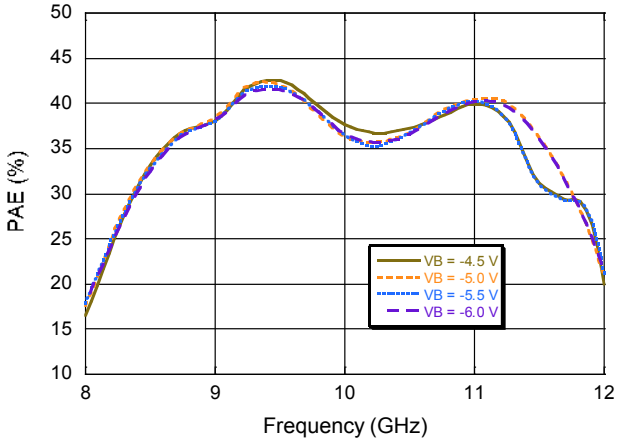

***Output Power vs. Frequency***




***Drain Current vs. Frequency***

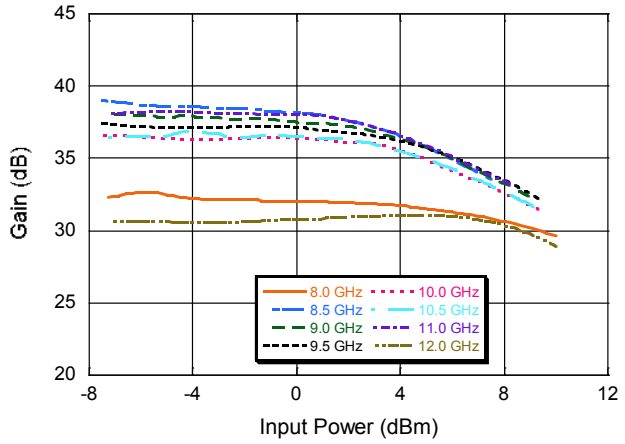



***PAE vs. Frequency***

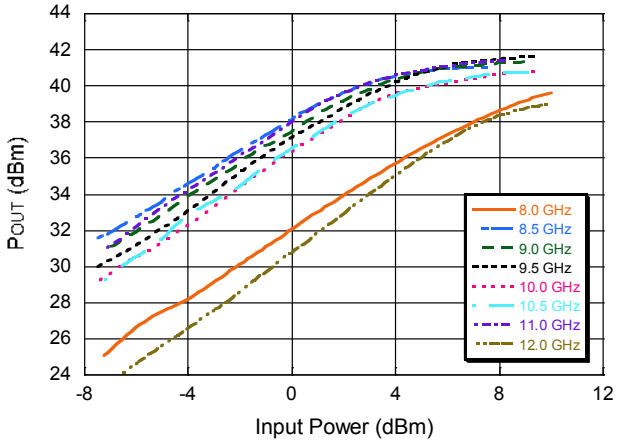


## Typical Pulsed Performance Curves over Frequency (Bias Circuit Voltage = -5 V)

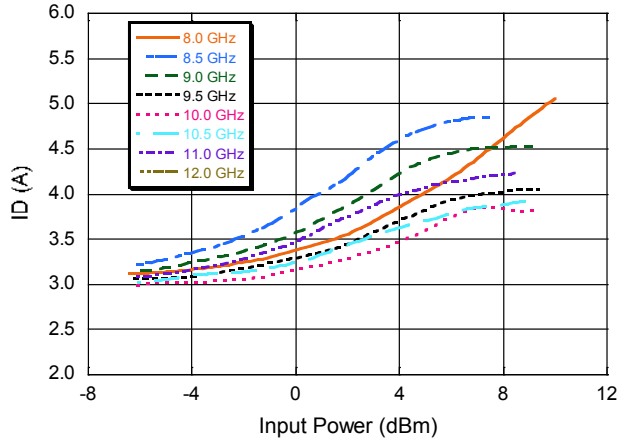
***Gain vs. Input Power***



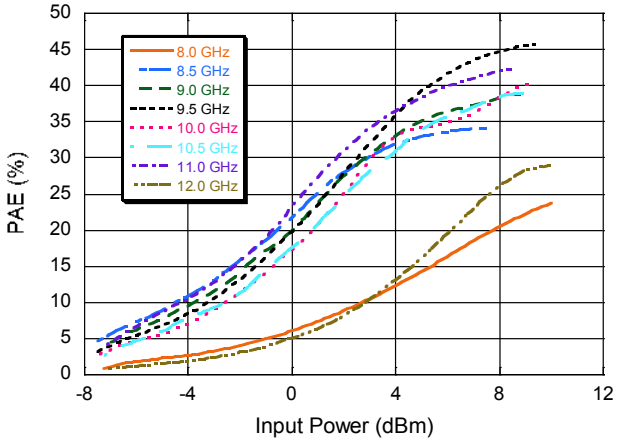

***Output Power vs. Input Power***



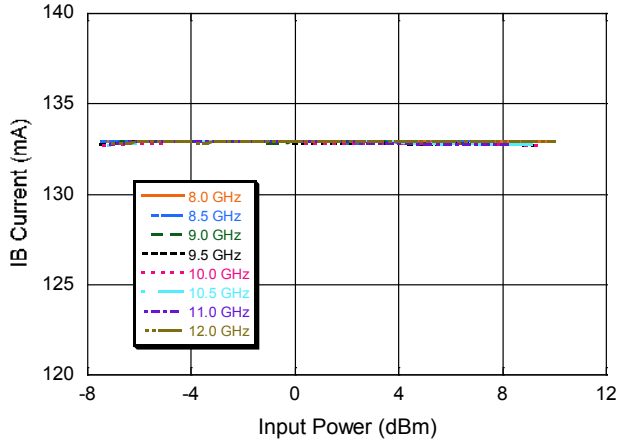

***Drain Current vs. Input Power***




***PAE vs. Input Power***

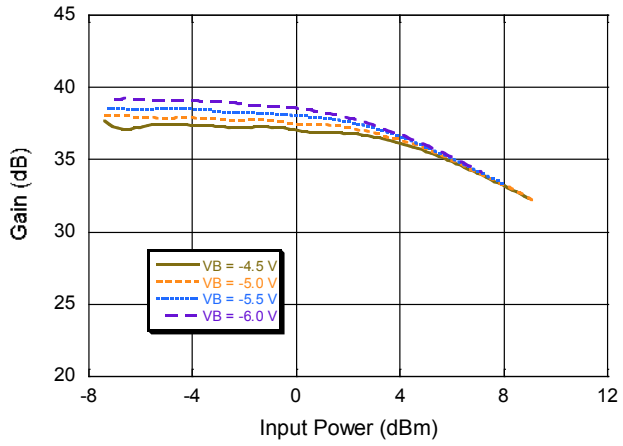



***Bias Circuit Current vs. Frequency***

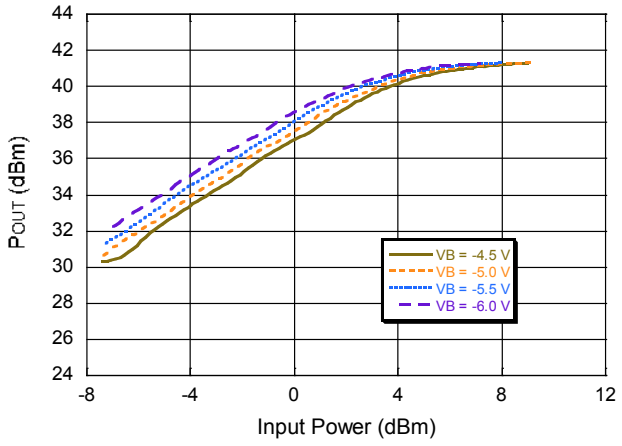


## Typical CW Performance Curves over Bias Circuit Voltage: Freq = 9 GHz

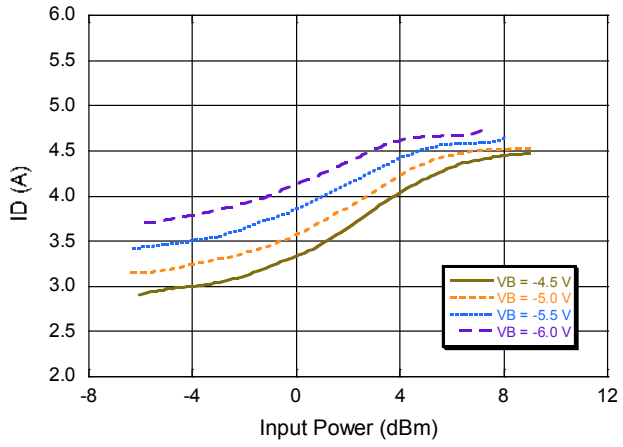
***Gain vs. Input Power***



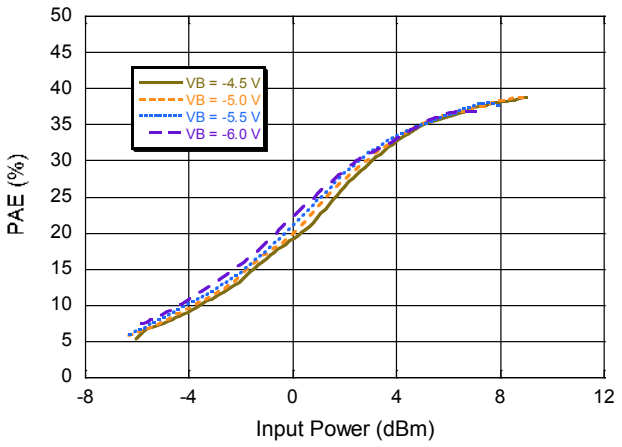

***Output Power vs. Input Power***




***Drain Current vs. Input Power***

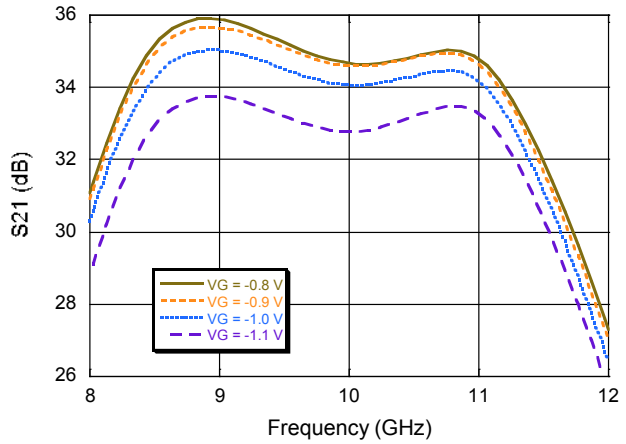



***PAE vs. Input Power***

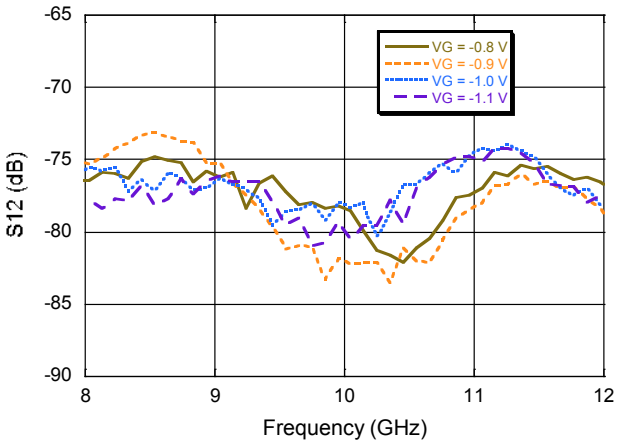


## Typical CW Performance Curves over Gate Voltage: VD = 6 V

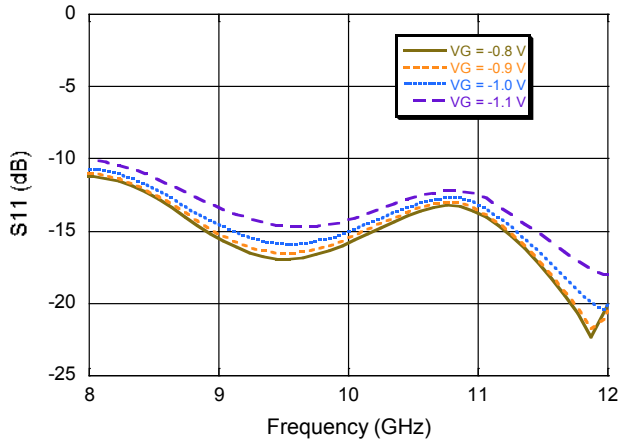
***Gain vs. Frequency***



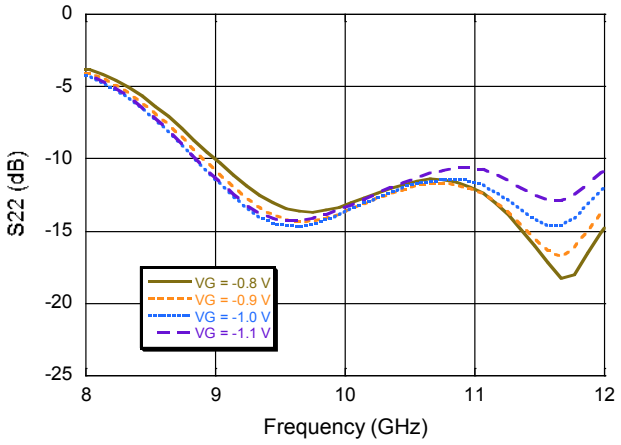

***Isolation vs. Frequency***




***Input Return Loss vs. Frequency***

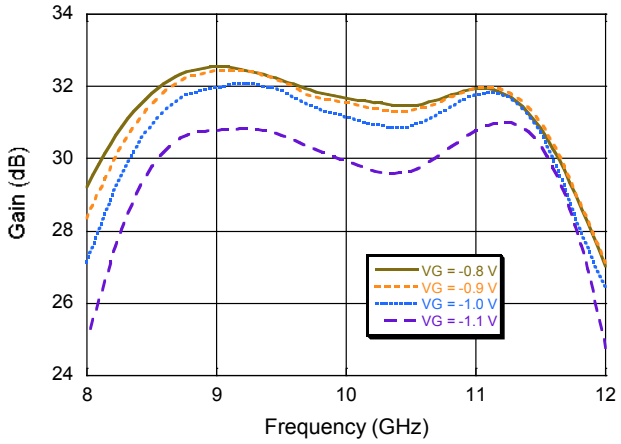



***Output Return Loss vs. Frequency***

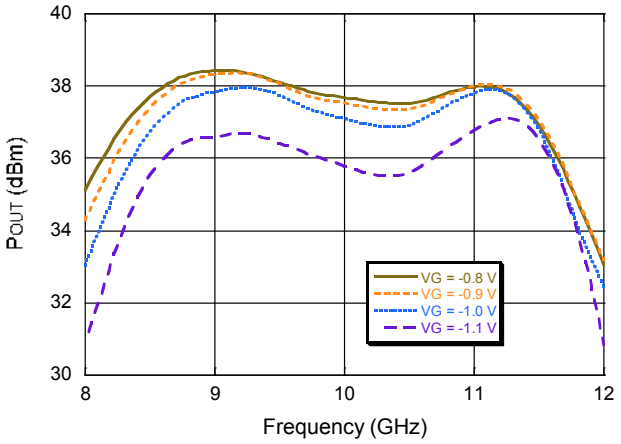


## Typical CW Performance Curves over Gate Voltage: VD = 6 V; Constant Pin = 6 dBm

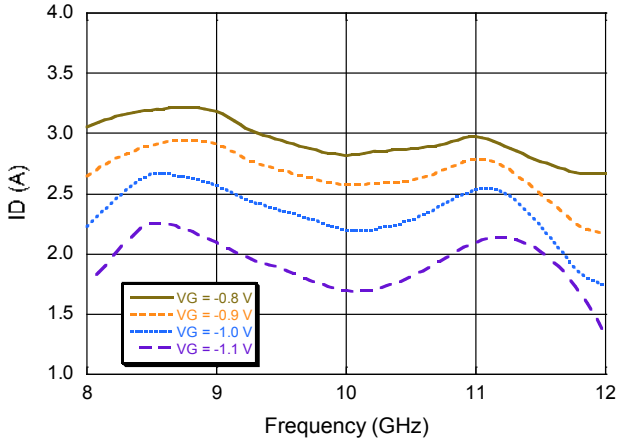
***Gain vs. Frequency***



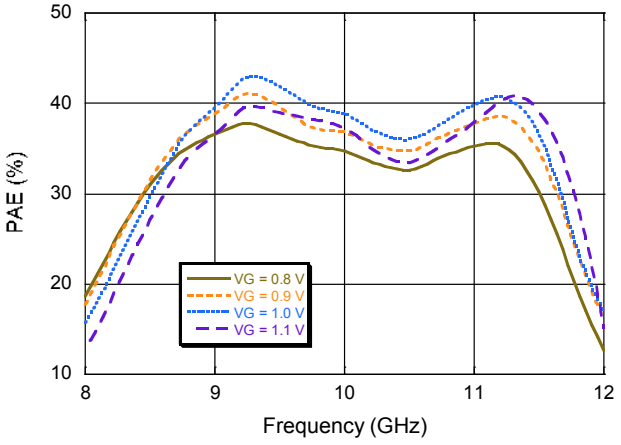

***Output Power vs. Frequency***




***Drain Current vs. Frequency***

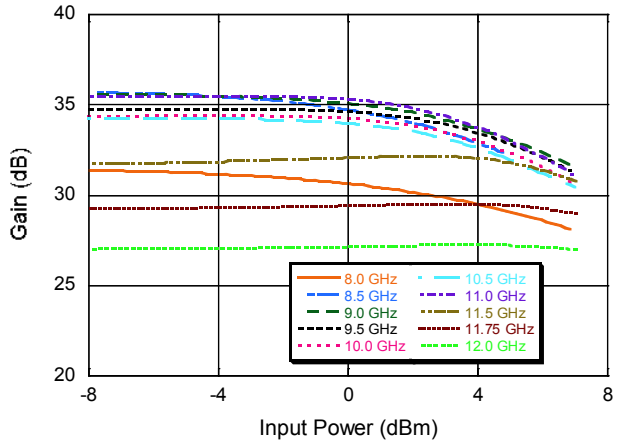



***PAE vs. Frequency***

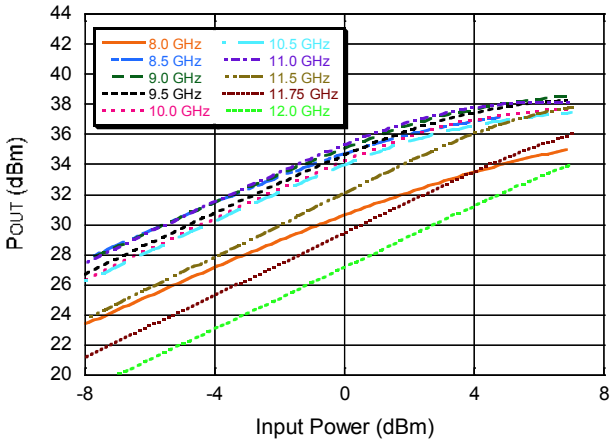


## Typical CW Performance Curves over Frequency: Gate Voltage = -0.9 V, VD = 6 V

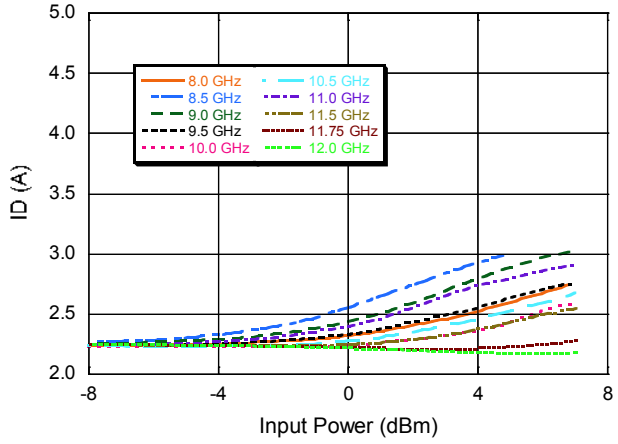
***Gain vs. Input Power***



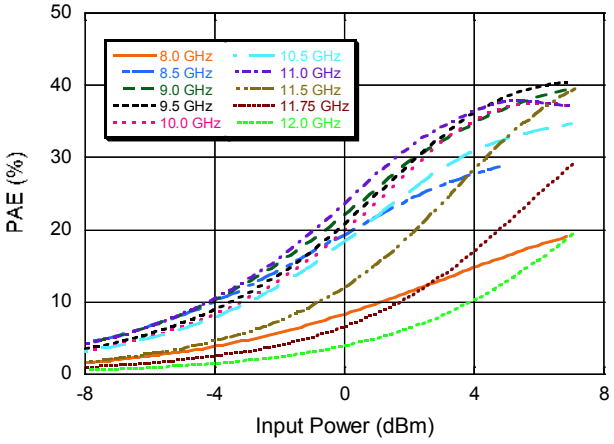

***Output Power vs. Input Power***



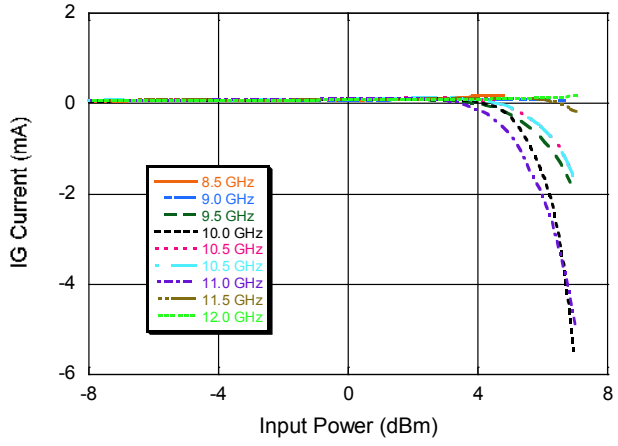

***Drain Current vs. Input Power***




***PAE vs. Input Power***




***Gate Current vs. Input Power***



# Applications Section

## Application Notes

**Note 1 - Biasing**
The gate bias is applied in one of the following:

1. Direct Gate Bias:- $V_G1$, $V_G2$, & $V_G3$ provide the direct gate bias input to the 3 MMIC stages. This method of biasing allows the user to control the total drain current without the scaling factor provided by the bias circuit . It is recommended that the gate voltage is supplied by both sides of the Die. Optimum performance can be achieved with a -0.9 V operation.
2. Bias Circuit Biasing:- Applying -5V to $V_B1$, $V_B2$, & $V_B3$ will typically draw 3.0A with no further adjustment necessary. Wafer lot variation may result in some devices experiencing higher or lower drain currents than the typical 3.0A. It is necessary to connect the Bias Circuit Ground (Pad 2,7,11,21, 25, & 30) to ground in order for this bias circuit to function correctly. It is recommended that the bias circuits on both sides of the PA are used.

**Note 2 - Bias Sequence**
When switching on the PA, In each case, the gate bias must be applied before the drain voltage is applied. The Drain Voltage $V_D1$, $V_D2$, & $V_D3$ should be biased from the top and bottom sides of the die.

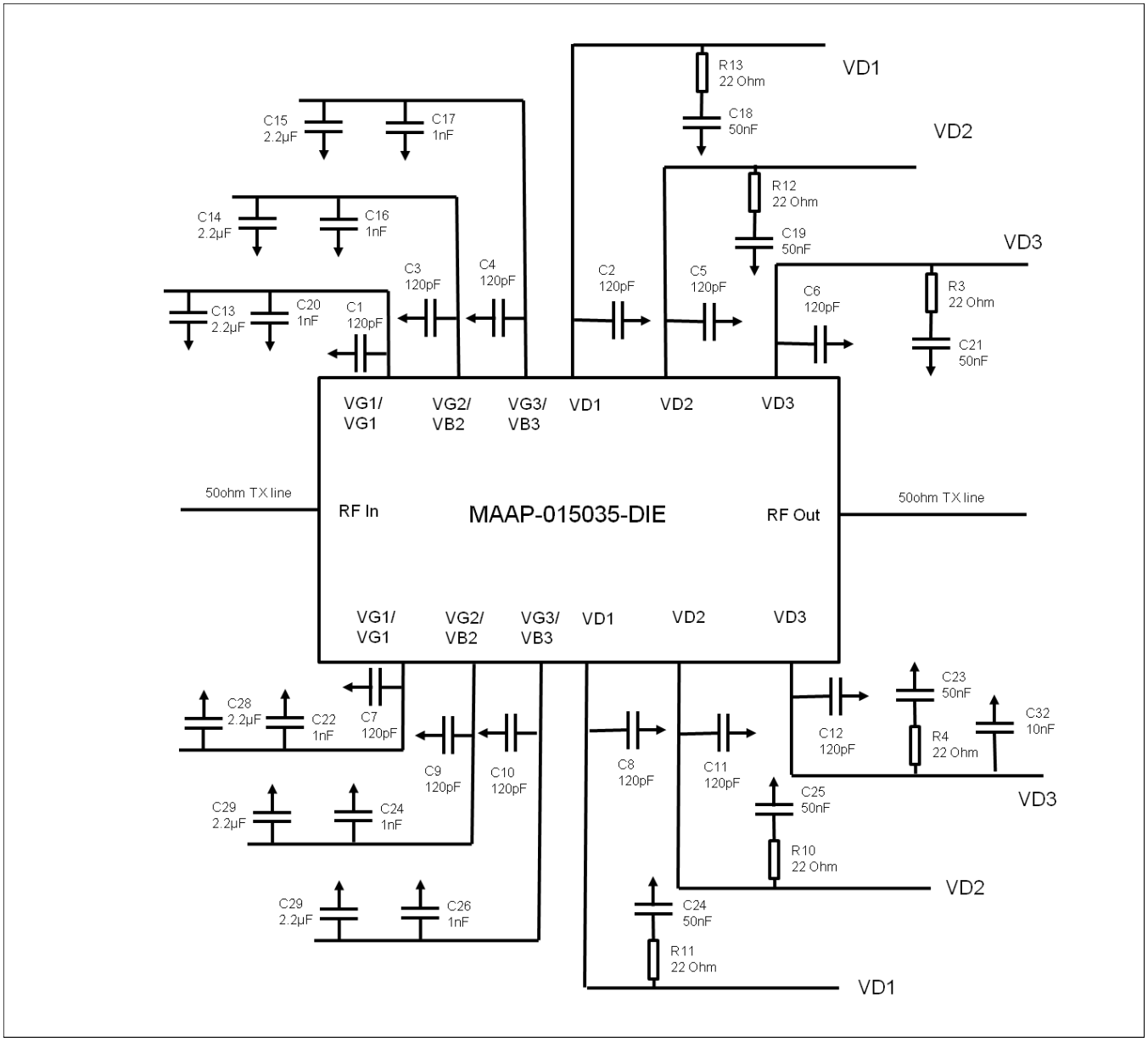
**Note 3 - Decoupling Circuits**
Each bias pad, $V_G$ or $V_B$, and $V_D$ must have a decoupling capacitor of 100 pF as close to the device as possible, as is shown in the bonding diagrams. In the case where the bias circuit is used the additional bond wire to ground must be made as short as possible.
Under pulsed operation a large capacitance on the Drain will cause a “ringing” effect on the supply voltage. This potentially produces a high voltage at the PA terminals. A recommended decoupling circuit is provided where shunt decoupling capacitors are connected in series with a resistor to minimize this effect.

**Note 4 - Pulse Operation**
The performance of the MAAP-015035-DIE is characterized under pulsed conditions with a duty cycle of 5% consisting of a pulse width of 5 µS applied to the drain. Under pulsed conditions the gate is constantly biased using either the on chip bias circuit or using a gate voltage directly applied to the PA. It is recommended that the die is mounted with an adequate thermal solution.

**Note 5 - CW Operation**
The PA is only recommended for CW operation at reduced drain voltages. With a recommended drain voltage of 6V, and a direct gate voltage of –0.9V or using the on chip bias circuit at –5V.

**Note 6 - Input / Output Transitions**
The PA performance must be achieved in a 50ohm impedance environment on the RF input and output. To maintain performance three Bond wires are recommended on the output of the PA each with a maximum length of less than 600µm. Longer bond wire lengths can be used providing bond pad compensation, in the form of a stub, is used on the application board.

## Application Circuit



# Applications Section

## Handling and Assembly

### Die Attachment

This product is manufactured from 0.100 mm (0.004") thick substrate and has vias through to the backside to enable grounding to the circuit. Microstrip substrates should be brought as close to the die as possible and bond wire lengths on the input and output kept as short as possible. The mounting surface should be clean and flat. If using conductive epoxy, recommended epoxies are Tanaka TS3332LD, Die Mat DM6030HK or DM6030HK-Pt cured per the manufacturer's cure schedule. Epoxy should be applied in accordance with the manufacturers specifications and should avoid contact with the top surface of the die. An epoxy fillet should be visible around the total die periphery. For additional information please see the MACOM "Epoxy Specifications for Bare Die" application note. If eutectic mounting is preferred, then a flux-less gold-tin (AuSn) preform, approximately 0.0012 thick, placed between the die and the attachment surface should be used. A die attach bonder that utilizes a heated collet and provides scrubbing action to ensure total wetting to prevent void formation in a nitrogen atmosphere is recommended. The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280ºC (Note: Gold Germanium should be avoided). The work station temperature should be 310ºC +/-10ºC. Exposure time to these extreme temperatures should be kept to minimum. The die and collet should be pre-heated, to avoid excessive thermal shock during assembly. Avoidance of air bridges and force impact are critical during placement.

### Wire Bonding

Windows are provided in the surface passivation above the bond pads to allow wire bonding to the die's gold bond pads. The recommended wire bonding procedure uses 0.076 mm x 0.013 mm (0.003" x 0.0005") 99.99% pure gold ribbon with 0.5-2% elongation to minimize RF port bond inductance. Gold 0.025 mm (0.001") diameter wedge or ball bonds are acceptable for DC Bias connections. Aluminium wire should be avoided. Thermo-compression bonding is recommended though thermo-sonic bonding may be used providing the ultrasonic content of the bond is minimized. Bond force, time and ultrasonic's are all critical parameters. Bonds should be made from the bond pads on the die to the package or substrate. All bonds should be as short as possible.