PI3WVR31310A

DP/HDMI 1:3 De-mux/Mux switches

Features

- DP 1:3 De-Mux or 3:1 Mux switch with 4 high speed differential, AUX/DDC, HPD and CAB_DET channels
- Pin selection for 1:3 DEMUX or 3:1 MUX
- HDMI 3:1 Mux switch with 4 high speed differential, DDC and HPD channels
- HDMI-mode only supports HDMI-sink application, not support HDMI-source application.
- Pin selection for DP mode or HDMI mode
- All ports support up to DP1.2 at 5.4Gb/s or HDMI 2.0 at 6Gb/s
- Supports manual switching or HPD auto priority selection in 1:3 DEMUX, in DP mode
- Low current consumption
- 3.3V power supply
- ESD protection on all I/O pins for 2kV HBM
- Package:

  60 pin TQFN (5x9mm)

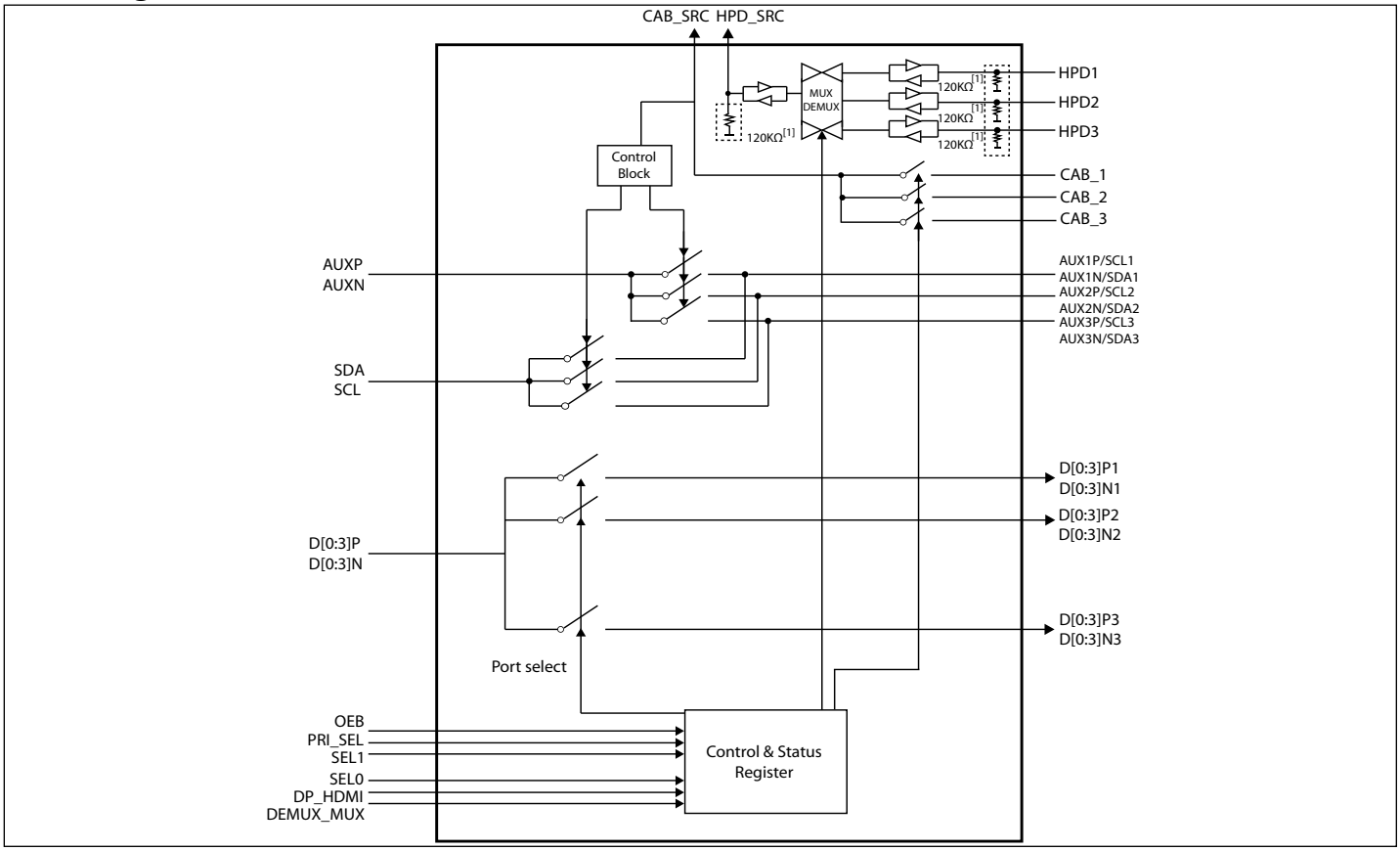
Description

Pericom Semiconductor's PI3WVR31310A is a 3:1 Mux or 1:3 Demux high speed passive switch supporting DP 1.2, HDMI 1.4, HDMI 2.0. At DEMUX mode, all three output ports support auto port priority selection by detecting HPD1/2/3 input or manual selection. At MUX mode, HPD1/2/3 will change from input to output, there is no auto port priority selection.

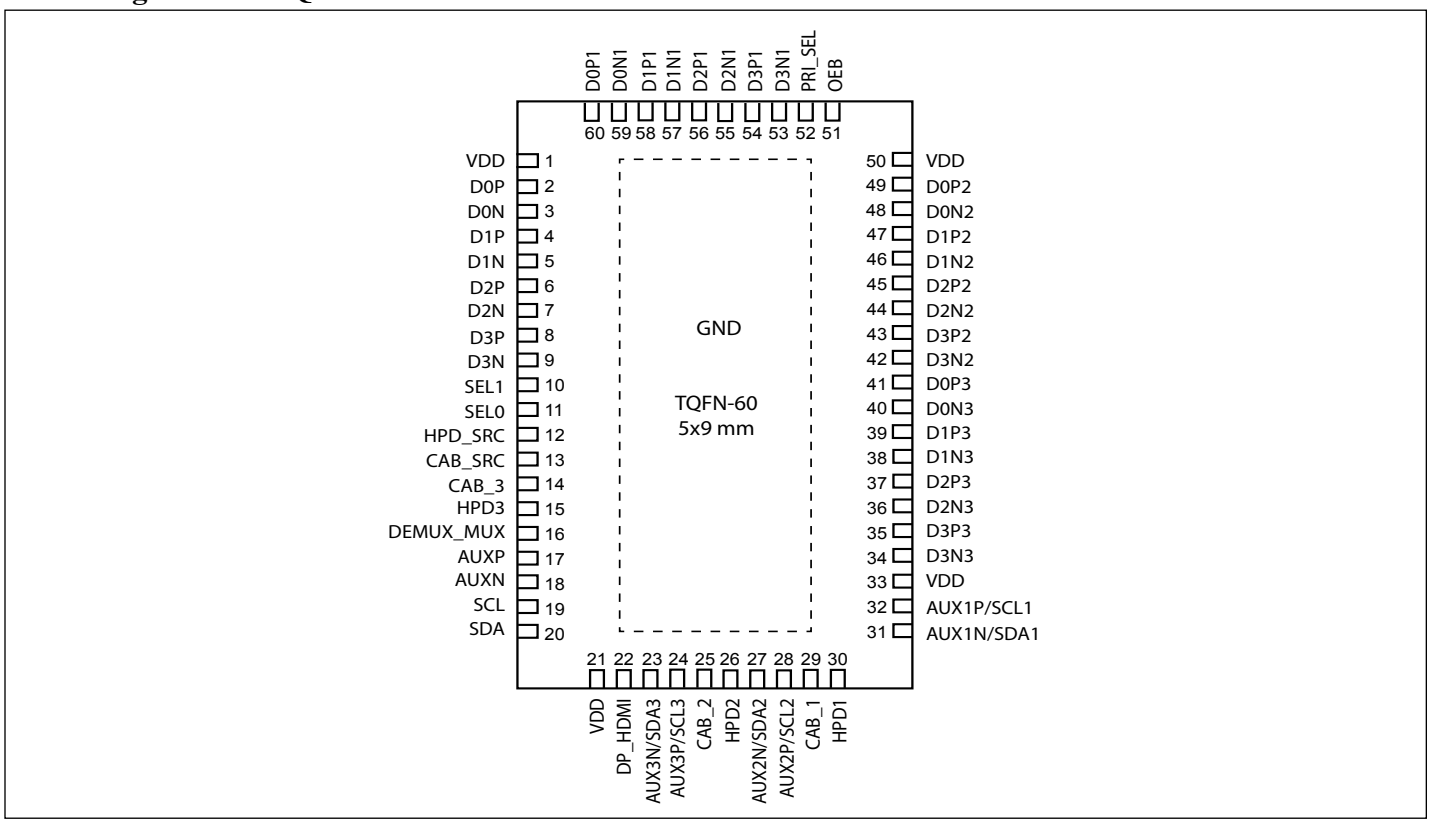
Application

- Notebook, Monitor, Switch box or TV sink application

Block Diagram



Pin Configuration: TQFN-60



Note: 1. The 120kΩ pull down resistor is not always on.

Pin Description

pin#	pin Name	Signal Type	Description
2, 4, 6, 8, 3, 5, 7, 9	D0P, D1P, D2P, D3P, D0N, D1N, D2N, D3N	IO	4 differential pair I/O (DP or HDMI)
60, 58, 56, 54, 59, 57, 55, 53	D0P1, D1P1, D2P1, D3P1, D0N1, D1N1, D2N1, D3N1	IO	4 differential pair I/O (DP or HDMI) for port 1
49, 47, 45, 43, 48, 46, 44, 42	D0P2, D1P2, D2P2, D3P2, D0N2, D1N2, D2N2, D3N2	IO	4 differential pair I/O (DP or HDMI) for port 2
41, 39, 37, 35, 40, 38, 36, 34	D0P3, D1P3, D2P3, D3P3, D0N3, D1N3, D2N3, D3N3	IO	4 differential pair I/O (DP or HDMI) for port 3

pin#	pin Name	Signal Type	Description
31, 27, 23, 32, 28, 24	AUX1N/SDA1, AUX2N/SDA2, AUX3N/SDA3, AUX1P/SCL1, AUX2P/SCL2, AUX3P/SCL3	IO	AUX (DP) or DDC (HDMI) input from three ports
18, 17	AUXN, AUXP	IO	AUX output
20, 19	SDA, SCL	IO	DDC output
30, 26, 15, 12	HPD1, HPD2, HPD3, HPD_SRC	IO	When DEMUX_MUX = low (1:3 DEMUX mode), HPD1_2_3 are inputs, HPD_SRC is output; When DEMUX_MUX = high (3:1 MUX mode), HPD1_2_3 are outputs, HPD_SRC is input
29, 25, 14, 13	CAB_1, CAB_2, CAB_3, CAB_SRC	IO	CAB_1, CAB_2, CAB_3, CAB_SRC
51	OEB	I	OEB=0, device active; OEB=1, device shut down
52	PRI_SEL	I	PRI_SEL is for priority selection as in priority-selection-table, but only for 1:3 DEMUX mode. PRI_SEL has internal 100K divider between VDD and GND for middle-state with VDD/2.
16	DEMUX_MUX	I	DEMUX_MUX is for HPD direction selection, see truth table
22	DP_HDMI	I	DP port or HDMI port, see truth table
11	SEL0	I	Port selection pins, see truth table
10	SEL1	I	Port selection pins, see truth table
1, 21, 33, 50	VDD	Power	3.3V VDD
Center Pad	GND	Ground	Bottom GND EPAD

Pin mapping for dual mode DP source DEMUX to DP output

DP mode	HDMI/DVI mode	WVR31310A input pins	WVR31310A port1 output	WVR31310A port2 output	WVR31310A port3 output	DP mode
ML_lan0(P)	TX2+	D0P	D0P1	D0P2	D0P3	ML_lan0(P)
ML_lan0(N)	TX2-	D0N	D0N1	D0N2	D0N3	ML_lan0(N)
ML_lan1(P)	TX1+	D1P	D1P1	D1P2	D1P3	ML_lan1(P)
ML_lan1(N)	TX1-	D1N	D1N1	D1N2	D1N3	ML_lan1(N)
ML_lan2(P)	TX0+	D2P	D2P1	D2P2	D2P3	ML_lan2(P)
ML_lan2(N)	TX0-	D2N	D2N1	D2N2	D2N3	ML_lan2(N)
ML_lan3(P)	TXC+	D3P	D3P1	D3P2	D3P3	ML_lan3(P)
ML_lan3(N)	TXC-	D3N	D3N1	D3N2	D3N3	ML_lan3(N)

Function Description

Default input format is DP. DP_HDMI can select between DP or HDMI input.

In Demux mode, there are 120K pull down in HPD1/HPD2/HPD3 pins. In Mux mode, there is 120K pull down in HPD_SRC pin.

Output port can be selected by manual or automatically in DEMUX mode.

Automatic port selection is done by detection of HPD presence from the output ports. If multiple HPD are detected, port selection depends on a priority scheme defined by PRI_SEL pin. There can be 3 priority schemes. When PRI_SEL=low, the port priority order is port1/port2/port3; when PRI_SEL=high, the port priority order is port2/port3/port1; when PRI_SEL=M (open), the port priority order is port3/port1/port2.

When port 1 or port 2 or port 3 is selected in DP application, and CAB=LOW, AUX/DDC input pins are now AUX channel. AUXP will have 100Kohm resistor to GND while AUXN will have 100Kohm resistor to VDD in external port side. Max. AUX data rate can be 720Mb/s. DDC switch inside is off.

When port 1 or port 2 or port 3 is active in dual mode DP or HDMI application, and CAB=HIGH, AUX/DDC input pins are now DDC channel. AUX switch inside is off, DDC switch is on. The DDC switch can support 5V input, and output Vpass is less than 3.3V limit.

HPD is CMOS buffer, and support 5v inputs. When used as DEMUX, There're 120kΩ pull-down resistors inside connected to HPD1, HPD2, HPD3 as input, and when used as MUX, 120k resistor connected to HPD_SRC as input.

Truth Table

DEMUX_MUX

DEMUX_MUX	HPD_SRC	HPD1/2/3
0 (DEMUX)	output	input
1 (MUX)	input	output

DP_HDMI

DP_HDMI	Mode
0	DP Mode
1	HDMI Mode

SLE1/SEL0 in 1:3 DP modes

SEL1	SEL0	PRI_SEL (priority selection)	HPD/CAB_DET	D[0:3]P, D[0:3]N, AUX/DDC
0	0	NC	HPD1/CAB_1	Port 1
0	1	NC	HPD2/CAB_2	Port 2
1	0	NC	HPD3/CAB_3	Port 3
1	1	Auto-selection	See priority table	See priority table

SLE1/SEL0 in 3:1 HDMI mode and DP mode

SEL1	SEL0	PRI_SEL (priority selection)	HPD	D[0:3]P, D[0:3]N, AUX/DDC
0	0	NC	HPD=HPD1, HPD2/3=0	Port 1
0	1	NC	HPD=HPD2, HPD1/3=0	Port 2
1	0	NC	HPD=HPD3, HPD1/2=0	Port 3
1	1	NC	NC	NC

AUX and DDC

PORT	DP_HDMI	CAB_1	CAB_2	CAB_3	AUXP	AUXN	SCL	SDA
When Port1 Selected	0	0	x	x	AUX1P	AUX1N	Hi-Z	Hi-Z
	0	1	x	x	Hi-Z	Hi-Z	SCL1	SDA1
	1	1	x	x	Hi-Z	Hi-Z	SCL1	SDA1
When Port2 Selected	0	x	0	x	AUX2P	AUX2N	Hi-Z	Hi-Z
	0	x	1	x	Hi-Z	Hi-Z	SCL2	SDA2
	1	x	1	x	Hi-Z	Hi-Z	SCL2	SDA2
When Port3 Selected	0	x	x	0	AUX3P	AUX3N	Hi-Z	Hi-Z
	0	x	x	1	Hi-Z	Hi-Z	SCL3	SDA3
	1	x	x	1	Hi-Z	Hi-Z	SCL3	SDA3

Priority Selection Table

PRI_SEL (Priority order)	HPD1	HPD2	HPD3	HPD_SRC	CAB_SRC	AUXP/AUXN	SDA/SCL
0	0	0	0	0	Hi-Z	Hi-Z	Hi-Z
0	1	x	x	HPD1	CAB1	AUX1P/AUX1N	SDA1/SCL1
0	0	1	x	HPD2	CAB2	AUX2P/AUX2N	SDA2/SCL2
0	0	0	1	HPD3	CAB3	AUX3P/AUX3N	SDA3/SCL3
M	0	0	0	0	Hi-Z	Hi-Z	Hi-Z
M	1	x	0	HPD1	CAB1	AUX1P/AUX1N	SDA1/SCL1
M	0	1	0	HPD2	CAB2	AUX2P/AUX2N	SDA2/SCL2
M	x	x	1	HPD3	CAB3	AUX3P/AUX3N	SDA3/SCL3
1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z
1	1	0	0	HPD1	CAB1	AUX1P/AUX1N	SDA1/SCL1
1	x	1	x	HPD2	CAB2	AUX2P/AUX2N	SDA2/SCL2
1	x	0	1	HPD3	CAB3	AUX3P/AUX3N	SDA3/SCL3

Note: M= VDD/2 or open (with internal VDD/2)

PRI_SEL (Priority order)	HPD1	HPD2	HPD3	D0P	D1P	D2P	D3P	D0N	D1N	D2N	D3N
0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	x	x	D0P1	D1P1	D2P1	D3P1	D0N1	D1N1	D2N1	D3N1
0	0	1	x	D0P2	D1P2	D2P2	D3P2	D0N2	D1N2	D2N2	D3N2
0	0	0	1	D0P3	D1P3	D2P3	D3P3	D0N3	D1N3	D2N3	D3P3
M	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
M	1	x	0	D0P1	D1P1	D2P1	D3P1	D0N1	D1N1	D2N1	D3N1
M	0	1	0	D0P2	D1P2	D2P2	D3P2	D0N2	D1N2	D2N2	D3N2
M	x	x	1	D0P3	D1P3	D2P3	D3P3	D0N3	D1N3	D2N3	D3P3
1	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	1	0	0	D0P1	D1P1	D2P1	D3P1	D0N1	D1N1	D2N1	D3N1
1	x	1	x	D0P2	D1P2	D2P2	D3P2	D0N2	D1N2	D2N2	D3N2
1	x	0	1	D0P3	D1P3	D2P3	D3P3	D0N3	D1N3	D2N3	D3P3

Note: M= VDD/2 or open (with internal VDD/2)

Note: For priority selection control, when PRI_SEL = 0, the order is port1/port2/port3; when PRI_SEL = 1, the order is port2/port3/port1; when PRI_SEL = M, the order is port3/port1/port2.

Maximum Ratings

(Above which useful life may be impaired. For user guidelines not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +4.6V
High Speed Channel Input Voltage (DP Mode)	–0.5V to 2V
High Speed Channel Input Voltage (HDMI Mode)	2.4V to 3.6V
DDC and HPD channels Input Voltage	–0.5V to 6V
DC Output Current	40mA
Power Dissipation	0.2W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

Recommended Operation Conditions

V_{DD} = 3.3V ±10%, Min and Max apply for TA between -40°C to 85°C Typical values are referenced to TA = 25°C

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage		3.0	3.3	3.6	V
I_{DD}	VDD supply current	V_{DD}=3.3V		1		mA
Istd	Supply current when OEB disable HDMI Mode	V_{DD}=3.6V, OEB=high DP_HDMI=1		0.7		mA
	Supply current when OEB disable DP Mode	V_{DD}=3.6V, OEB=high DP_HDMI=0		10		uA

DC Electrical Characteristics for Switching over Operating Range

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
OEB, SEL1, SEL0						
I_{IH}	High level digital input current	V_{IH} =V_{DD}	-10		40	µA
I_{IL}	Low level digital input current	V_{IL} = GND	-10		10	µA
V_{IH}	High level digital input voltage		2.0			V
V_{IL}	Low level digital input voltage		0		0.8	V
DEMUX_MUX						
I_{IH}	High level digital input current	V_{IH} =VDD	-10		40	µA
I_{IL}	Low level digital input current	V_{IL} = GND	-10		10	µA
V_{IH}	High level digital input voltage		2.7			V
V_{IL}	Low level digital input voltage		0		0.8	V
DP_HDMI						
R_{pd}	Inter Pull-down resistor on DP_HDMI			100		kΩ
V_{IH}	High level digital input voltage		0.7Vdd			V
V_{IL}	Low level digital input voltage		0		0.3Vdd	V

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
HPD_SRC (when HPD_SRC is output, HPD 1, 2, 3 are inputs)						
V_{IH}	High level digital input voltage	V_{DD}=3.3V	2.0			V
V_{IL}	Low level digital input voltage	V_{DD}=3.3V	0		0.8	V
$V_{OL\_HPD\_SRC}$	Buffer Output Low Voltage	I_{OL} = 4 mA			0.4	V
$V_{OH\_HPD\_SRC}$	Buffer Output Low Voltage	I_{OH} = 4 mA	2.4			V
HPD_Sink (when HPD_SRC is input, HPD 1, 2, 3 are as sink outputs)						
V_{IH}	High level digital input voltage	V_{DD}=3.3V	2.0			V
V_{IL}	Low level digital input voltage		0		0.8	V
$V_{OL\_HPD\_Sink}$	Buffer Output Low Voltage	I_{OL} = 4 mA			0.4	V
$V_{OH\_HPD\_Sink}$	Buffer Output Low Voltage	I_{OH} = 4 mA	2.4			V
CAB						
I_{LK}	Input leakage current	Switch is off, Vin=5.5V	-50		50	uA
C_{IO}	Input/Output capacitance when passive switch on			10		pF
R_{ON}	Passive Switch resistance	I_O = 3mA, V_O = 0.4V		25	50	Ω
V_{pass}	Switch Output voltage	V_I=3.3V, I_I=100uA	3.0	3.5	4.0	V
CI(source)	Source side CAB capacitance	V_I peak-peak = 1V, 100 KHz		3.5		pF
CI(sink)	Sink side CAB capacitance when			6.5		pF
SDA/SCL,SDA1/SCL1, SDA2/SCL2 , SDA3/SCL3 (passive switch)						
I_{LK}	Input leakage current	DDC switch is off, Vin=5.5V	-50		50	uA
C_{IO}	Input/Output capacitance when passive switch on	V_I peak-peak = 1V, 100 KHz		10		pF
R_{ON}	Passive Switch resistance	I_O = 3mA, V_O = 0.4V		25	50	Ω
Vpass	Switch Output voltage	V_I=5.0V, I_I=100uA V_{DD}=3.3V	1.5	2.0	2.5	V
CI(source)	Source side DDC capacitance (passive switch off.)	V_I peak-peak = 1V, 100 KHz		2.5		pF
CI(sink)	Sink side DDC capacitance (passive switch off.)	V_I peak-peak = 1V, 100 KHz		9		pF
AUXP, AUXN, AUXnP/SCLn, AUXnN/SDAn						
I_{LK}	Input leakage current	DDC switch is off, Vin=5.5V	-50		50	uA
C_{IO}	Input/Output capacitance when passive switch on	V_I peak-peak = 1V, 100 KHz		7		pF
R_{ON}	Passive Switch resistance	I_O = 3mA, V_O = 0.4V		5	15	Ω
V_{pass}	Switch Output voltage	V_I=5.5V, I_I=100uA V_{DD}=3.3V	3.0	4.0	4.5	V
CI(source)	Source side capacitance (passive switch off.)	V_I peak-peak = 1V, 100 KHz		2.5		pF

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
CI(sink)	Sink side capacitance (passive switch off.)	V_I peak-peak = 1V, 100 KHz		3.5		pF
High Speed Channel (D[0:3]P/N – D[0:3]P1N1, D[0:3]P/N – D[0:3]P2N2)						
V_{IK}	Clamp Diode Voltage (HS Channel)	V_{DD} = Max., I_{IN} = –18mA		–1.6	–1.8	V
I_{IH}	Input HIGH Current	V_{DD} = Max., V_{IN} = V_{DD}			±10	µA
I_{IL}	Input LOW Current	V_{DD} = Max., V_{IN} = GND			±10	
R_{ON_HS}	On resistance between input to out- put for high speed signals	$V_{INPUT,cm}$ = 0V to 0.8V, $V_{INPUT, diff}$ < 1.0$V_{p-p,diff}$, V_{DD} = 3.0V, I_{INPUT} = 20mA		8	12	Ohm
		$V_{INPUT,cm}$ = 2.2V to 3.1V, $V_{INPUT, diff}$ < 1.2Vp-p,diff, V_{DD} = 3.0V, I_{INPUT} = 20mA		8	12	Ohm
Input signal voltage range	HDMI MUX mode	Channel on	2.4		3.3	V
	HDMI MUX mode	Channel off	0		3.3	V

Note: High speed channel does not support Ioff when VDD=0

Dynamic Electrical Characteristics

Parameter	Description	Test Conditions		Min.	Typ.(1)	Max.	Unit
SCL, SDA channel, AUX channel, CAB channel (passive switch)							
t_{pd}(DDC)	Propagation delay from SCLn/SDAn to SCL/SDA or SCL/SDA to SCLn/SDAn In passive SW on.	C_L = 10pF, in passive switch				5	ns
		C_L = 10pF, in active switch (1.5k to 5k pull high, 10pf to GND)				60	
Control and Status Pins (HPDn, HPD_SRC)							
tpd(HPD)	Propagation delay (from HPDx to the active port of HPD_SRC, high to low)	C_L = 10pF, manual selection mode; auto mode refer to auto timing			10		ns
tsx(HPD)	Switch time (from port select to the latest HPD)				5		us
X_{TALK}	Crosstalk on High Speed Channels	See Fig.1 for Measurement Setup	f = 2.7 GHz		-26	-23	dB
			f = 3.0 GHz		-24	-21	
O_{IRR}	OFF Isolation on High Speed Channels	See Fig. 2 for Measurement Setup	f = 2.7 GHz		-21	-19	
			f = 3.0 GHz		-21	-19	
I_{LOSS}	Differential Insertion Loss on High speed channels	@5.4Gbps (see figure 3, Vcom = 0V)		-1.8	-1.6		dB
I_{LOSS}	Differential Insertion Loss on High Speed HDMI Channels	@6Gbps (see figure 3, Vcom = 3.0V)			-2.5		dB
R_{loss}	Differential Return Loss on High speed channels	@ 2.7GHz (5.4Gbps)			-18	-15	dB
BW_Dx±	Bandwidth -3dB for Main High speed path (Dx±)	See figure 3		5.0	5.4		GHz
BW_Dx±	Bandwidth -3dB for Main high speed HDMI path (Dx±)	See figure 3		4.7	5.0		GHz
BW_AUX	Bandwidth -3dB for AUX	See figure 3		1.2	1.5		GHz
Tsw a-b	time it takes to switch from port A to port B	Manual selection				1	us
Tsw b-a	time it takes to switch from port B to port A	Manual selection				1	us
$T_{startup}$	Vdd valid to channel enable	Manual selection				10	us
T_{wakeup}	Enabling output by changing OEB from High to Low	Manual selection				10	us

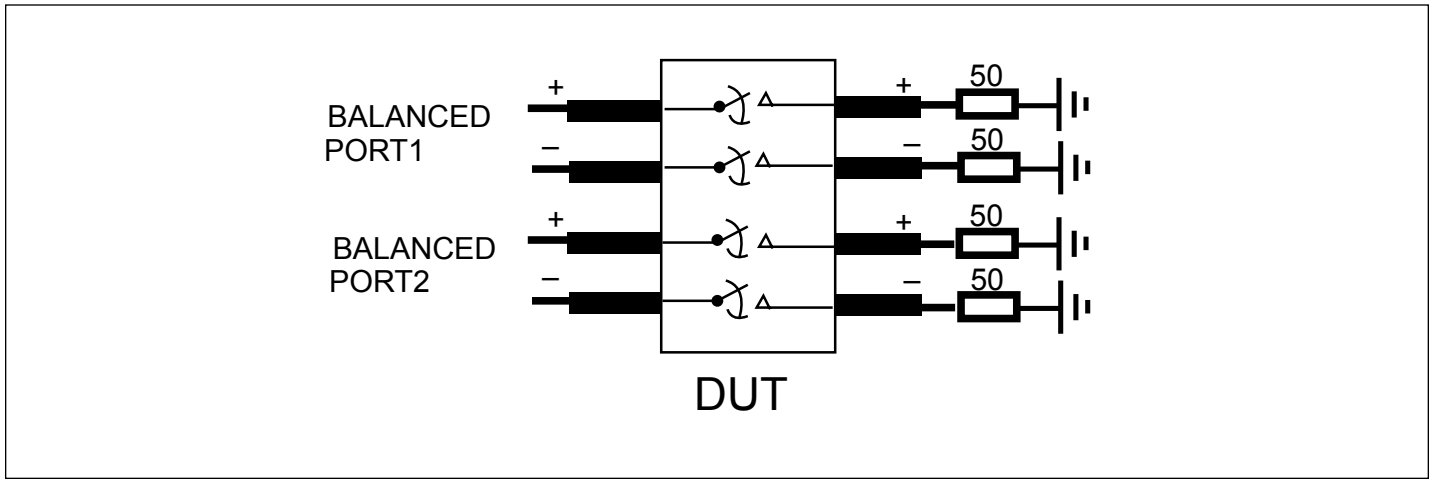


Fig 1. Crosstalk Setup

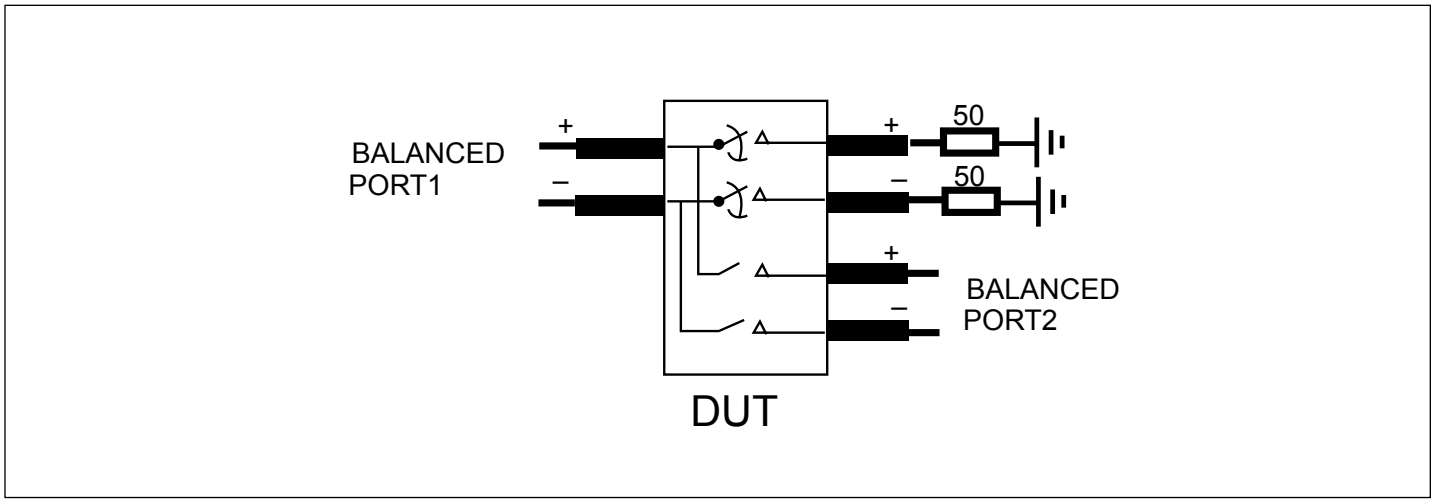


Fig 2. Off-isolation setup

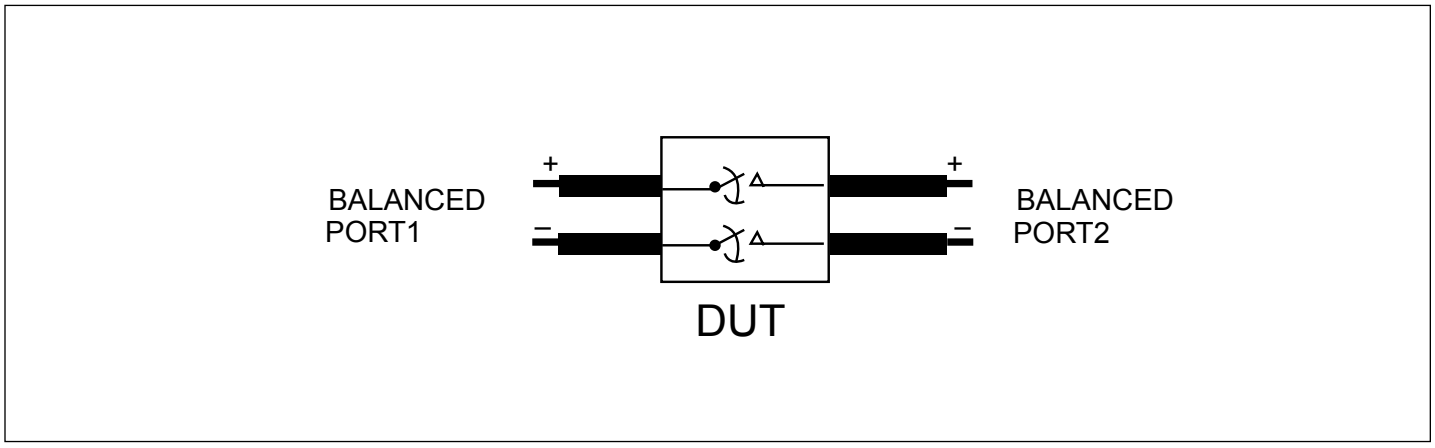


Fig 3. Differential Insertion Loss

HPD timing waveform (DEMUX mode)

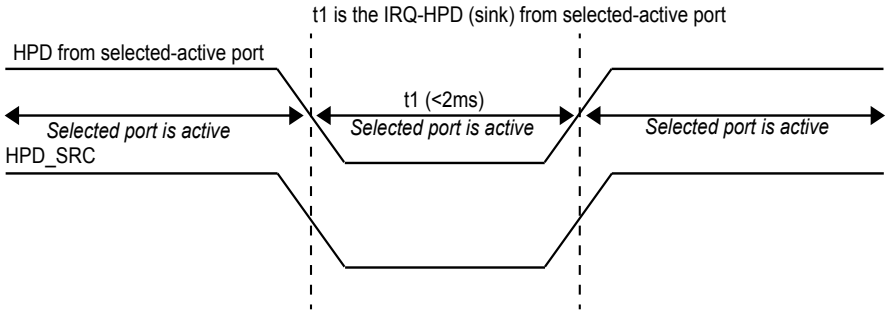


Fig 4. HPD timing t1. HPD_SRC low and the active of selected port will follow t1, if t1 further extended less than t2 (125ms) when auto switch and manual switch

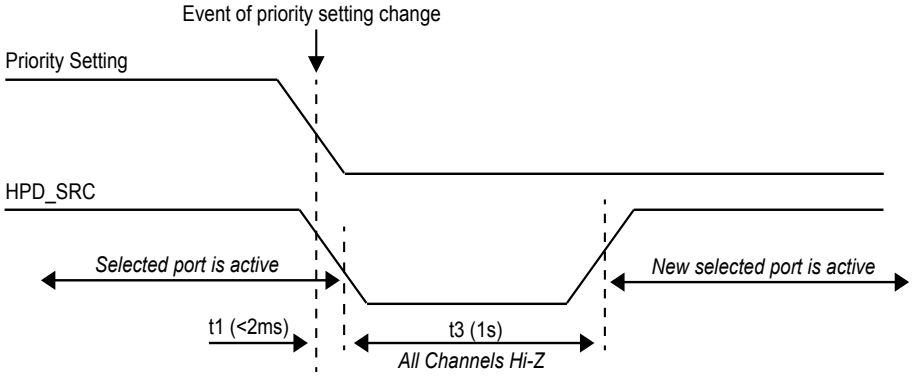


Fig 5. HPD timing t3. All channels" include DP-HDMI data, AUX, DDC, HPD and CAB_DET when auto switch

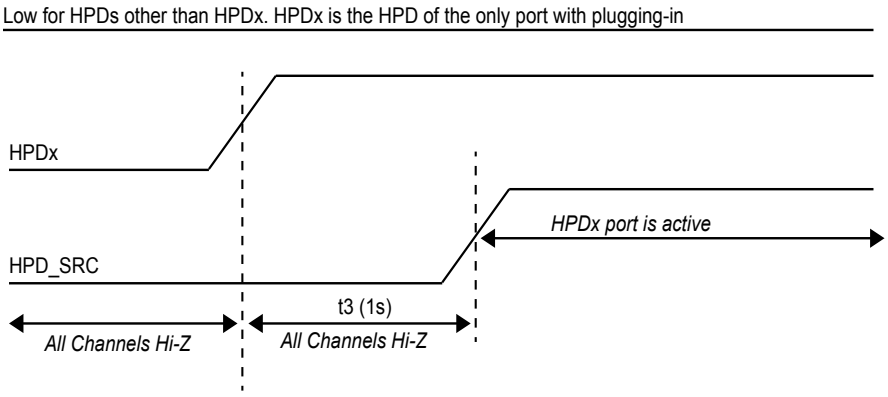


Fig 6. HPD timing t3 when auto switch

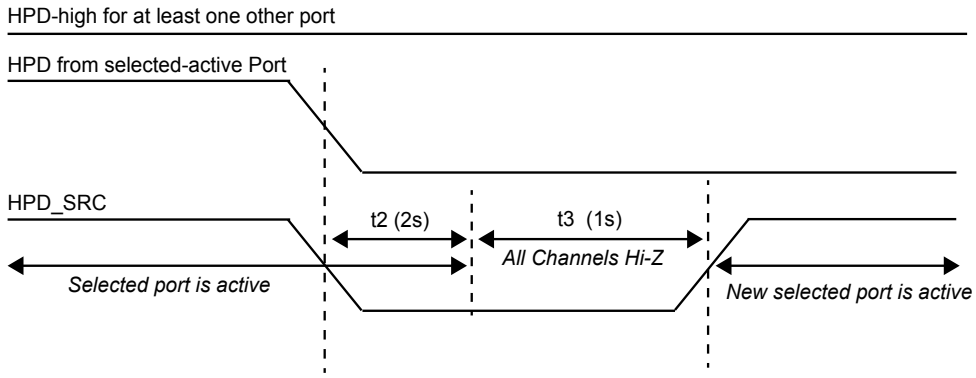


Fig 7. HPD timing when auto switch

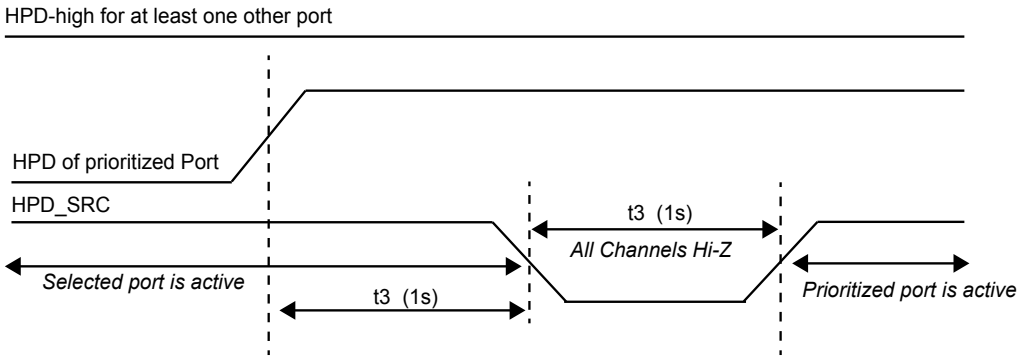


Fig 8. HPD timing when auto switch

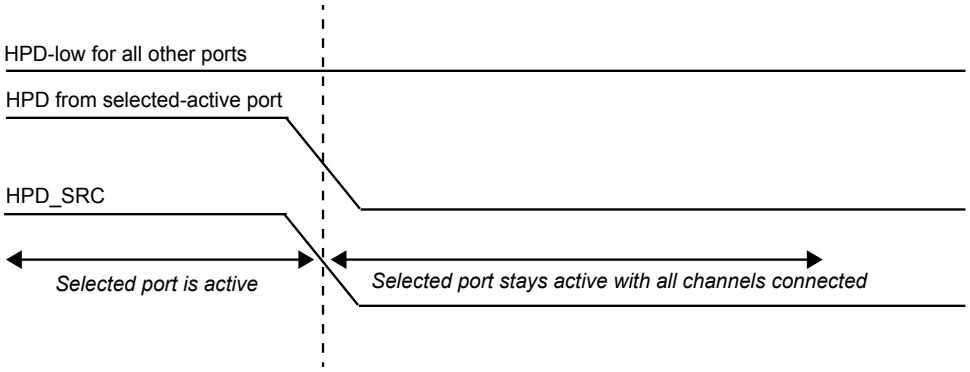


Fig 9. HPD timing when auto switch and manual switch

Port Selection by Manual Mode

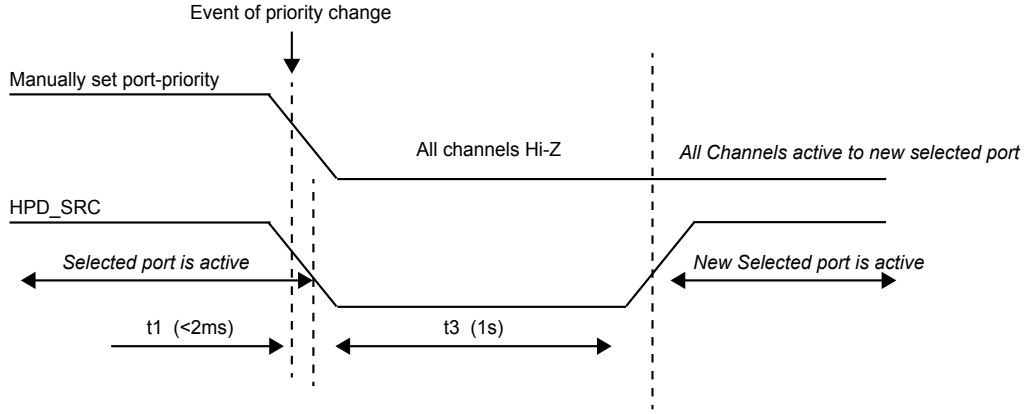
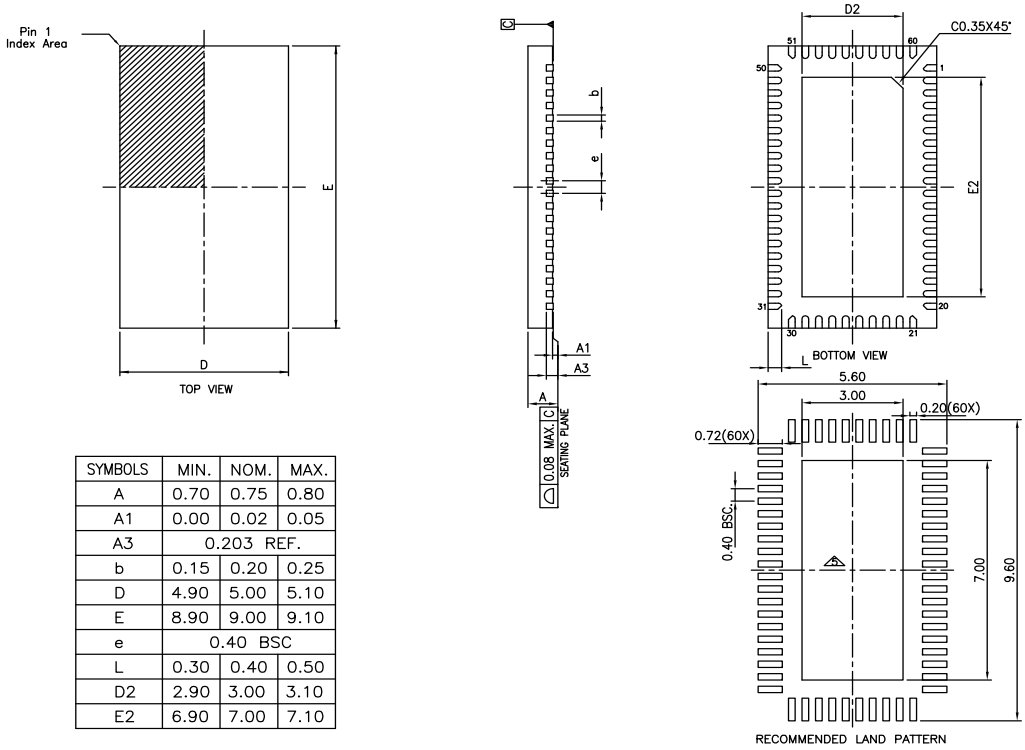


Fig10. HPD timing t3. All channels when auto switch

Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
HPD auto switching timing					
HPD pulse duration when treated as an IRQ –t1 (Figure 4)				2	ms
Propagation delay of HPDx Desertion –t2 (Figure 7)		1.2s	2s	3s	s
HPD_SRC low duration when the outputs are switched –t3(Figure 5, 6, 7, 8, 10); Propagation delay of HPDx assertion (Figure 8)		0.6s	1s	1.5s	s

Packaging Mechanical: ZL60



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	8.90	9.00	9.10
e		0.40 BSC	
L	0.30	0.40	0.50
D2	2.90	3.00	3.10
E2	6.90	7.00	7.10

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

PERICOM Enabling Serial Connectivity — DATE: 04/08/14

DESCRIPTION: 60-PIn, TQFN 5X9mm

PACKAGE CODE: ZL (ZL60)

DOCUMENT CONTROL #: PD-2182 — REVISION: –

14-0044

Note: For latest package info, please check: http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description
PI3WVR31310AZLE	ZL	60-Pin, (TQFN) 5X9mm
PI3WVR31310AZLEX	ZL	60-Pin, (TQFN) 5X9mm, Tape & Reel

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging